D.Module2.ADDA500K16

Board Revision 1.0 **Document Revision 1.0** **Nov 12, 2014**

Key Features

- six single-ended / three differential inputs
- two single-ended outputs
- simultaneous sampling up to 500ksps
- 16-bit resolution
- programmable input range and sampling frequency
- gain and offset calibration
- up to four boards can be stacked to form a 24 channel data acquisition system

Applications

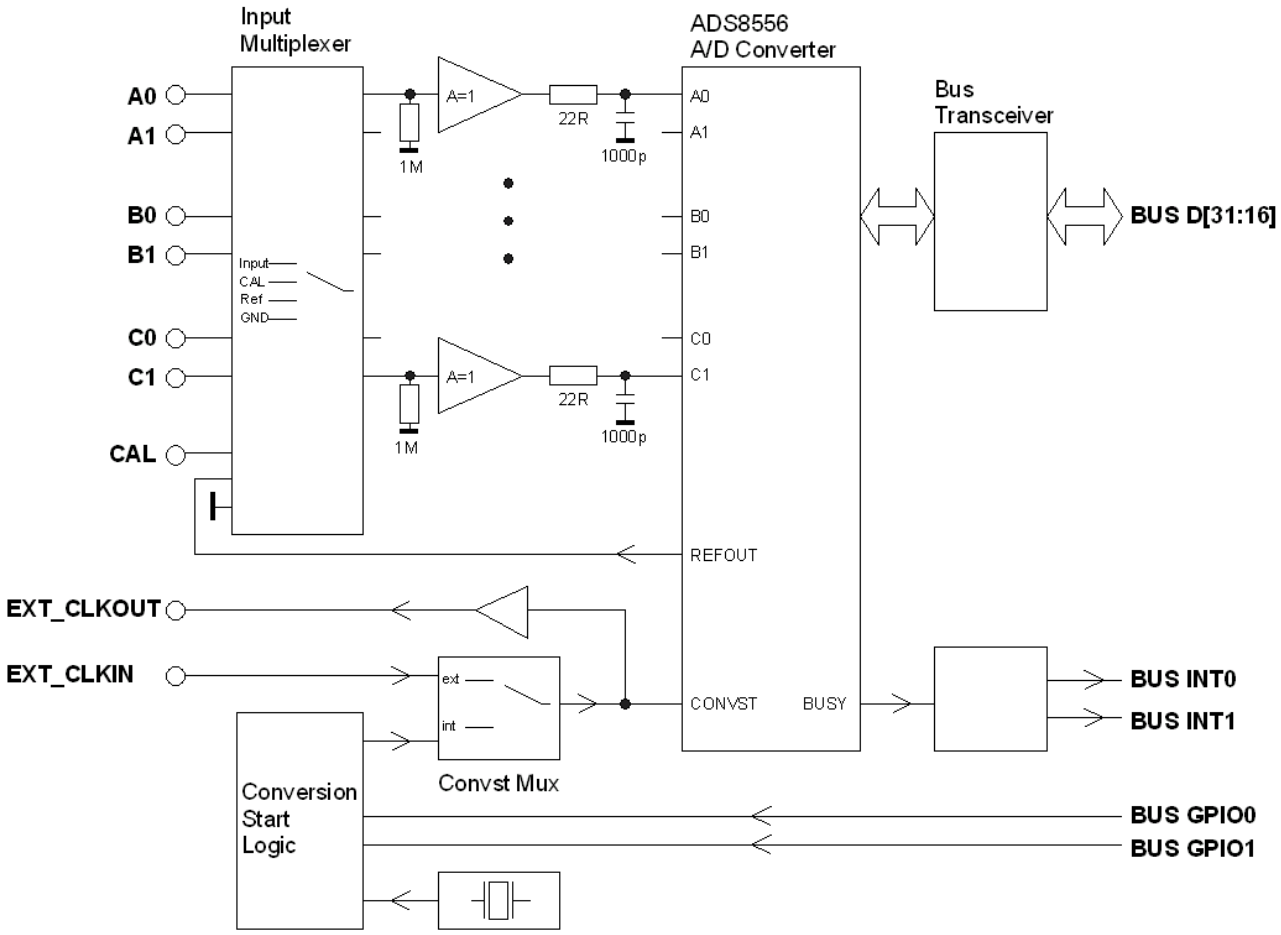
- motor control
- power-line monitoring
- sensor digitizing

The D.Moduel2.ADDA500K2 is a 6-channel, 500ksps, data acquisition daughter board for the D.Module2 series DSP boards. It features an ADS8556 A/D converter with 16 bit resolution, a dual-channel 16-bit DAC8822 D/A converter, a clock generator, and the D.Module2 external bus interface. The input voltage range is programmable from ±1V to ±3V. An OEM version with ±12.5V input range is available too.

Gain and offset can be calibrated at any time. An input multiplexer switches between the analog input, 0V, the internal reference, or an external calibration reference source.

Sampling is triggered by a programmable on-board clock generator (4 to 500 ksps) or by an external sampling clock.

Analog Inputs



No anti-aliasing filters are provided. If the input signals are not already band-limited, a suitable low-pass filter must be added externally. The internal bandwidth of the buffer stage and the ADC is 5MHz, which allows to use the ADDA500K16 in sub-sampling applications.

The input voltage range is configurable in software: the ADC reference is programmable from 0.5 to 3V, the fullscale input voltage is either 2*Vref or 4*Vref. The supply voltage of course limits the max. input voltage. The standard ADDA500K16 board operates on ±5V supply rails and allows an input voltage range ±1 .. ±3V. The default setting is ±2.5V. The 15V OEM version with ±15V supply can be used with input voltages up to ±12.5V (default: ±10V)

Differential signals should be connected to the A0/A1, B0/B1 or C0/C1 input pairs. The non-inverted input is x0, the inverted signal is connected to x1.The difference signal is calculated in software by subtraction.

Offset and gain errors may be calibrated in software by taking measurements with the input multiplexer set to GND (offset error) or Vref or CAL (gain error). Gain and offset errors are largely temperature-dependent. Ensure proper warm-up before a calibration is performed.

Conversion Start

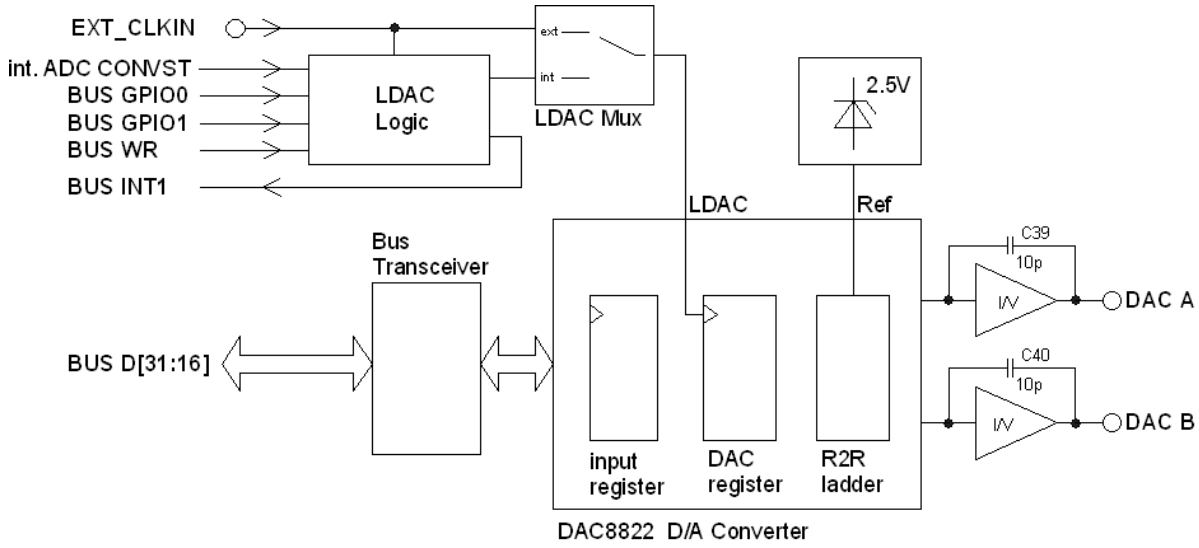
The ADS8556 A/D Converter starts a conversion at the rising edge of the CONVST (conversion start) signal. In digital signal processing applications the analog inputs are typically sampled at equidistant intervals. A sampling clock will periodically start ADC conversions. The maximum sampling clock is 500kHz. A rising edge on CONVST will put the ADC sample hold circuit into hold mode and start the analog to digital conversion. An interrupt is generated at the end of the conversion time, which is 1.26µs on the ADS8556. Now the data can be read. Data must be read before the next rising edge on CONVST.

A conversion start can be generated by

- the on-board programmable clock generator
- one of the two available GPIO inputs, e.g. driven by a DSP timer output
- an external trigger or an external periodic sampling clock

The EXT_CLKOUT signal is used in cascaded systems to synchronize multiple ADDA500K16 boards.

Analog Outputs



The two analog outputs provide a ±2.5V full scale voltage output with 0.5µsecs settling. A first-order smoothing filter is included. At power-on or reset the outputs are initialized to 0V.

Output update can be synchronized to the A/D conversion, triggered by one of the GPIO inputs (e.g. driven by a DSP timer output), triggered by an external clock, or triggered by the DSP write operation. An interrupt is generated if the D/A converter is ready to accept new data.

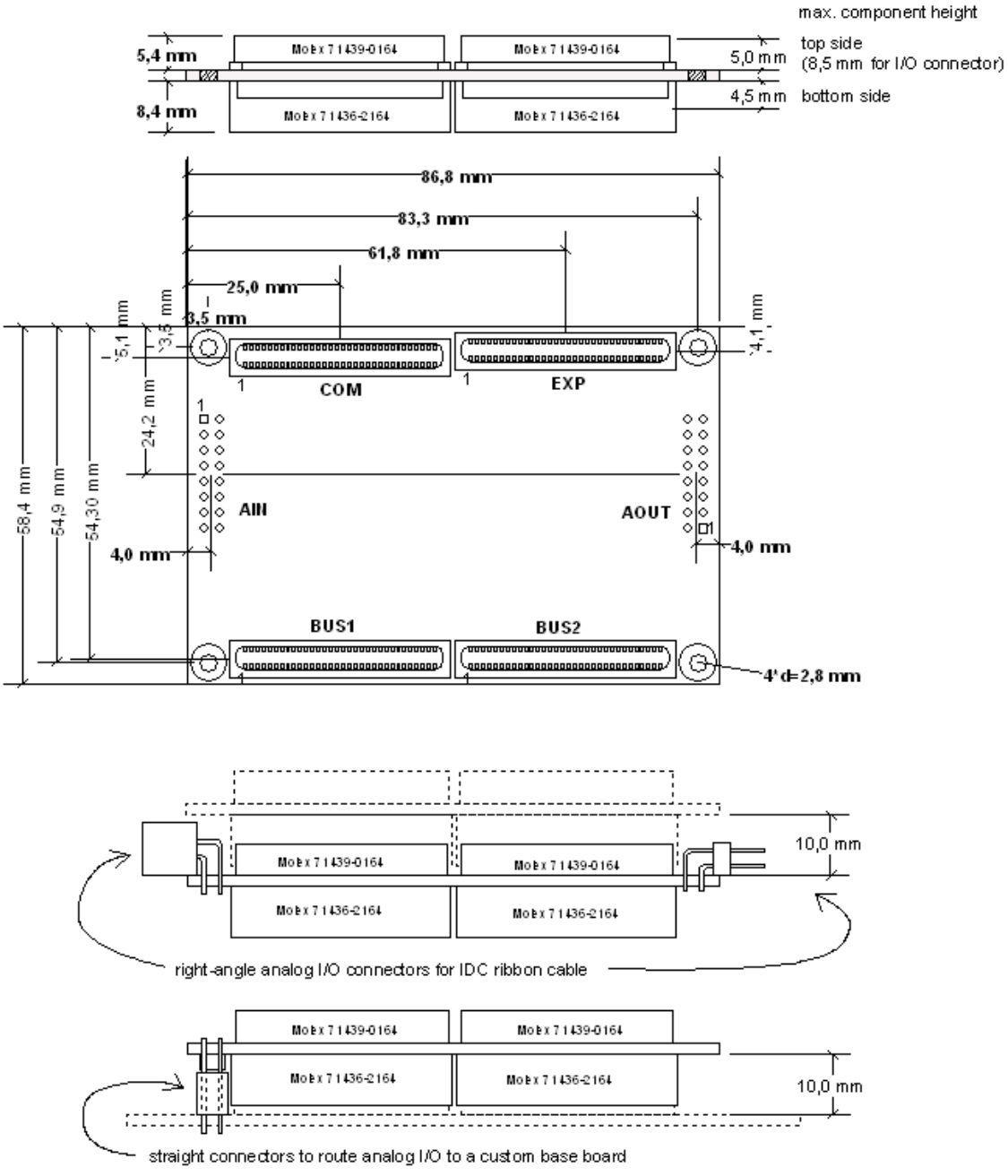
Power Supply

The D.Module2.ADDA500K16 requires separate analog and digital power supplies. The digital logic operates on 3.3V ±5%. The analog circuits are powered by a split ±5V ±5% supply. The -15V OEM version of the ADDA500K16 requires a ±15V ±10% analog supply.

Digital and analog grounds are connected on the D.Module2.ADDA500K16.

Switch mode regulators may be used for the analog power supply. The board includes LC filters in the analog power rails and tolerates up to 40mV supply ripple and noise.

Mechanical Dimensions



Connector Pinout

Connector and Pin	Signal	Description
BUS1 – 1, 2	VCC	Positive Digital Power Supply 3.3V
BUS1 – 3.4	GND	Digital Power Supply 0V
BUS1 – 5	RESOUT_N	Reset Input to ADDA500K16, active low
BUS1 – 7	INT0_N	Interrupt Output to DSP board, active low
BUS1 – 9	INT1_N	Interrupt Output to DSP board, active low
BUS1 – 13	OE_N	Data bus driver direction control, input to ADDA500K16, low = ADDA500K16 to DSP
BUS1 – 15	RD_N	Read Strobe input to ADDA500K16, active low
BUS1 – 17	WR _N	Write Strobe input to ADDA500K16, active low
BUS1 – 20	CS0_N	Chip Select input to ADDA500K16, active low
BUS1 – 22	CS1_N	Chip Select input to ADDA500K16, active low
BUS1 – 21, 23, 25	A0, A1, A2	Address lines, input to ADDA500K16
BUS1 – 30,31,33,34	A16..A19	Address lines, input to ADDA500K16
BUS1 – 36,37,38,39,41,42,44,45,46, 47,49,50,52,53,54,55	D16 .. D31	Data line, bidirectional D16 = LSB, D31 = MSB
BUS1 – 57	GPIO0	GPIO input to ADDA500K16
BUS1 – 58	GPIO1	GPIO input to ADDA500K16
BUS1 – 59, 60	AGND	Analog Power Supply 0V, internal connection to GND
BUS1 – 61, 62	AVPOS	Positive Analog Power Supply +5V
BUS1 – 63, 64	AVNEG	Negative Analog Power Supply -5V
AIN – 1	IN_A0	analog input channel A0
AIN – 3	IN_A1	analog input channel A1
AIN – 7	IN_B0	analog input channel B0
AIN – 9	IN_B1	analog input channel B1
AIN – 13	IN_C0	analog input channel C0
AIN – 15	IN_C1	analog input channel C1
AIN – 5 ,7	CAL	external calibration source input
AIN – 2,4,6,8,10,12,14,16	AGND	analog ground, internal connection to GND
AOUT – 3	OUT_A	analog output channel A
AOUT – 7	OUT_B	analog output channel B
AOUT – 11	EXTCLK_OUT	clock output to synchronize other ADDA500K16 boards
AOUT – 13	EXTCLK_IN	external sampling clock input
AOUT – 1,2,4,5,6,8,9,10,12,14,15,16	AGND	analog ground, internal connection to GND

Electrical Characteristics

Analog Inputs	6 single-ended channels (3 differential) bipolar input range programmable ±1.. ±3V, default ±2.5V overvoltage protection up to 40V input impedance 1 MΩ || 25pF -3dB bandwidth 5 MHz
A/D Converter	Texas Instruments ADS8556 resolution 16 bit max. sampling frequency 500 ksps
Analog Outputs	2 single-ended channels bipolar output ±2.5V output resistance 50 Ω -3dB bandwidth 3MHz
D/A Converter	Texas Instruments DAC8822 resolution 16 bit settling time 0.5 µs
Calibration	by software, ADC inputs can be switched to GND, ADC reference voltage, or external Calibration Input
Clocks	internal ADC conversion start, programmable external ADC conversion start, thigh min 1.26µs, tlow min 30ns ADC conversion start via GPIO0 or GPIO1 DAC update synchronous to ADC conversion, triggered by GPIO0 or GPIO1, or transparent mode external clock level: 3.3V LVTTL/LVCMOS compatible
Power Supply	digital: 3.3V ±5%, typ. 50 mA, max. 70 mA analog: ± 5V ±5%, typ. 150 mA, max. 250 mA
Digital Interface	D.Module2.Bus compatible 16-bit parallel asynchronous interface, LVTTL data format 2's complement decoder for 2 chip selects and 16 different base addresses
Interface Timing	Setup min 10ns, Strobe min 30ns, Hold min 10ns write: data valid before trailing write strobe: min 7ns read: data valid after leading read strobe : max 18ns
Temperature Range	-40 .. +85°C

Ordering Information

D.Module2.ADDA500K16	6-channel data acquisition daughter board
Options	-15V: OEM version with 12.5V input range
DS.ADDA500K16	Software Development Support

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