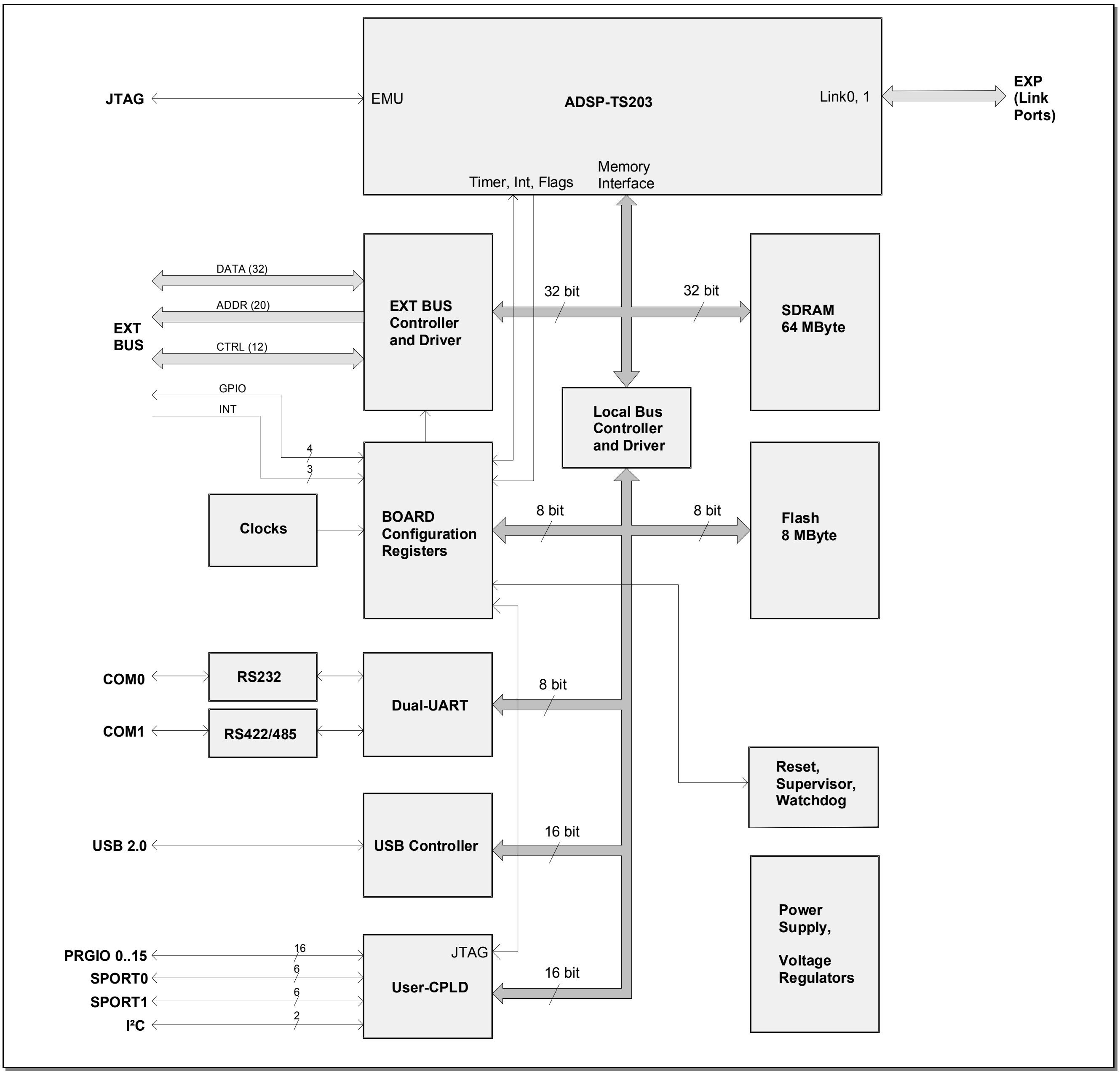
D.Module2.TS203 Technical Data Sheet

Board Revision 1.0 | **Document Rev. 1.2** | **Nov 2011**

SUMMARY

- Highest precision and performance floating point DSP module for radar, sonar, image processing, ultrasonics, and other demanding applications
- 3000 MFLOPS, 500 MHz, Analog Devices ADSP-TS203 TigerSHARC® IEEE floating point processor
- High bandwidth interfaces to data acquisition peripherals and FPGAs: 500M-Bytes/s parallel bus, 1G-Byte/s Link Ports
- High-speed USB2.0 peripheral controller
- Dual UART with auto-flow control, receive and transmit FIFOs, RS232 and RS422/485 interface
- 128 macrocell in-system programmable User-CPLD
- Large on-board memories: 64M-Byte SDRAM, 8M-Byte Flash
- 3.3V single-supply, Supervisor and Watchdog
- D.Module.BIOS programming support for all on-board resources, USB / RS232-based Setup Utility for convenient field-maintenance

BLOCK DIAGRAM



The D.Module2 series represents the next generation of high-performance,stand-alone DSP boards. These boards are optimized for highest I/O bandwidth to satisfy even demanding applications. The 32-bit wide external bus, configured in synchronous mode, can transfer up to 500M bytes/s of data between DSP and peripherals.

The self-stacking design allows to build complete signal processing systems by stacking the required DSP, I/O, data acquisition,and networking modules. If data preprocessing is needed, an FPGA module can be inserted between data acquisition and DSP.

Besides the high-speed peripheral bus all D.Module2 DSP boards provide a variety of interfaces: two UARTs, USB2.0 peripheral controller, and in-system user-programmable I/O ports. An extra connector is reserved for DSP-specific extensions like the Link ports in case of the TS203 module.

The high-speed design required special care for signal integrity and EMC. The PCB uses auxiliary GND planes to shield signals and provide controlled impedance signal paths, the power supply lines are extensively filtered, and the connector pinout provides ample signal return ground connections.

Programming support for all on-board peripherals is provided by the D.Module2.BIOS, a set of functions resident in the module's Flash Memory, covering initialization, configuration, and data transfer. Hardware dependencies are encapsulated by the BIOS, hence no software adaptations due to peripheral component or silicon revision changes are required in the user and application programs.

A Setup Utility, also resident in the Flash Memory, provides straightforward field maintenance via USB or RS232: data and program upload, configuration changes, and basic debugging functionality are available without the need for special emulator or programming equipment.

PROCESSOR

The DModule2.TS203 is built around the Analog Devices ADSP-TS203 floating-point DSP. The TigerSHARC® core provides two computational units, each with 32 registers, multiplier, shifter, and ALU. Two integer ALUs with 32 registers are used for for address generation and as additional general purpose registers.

The TS203 also features a 10-channel DMA controller, two high-speed link ports for inter-processor communications and FPGA interface, and 4M Bit internal DRAM memory.

SDRAM

64M bytes, 32-bit wide SDRAM is used on the D.Module2.TS203. Operating at up to 125 MHz, a throughput of 500M byte/s can be achieved. SDRAM can be used for program code and data. SDRAM is used most efficiently in conjunction with DMA to move the required data and/or functions into internal DRAM before processing.

FLASH MEMORY

8M bytes non-volatile Flash Memory provide storage for application programs, user data, and configuration settings. The Flash Memory also stores the board's hardware settings, the D.Module2.BIOS API functions, and the Setup and Recovery Utility programs. The D.Module2.BIOS functions provide erase, (block)write and (block)read functions, and a function to program the Flash with Intel-Hex files. The bootload function loads and executes programs stored in the Flash Memory.

Two boot sectors are hardware write protected. These sectors hold the module hardware configuration and the Recovery utility program. Even in case the flash memory is completely erased or overwritten by accident, these sectors remain intact and allow to recover the D.Module2.BIOS and the application without any special programming equipment.

EXTERNAL BUS INTERFACE

The bus interface is used to connect external peripherals like data acquisition boards or FPGAs.. It is configurable to asynchronous and synchronous mode. Synchronous mode, achieves data transfer rates up to 500M bytes/sec and supports FlyBy DMA transfers between SDRAM and external devices. Asynchronous transfer timing is widely programmable. External devices can request additional wait states via the WAIT_N input. Up to 125M bytes/sec. throughput can be achieved.

The bus interface consists of a 32 bit wide data bus, 12 control signals, 20 address lines, and three external interrupt or DMA request inputs. Four GPIO signals are configurable in the Board Configuration Register and allow to route the DSP Timer and FLAG signals to external peripherals. Two pre-decoded memory areas are available, which can be individually configured to different data formats, synchronous or asynchronous operation, and bus timings.

The bus drivers source/sink up to 24mA and are able to drive long signal lines with passive or active termination. In synchronous configuration the bus drivers operate registered to maximize setup and hold timing margins for the external peripherals.

USB

The Philips isp1582 USB2.0 device controller provides a high-speed interface for data exchange with a PC. 15..20M bytes/sec data throughput can be achieved. Bulk, Interrupt and isochronous transfers are supported. The D.Module2.BIOS greatly simplifies USB communications by providing a predefined interface with up to four user-configurable endpoints. The DSP accesses the USB controller with CPU or DMA data transfers. An 8K byte Fifo buffers incoming and outgoing data. In user-defined configurations up to 14 endpoints (7IN, 7OUT) can be used.

UART

A dual-channel UART with RS232 and RS422/485 line interface provides additional communication paths, supporting up to 230K baud on RS232 and 3M baud on RS422/485. The UART features 64 bytes transmit and receive Fifo for efficient block transfers and Xon/Xoff or RTS/CTS auto-flow-control. Data transfers can be accomplished by CPU (polling or interrupts) and DMA. The DModule2.BIOS provides configuration and data transfer functions.

I²C

An I²C interface to control and configure peripherals like Audio Codecs, Image Sensors, and the analogue front-ends of data acquisition boards can be implemented in the User-CPLD. I²C is also usable to expand the system with additional GPIO signals and attach temperature and voltage monitors.

USER-CPLD

The 256 macro-cell User-CPLD provides 16 programmable I/O signals, which can be configured as bit-programmable ports, serial interfaces, quadrature decoder, PWM output, etc. The User-CPLD is in-system programmable. Re-programming is done via a serial or USB connection in Setup mode.

POWER SUPPLY

The D.Module2.TS203 operates from a 3.3V single supply. All other required voltages (core voltage, RS232 driver supply, , etc.) are generated on-board by high-efficiency switch-mode converters and charge-pumps. The power supply is controlled by a supervisor chip, which guarantees a proper hardware reset on power-on, power-off, and brown-out conditions.

WATCHDOG

Stand-alone systems typically require methods for automatic recovery from system faults. One of these methods is activating the watchdog circuit. It will reset and reboot the system if the DSP program crashes and fails to trigger the watchdog periodically. The watchdog can be enabled (but not disabled) by software, or permanently by closing a solder link.

SYNCHRONOUS SERIAL PORTS

The TS203 does not provide built-in serial ports like many other DSPs. However, the User-CPLD can be used to implement these ports. Synchronous serial ports are typically used to interface industry-standard A/D and D/A converters.

BOARD CONFIGURATION

D.Module2 boards use a jumperless design, all board settings are software-configurable in the Board Configuration Register. The configuration can be set by the user program, or – preferably – stored in the Module Configuration File. At system start-up the Module configuration File is read and DSP clock, bus clock, and other options are configured accordingly.

The Board Configuration Register also provides multiplexers to route internal or external interrupt events to the DSP, and control and status registers for all on-board peripherals.

D.MODULE2.BIOS

The BIOS is a set of API functions, permanently stored in the Flash Memory. These functions are copied to internal DRAM at system start-up and are available to all user programs. BIOS functions cover initialization, configuration, and data transfer functions for the on-board peripherals. The reason to store these functions permanently in the Flash Memory, rather than providing them as a library, is the close coupling between low-level API functions and hardware: Should one of the module's peripherals need to be substituted during product lifetime, the BIOS will be adapted to the new hardware and the application program will continue to work without any changes.

USB functions

- open, close
- configure endpoints
- status change callback
- custom string descriptor table
- interrupt handler
- blockwrite, blockread
- low-level functions for user-defined interfaces

UART functions

- open, close
- configure
- write, blockwrite, write string
- read, blockread, read string

Flash Memory Functions

- open, get architecture information
- sector erase
- write, write block
- read, read block
- write Intel-Hex file

Board Functions

- initialize
- bootload
- get hardware and software revision
- DSP configuration and clocking
- external bus configuration and clocking
- delay
- watchdog enable and trigger
- interrupt, DMA, and GPIO mapping
- read and clear multiplexed interrupts

SETUP AND RECOVERY PROGRAM

Also permanently stored in the Flash Memory are the Setup and Recovery utility programs. The Setup program communicates via RS232 or USB. It allows to upload Intel-Hex program and data files to the Flash Memory, upload a Module Configuration File, load and execute programs from Flash, re-program the User-CPLD, and provides some basic debugging functions like reading and writing memory and memory-mapped peripherals. Setup is intended for field maintenance: Service technicians can upload program updates without direct access to the DSP hardware, and execute diagnostics and calibration programs stored in the Flash Memory.

The Recovery utility is stored in a hardware write protected Flash sector. Should the Flash be erased or overwritten accidentally, this program can be used to re-install the corrupted programs. Recovery uses a RS232 connection. Even severe problems can be fixed in-field without special emulator programming equipment.

Setup is invoked during a module reset by pulling the SETUP_N input low, or at any time from within an application program by calling the BIOS bootload function: DM2_bootload (0x10000). Recovery is invoked at module reset by pulling both SETUP_N and IN1_N inputs low.

MEMORY MAP

Address	Memory	Location	Width	Description
0x0000.0000 .. 0x0000.7FFF	DRAM	internal	32 bit	32K words internal memory block 0
0x0004.0000 .. 0x0004.7FFF	DRAM	internal	32 bit	32K words internal memory block 2
0x0008.0000 .. 0x0008.7FFF	DRAM	internal	32 bit	32K words internal memory block 4
0x000C.0000 .. 0x000C.6DFF	DRAM	internal	32 bit	27.5K words internal memory block 6
0x000C.6E00 .. 0x000C.7FFF	DRAM	internal	32 bit	4.5K words reserved for BIOS in memory block 6
0x3000.0000 .. 0x300F.FFFF	MS0	external	32 bit	External Bus Interface CS0
0x3800.0000 .. 0x380F.FFFF	MS1	external	32 bit	External Bus Interface CS1
0x4000.0000 .. 0x407F.FFFF	MSSD0	external	32 bit	8M words SDRAM
0x5000.0000 .. 0x507F.FFFF	MSSD1	external	32 bit	8M words SDRAM
0x8000.0000 .. 0x807F.FFFF	MSH	external	8 bit	8M bytes Flash Memory
0x8800.0000 .. 0x8800.0084	MSH	external	16 bit	USB Controller
0x8A00.0000 .. 0x8A00.0007	MSH	external	8 bit	UART 0
0x8B00.0000 .. 0x8B00.0007	MSH	external	8 bit	UART 1
0x8C00.0000 .. 0x8C00.003F	MSH	external	8 bit	User-CPLD
0x8E00.0000 .. 0x8E00.000F	MSH	external	8 bit	Board Configuration Registers

BOARD CONFIGURATION REGISTER

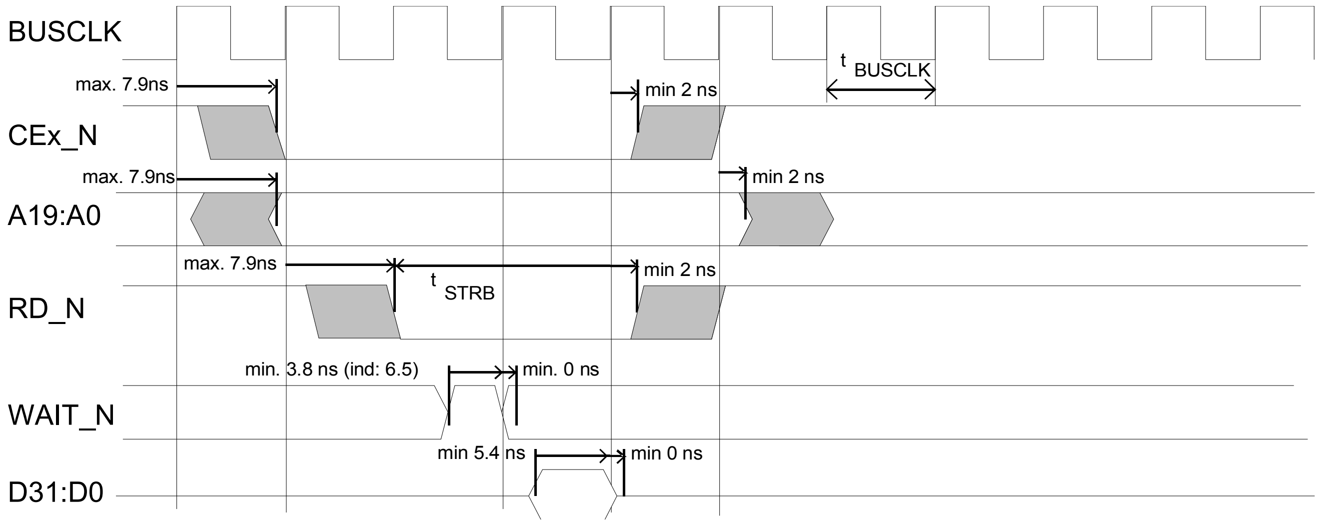
Register	D7	D6	D5	D4	D3	D2	D1	D0
USBCTRL	USBRES	-	-	-	-	INTSTAT	EOT_WR	EOT_RD
UARTCTRL	UARTRES	-	-	-	-	-	DRVEN_1	DRVEN_0
CPLDCTRL	CPLDRES	-	-	JTAG_EN	TDO	TDI	TMS	TCK
BUSCTRL	RESOUT	-	-	-	-	RDBUF	FLYBY	SYNC
WDOGCTRL	-	-	-	-	-	-	ENABLE	TRIGGER
DSPCTRL	DSPRES	CONFIG	LINK4	LINKBOOT	DSPCLKRAT		BUSCLK	
SETUPSTAT	-	-	-	-	-	SETUP	IN1	IN0
reserved	-	-	-	-	-	-	-	-
INTMUXLO	IRQ1_SOURCE				IIRQ0_SOURCE			
INTMUXHI	IRQ3_SOURCE				IRQ2_SOURCE			
DMAMUXLO	DMAR1_SOURCE				DMAR0_SOURCE			
DMAMUXHI	DMAR3_SOURCE				DMAR2_SOURCE			
GPIOMUXLO	GPIO1				GPIO0			
GPIOMUXHI	GPIO3				GPIO2			
MUXINTEN	UART1	UART0	CPLDINTY	CPLDINTX	USB	-	-	-
MUXINTSRC	UART1	UART0	CPLDINTY	CPLDINTX	USB	-	-	-

SPECIFICATIONS

DSP	Analog Devices TigerSHARC® ADSP-TS203, 32-bit floating-point DSP configurable core clock:300 .. 500 MHz
Memory	4M bit DSP-internal DRAM 64M bytes SDRAM, operating at up to 125 MHz, 32 bits wide, 500M bytes/sec throughput 8M bytes non-volatile Flash Memory, sector architecture , 8 bits wide
USB	NXP / Philips isp1582 USB2.0 peripheral controller, supports USB 1.1 and USB 2.0 up to 14 endpoints, 8K bytes shared FIFO, DMA support
UART	16C752 dual-channel UART, RS232 and RS422/485 line interface max. 230.4K baud RS232, 3M baud RS422/485, 64 bytes transmit and receive Fifos, DMA support, Auto-flow-control (Xon/Xoff, RTS/CTS)
I²C	can be implemented in User-CPLD
Timer	two, 64-bit wide, DSP-internal, one Timer with external output additional timers can be implemented in the User-CPLD
Link Ports	two, full duplex, 1 or 4 bits wide, LVDS, 1G byte/sec max. throughput
External Bus Interface	32 bit wide data bus, 20 address lines, 12 control signals supports synchronous and asynchronous operation, programmable and external wait states up to 500M bytes/sec throughput in synchronous mode configurable bus clock: 75, 83, 100, or 125 MHz 3 external interrupt inputs, also usable as DMA trigger
Sync. Serial Ports	up to two ports can be implemented in User-CPLD
Watchdog	enabled by software or hardware, timeout: 1 second
Emulation	standard 14-pin header, compatible with all Analog Devices JTAG in-circuit emulators
Supply Voltage VCC	3.3 V ± 5%
Power Consumption	TBD
Operating Temperature	0 .. +70 °C
Logic Levels	LVTTL, High-Level min. 2V, max. 3.5V, Low Level min. -0.2V, max. 0.8V output drive: external bus interface: ± 24mA, all others ± 8mA
Size	86.8 x 58.4 mm, overall height: 22.5mm
Weight	45g
Connectors	COM, EXP, BUS1 and BUS2 : Molex 71436-2164 Emulator: standard 14-pin header
industrial grade version	operating temperature -40 .. +85°C uses ADSP-TS201 DSP with 24M bit internal memory external bus and SDRAM clock 75, 83, or 100 MHz

TIMINGS

external bus asynchronous read



Timing	min	max	Description
t_{Setup}	1 BUSCLK cycle *1)		address and CEx_N setup before read strobe activated
t_{Strobe}	programmed STROBE cycles *1)		read strobe width
t_{Hold}	1 BUSCLK cycle *1)		address hold after read strobe deactivated
$t_{Data\ Setup}$	5.4 ns		data valid before last read strobe cycle
$t_{Data\ Hold}$	0 ns		data valid after last read strobe cycle
$t_{Wait\ Setup}$	3.8 ns 6.5 ns ind. grade		WAIT_N high before BUSCLK rising edge *2)
$t_{Wait\ Hold}$	0 ns		WAIT_N high after BUSCLK rising edge *2)

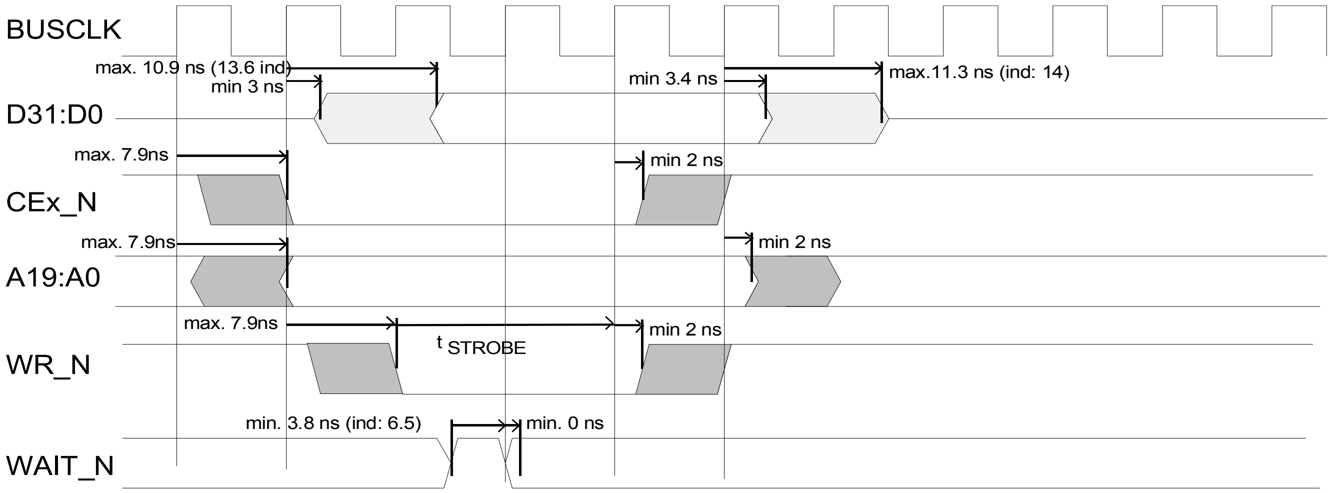
*1) The timing is based on BUSCLK, which is programmable to 75 MHz (13ns cycle time), 83.3 MHz (12 ns cycle time), 100 MHz (10 ns cycle time), or 125 MHz (8 ns cycle time) The number of read strobe cycles is determined by the wait states programmed in the SYSCON register: 0 to 3 wait states = 1 to 4 BUSCLK cycles. The diagram shows a 3-cycle read (2 wait states programmed in SYSCON register)

*2) WAIT_N is sampled on the rising BUSCLK edge one cycle before the programmed strobe period ends. If WAIT_N is found low at this time, the current bus cycle is extended until WAIT_N is sampled high.

Asynchronous bus transfers use the “Slow Device Protocol”, which is selected by setting the SLOW bit = 1 in the TS203 SYSCON register and SYNC bit = 0 in the Board Configuration BUSCTRL register. This protocol is intended to connect asynchronous peripherals to the TS203. However, all signals are referenced to BUSCLK: The TS203 changes its bus interface outputs max. 4ns after a rising BUSCLK edge. The bus drivers on the D.Moudle2.TS203 add 3.9 ns delay, hence signals are valid after 7.9ns worst case. Data is read at the end of the last read cycle and must be valid 1.5ns before the rising BUSCLK edge. Again the bus drivers on the D.Module2 add a worst case 3.9ns delay, hence data must be valid 5,4 ns before the rising BUSCLK edge. A peripheral device must drive

data valid after RD_N falling edge:	< strobe cycles * t_{BUSCLK} - 13.3ns
data valid after CEx_N falling edge::	< (strobe cycles + 1) * t_{BUSCLK} - 13.3ns
data valid after address valid:	< (strobe cycles + 1) * t_{BUSCLK} - 13.3ns
data hold after RD_N or CE_N rising edge:	> 0 ns

external bus asynchronous write



Timing	**min**	**max**	**Description**
t Swtup	1 BUSCLK cycle *1)		address and CEx_N setup before write strobe activated
t Strobe	programmed STROBE cycles *1)		write strobe width
t Hold	1 BUSCLK cycle *1)		address hold after write strobe deactivated
t Data Active		3ns	data bus driver active after strobe cycle begins
t Data Valid		10.9 ns 13.6ns ind. grade	data valid after strobe cycle begins
t Data Hold	3.4 ns		data hold after last strobe cycle
t Data Hi-Z		11.3 ns 14 ns ind. grade	data bus driver in high impedance after last strobe cycle
t Wait Setup	3.8 ns 6.5 ns ind. grade		WAIT_N high before BUSCLK rising edge *2)
t Wait Hold	0 ns		WAIT_N high after BUSCLK rising edge *2)

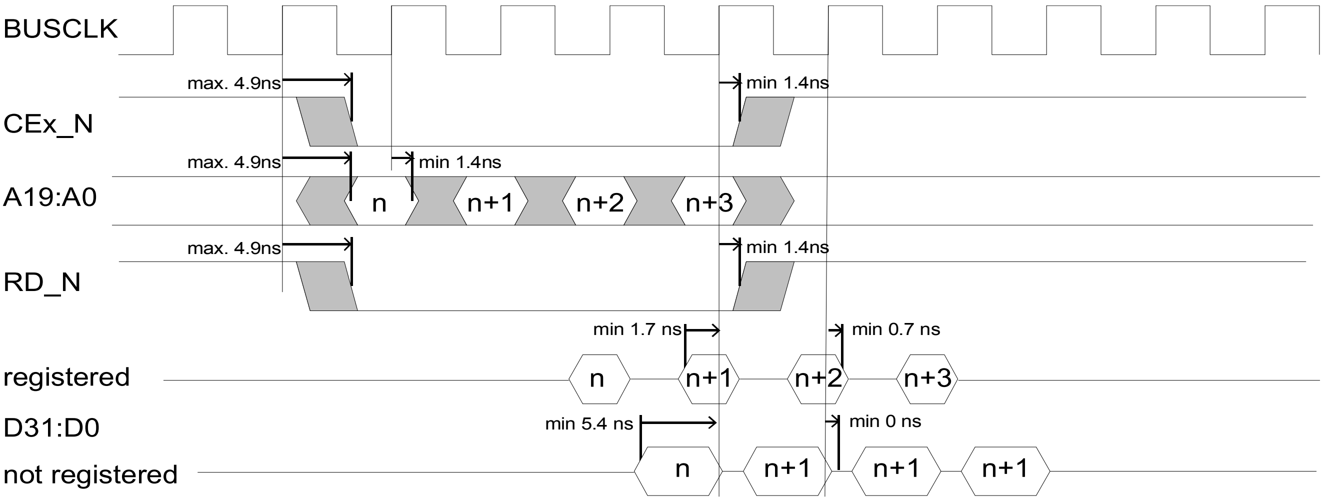
*1) The timing is based on BUSCLK, which is programmable to 75 MHz (13ns cycle time), 83.3 MHz (12 ns cycle time), 100 MHz (10 ns cycle time), or 125 MHz (8 ns cycle time) The number of write strobe cycles is determined by the wait states programmed in the SYSCON register: 0 to 3 wait states = 1 to 4 BUSCLK cycles. The diagram shows a 3-cycle write (2 wait states programmed in SYSCON register)

*2) WAIT_N is sampled on the rising BUSCLK edge one cycle before the programmed strobe period ends. If WAIT_N is found low at this time, the current bus cycle is extended until WAIT_N is sampled high.

An asynchronous peripheral device sees:

data valid before WR_N rising edge :	> strobe cycles * t_{BUSCLK} - 8.9 ns
data valid before CE_N rising edge:	> strobe cycles * t_{BUSCLK} - 8.9 ns
data valid after WR_N rising edge:	> t_{BUSCLK} + 1.4 ns
data valid after CE_N rising edge:	> t_{BUSCLK} + 1.4 ns

external bus synchronous read



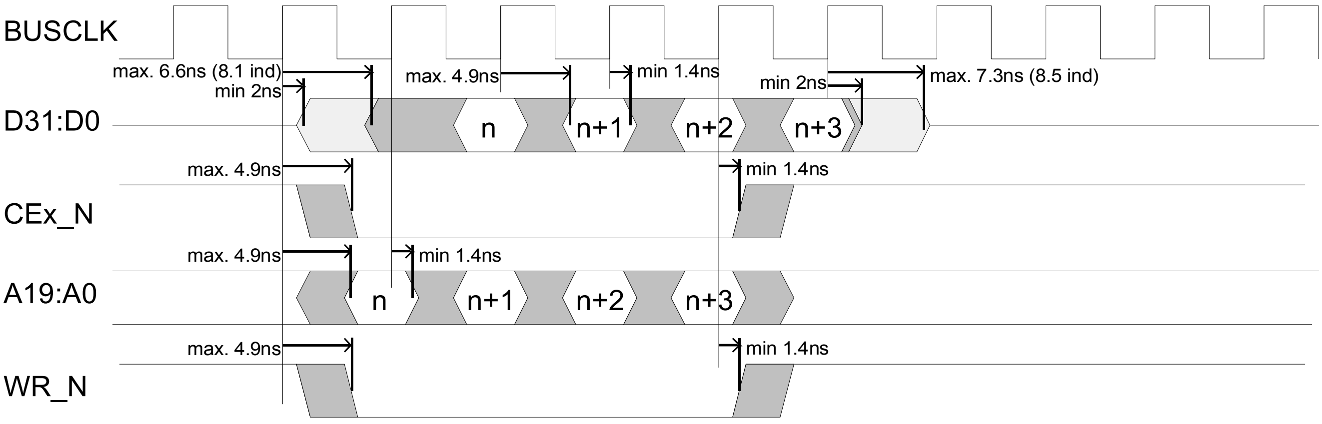
Timing	min	max	Description
t Ctrl Valid	1.4 ns	4.9 ns	control signals (CEx_N, RD_N and ADDR) valid after BUSCLK rising edge
t Data Setup	1.7 ns 5.4 ns		data setup to BUSCLK rising edge, registered mode data setup if data bus not registered
t Data Hold	0.7ns 0 ns		data hold after BUSCLK rising edge, registered mode data hold if data bus not registered

BUSCLK is programmable to 75 MHz (13ns cycle time), 83.3 MHz (12 ns cycle time), 100 MHz (10 ns cycle time), or 125 MHz (8 ns cycle time)

Synchronous mode is selected by setting the SYNC bit in the Module Configuration BUSCTRL register. The TS203 SYSCON register must be configured to “pipelined protocol” and a 4 cycle pipe. Synchronous mode is most efficiently used with burst transfers. The diagram shows a burst of 4 reads.

The synchronous interface is configurable to registered or unregistered reads. The default registered reads simplify the interface because of relaxed data setup timing. Unregistered reads however offer one more pipeline cycle between read command and data. Unregistered read mode is selected by setting the RDBUF bit in the Module Configuration BUSCTRL register.

external bus synchronous write



Timing	min	max	Description
$t_{Ctrl\ Valid}$	1.4 ns	4.9 ns	control signals (CEx_N, WR_N and ADDR) valid after BUSCLK rising edge
t_{Data_Active}	2 ns	6.6 ns 8.1 ns ind. grade	data bus driver active after BUSCLK rising edge
t_{Data_Valid}	1.4 ns	4.9 ns	data valid after BUSCLK rising edge
$t_{Data\ Hi\text{-}Z}$	2 ns	7.3 ns 8.5 ns ind. grade	data bus in high impedance after BUSCLK rising edge

BUSCLK is programmable to 75 MHz (13ns cycle time), 83.3 MHz (12 ns cycle time), 100 MHz (10 ns cycle time), or 125 MHz (8 ns cycle time)

Link Port Timings

these signals are directly connected to the DSP. Please refer to the Analog Devices ADSP-TS203 data sheet for detailed information

PINOUT AND SIGNAL DESCRIPTION

COM Connector

Signal	Pin	Type	Description
GND_IN	1,2,3,4	PWR	Power Supply Input, 0V
VCC_IN	5,6,7,8	PWR	Power Supply Input, 3.3V
SETUP_N	9	I	Setup Input, active low, internal 10K pull-up, start Setup-Utility if found low at reset
IN0_N	10	I	active low, internal 10K pull-up, start Recovery-Utility if SETUP_N and IN0_N are found low at reset
IN1_N	12	I	active low, internal 10K pull-up, reserved for configuration
RESIN_N	11	I	Reset Input, active low, internal 10K pull-up
USB_VCC	13	I	USB Power, supplied by Host or Hub, used to detect USB cable
USB_GND	15	I	USB power and reference signal ground
USB_D+	14	IO DIF	USB data, non-inverted signal
USB_D-	16	IO DIF	USB data, inverted signal
CTS0	19	I	UART0, RS232 CTS (if RS422: RDX0-)
RTS0	20	O	UART0, RS232 RTS (if RS422: TXD0-)
RXD0	21	I	UART0, RS232 data input (if RS422: RXD0+)
TXD0	22	O	UART0, RS232 data input (if RS422: TXD0+)
RXD1-	25	I DIF	UART1, RS422 inverted data input (if RS232: CTS1)
RXD1+	27	I DIF	UART1, RS422 non-inverted data input (if RS232: RXD1)
TXD1-	26	O DIF	UART1, RS422 inverted data output (if RS232: RTS1)
TXD1+	28	O DIF	UART1, RS422 non-inverted data output (if RS232: TXD1)
ETH_GND	29, 30		n.c.
ETH_RX+	31	I DIF	n.c.
ETH_RX-	33	I DIF	n.c.
ETH_TX+	32	O DIF	n.c.
ETH_TX-	34	O DIF	n.c.
SCL	37	IOZ	I²C Bus Clock, internal 4K7 pull-up, connected to User-CPLD
SDA	38	IOZ	I²C Bus Data, internal 4K7 pull-up, connected to User-CPLD
PRGIO0..15	43,45,46,48, 49,50,51,53, 54,56,57,58, 59,61,62,64	IOZ	programmable I/O signals from User-CPLD
SGND	17,18,23,24, 35,36,40,41, 44,47,52,55, 60,63		Signal Ground (signal current return path)

I – Input, O – Output, IO – bidirectional, Z – high impedance, PWR – power, DIF – differential signal

EXP Connector

Signal	Pin	Type	Description
L0DATI0P, L0DATI0N, L0DATI1P, L0DATI1N, L0DATI2P, L0DATI2N, L0DATI3P, L0DATI3N	2, 4, 3, 5, 10, 12, 13, 15	I DIF	Link Port 0 LVDS receiver data inputs
L0DATO0P, L0DATO0N, L0DATO1P, L0DATO1N, L0DATO2P, L0DATO2N, L0DATO3P, L0DATO3N	18, 20, 19, 21, 26, 28, 27, 29	O DIF	Link Port 0 LVDS transmitter data outputs
L0CLKINP, L0CLKINN	8, 7	I DIF	Link Port 0 LVDS receiver clock input
L0CLKOP, L0CLKON	24, 23	O DIF	Link Port 0 LVDS transmitter clock output
L0ACKO	15	O	Link Port 0 receiver acknowledge output
L0ACKI	31	I	Link Port 0 transmitter acknowledge input
L0BCMPI	16	I	Link Port 0 receiver block completion input
L0BCMPO	32	O	Link Port 0 transmitter block completion output
L1DATI0P, L1DATI0N, L1DATI1P, L1DATI1N, L1DATI2P, L1DATI2N, L1DATI3P, L1DATI3N	34, 36, 35, 37, 42, 44, 43, 45	I DIF	Link Port 1 LVDS receiver data inputs
L1DATO0P, L1DATO0N, L1DATO1P, L1DATO1N, L1DATO2P, L1DATO2N, L1DATO3P, L1DATO3N	50, 52, 51, 53, 58, 60, 59, 61	O DIF	Link Port 1 LVDS transmitter data outputs
L1CLKINP, L1CLKINN	40, 39	I DIF	Link Port 1 LVDS receiver clock input
L1CLKOP, L1CLKON	56, 55	O DIF	Link Port 1 LVDS transmitter clock output
L1ACKO	47	O	Link Port 1 receiver acknowledge output
L1ACKI	63	I	Link Port 1 transmitter acknowledge input
L1BCMPI	48	I	Link Port 1 receiver block completion input
L1BCMPO	64	O	Link Port 1 transmitter block completion output
SGND	1,6,9,14, 17,22,25,30, 33,38,41,46, 49,54,57,61		Signal Ground (signal current return path)

I – Input, O – Output, IO – bidirectional, Z – high impedance, PWR – power, DIF – differential signal

BUS 1 Connector

Signal	Pin	Type	Description
VCC_OUT	1, 2	PWR	Power Supply Output to Peripherals, +3.3V
GND_OUT	3, 4	PWR	Power Supply Output to Peripherals, 0V
AGND	59, 60	PWR	Analog Power Supply to Peripherals, 0V
AVCC+	61, 62	PWR	Analog Power Supply to Peripherals, positive voltage rail
AVCC-	63, 64	PWR	Analog Power Supply to Peripherals, negative voltage rail
RESOUT_N	5	O	Reset Output to Peripherals, active low
BUSCLK	6	O	Bus Clock, use if external bus configured to synchronous operation
INT0_N, INT1_N, INT2_N	7, 9, 10	I	External Interrupt Inputs, active low, internal 1K pull-up
BE2_N, BE3_N	12, 14	O	Byte Enable for D16..D23 and D24..D31, not used, internally connected to GND
OE_N	13	O	Output Enable, active low, identical to RD_N on D.Module2.TS203
RD_N	15	O	Read Strobe, active low
WR_N	17	O	Write Strobe, active low
WAIT_N	18	I	Wait State Request, active low, internal 1K pull-up
CS0_N	20	O	Chip Select 0, active low
CS1_N	22	O	Chip Select 1, active low
A0..A5	21,23,25,26, 28,29	O	Address Bus
A16..A19	30,31,33,34	O	Address Bus
D16..D31	36,37,38,39, 41,42,44,45, 46,47,49,50, 52,53,54,55	IOZ	Data Bus
GPIO0, GPIO1	57, 58	IOZ	General Purpose IO, or IORD_N, IOWR_N during FlyBy DMA Transfers
SGND	8,11,16,19, 24,27,32,35, 40,43,48,51, 56		Signal Ground (signal current return path)

I – Input, O – Output, IO – bidirectional, Z – high impedance, PWR – power

BUS 2 Connector

Signal	Pin	Type	Description
VCC_OUT	63, 64	PWR	Power Supply Output to Peripherals, +3.3V
GND_OUT	61, 62	PWR	Power Supply Output to Peripherals, 0V
AGND	5, 6	PWR	Analog Power Supply to Peripherals, 0V
AVCC+	3, 4	PWR	Analog Power Supply to Peripherals, positive voltage rail
AVCC-	1, 2	PWR	Analog Power Supply to Peripherals, negative voltage rail
GPIO2, GPIO3	7, 8	IOZ	General Purpose IO
D0..D15	9,10,11,12, 14,15,16,17, 19,20,22,23, 24,25,27,28	IOZ	Data Bus
A6..A15	30,31,32,33, 35,36,38,39, 40,41	O	Address Bus
BE0_N, BE1_N	43, 44	O	Byte Enable for D0..D7 and D8..D15, not used, internally connected to GND
DATR0	46	I	Sync Serial Port 0, data receiver, connected to User-CPLD
CLKR0	47	IO	Sync Serial Port 0, receive clock input or output, connected to User-CPLD
FSR0	48	IO	Sync Serial Port 0, receive frame sync input or output, connected to User-CPLD
DATX0	49	O	Sync Serial Port 0, data transmitter, connected to User-CPLD
CLKX0	51	IO	Sync Serial Port 0, transmit clock input or output, connected to User-CPLD
FSX0	52	IO	Sync Serial Port 0, transmit frame sync input or output, connected to User-CPLD
DATR1	54	I	Sync Serial Port 1, data receiver, connected to User-CPLD
CLKR1	55	IO	Sync Serial Port 1, receive clock input or output, connected to User-CPLD
FSR1	56	IO	Sync Serial Port 1, receive frame sync input or output, connected to User-CPLD
DATX1	57	O	Sync Serial Port 1, data transmitter, connected to User-CPLD
CLKX1	58	IO	Sync Serial Port 1, transmit clock input or output, connected to User-CPLD
FSX1	59	IO	Sync Serial Port 1, transmit frame sync input or output, connected to User-CPLD
RESOUT_N	60	O	Reset Output to Peripherals, active low
SGND	13,18,21,26, 29,34,37,42, 45,50,53,		Signal Ground (signal current return path)

I – Input, O – Output, IO – bidirectional, Z – high impedance, PWR – power

BUS 1

Pin	Signal	Signal	Pin
1	VCC_OUT	VCC_OUT	2
3	GND_OUT	GND_OUT	4
5	RESOUT_N	BUSCLK	6
7	INT0_N	SGND	8
9	INT1_N	INT2_N	10
11	SGND	BE2_N	12
13	OE_N	BE3_N	14
15	RD_N	SGND	16
17	WR_N	WAIT_N	18
19	SGND	CS0_N	20
21	A0	CS1_N	22
23	A1	SGND	24
25	A2	A3	26
27	SGND	A4	28
29	A5	A16	30
31	A17	SGND	32
33	A18	A19	34
35	SGND	D16	36
37	D17	D18	38
39	D19	SGND	40
41	D20	D21	42
43	SGND	D22	44
45	D23	D24	46
47	D25	SGND	48
49	D26	D27	50
51	SGND	D28	52
53	D29	D30	54
55	D31	SGND	56
57	GPIO0	GPIO1	58
59	AGND	AGND	60
61	AVCC+	AVCC+	62
63	AVCC-	AVCC-	64

COM

Pin	Signal	Signal	Pin
1	GND_IN	GND_IN	2
3	GND_IN	GND_IN	4
5	VCC_IN	VCC_IN	6
7	VCC_IN	VCC_IN	8
9	SETUP_N	IN0_N	10
11	RESIN_N	IN1_N	12
13	USB_VCC	USB_D+	14
15	USB_GND	USB_D-	16
17	SGND	SGND	18
19	CTS_0	RTS_0	20
21	RXD_0	TXD_0	22
23	SGND	SGND	24
25	RXD_1-	TXD_1-	26
27	RXD_1+	TXD_1+	28
29	ETH_GND / nc	ETH_GND / nc	30
31	ETH_RX+ / nc	ETH_TX+ / nc	32
33	ETH_RX- / nc	ETH_TX- / nc	34
35	SGND	SGND	36
37	SCL	SDA	38
39	rsvd	SGND	40
41	SGND	rsvd	42
43	PRGIO0	SGND	44
45	PRGIO1	PRGIO2	46
47	SGND	PRGIO3	48
49	PRGIO4	PRGIO5	50
51	PRGIO6	SGND	52
53	PRGIO7	PRGIO8	54
55	SGND	PRGIO9	56
57	PRGIO10	PRGIO11	58
59	PRGIO12	SGND	60
61	PRGIO13	PRGIO!4	62
63	SGND	PRGIO15	64

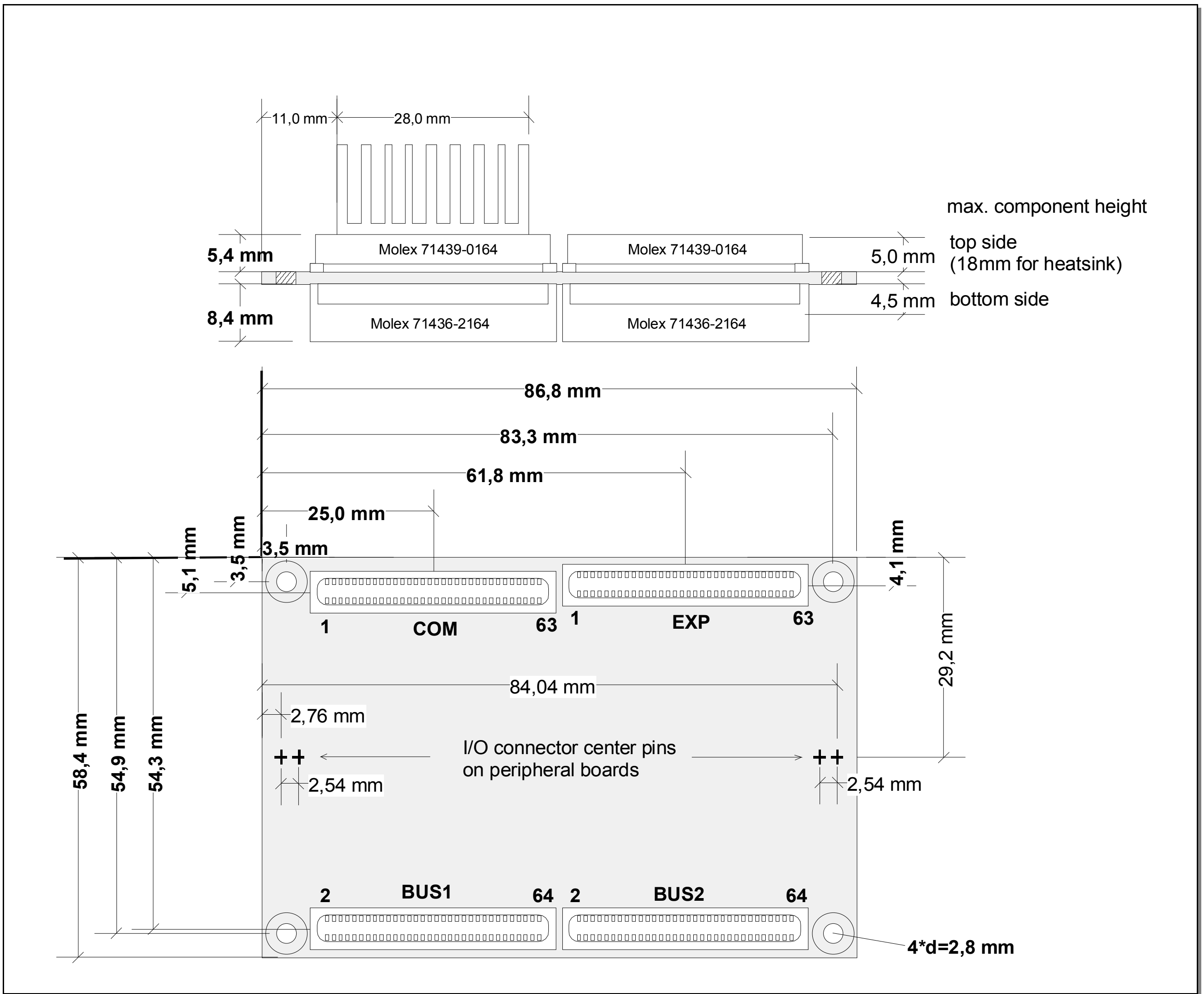
BUS 2

Pin	Signal	Signal	Pin
1	AVCC-	AVCC-	2
3	AVCC+	AVCC+	4
5	AGND	AGND	6
7	GPIO2	GPIO3	8
9	D0	D1	10
11	D2	D3	12
13	SGND	D4	14
15	D5	D6	16
17	D7	SGND	18
19	D8	D9	20
21	SGND	D10	22
23	D11	D12	24
25	D13	SGND	26
27	D14	D15	28
29	SGND	A6	30
31	A7	A8	32
33	A9	SGND	34
35	A10	A11	36
37	SGND	A12	38
39	A13	A14	40
41	A15	SGND	42
43	BE0_N	BE1_N	44
45	SGND	DATR0	46
47	CLKR0	FSR0	48
49	DATX0	SGND	50
51	CLKX0	FSX0	52
53	SGND	DATR1	54
55	CLKR1	FSR1	56
57	DATX1	CLKX1	58
59	FSX1	RESOUT_N	60
61	GND_OUT	GND_OUT	62
63	VCC_OUT	VCC_OUT	64

EXP

Pin	Signal	Signal	Pin
1	SGND	L0DATI0P	2
3	L0DATI1P	L0DATI0N	4
5	L0DATI1N	SGND	6
7	L0CLKINN	L0CLKINP	8
9	SGND	L0DATI2P	10
11	L0DATI3P	L0DATI2N	12
13	L0DATI3N	SGND	14
15	L0ACKO	L0BCMPI	16
17	SGND	L0DATO0P	18
19	L0DATO1P	L0DATO0N	20
21	L0DATO1N	SGND	22
23	L0CLKOUTN	L0CLKOUTP	24
25	SGND	L0DATO2P	26
27	L0DATO3P	L0DATO2N	28
29	L0DATO3N	SGND	30
31	L0ACKI	L0BCMPO	32
33	SGND	L1DATI0P	34
35	L1DATI1P	L1DATI0N	36
37	L1DATI1N	SGND	38
39	L1CLKINN	L1CLKINP	40
41	SGND	L1DATI2P	42
43	L1DATI3P	L1DATI2N	44
45	L1DATI3N	SGND	46
47	L1ACKO	L1BCMPI	48
49	SGND	L1DATO0P	50
51	L1DATO1P	L1DATO0N	52
53	L1DATO1N	SGND	54
55	L1CLKOUTN	L1CLKOUTP	56
57	SGND	L1DATO2P	58
59	L1DATO3P	L1DATO2N	60
61	L1DATO3N	SGND	62
63	L1ACKI	L1BCMPO	64

MECHANICAL DIMENSIONS



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