DMX 973

70 x 32 Pixel Graphic Dot Matrix Display

The DMX 973 incorporates the latest LCD controller LSI to provide a unique combination of compact size and ease of use. Easy to install, it is pin compatible with any character display based on the popular LCDII system. Any existing application can be upgraded to a graphic display with a change of software (8 bit mode only). Supplied with bezel, window and clips.

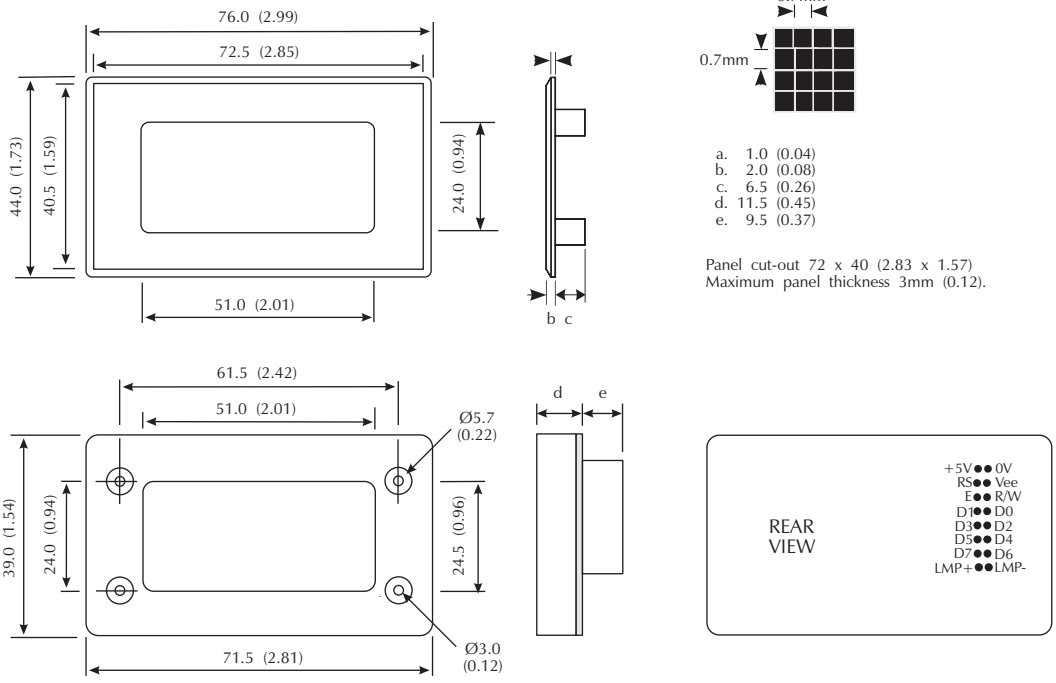
- 'Supertwist' LCD
- High Contrast
- LED Backlight
- Pin Compatible With Character Types
- 68XX or 80XX Interface

Stock Number Standard Display				DMX 973
Specification	**Min.**	**Typ.**	**Max.**	**Unit**
Supply Voltage (V+)	4.5	5.0	5.5	V
Supply Current — Normal		4.0		mA
Supply Current — Standby		0.2		mA
Input Voltage High	2.0		V+	V
Input Voltage Low	0		0.8	V
Output Voltage High	2.4			V
Output Voltage Low			0.4	V
Backlight Supply Voltage		5	5.5	V
Backlight Supply Current		50	90	mA

CONNECTOR SOURCING GUIDE

METHOD	Cable Mounting IDC Supplied With Product

DIMENSIONS (All dimensions in mm (inches)



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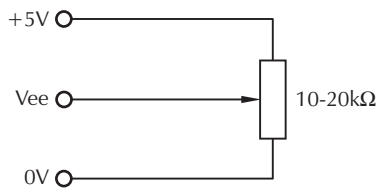
PIN FUNCTIONS

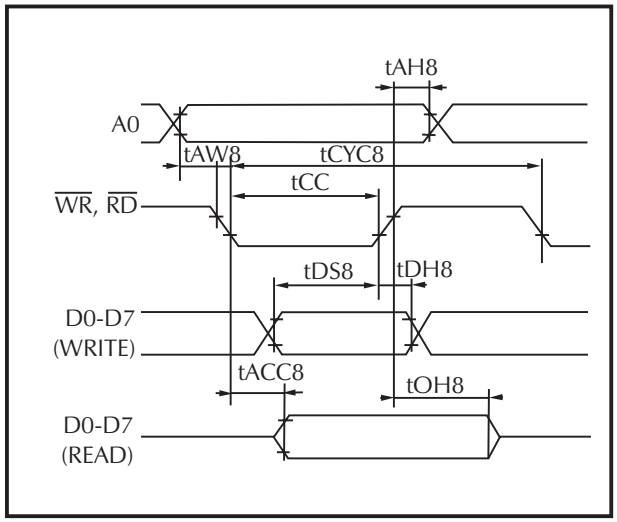
1.	0V.	}Power supply.
2.	+5V.	
3.	Vee.	LCD contrast control input (see diagram).
4.	RS.	Register Select input.
5.	R/W ($\overline{WR}$).	Read/Write input.
6.	E ($\overline{RD}$).	Enable signal.
7-14.	D0-D7.	8Bit bi-directional µP data bus.
15.	LMP-.	}Backlight supply, maximum 90mA.
16.	LMP+.	

CONTRAST CONTROL



READ/WRITE TIMING FOR THE 80-PORT MPU

TIMING CHART

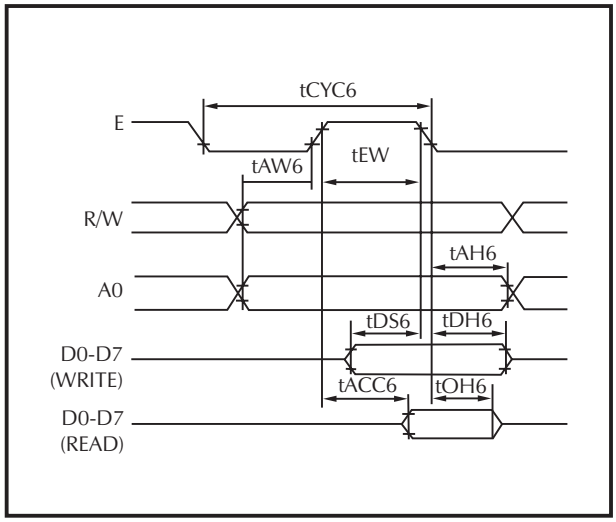


AC CHARACTERISTICS

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Address hold time	A0	tAH8		10	-	-	ns
Address set-up time		tAW8		20	-	-	ns
System cycle time	$\overline{WR}$, $\overline{RD}$	tCYC8		1000	-	-	ns
Control pulse width		tCC		200	-	-	ns
Data set-up time	D0-D7	tDS8		80	-	-	ns
Data hold time		tDH8		10	-	-	ns
$\overline{RD}$ access time		tACC8	CL=100pF	-	-	90	ns
Output disable time		tOH8		10	-	60	ns

READ/WRITE TIMING FOR THE 68-PORT MPU

TIMING CHART



AC CHARACTERISTICS

Parameter		Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
System cycle time		A0, R/$\overline{W}$	tCYC6		1000	-	-	ns
Address set-up time			tAW6		20	-	-	ns
Address hold time			tAH6		10	-	-	ns
Data set-up time		D0-D7	tDS6		80	-	-	ns
Data hold time			tDH6		10	-	-	ns
Output disable time			tOH6		10	-	60	ns
Access time			tACC6		-	-	90	ns
Enable pulse width	READ	E	tEW		100	-	-	ns
	WRITE				80	-	-	ns

INSTRUCTIONS

	COMMANDS	CODE											FUNCTION
		A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	
1	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns all display on or off, independently of display RAM data or internal status. 1: ON 0: OFF (Power saving mode with static drive on).
2	Display Start Line	0	1	0	1	1	0	Display Start Address (0-31)					Specifies RAM line corresponding to upper most line (COM0) of display.
3	Set Page Address	0	1	0	1	0	1	1	1	0	Page (0-3)		Sets display RAM page in page address register.
4	Set Column (Segment)	0	1	0	0	Column Address (0-79)							Sets display RAM column address in column address register.
5	Read Status	0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0	Reads the following status; BUSY 1: Internal operation, 0: Ready ADC 1: CW output (forward), 0: CCW output (reverse) ON/OFF 1: Display off, 0: Display on RESET 1: Being reset 0: Normal
6	Write Display Data	1	1	0	Write Data								Writes data from data bus into display RAM. Display RAM location whose address has been preset is accessed. After access, the column address is incremented by 1.
7	Read Display Data	1	0	1	Read Data								Reads data from display RAM onto data bus.
8	Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	Used to invert relationship of assignment between display RAM column addresses and segment driver outputs. 0: CW output (forward) 1: CCW output (reverse).
9	Static Drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects normal display or static driving operation. 1: Static drive (power saving mode). 0: Normal driving.
10	Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increments column address counter by 1 when display data is written. (This is not done when data is read.)
11	END	0	1	0	1	1	1	0	1	1	1	0	Clears Read Modify Write mode.
12	Reset	0	1	0	1	1	1	0	0	0	1	0	Sets display start line register on the first line. Also sets column address counter and page address counter to 0.

1. **Display ON/OFF** - This command turns the display on and off.

2. **Display Start Line** - This command specifies a line address thus making it the line that corresponds to ROW 0. Display begins with the specified line address and covers lines in ascending order. Dynamic line address change with the Display Start Line commands enables column-wise scrolling or page change.

3. **Set Page Address** - This command is used to specify a page address equivalent to a row address for MPU access to the display data RAM. A required bit of the display data RAM can be accessed by specifying its page address and column address. Changing the page address causes no change in display.

4. **Column Address** - This command specifies the display data RAM column address. The column address is incremented by 1 each time the MPU accesses the display data RAM. Thus it is possible for the MPU to gain continuous access to only the data. The incrementing stops with address 79, the page address is not continuously changed.

5. **Read Status**

BUSY: BUSY = '1' means that system is performing an internal operation or is reset. No command is accepted before BUSY = '0'. As long as the cycle time requirement is met, no BUSY check is needed.
ADC: Indicates assignment of column addresses to segment drivers.
0: Inverted (column address 79-n segment driver n). }This bit is the reverse of the select ADC command.
1: Forward (column address n segment driver n).
ON/OFF: Indicates display on or off.
0: Display on. }This is the reverse of the Display ON/OFF command.
1: Display off.
RESET: Indicates that system is being initialized by the RES signal or the Reset command.
0: Display mode. }RES is generated internally at Power On.
1: Being reset.

6. **Write Display Data** - This command allows the MPU to write 8 bits of data into the display data RAM. Once the data is written, the column address is automatically incremented by 1, this enables the MPU to write multi-word data continuously.

7. **Read Display Data** - This command allows the MPU to read 8 bits of data from the display data RAM location specified by a column address and a page address. Once the data is read, the column address is automatically incremented by 1, this enables the MPU to read multi-word data continuously. A dummy read is needed immediately after the column address is set.

8. **Select ADC** - This command inverts the relation of assignments between display data RAM column addresses and segment driver outputs. In other words, the Select ADC command can software invert the order of segment driver output pins. Incrementing the column address by 1, which takes place after the MPU writing or reading display data, follows the sequence of column addresses.
D=0: Clockwise output (forward). D=1: Anticlockwise output (reverse).

9. **Static Drive ON/OFF** - This command forces all display to be on and, at the same time, all common output to be selected.
D=0 Static drive off. D=1: Static drive on

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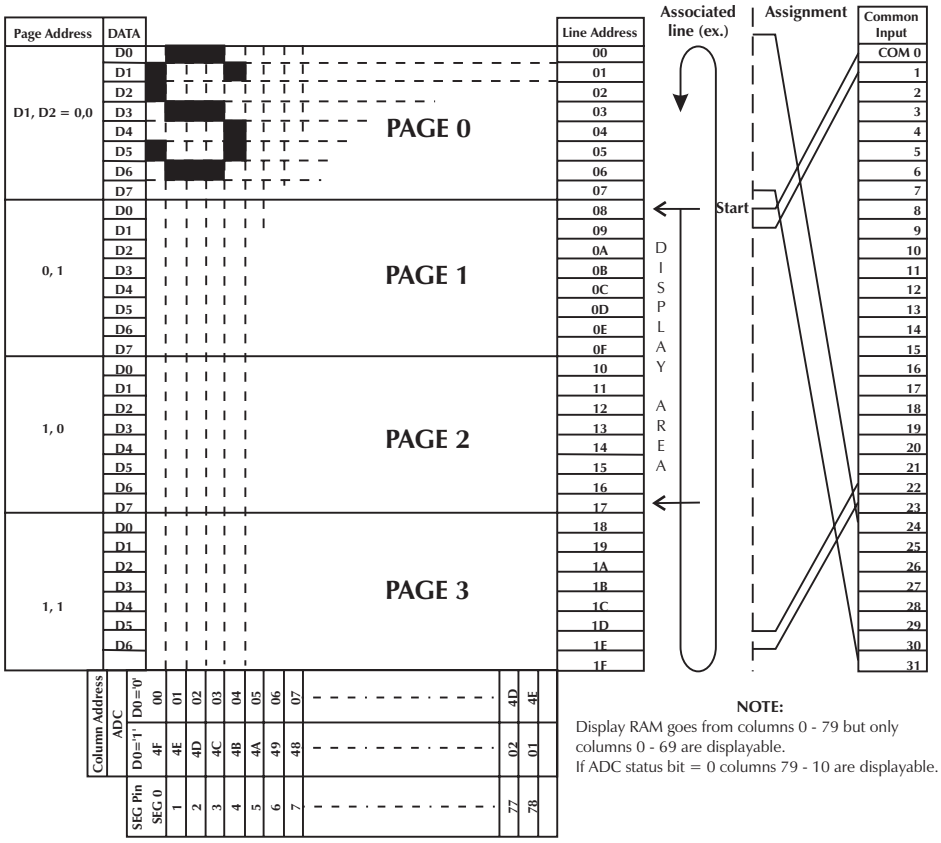
10. **Read Modify Write** - This command is used with the End command in a pair. Once it has been entered, the column address will be incremented not by the Read Display data command but by the Write Display Data command only. This mode will stay until the End command is entered. Entry of the End command causes the column address to return to the address which was valid when the Read Modify Write command was entered. This function lessens the load of the MPU when the data in a specific display area is repeatedly updated (as blinking cursor). Even in the Read Modify Write mode, any command other than Read/Write Data and Set Column Address may be used.

11. **End** - This command cancels the Read Modify Write command, returning the column address to the initial mode address.

12. **Reset** - This command initializes the display start line register, column address counter and page address counter without any effect on the display data RAM. The reset operation follows entry of the Reset command. Initialization at power-on is performed not by the Reset command but by an internal power-on Reset circuit.

Save Power (Combined Command) - Static Drive On with Display Off invokes power saving mode, reducing current consumption to nearly static current level. During this mode, the module has the following conditions:
a. It stops driving the LCD; the segment and common driver outputs are at V+ level.
b. The display data and operational mode are held. The power saving mode is cancelled by Display On or Static Drive Off. Leave Vee pin open circuit or connect to V+.

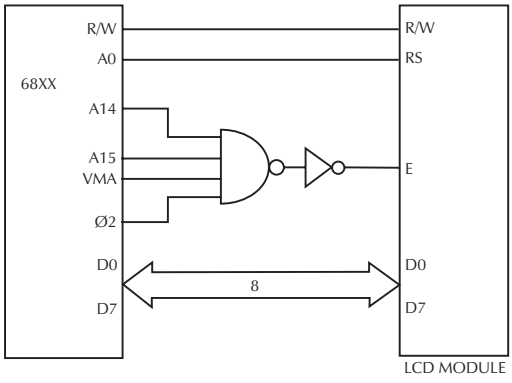
Relationship between Display Data RAM locations and Addresses - Example shows Display Start Line set to 08



NOTE:
Display RAM goes from columns 0 - 79 but only columns 0 - 69 are displayable.
If ADC status bit = 0 columns 79 - 10 are displayable.

VARIOUS OPERATING MODES

INTERFACE WITH 68XX



INTERFACE WITH 80XX SERIES