DMX 916

16 Character, 2 Line Dot Matrix Display

The DMX 916 sets new standards for dot matrix displays. It can be bolted or panel mounted using the bezel, clips and window supplied. The interface is compatible with the Hitachi LCDII/IIA standard and connection is by way of a 16 way ribbon cable connector. This is in the popular 14 pin format but with extra pins for the backlight. The unit can be optionally backlit with a simple 5V supply.

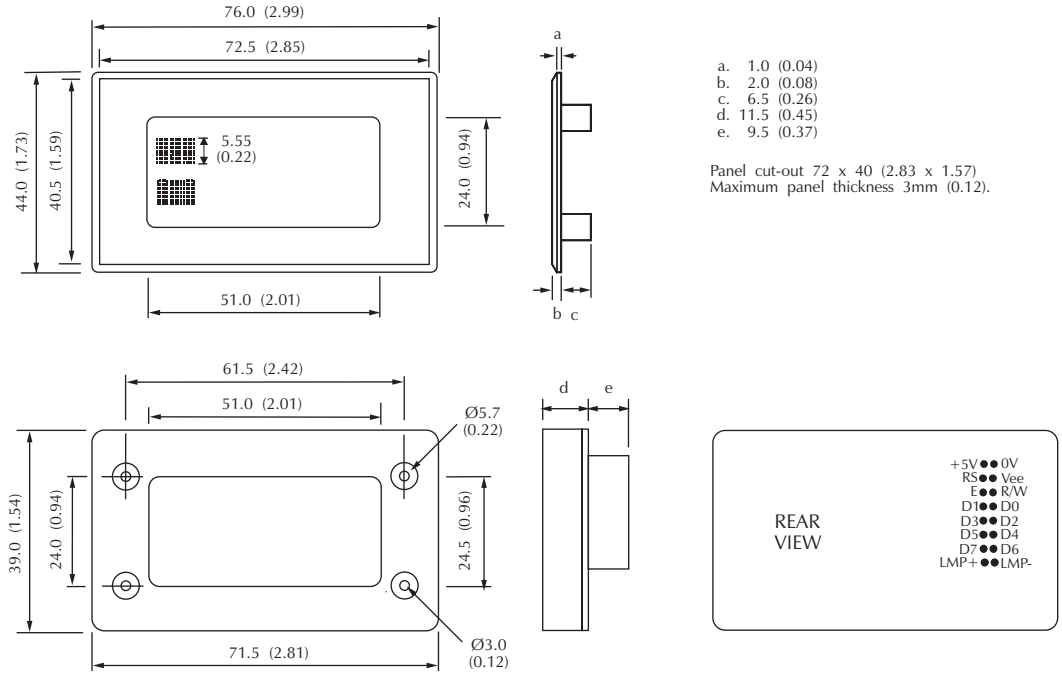
- Easy to Install
- High Contrast
- LED Backlight
- Supplied With Bezel
- HD 44780 Compatible Interface

Stock Number Standard Display				DMX 916
Specification	Symbol	Min.	Typ.	Max.	Unit
Input 'High' Voltage	VIH	2.2		Vdd	V
Input 'Low' Voltage	VIL	-0.3		0.6	V
Output 'High' Voltage	VOH	2.4			V
Output 'Low' Voltage	VOL			0.4	V
Power Supply Voltage	Vdd	4.5	5	5.5	V
Power Supply Current	Idd		0.5	5	mA
Contrast Control	Vee	-1.0	0	Vdd	V
Backlight Supply Voltage			5	5.5	V
Backlight Supply Current			50	90	mA

CONNECTOR SOURCING GUIDE

METHOD	Cable Mounting IDC Supplied With Product

DIMENSIONS All dimensions in mm (inches)



a. 1.0 (0.04)
b. 2.0 (0.08)
c. 6.5 (0.26)
d. 11.5 (0.45)
e. 9.5 (0.37)

Panel cut-out 72 x 40 (2.83 x 1.57)
Maximum panel thickness 3mm (0.12).

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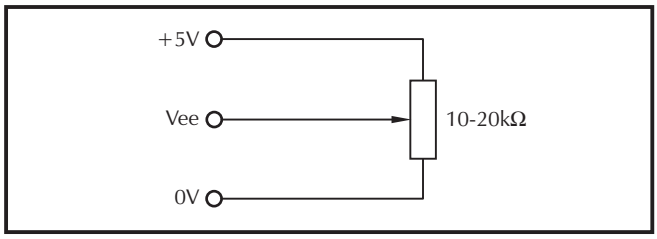
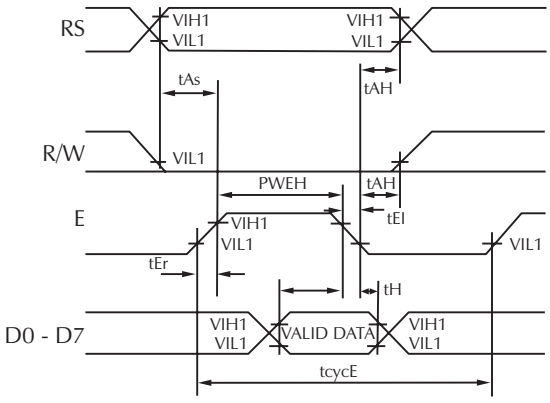
PIN FUNCTIONS

1.	0V	}Power supply.
2.	+5V	
3.	Vee	LCD contrast control input (see diagram).
4.	RS	Register Select input.
5.	R/W	Read/Write input.
6.	E	Enable signal.
7-14.	D0-D7	8Bit bi-directional µP data bus.
15.	LMP-	}Backlight supply, maximum 90mA.
16.	LMP+	



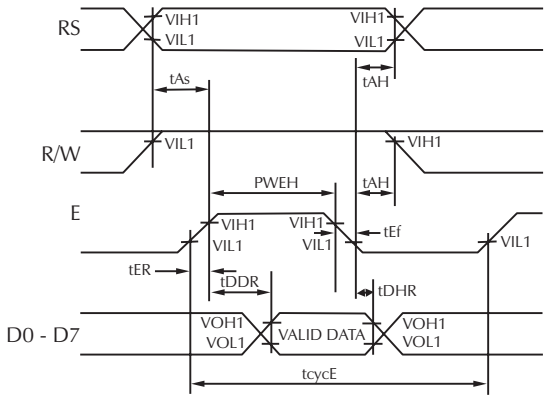
Item	Symbol		Standard Value			Unit
			Min.	Typ.	Max.	
Enable Cycle Time	tcycE	See READ and WRITE diagram	1000	-	-	nS
Enable Pulse Width, High Level	PWEH	See READ and WRITE diagram	450	-	-	nS
Enable Rise and Decay Time	tEr, tEf	See READ and WRITE diagram	-	-	25	nS
Address Setup Time, RS, R/W, -E	tAs	See READ and WRITE diagram	140	-	-	nS
Data Delay Time	tDDR	See WRITE diagram	-	-	320	nS
Data Setup Time	tDSW	See READ diagram	195	-	-	nS
Data Hold Time	tH	See READ diagram	10	-	-	nS
Data Hold Time	tDHR	See WRITE diagram	20	-	-	nS
Address Hold Time	tAH	See READ and WRITE diagram	10	-	-	nS

WRITE OPERATION



(Write Data from MPU to MODULE)

READ OPERATION



(Read Data from MODULE to MPU)

INSTRUCTIONS

Instruction	Code										Description	Execute Time (Maximum)
	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (Address 0).	1.64mS
Cursor at Home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (Address 0). Also returns the display being shifted to the original position. DD RAM contents remain unchanged.	1.64mS
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies whether or not to shift the display. These operations are performed during data write and read.	40µS
Display On/Off control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of all display (D) cursor ON/OFF (C) and blink of cursor position character (B).	40µS
Cursor/Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without changing DD RAM contents.	40µS
Function Set	0	0	0	0	1	DL	L	F	*	*	Sets interface data length (DL) number of display line (L) and character font (F).	40µS
CG RAM Address Set	0	0	0	1	ACG						Sets the CG RAM address. CG RAM data is sent and received after this setting.	40µS
DD RAM Address Setting	0	0	1	ADD							Sets the DD RAM address. DD RAM is sent and received after this setting.	40µS
Busy Flag/Address Read	0	1	BF	AC							Reads Busy Flag (BF) indicating internal operation is being performed and reads address counter contents.	40µS
CG RAM/DD RAM Data Write	1	0	WRITE DATA								Writes data into DD RAM or CG RAM.	40µS
CG RAM/DD RAM Data Read	1	1	READ DATA								Reads data from DD RAM or CG RAM	40µS

Clear Display -
Writes the space code (20 hex) to all DD RAM addresses. The cursor returns to Address 0 and the display, if it has been shifted, will return to its original position. Because all the DD RAM contents have 20 written to them, this instruction should not be used if general data is kept in "Invisible" DD memory.

Entry Mode Select
I/D: Increments (I/D=1) or decrements (I/D=0) the DD Ram address by one upon writing into or reading from the DD RAM a character. The same applies when writing to and reading from the CG RAM. The advantage of this instruction is that you do not need to set the DD RAM or CG RAM address between each data entry if the data is sent in the correct order.
S: When S=0 the display stays still and the cursor moves to the left or right (CG RAM address up or down) depending on I/D status. When S=1 the cursor does not move but the display shifts to the left or right according to I/D status. Writing to or reading from CG RAM is not affected by S status.

Cursor or Display Shift
The instruction will shift either the cursor or the display to the right or the left without writing to or reading from the display. It has to be executed for as many times as shifts are required.
S/C=1 The display shifts. S/C=0 The cursor shifts R/L=1 Shift to the right. R/L=0 Shift to the left.

Display ON/OFF Control
D. Display is turned ON when D=1 and OFF when D=0. When the display is turned off due to D=0, the display data remains in the DD RAM and it can be displayed immediately by setting D=1.

C. The cursor is displayed when C=1 and not displayed when C=0. Even if the cursor disappears, the function of I/D etc. does not change during display data write. The cursor is displayed using 5 dots in the 8th line when the 5x7 character font is selected.

B. The character residing at the cursor position blinks when B=1. The blink is done by switching between all the black dots and display characters at 0.4 second intervals. The cursor and the blink can be set concurrently.

Function Set
The DMX 916 can be operated in a four or eight bit data entry mode.
DL=1. Data is read or written in eight bits.
DL=0. Data is read or written in four bits on DB7 - DB4. Upper nibble first, lower second.
N. Sets either 1-line (N=0) or 2-line (N=1) operation. Use N=1 for DMX 916.
F. Sets either 5x7 (F=0) or 5x10 (F=1) character font. Use F=0 for DMX 916.

Set CG RAM Address
Sets the CG RAM address in a binary number of ACG in the address counter. All data read/write operations access the CG RAM afterwards.

Set DD RAM Address
Sets the DD RAM address in a binary number of ADD in the address counter. All data read/write operations access the DD RAM afterwards.

Read Busy Flag and Address
This instruction will read the busy flag and either the DD or CG address (determined by the previous Address Set).
BF=1. The DMX is busy executing the previous instruction. The next instruction will not be accepted until BF=0. The address contents (AC) are those of CG RAM and DD RAM previously shown.

Write Data to CG or DD RAM
Writes binary data to the CG or the DD RAM. Whether the CG or the DD RAM is to be written into is determined by the previous Address Set. After write, the address is automatically incremented or decremented by one according to the entry mode. Display shift also follows the entry mode.

Read Data from CG or DD RAM
Will read data from the CG or DD ram (determined by the previous Address Set). Ensure that the required RAM address is set before executing this instruction. After the read instruction, the address will automatically be incremented or decremented according to the entry mode. Display shift, however, is not performed regardless of entry mode types.

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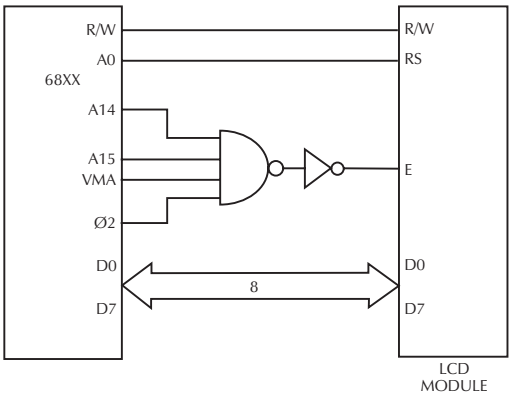
FONT TABLE

NOTE -Characters with lower case descenders e.g. μ, β etc. will only be partially displayed by the DMX 916.

VARIOUS OPERATING MODES

INTERFACE WITH 68XX



INTERFACE WITH 80XX SERIES