

HIGH TEMPERATURE EDGE-TRIGGERED D FLIP-FLOP FAMILY

FEATURES

- ▲ Wide operating supply voltage from 2.8V to 5.5V.
- ▲ Operational beyond the -60°C to +230°C temperature range.
- ▲ Up to ±8mA output drive.
- ▲ Schmitt-Trigger Inputs allow better switching noise immunity.
- ▲ Ruggedized SMT packages.
- ▲ Also available as bare die.

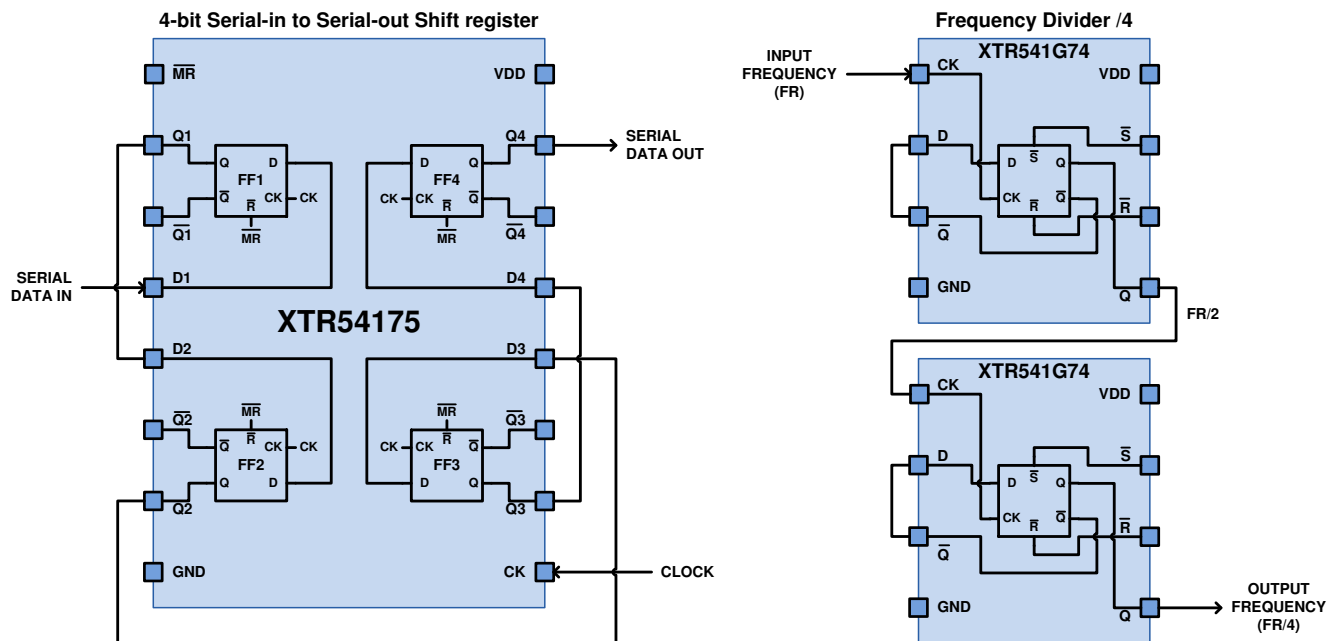
APPLICATIONS

- ▲ Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole.

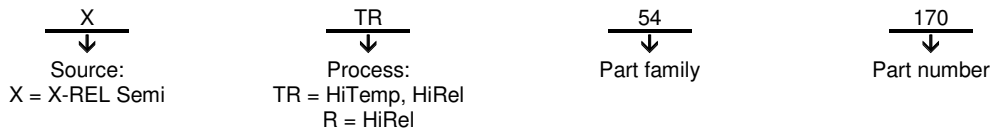
DESCRIPTION

The XTR54170 is a family of positive-edge-triggered D-type flip-flops. XTR54175 have four D-type flip-flops with individual data input D and both Q and \bar{Q} outputs. The common clock CK and master reset \bar{MR} inputs trigs and resets all flip-flops simultaneously. XTR541G74 have a single D-type flip-flop with data D and clock CK inputs, Q and \bar{Q} outputs, and set \bar{S} and reset \bar{R} inputs. Parts from the XTR54170 family are available in ruggedized SMT and through-hole packages. Parts are also available as bare dies.

PRODUCT HIGHLIGHTS



ORDERING INFORMATION



Product Reference	Temperature Range	Package	Pin Count	Marking
XTR54170-BD	-60°C to +230°C	Bare die		XTR54170
XTR54175-S	-60°C to +230°C	Ceramic SOIC	16	XTR54175
XTR54175-D	-60°C to +230°C	Side braze DIP	16	XTR54175
XTR541G74-F	-60°C to +230°C	Flatpack with exposed pad	8	XTR541G74
XTR541G74-D	-60°C to +230°C	Side braze DIP	8	XTR541G74

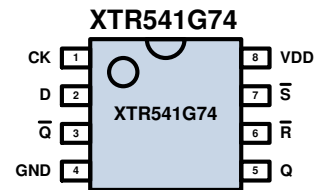
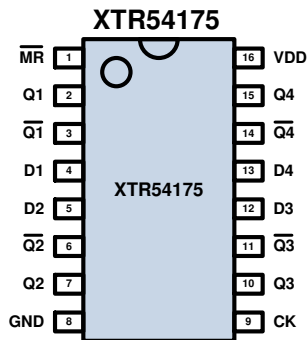
Other packages and packaging configurations possible upon request.

ABSOLUTE MAXIMUM RATINGS

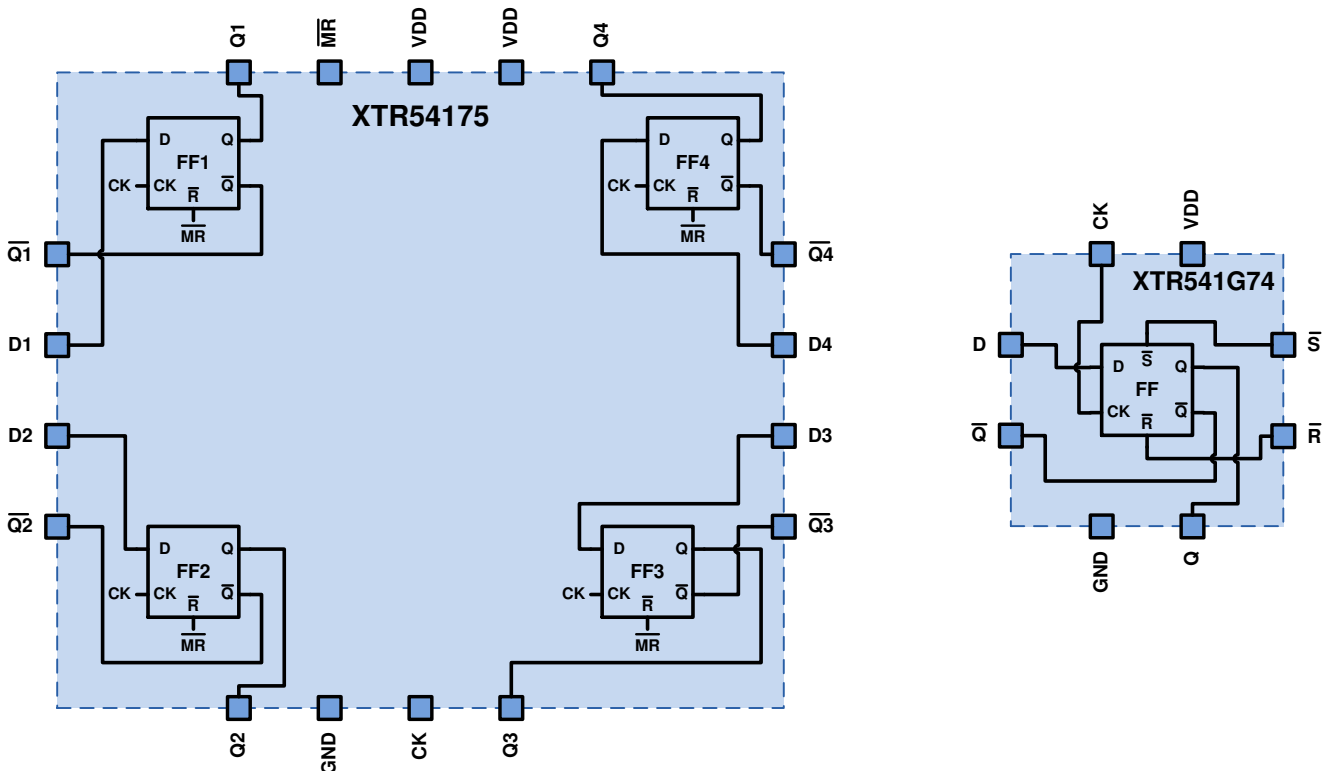
Voltage on any pin to GND	-0.5 to 6.0V
Storage Temperature Range	-70°C to +230°C
Operating Junction Temperature Range	-70°C to +300°C
ESD Classification	1kV HBM MIL-STD-883

Caution: Stresses beyond those listed in “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to “ABSOLUTE MAXIMUM RATINGS” conditions for extended periods may permanently affect device reliability.

PRODUCT VARIANTS



BLOCK DIAGRAM



Please contact X-REL for XTR74170-BD block diagram and die information.

PIN DESCRIPTION

XTR54175		
Pin Number	Name	Description
1	MR	Master reset, which resets all flip-flops simultaneously
2	Q1	Non-inverting output of FF1
3	$\bar{Q}1$	Inverting output of FF1
4	D1	Schmitt-Triggered input of FF1
5	D2	Schmitt-Triggered input of FF2
6	$\bar{Q}2$	Inverting output of FF2
7	Q2	Non-inverting output of FF2
8	GND	Negative supply voltage
9	CK	Positive edge trigger input of all flip-flops.
10	Q3	Non-inverting output of FF3
11	$\bar{Q}3$	Inverting output of FF2
12	D3	Schmitt-Triggered input of FF3
13	D4	Schmitt-Triggered input of FF4
14	$\bar{Q}4$	Inverting output of FF4
15	Q4	Non-inverting output of FF4
16	VDD	Positive supply voltage

XTR541G74		
Pin Number	Name	Description
1	CK	Positive edge trigger input
2	D	Schmitt-Triggered input of FF
3	\bar{Q}	Inverting output of FF
4	GND	Negative supply voltage
5	Q	Non-inverting output of FF
6	\bar{R}	Schmitt-Triggered reset input of FF
7	\bar{S}	Schmitt-Triggered set input of FF
8	VDD	Positive supply voltage

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Supply voltage VDD-GND	2.8		5.5	V
Voltage on D1, D2, D3, D4, D, \bar{MR} , R, \bar{S} , CK	0 ¹		VDD ¹	V
Junction Temperature ² T_j	-60		230	°C

¹ During transient operation, these pins can reach values under 0V and above VDD. Extreme values are limited by internal clamping diodes to GND and to VDD.

² Operation beyond the specified temperature range is achieved.

ELECTRICAL SPECIFICATIONS
XTR54175 ELECTRICAL SPECIFICATIONS

 Unless otherwise stated, specification applies for $-60^{\circ}\text{C} < T_j < 230^{\circ}\text{C}$.

Parameter	Condition	Min	Typ	Max	Units
Supply voltage					
VDD		2.8		5.5	V
Input voltage					
High-level Input Voltage V_{IH}	VDD=2.8V VDD=3.3V VDD=5V VDD=5.5V	2.1 2.4 3.6 3.8			V
Low-level Input Voltage V_{IL}	VDD=2.8V VDD=3.3V VDD=5V VDD=5.5V			0.9 1.0 1.6 1.8	V
Output voltage					
High-level Output Voltage V_{OH}	VDD=2.8V, $I_{OUT}=4\text{mA}$ (sink) VDD=3.3V, $I_{OUT}=6\text{mA}$ (sink) VDD=5V, $I_{OUT}=8\text{mA}$ (sink) VDD=5.5V, $I_{OUT}=8\text{mA}$ (sink)	2.5 2.95 4.7 5.2			V
Low-level Output Voltage V_{OL}	VDD=2.8V, $I_{OUT}=4\text{mA}$ (source) VDD=3.3V, $I_{OUT}=6\text{mA}$ (source) VDD=5V, $I_{OUT}=8\text{mA}$ (source) VDD=5.5V, $I_{OUT}=8\text{mA}$ (source)	220 250 200 180			mV
Timing Requirements					
Clock Frequency f_{CK}	VDD=2.8V VDD=3.3V VDD=5V			10 15 20	MHz
Clock Pulse-width t_w	VDD=2.8V VDD=3.3V VDD=5V	15 10 5			ns
Setup Time t_{SU}	VDD=2.8V VDD=3.3V VDD=5V	3 3 2			ns
Hold Time t_{HD}	VDD=2.8V VDD=3.3V VDD=5V	8 6 3			ns
Master Reset Pulse-width t_{w_MR}	VDD=2.8V VDD=3.3V VDD=5V	25 20 12			ns
Removal Time t_{REM}	\overline{MR} going inactive to rising edge of CK VDD=2.8V VDD=3.3V VDD=5V	20 15 6			ns
Switching Characteristics					
Propagation Delay from CK to Q or \overline{Q} t_{PD_CK}	VDD=2.8V VDD=3.3V VDD=5V	24 15 8		70 50 26	ns
Rise Time Q or \overline{Q} t_{RISE}	VDD=2.8V VDD=3.3V VDD=5V	7 5 3		20 15.5 9	ns
Fall Time Q or \overline{Q} t_{FALL}	VDD=2.8V VDD=3.3V VDD=5V	8 5.5 3.3		21 16.5 9	ns
Propagation Delay from MR to Q or \overline{Q} t_{PD_MR}	VDD=2.8V VDD=3.3V VDD=5V	23 15 8		66 47 24	ns

XTR541G74 ELECTRICAL SPECIFICATIONS

 Unless otherwise stated, specification applies for $-60^{\circ}\text{C} < T_j < 230^{\circ}\text{C}$.

Parameter	Condition	Min	Typ	Max	Units
Supply voltage					
VDD		2.8		5.5	V
Input voltage					
High-level Input Voltage V_{IH}	VDD=2.8V VDD=3.3V VDD=5V VDD=5.5V	2.1 2.4 3.6 3.8			V
Low-level Input Voltage V_{IL}	VDD=2.8V VDD=3.3V VDD=5V VDD=5.5V			0.9 1.0 1.6 1.8	V
Output voltage					
High-level Output Voltage V_{OH}	VDD=2.8V, $I_{OUT}=4\text{mA}$ (sink) VDD=3.3V, $I_{OUT}=6\text{mA}$ (sink) VDD=5V, $I_{OUT}=8\text{mA}$ (sink) VDD=5.5V, $I_{OUT}=8\text{mA}$ (sink)	2.5 2.95 4.7 5.2			V
Low-level Output Voltage V_{OL}	VDD=2.8V, $I_{OUT}=4\text{mA}$ (source) VDD=3.3V, $I_{OUT}=6\text{mA}$ (source) VDD=5V, $I_{OUT}=8\text{mA}$ (source) VDD=5.5V, $I_{OUT}=8\text{mA}$ (source)	220 250 200 180			mV
Timing Requirements					
Clock Frequency f_{CK}	VDD=2.8V VDD =3.3V VDD=5V			10 15 20	MHz
Clock Pulse-width t_w	VDD=2.8V VDD=3.3V VDD=5V	15 10 5			ns
Setup Time t_{SU}	VDD=2.8V VDD =3.3V VDD=5V	6 4 3			ns
Hold Time t_{HD}	VDD=2.8V VDD=3.3V VDD=5V	10 6 3			ns
Set or Reset Pulse-width t_{W_SR}	VDD=2.8V VDD=3.3V VDD=5V	25 20 12			ns
Removal Time t_{REM}	\bar{R} or \bar{S} going inactive to rising edge of CK VDD=2.8V VDD=3.3V VDD=5V	20 15 6			ns
Switching Characteristics					
Propagation Delay from CK to Q or \bar{Q} t_{PD_CK}	VDD=2.8V VDD=3.3V VDD=5V	24 15 8		70 50 26	ns
Rise Time Q or \bar{Q} t_{RISE}	VDD=2.8V VDD=3.3V VDD=5V	7 5 3		20 15.5 9	ns
Fall Time Q or \bar{Q} t_{FALL}	VDD=2.8V VDD=3.3V VDD=5V	8 5.5 3.3		21 16.5 9	ns
Propagation Delay from \bar{S} or \bar{R} to Q or \bar{Q} t_{PD_SR}	VDD=2.8V VDD=3.3V VDD=5V	23 14 7		70 51 28	ns

THEORY OF OPERATION

Introduction

The XTR54170 is a family of positive-edge-triggered D-type flip-flops.

XTR54175 have four D-type flip-flops with individual data input D and both Q and \bar{Q} outputs. The common clock CK and master reset \overline{MR} inputs trigs and resets all flip-flops simultaneously.

XTR541G74 have a single D-type flip-flop with data D and clock CK inputs, Q and \bar{Q} outputs, and set \bar{S} and reset \bar{R} inputs.

XTR54175 operation

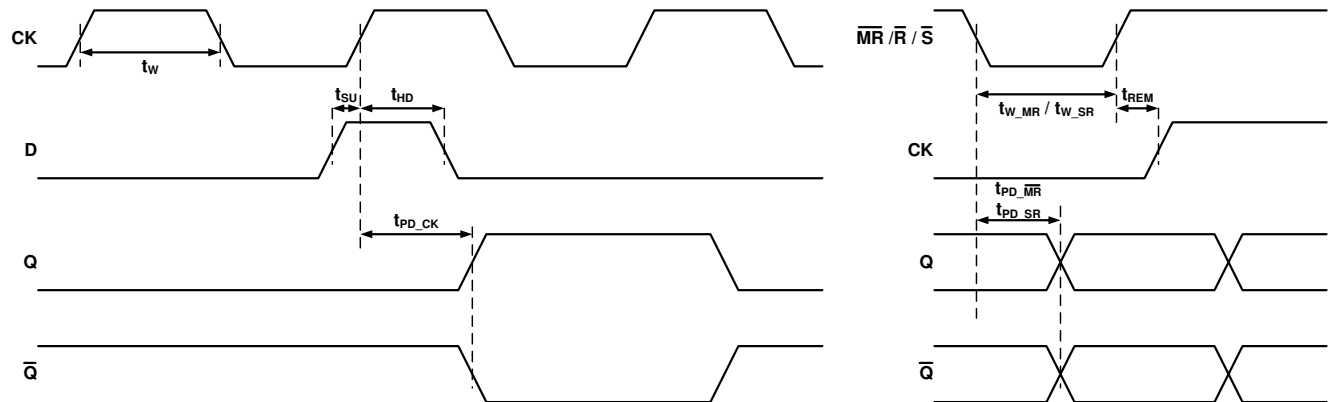
The XTR54175 architecture (for one flip-flop) is shown in the figure below.

A low level at the master reset (\overline{MR}) input reset the outputs, regardless of the levels of the other inputs. When \overline{MR} is inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

Truth Table

INPUTS			OUTPUTS	
\overline{MR}	CK	D	Q	\bar{Q}
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	\bar{Q}_0

Timing definition



XTR541G74 operation

The XTR541G74 architecture is shown in the figure below.

A low level at the set (\bar{S}) or reset (\bar{R}) inputs sets or resets the outputs, regardless of the levels of the other inputs. When \bar{S} and reset \bar{R} are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

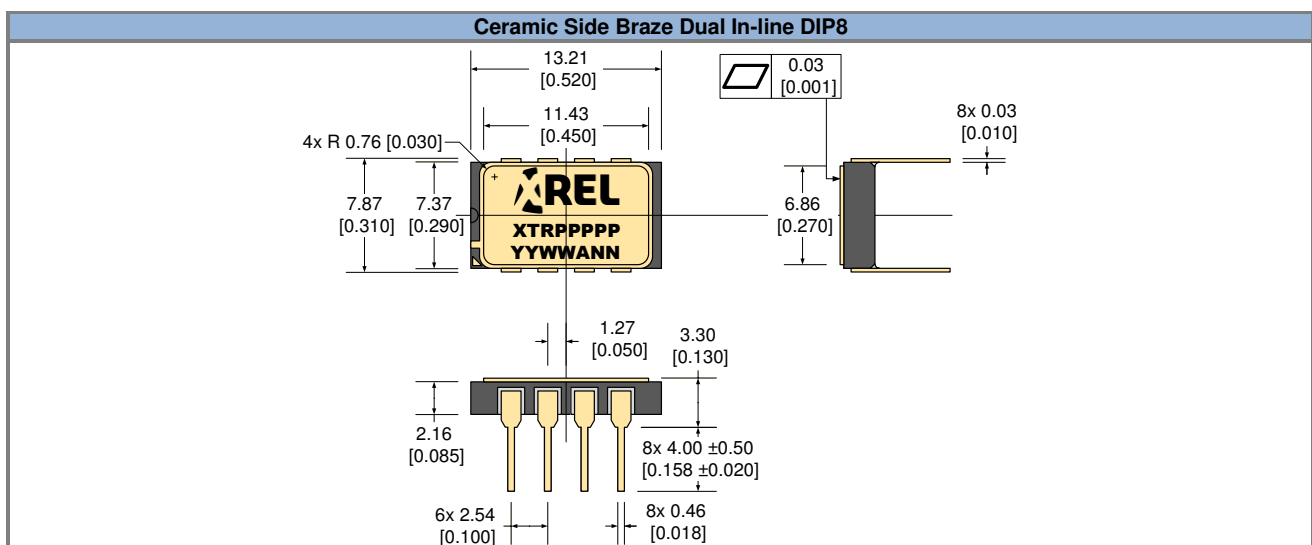
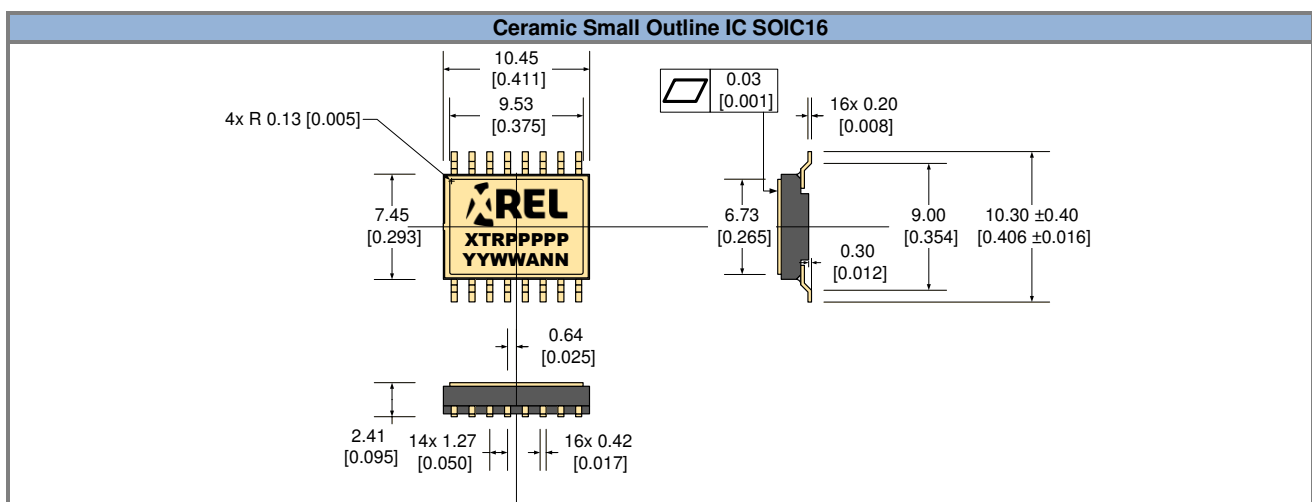
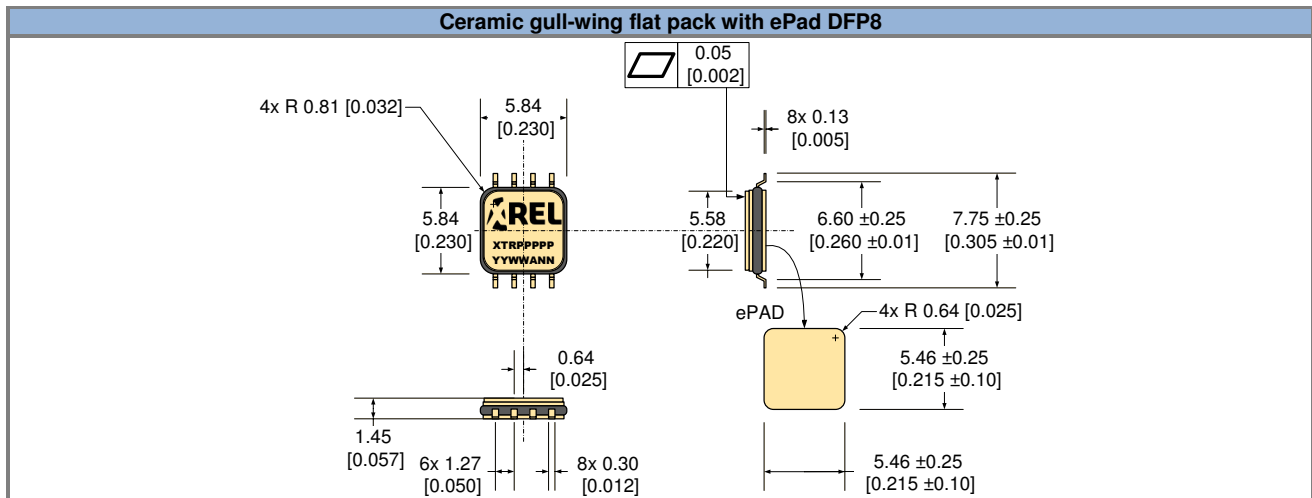
Truth Table

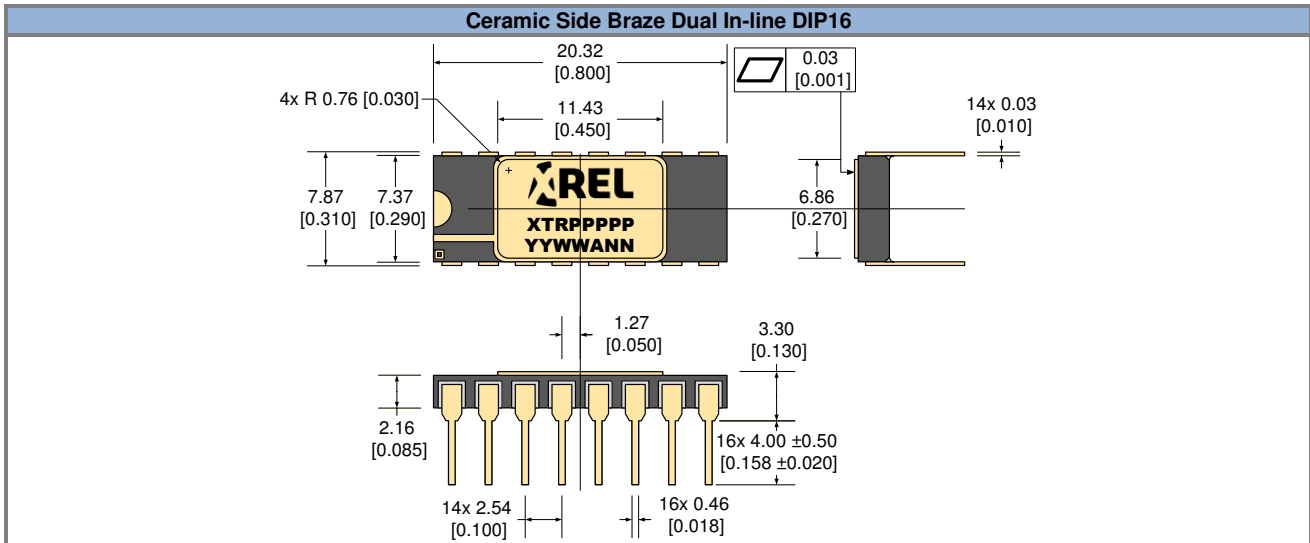
INPUTS				OUTPUTS	
\bar{S}	\bar{R}	CK	D	Q	\bar{Q}
L	L	X	X	L ¹	L ¹
L	H	X	X	H	L
H	L	X	X	L	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	\bar{Q}_0

¹ Outputs in this configuration will not persist when \bar{S} or \bar{R} returns to its inactive (HIGH) level. To guarantee known outputs when removing this state, make sure one of \bar{S} or \bar{R} remains in LOW state for at least a removal time.

PACKAGE OUTLINES

Dimensions shown in mm [inches].





Part Marking Convention	
Part Reference: XTRPPPPP	
XTR	X-REL Semiconductor, high-temperature, high-reliability product (XTRM Series).
PPPPP	Part number (0-9, A-Z).
Unique Lot Assembly Code: YYWWANN	
YY	Two last digits of assembly year (e.g. 11 = 2011).
WW	Assembly week (01 to 52).
A	Assembly location code.
NN	Assembly lot code (01 to 99).

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