HIGH TEMPERATURE BIDIRECTIONAL LEVEL TRANSLATORS FAMILY

FEATURES

▲ Supply voltage from 2.5V to 5.5V.
▲ Operational beyond the -60℃ to +230℃ temperature range.
▲ OE/DIR input can be referenced to VCCA or VCCB.
▲ Up to ±8mA output drive (Directional).
▲ Max Data Rates (Bidirectional)
- 8Mbps (Translate to 5V)
- 6Mbps (Translate to 3.3V)
- 4Mbps (Translate to 2.5V)

▲ Max Data Rates (Directional)
- 30Mbps (3.3 to 5V)
- 20Mbps (2.5 to 5V)
- 15Mbps (Translate to 3.3V)
- 10Mbps (Translate to 2.5V)

▲ Ruggedized SMT packages.
▲ Also available as bare die.

APPLICATIONS

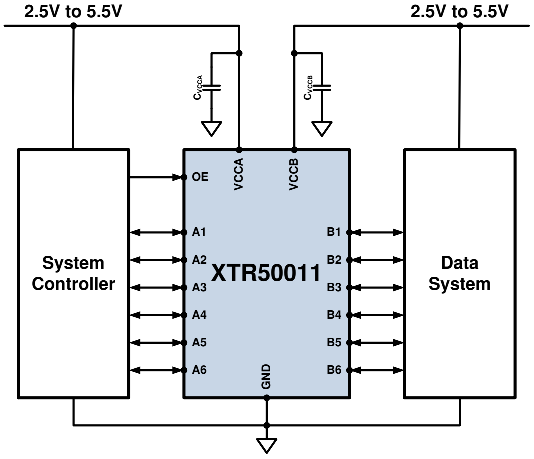
▲ Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole.
▲ Level shifted data transmission.

DESCRIPTION

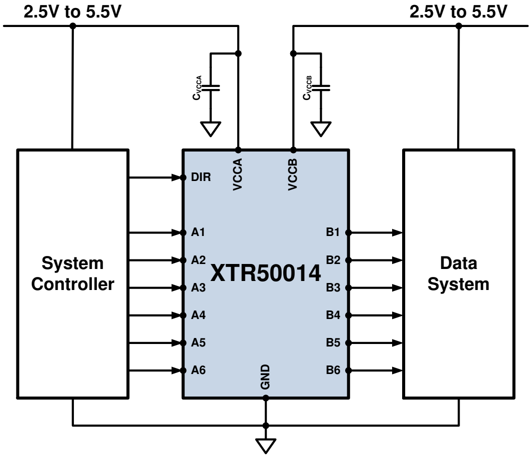
The XTR50010 is a family of bidirectional level translators that can be used for data communication between devices or systems operating at different supply voltages. XTR50010 is able to operate from -60℃ to +230℃, with supply voltages from 2.5V to 5.5V.
In XTR50011 or XTR50012, the communication direction between An and Bn ports are automatically and independently sensed by the circuit. This allows simultaneous data flow in any direction.
In XTR50014 or XTR50015, the DIR logic-level input is used to control the data flow direction. The DIR input can be powered by either VCCA or VCCB. This brings more flexibility at system level.
Parts from the XTR50010 family are available in ruggedized SMT and through-hole packages. Parts are also available as bare dies.

PRODUCT HIGHLIGHT

Bidirectional data transmission



Directional data transmission



ORDERING INFORMATION

X	TR	50	010
Source: X = X-REL Semi	Process: TR = HiTemp, HiRel; R = HiRel	Part family	Part number

Product Reference	Temperature Range	Package	Pin Count	Marking
XTR50010-BD	-60℃ to +230℃	Bare die		XTR50010
XTR50011-S	-60℃ to +230℃	Ceramic SOIC	16	XTR50011
XTR50011-D	-60℃ to +230℃	Ceramic side braze DIP	16	XTR50011
XTR50012-FE	-60℃ to +230℃	Gull-wing flat pack with ePad	8	XTR50012
XTR50012-D	-60℃ to +230℃	Ceramic side braze DIP	8	XTR50012
XTR50014-S	-60℃ to +230℃	Ceramic SOIC	16	XTR50014
XTR50014-D	-60℃ to +230℃	Ceramic side braze DIP	16	XTR50014
XTR50015-FE	-60℃ to +230℃	Gull-wing flat pack with ePad	8	XTR50015
XTR50015-D	-60℃ to +230℃	Ceramic side braze DIP	8	XTR50015

Other packages and packaging configurations possible upon request. Contact X-REL for plastic packaged parts.

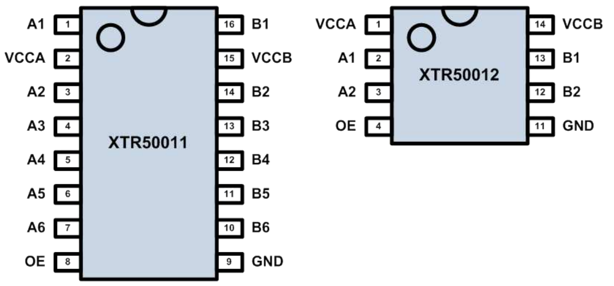
ABSOLUTE MAXIMUM RATINGS

Voltage on any pin to GND	-0.5 to 6.0V
Storage Temperature Range	-70°C to +230°C
Operating Junction Temperature Range	-70°C to +300°C
ESD Classification	1kV HBM MIL-STD-883

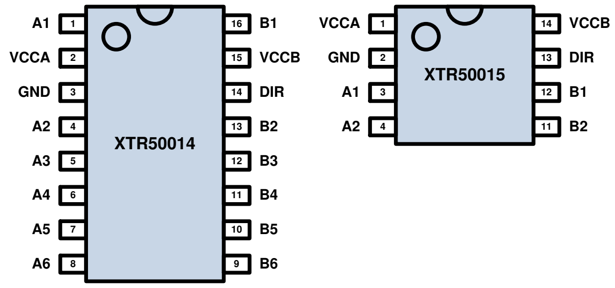
Caution: Stresses beyond *those listed in* "ABSOLUTE MAXIMUM RATINGS" *may cause permanent damage to the device. These are* stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of *the specifications is not implied. Exposure to* "ABSOLUTE MAXIMUM RATINGS" *conditions for extended periods may* permanently affect device reliability.

PRODUCT VARIANTS

Bidirectional versions

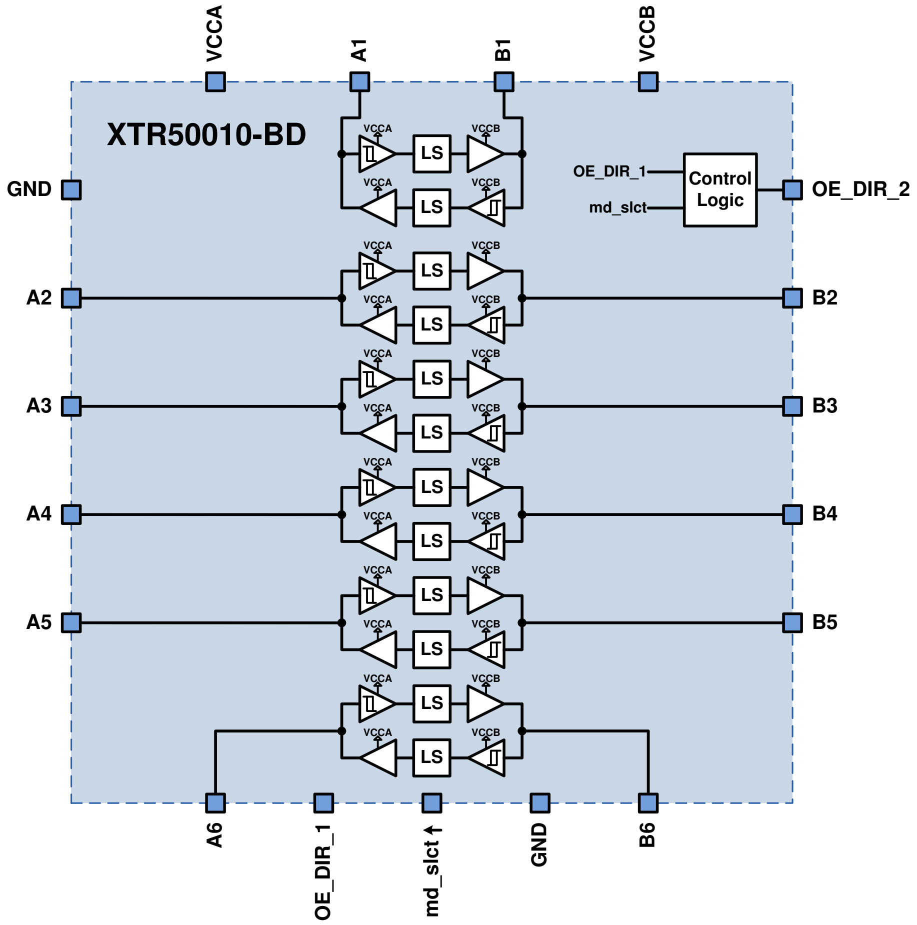


Directional versions



For FE package option, ePAD connected to GND

BLOCK DIAGRAM: XTR50010-BD



Arrows aside pad names indicate whether the input is internally pulled up or down.

PIN DESCRIPTION

XTR50011 – 6 Channel bidirectional		
Pin Number	**Name**	**Description**
1	A1	Bidirectional input/output with respect to B1 input/output.
2	VCCA	Supply voltage of An input/output.
3	A2	Bidirectional input/output with respect to B2 input/output.
4	A3	Bidirectional input/output with respect to B3 input/output.
5	A4	Bidirectional input/output with respect to B4 input/output.
6	A5	Bidirectional input/output with respect to B5 input/output.
7	A6	Bidirectional input/output with respect to B1 input/output.
8	OE	Output enable pin. When driven low, it puts all the outputs An, Bn to high impedance. OE pin can be referenced either to VCCA or VCCB.
9	GND	Common ground of VCCA and VCCB supplies.
10	B6	Bidirectional input/output with respect to A6 input/output.
11	B5	Bidirectional input/output with respect to A5 input/output.
12	B4	Bidirectional input/output with respect to A4 input/output.
13	B3	Bidirectional input/output with respect to A3 input/output.
14	B2	Bidirectional input/output with respect to A2 input/output.
15	VCCB	Supply voltage of Bn input/output.
16	B1	Bidirectional input/output with respect to A1 input/output.

XTR50012 – 2 Channel bidirectional		
Pin Number	**Name**	**Description**
1	VCCA	Supply voltage of An input/output.
2	A1	Bidirectional input/output with respect to B1 input/output.
3	A2	Bidirectional input/output with respect to B2 input/output.
4	OE	Output enable pin. When driven low, it puts all the outputs An, Bn to high impedance. OE pin can be referenced either to VCCA or VCCB.
5	GND	Common ground of VCCA and VCCB supplies.
6	B2	Bidirectional input/output with respect to A2 input/output.
7	B1	Bidirectional input/output with respect to A1 input/output.
8	VCCB	Supply voltage of Bn input/output.

XTR50014 – 6 Channel directional		
Pin Number	**Name**	**Description**
1	A1	Bidirectional input/output with respect to B1 input/output. Data direction is set with DIR pin.
2	VCCA	Supply voltage of An inputs/outputs.
3	GND	Common ground of VCCA and VCCB supplies.
4	A2	Bidirectional input/output with respect to B2 input/output. Data direction is set by DIR pin.
5	A3	Bidirectional input/output with respect to B3 input/output. Data direction is set by DIR pin.
6	A4	Bidirectional input/output with respect to B4 input/output. Data direction is set by DIR pin.
7	A5	Bidirectional input/output with respect to B5 input/output. Data direction is set by DIR pin.
8	A6	Bidirectional input/output with respect to B4 input/output. Data direction is set by DIR pin.
9	B6	Bidirectional input/output with respect to A6 input/output. Data direction is set by DIR pin.
10	B5	Bidirectional input/output with respect to A5 input/output. Data direction is set by DIR pin.
11	B4	Bidirectional input/output with respect to A4 input/output. Data direction is set by DIR pin.
12	B3	Bidirectional input/output with respect to A3 input/output. Data direction is set by DIR pin.
13	B2	Bidirectional input/output with respect to A2 input/output. Data direction is set by DIR pin.
14	DIR	Sets the data direction between An and Bn input/output. If DIR pin is driven high the data direction is from An to Bn. If DIR pin is driven low the data direction is from Bn to An. DIR pin can be referenced either to VCCA or VCCB.
15	VCCB	Supply voltage of Bn input/output.
16	B1	Bidirectional input/output with respect to A1 input/output. Data direction is set by DIR pin.

XTR50015 – 2 Channel directional		
Pin Number	**Name**	**Description**
1	VCCA	Supply voltage of An input/output.
2	GND	Common ground of VCCA and VCCB supplies.
3	A1	Bidirectional input/output with respect to B1 input/output. Data direction must be set with DIR pin.
4	A2	Bidirectional input/output with respect to B2 input/output. Data direction must be set with DIR pin.
5	B2	Bidirectional input/output with respect to A2 input/output. Data direction must be set with DIR pin.
6	B1	Bidirectional input/output with respect to A1 input/output. Data direction must be set with DIR pin.
7	DIR	Sets the data direction between An and Bn input/output. If DIR pin is driven high the data direction is from An to Bn. If DIR pin is driven low the data direction is from Bn to An. DIR pin can be referenced either to VCCA or VCCB.
8	VCCB	Supply voltage of Bn input/output.

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Supply voltage **VCCA/VCCB**	2.5		5.5	V
Voltage on An, Bn	0[1]		VCCA/VCCB[1]	V
Voltage on OE, DIR	0[1]		max(VCCA,VCCB)[1]	V
Junction Temperature[2] $\mathbf{T_j}$	-60		230	°C

[1] During transient operation, SW and OCS can reach values under 0V and above VIN. Extreme values are limited by internal clamping diodes to GND and to VCCA/VCCB.
[2] Operation beyond the specified temperature range is achieved.

ELECTRICAL SPECIFICATIONS

XTR50011/XTR50012 ELECTRICAL SPECIFICATIONS

Unless otherwise stated, specification applies for -60℃<T_j<230℃.

Parameter	Condition	Min	Typ	Max	Units
Supply voltage					
VCCA		2.5		5.5	V
VCCB		2.5		5.5	V
Quiescent current	on VCCA+VCCB supplies, T_{amb}=25℃, OE high		20		µA
	on VCCA+VCCB supplies, T_{amb}=25℃, OE low		10		µA
Input voltage					
High-level Input Voltage V_{IH}	VCCA/VCCB=2.5V	1.8			V
	VCCA/VCCB=3.3V	2.5			V
	VCCA/VCCB=5V	2.75			V
	VCCA/VCCB=5.5V	2.85			V
Low-level Input Voltage V_{IL}	VCCA/VCCB=2.5V			0.8	V
	VCCA/VCCB=3.3V			1.3	V
	VCCA/VCCB=5V			1.8	V
	VCCA/VCCB=5.5V			1.9	V
Output voltage					
High-level Output Voltage V_{OH}	VCCA/VCCB=2.5V, I_{OUT}=20µA (sink)	2.22			V
	VCCA/VCCB=3.3V, I_{OUT}=20µA (sink)	3.03			
	VCCA/VCCB=5V, I_{OUT}=20µA (sink)	4.73			
	VCCA/VCCB=5.5V, I_{OUT}=20µA (sink)	5.23			
Low-level Output Voltage V_{OL}	VCCA/VCCB=2.5V, I_{OUT}=20µA (source)	278			mV
	VCCA/VCCB=3.3V, I_{OUT}=20µA (source)	272			
	VCCA/VCCB=5V, I_{OUT}=20µA (source)	271			
	VCCA/VCCB=5.5V, I_{OUT}=20µA (source)	270			
Switching Characteristics					
Propagation delay t_{PD}	A to B, VCCA=2.5V, VCCB=2.5V, C_{OUT}=50pF	29		71	ns
	A to B, VCCA=2.5V, VCCB=3.3V, C_{OUT}=50pF	25		52	ns
	A to B, VCCA=2.5V, VCCB=5V, C_{OUT}=50pF	18		44	ns
	A to B, VCCA=3.3V, VCCB=2.5V, C_{OUT}=50pF	26		60	ns
	A to B, VCCA=3.3V, VCCB=3.3V, C_{OUT}=50pF	17		42	ns
	A to B, VCCA=3.3V, VCCB=5V, C_{OUT}=50pF	12		30	ns
	A to B, VCCA=5V, VCCB=2.5V, C_{OUT}=50pF	18		53	ns
	A to B, VCCA=5V, VCCB=3.3V, C_{OUT}=50pF	12		35	ns
	A to B, VCCA=5V, VCCB=5V, C_{OUT}=50pF	8		23	ns
OE Propagation delay t_{PD_LH}	OE to A, VCCA=2.5V, VCCB=2.5-5V, C_{OUT}=50pF	24		66	ns
	OE to A, VCCA=3.3V, VCCB=2.5-5V, C_{OUT}=50pF	12		42	ns
	OE to A, VCCA=5V, VCCB=2.5-5V, C_{OUT}=50pF	7		34	ns
	OE to B, VCCB=2.5V, VCCA=2.5-5V, C_{OUT}=50pF	14		43	ns
	OE to B, VCCB=3.3V, VCCA=2.5-5V, C_{OUT}=50pF	7		28	ns
	OE to B, VCCB=5V, VCCA=2.5-5V, C_{OUT}=50pF	5		16	ns
OE Propagation delay t_{PD_HL}	OE to A, VCCA=2.5V, VCCB=2.5-5V, C_{OUT}=50pF	120		280	ns
	OE to A, VCCA=3.3V, VCCB=2.5-5V, C_{OUT}=50pF	95		175	ns
	OE to A, VCCA=5V, VCCB=2.5-5V, C_{OUT}=50pF	75		130	ns
	OE to B, VCCB=2.5V, VCCA=2.5-5V, C_{OUT}=50pF	100		260	ns
	OE to B, VCCB=3.3V, VCCA=2.5-5V, C_{OUT}=50pF	90		170	ns
	OE to B, VCCB=5V, VCCA=2.5-5V, C_{OUT}=50pF	75		127	ns
Rise time t_{RISE}	A to B, VCCA=2.5-5V, VCCB=2.5V, C_{OUT}=50pF	4		16	ns
	A to B, VCCA=2.5-5V, VCCB=3.3V, C_{OUT}=50pF	3		10	ns
	A to B, VCCA=2.5-5V, VCCB=5V, C_{OUT}=50pF	2		6	ns
Fall time t_{FALL}	A to B, VCCA=2.5-5V, VCCB=2.5V, C_{OUT}=50pF	8		19	ns
	A to B, VCCA=2.5-5V, VCCB=3.3V, C_{OUT}=50pF	4		12	ns
	A to B, VCCA=2.5-5V, VCCB=5V, C_{OUT}=50pF	2		6	ns
Maximum data rate	A to B, VCCA=2.5-5V, VCCB=2.5V, C_{OUT}=50pF	4			Mbps
	A to B, VCCA=2.5-5V, VCCB=3.3V, C_{OUT}=50pF	6			Mbps
	A to B, VCCA=2.5-5V, VCCB=5V, C_{OUT}=50pF	8			Mbps

XTR50014/XTR50015 ELECTRICAL SPECIFICATIONS

Unless otherwise stated, specification applies for -60℃<T_j<230℃.

Parameter	Condition	Min	Typ	Max	Units
Supply voltage					
VCCA		2.5		5.5	V
VCCB		2.5		5.5	V
Quiescent current	on VCCA+VCCB supplies, T_{amb}=25℃, DIR high		20		µA
	on VCCA+VCCB supplies, T_{amb}=25℃, DIR low		10		µA
Input voltage					
High-level Input Voltage V_{IH}	VCCA/VCCB=2.5V	1.8			V
	VCCA/VCCB=3.3V	2.5			V
	VCCA/VCCB=5V	2.75			V
	VCCA/VCCB=5.5V	2.85			V
Low-level Input Voltage V_{IL}	VCCA/VCCB=2.5V			0.8	V
	VCCA/VCCB=3.3V			1.3	V
	VCCA/VCCB=5V			1.8	V
	VCCA/VCCB=5.5V			1.9	V
Output voltage					
High-level Output Voltage V_{OH}	VCCA/VCCB=2.5V, I_{OUT}=2mA (sink)	2.34			V
	VCCA/VCCB=3.3V, I_{OUT}=4mA (sink)	3.08			
	VCCA/VCCB=5V, I_{OUT}=8mA (sink)	4.71			
	VCCA/VCCB=5.5V, I_{OUT}=8mA (sink)	5.22			
Low-level Output Voltage V_{OL}	VCCA/VCCB=2.5V, I_{OUT}=2mA (source)	180			mV
	VCCA/VCCB=3.3V, I_{OUT}=4mA (source)	195			mV
	VCCA/VCCB=5V, I_{OUT}=8mA (source)	210			mV
	VCCA/VCCB=5.5V, I_{OUT}=8mA (source)	185			mV
Switching Characteristics					
Propagation delay t_{PD}	From A to B, VCCA=2.5V, VCCB=2.5V, C_{OUT}=50pF	44		90	ns
	From A to B, VCCA=2.5V, VCCB=3.3V, C_{OUT}=50pF	30		67	ns
	From A to B, VCCA=2.5V, VCCB=5V, C_{OUT}=50pF	23		50	ns
	From A to B, VCCA=3.3V, VCCB=2.5V, C_{OUT}=50pF	37		87	ns
	From A to B, VCCA=3.3V, VCCB=3.3V, C_{OUT}=50pF	18		57	ns
	From A to B, VCCA=3.3V, VCCB=5V, C_{OUT}=50pF	14.5		37.5	ns
	From A to B, VCCA=5V, VCCB=2.5V, C_{OUT}=50pF	29.5		79	ns
	From A to B, VCCA=5V, VCCB=3.3V, C_{OUT}=50pF	19		50	ns
	From A to B, VCCA=5V, VCCB=5V, C_{OUT}=50pF	10		30	ns
DIR Propagation delay $t_{PD\_DIR\_LH}$	DIR to A, VCCA=2.5V, VCCB=2.5-5V, C_{OUT}=50pF	37		96	ns
	DIR to A, VCCA=3.3V, VCCB=2.5-5V, C_{OUT}=50pF	18		59	ns
	DIR to A, VCCA=5V, VCCB=2.5-5V, C_{OUT}=50pF	10		37	ns
	DIR to B, VCCB=2.5V, VCCA=2.5-5V, C_{OUT}=50pF	18		67	ns
	DIR to B, VCCB=3.3V, VCCA=2.5-5V, C_{OUT}=50pF	10		53	ns
	DIR to B, VCCB=5V, VCCA=2.5-5V, C_{OUT}=50pF	7.5		48	ns
DIR Propagation delay $t_{PD\_DIR\_HL}$	DIR to A, VCCA=2.5V, VCCB=2.5-5V, C_{OUT}=50pF	140		290	ns
	DIR to A, VCCA=3.3V, VCCB=2.5-5V, C_{OUT}=50pF	112		181	ns
	DIR to A, VCCA=5V, VCCB=2.5-5V, C_{OUT}=50pF	87		133	ns
	DIR to B, VCCB=2.5V, VCCA=2.5-5V, C_{OUT}=50pF	101		282	ns
	DIR to B, VCCB=3.3V, VCCA=2.5-5V, C_{OUT}=50pF	91		266	ns
	DIR to B, VCCB=5V, VCCA=2.5-5V, C_{OUT}=50pF	89		256	ns
Rise time t_{RISE}	A to B, VCCA=2.5-5V, VCCB=2.5V, C_{OUT}=50pF	5		17	ns
	A to B, VCCA=2.5-5V, VCCB=3.3V, C_{OUT}=50pF	3		11	ns
	A to B, VCCA=2.5-5V, VCCB=5V, C_{OUT}=50pF	2		6	ns
Fall time t_{FALL}	A to B, VCCA=2.5-5V, VCCB=2.5V, C_{OUT}=50pF	8		21	ns
	A to B, VCCA=2.5-5V, VCCB=3.3V, C_{OUT}=50pF	4		11	ns
	A to B, VCCA=2.5-5V, VCCB=5V, C_{OUT}=50pF	2		6	ns
Maximum data rate	A to B, VCCA=2.5-5V, VCCB=2.5V, C_{OUT}=50pF	10			Mbps
	A to B, VCCA=2.5-5V, VCCB=3.3V, C_{OUT}=50pF	15			Mbps
	A to B, VCCA=2.5V, VCCB=5V, C_{OUT}=50pF	20			Mbps
	A to B, VCCA=3.3V, VCCB=5V, C_{OUT}=50pF	30			Mbps

THEORY OF OPERATION

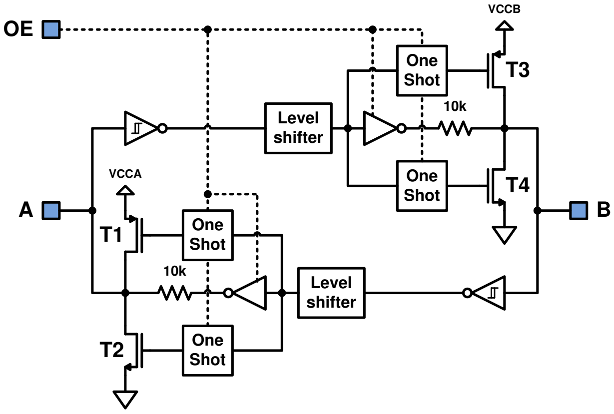
Introduction

The XTR50010 is a family of bidirectional level translators that can be used for data communication between devices or systems operating at different supply voltages.
XTR50010 parts are able to operate from -60℃ to +230℃, with supply voltages from 2.5V to 5.5V.

Operation Modes

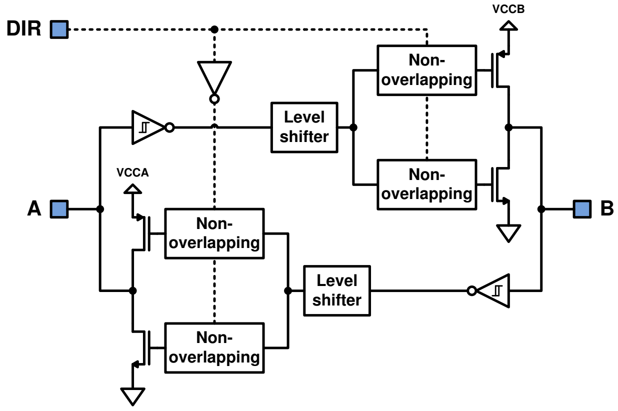
XTR50011/XTR50012 operation (bidirectional)

The block architecture for one I/O channel of XTR50011 or XTR50012 devices is shown in the figure below. These devices do not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a static state, the output drivers of the XTR50011 or XTR50012 can maintain a high or low, but are designed to present a weak output (10kΩ output impedance), so that they can be overdriven by an external, low-impedance driver when data on the bus starts flowing in the opposite direction. However, load capacitors of up to 50pF can be connected at the output as theses capacitors will be charged and discharged during transitions by strong drivers controlled by the “One-Shot” blocks of the figure below.
The One-Shot blocks driving the output transistors T1-T4 detect rising or falling edges of input signal on the A or B ports. During a rising edge, the One-Shot blocks turn on the PMOS transistors T1 and T3 for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the One-Shot blocks turn on the NMOS transistors T2 and T4 for a short duration, which speeds up the high-to-low transition. After the rising or falling transition, the state is maintained with 10kΩ output impedance drivers.



XTR50014/XTR50015 operation (directional)

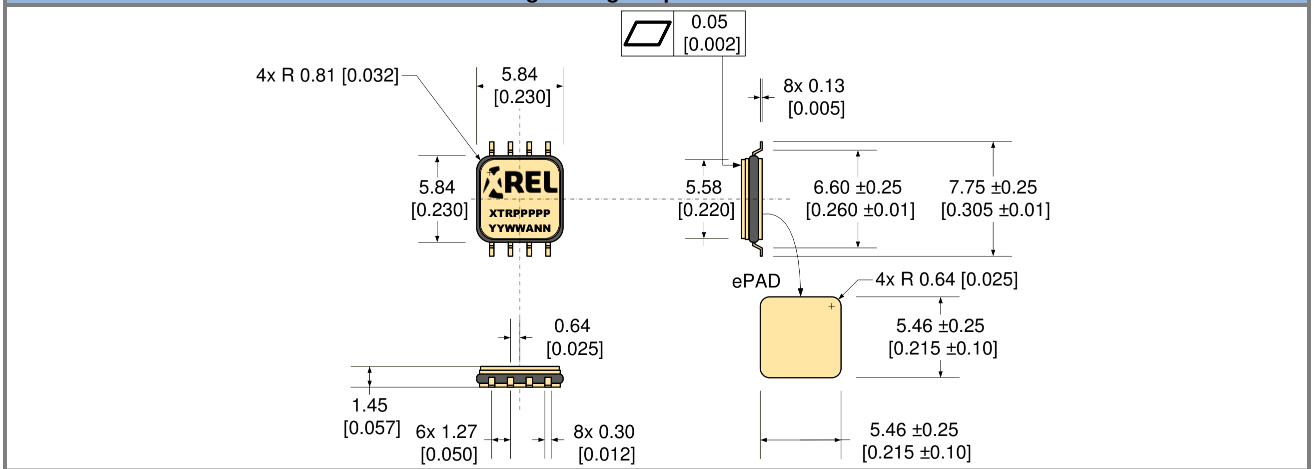
The block architecture for one I/O channel of XTR50014 or XTR50015 is shown in the figure below. These devices are designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess short-circuit current on the power supplies.
The DIR input can be powered either by VCCA or VCCB. This brings more flexibility at system level.



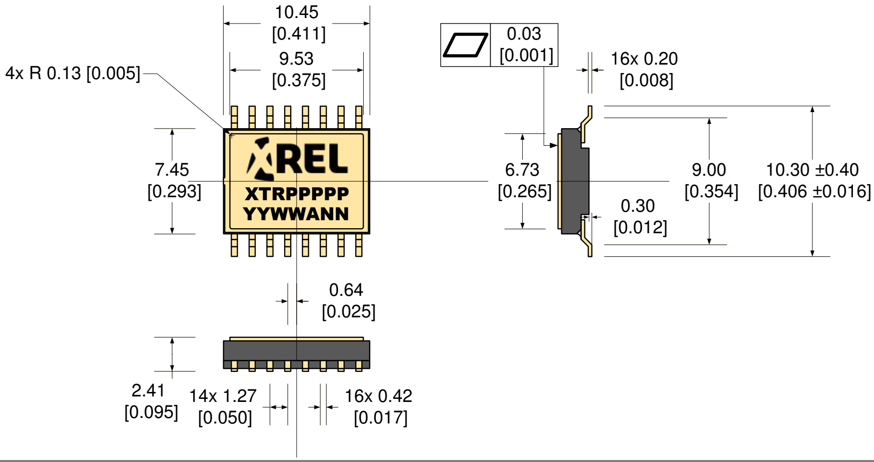
PACKAGE OUTLINES

Dimensions shown in mm [inches].

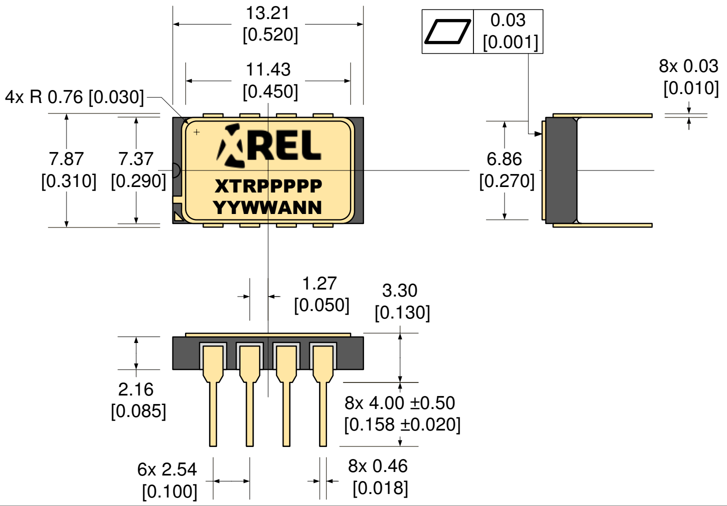
Ceramic gull-wing flat pack with ePad DFP8



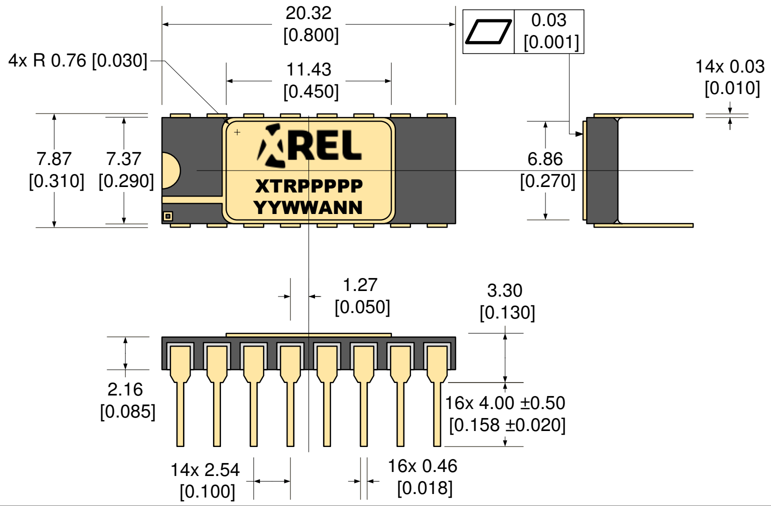
Ceramic Small Outline IC SOIC16



Ceramic Side Braze Dual In-line DIP8



Ceramic Side Braze Dual In-line DIP16



Part Marking Convention

Part Reference: XTRPPPPPP	
XTR	X-REL Semiconductor, high-temperature, high-reliability product (XTRM Series).
PPPPP	Part number (0-9, A-Z).
Unique Lot Assembly Code: YYWWANN	
YY	Two last digits of assembly year (e.g. 11 = 2011).
WW	Assembly week (01 to 52).
A	Assembly location code.
NN	Assembly lot code (01 to 99).

IMPORTANT NOTICE & DISCLAIMER

CONTACT US

For more information on X-REL Semiconductor’s products, technical support or ordering:

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