

HIGH-TEMPERATURE MULTI-FUNCTION LOGIC GATES

FEATURES

- ▲ Operational beyond the -60°C to +230°C temperature range.
- ▲ Supply voltage from 2.8V to 5.5V.
- ▲ Schmitt trigger inputs.
- ▲ Compatible with NAND, NOR, XOR, INVERTER functions of the standard 54HC family.
- ▲ Latch-up free.
- ▲ Ruggedized SMT and thru-hole packages.
- ▲ Also available as bare die.

APPLICATIONS

- ▲ Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole.
- ▲ Combinatorial logic circuits.

DESCRIPTION

XTR54000 is a configurable logic device able to provide four different functions from the same silicon part. The full featured part is available in a 16-pin package where two pins are used to select the corresponding logic function of the other left-aligned 14 pins. Available functions are 2-input NAND, NOR, XOR, INVERTER.

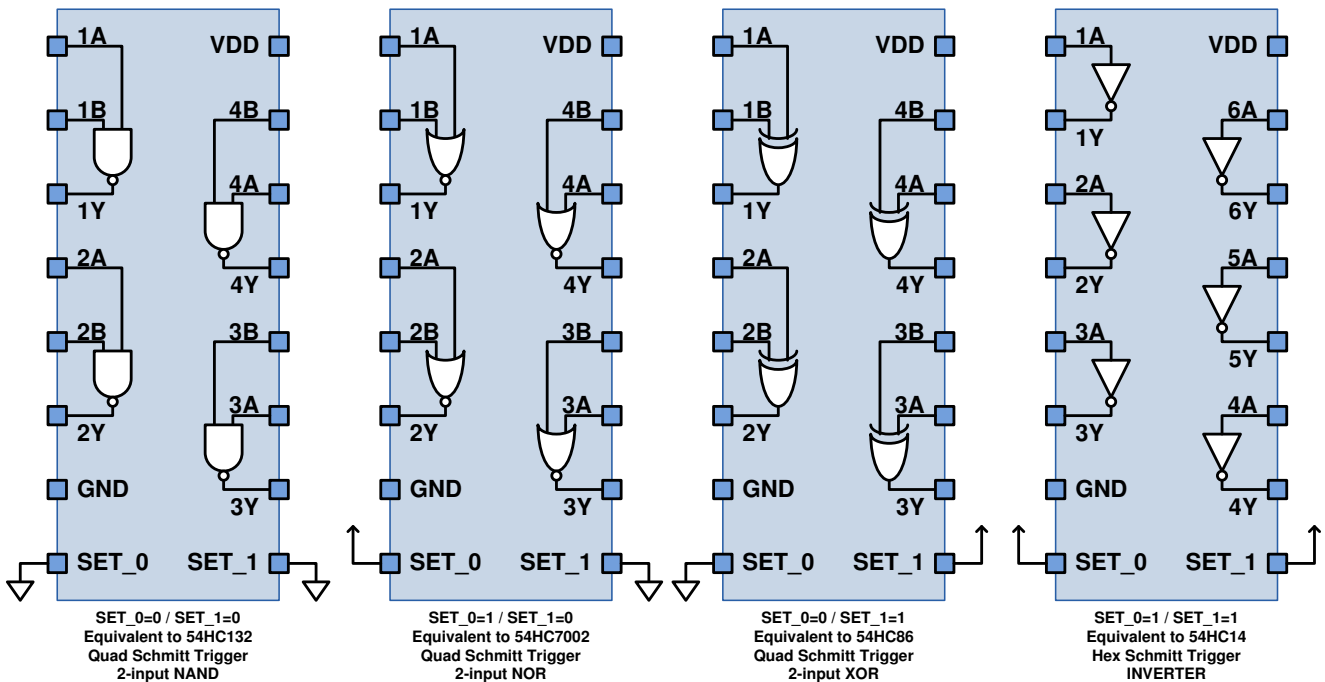
The logic function can also be selected during assembly into 14-pin packages offering pin-to-pin compatibility with standard parts from the 54HC family.

In all configurations, all inputs are Schmitt trigger for increased noise margin.

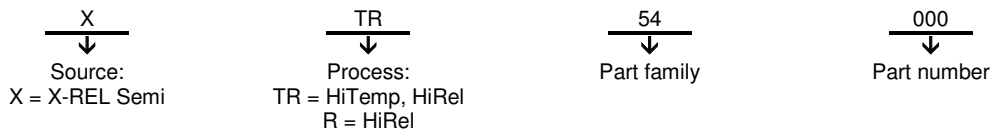
XTR54000 parts have been designed to reduce system cost and ease adoption by reducing the learning curve and providing smart and easy to use features.

Parts from the XTR54000 family are available in ruggedized SMT and thru-hole packages. Parts are also available as bare dies.

PRODUCT HIGHLIGHT



ORDERING INFORMATION



Product Reference	Description	Temperature Range	Package	Pin Count	Marking
XTR54000-BD	Configurable device	-60°C to +230°C	Bare die		XTR54000
XTR54000-TD	Configurable device	-60°C to +230°C	Tested bare die		XTR54000
XTR54000-S	Configurable device	-60°C to +230°C	Ceramic SOIC	16	XTR54000
XTR54000-D	Configurable device	-60°C to +230°C	Ceramic side braze DIL	16	XTR54000
XTR54132-D	Quad 2-input NAND	-60°C to +230°C	Ceramic side braze DIL	14	XTR54132
XTR547002-D	Quad 2-input NOR	-60°C to +230°C	Ceramic side braze DIL	14	XTR547002
XTR5486-D	Quad 2-input XOR	-60°C to +230°C	Ceramic side braze DIL	14	XTR5486
XTR5414-D	Hex INVERTER	-60°C to +230°C	Ceramic side braze DIL	14	XTR5414

For some packages or packaging configurations, MOQ may apply.
 Other packages and packaging configurations possible upon request.

ABSOLUTE MAXIMUM RATINGS

Supply voltage VDD to GND (V_{DD})	-0.5 to 6V
Voltage on any pin, input or output, to GND	-0.5 to $V_{DD}+0.5V$
Input clamp current I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	$\pm 20mA$
Output clamp current I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	$\pm 20mA$
Continuous output current I_O ($V_O = 0$ to V_{DD})	$\pm 20mA$
Storage Temperature Range	-70°C to +230°C
Operating Junction Temperature Range	-70°C to +300°C
ESD Classification	2kV HBM MIL-STD-883

Caution: Stresses beyond those listed in “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to “ABSOLUTE MAXIMUM RATINGS” conditions for extended periods may permanently affect device reliability.

PRODUCT VARIANTS

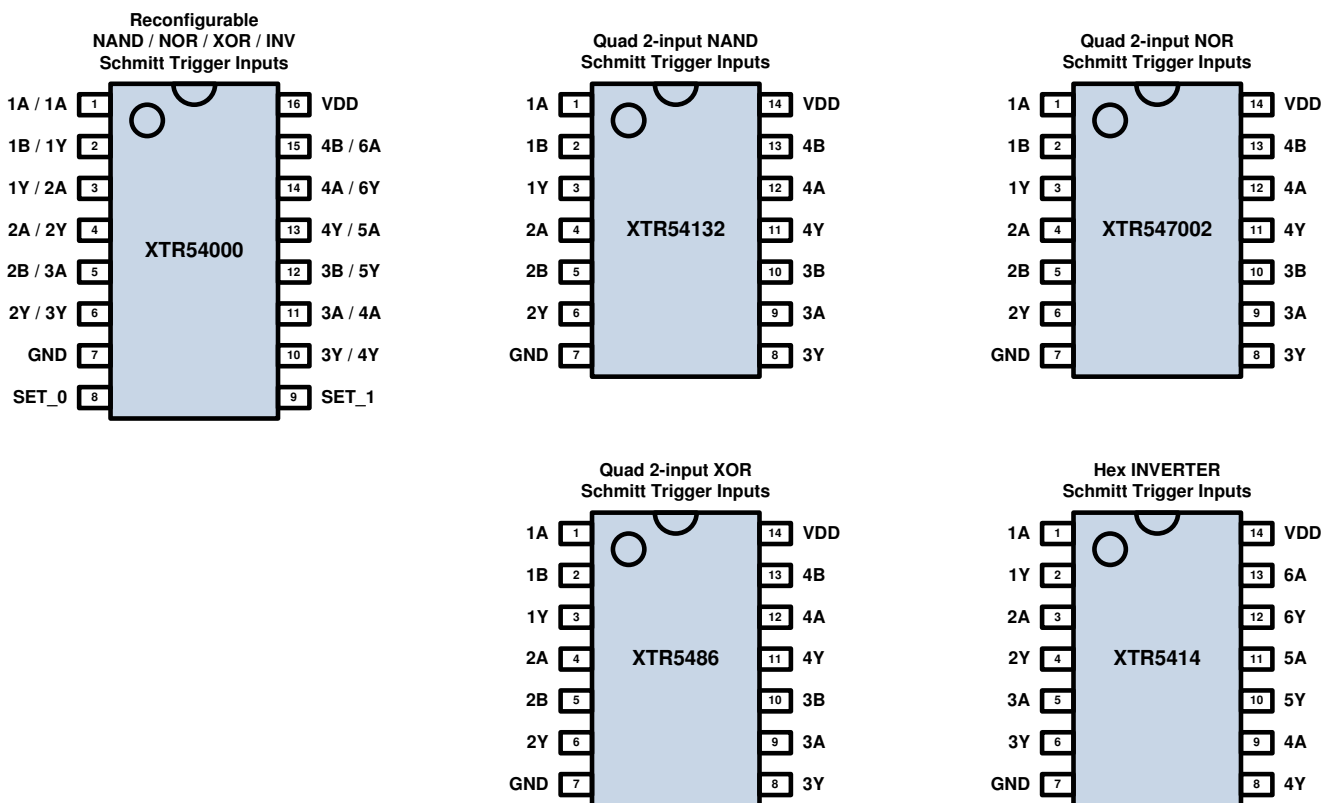


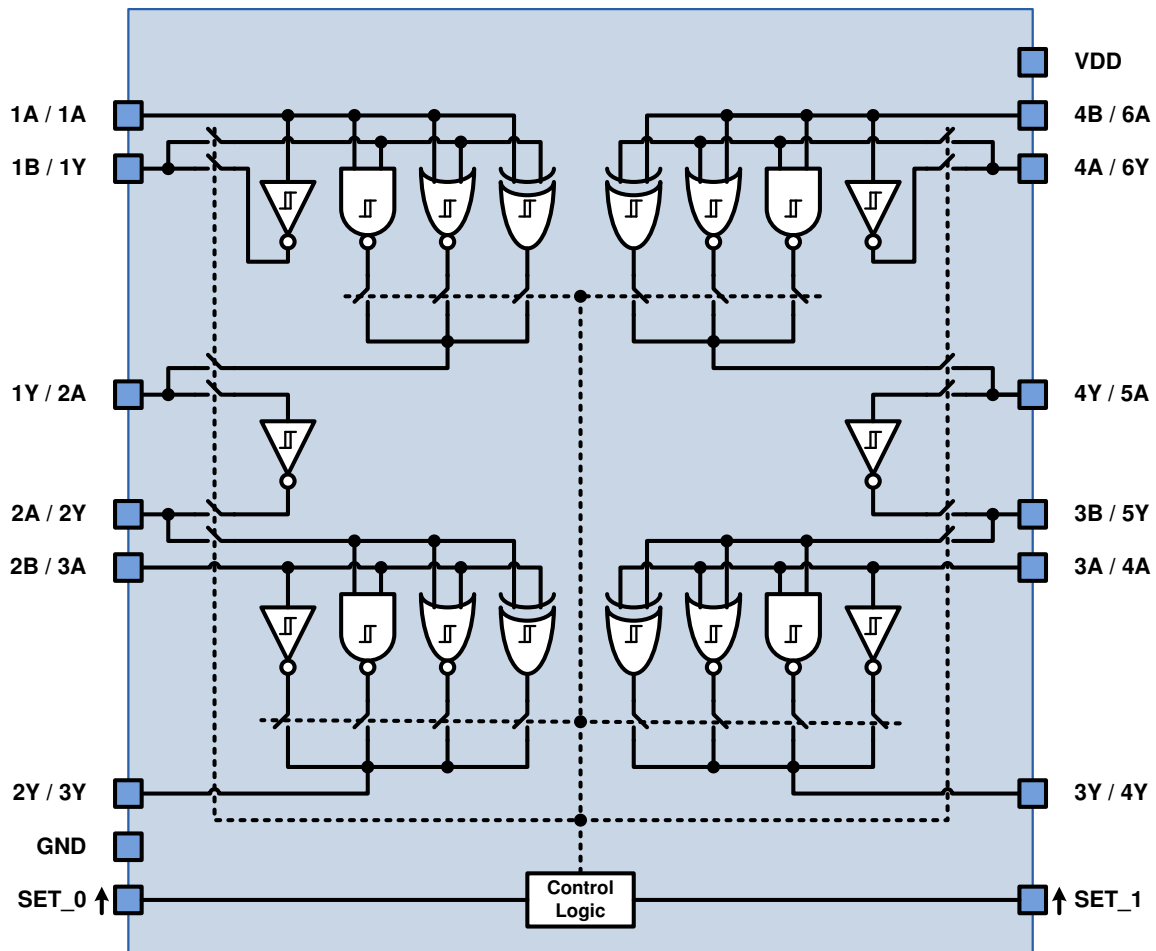
Table 1. Function Table

SET_1	SET_0	Function	Equivalent part
0	0	Quad 2-input NAND	54HC132
0	1	Quad 2-input NOR	54HC7002
1	0	Quad 2-input XOR	54HC86 ¹
1	1	Hex INVERTER ²	54HC14

¹ The standard 54HC86 has standard CMOS inputs. The XTR5486 has Schmitt trigger inputs.

² Default configuration when SET_0 and SET_1 are left floating.

BLOCK DIAGRAM



Arrows aside pin names indicate whether the input is internally pulled up.

PIN DESCRIPTION

XTR54000		
Pin Number	Name	Description
1	1A / 1A	Input A of first 2-input gate / Input of first inverter.
2	1B / 1Y	Input B of first 2-input gate / Output of first inverter.
3	1Y / 2A	Output of first 2-input gate / Input of second inverter.
4	2A / 2Y	Input A of second 2-input gate / Output of second inverter.
5	2B / 3A	Input B of second 2-input gate / Input of third inverter.
6	2Y / 3Y	Output of second 2-input gate / Output of third inverter.
7	GND	Circuit ground.
8	SET_0	LSB of function selection bits. Internally pulled-up.
9	SET_1	MSB of function selection bits. Internally pulled-up.
10	3Y / 4Y	Output of third 2-input gate / Output of fourth inverter.
11	3A / 4A	Input A of third 2-input gate / Input of fourth inverter.
12	3B / 5Y	Input B of third 2-input gate / Output of fifth inverter.
13	4Y / 5A	Output of fourth 2-input gate / Input of fifth inverter.
14	4A / 6Y	Input A of fourth 2-input gate / Output of sixth inverter.
15	4B / 6A	Input B of fourth 2-input gate / Input of sixth inverter.
16	VDD	Supply voltage.

XTR54132 Quad NAND / XTR547002 Quad NOR / XTR5486 Quad XOR

Pin Number	Name	Description
1	1A	Input A of first 2-input gate.
2	1B	Input B of first 2-input gate.
3	1Y	Output of first 2-input gate.
4	2A	Input A of second 2-input gate.
5	2B	Input B of second 2-input gate.
6	2Y	Output of second 2-input gate.
7	GND	Circuit ground.
8	3Y	Output of third 2-input gate.
9	3A	Input A of third 2-input gate.
10	3B	Input B of third 2-input gate.
11	4Y	Output of fourth 2-input gate.
12	4A	Input A of fourth 2-input gate.
13	4B	Input B of fourth 2-input gate.
14	VDD	Supply voltage.

XTR5414 Hex Inverter

Pin Number	Name	Description
1	1A	Input of first inverter.
2	1Y	Output of first inverter.
3	2A	Input of second inverter.
4	2Y	Output of second inverter.
5	3A	Input of third inverter.
6	3Y	Output of third inverter.
7	GND	Circuit ground.
8	4Y	Output of fourth inverter.
9	4A	Input of fourth inverter.
10	5Y	Output of fifth inverter.
11	5A	Input of fifth inverter.
12	6Y	Output of sixth inverter.
13	6A	Input of sixth inverter.
14	VDD	Supply voltage.

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Supply voltage V_{DD}	2.8		5.5	V
Voltage on any pin, input or output, with respect to GND.	0		V_{DD}	V
Ambient Temperature ¹ T_{amb}	-60		230	°C

¹ Operation beyond the specified temperature range is achieved.

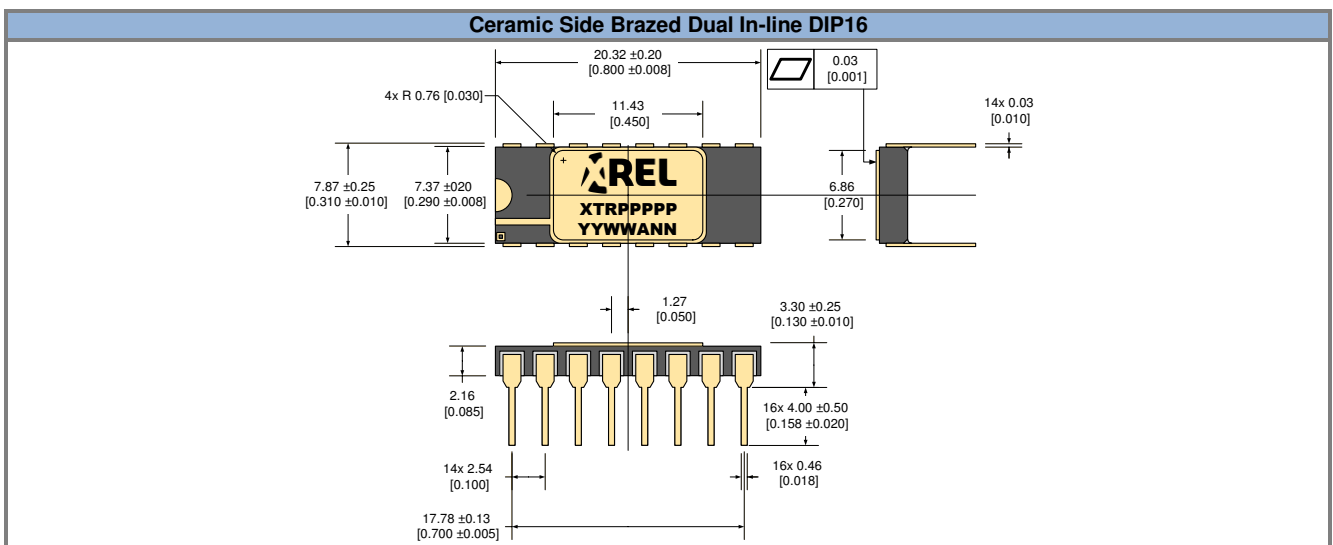
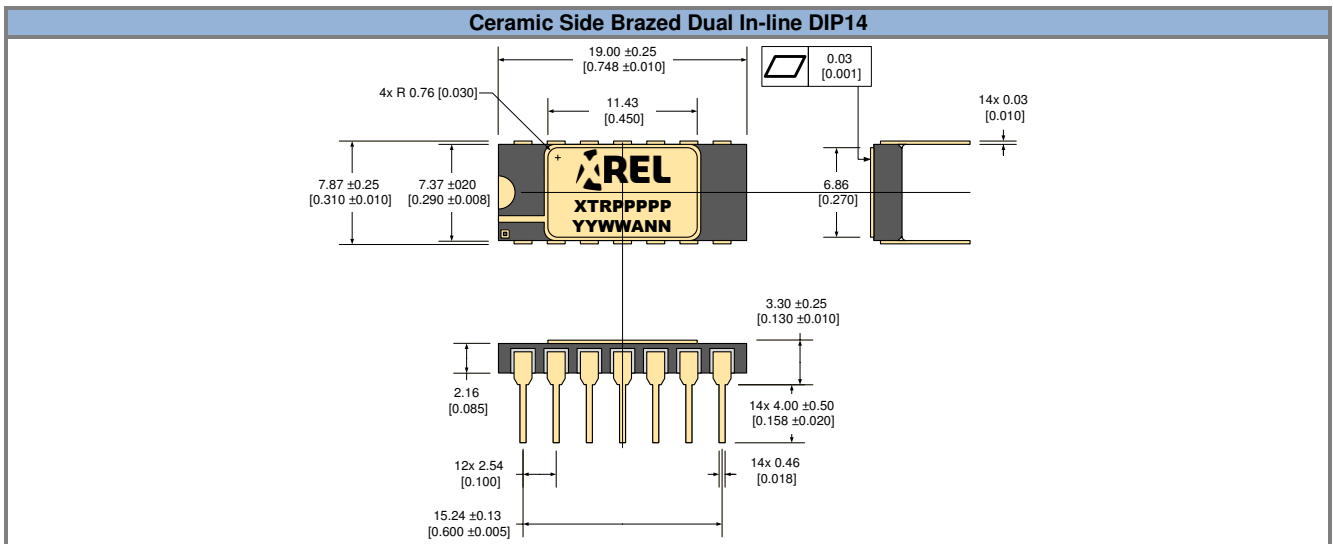
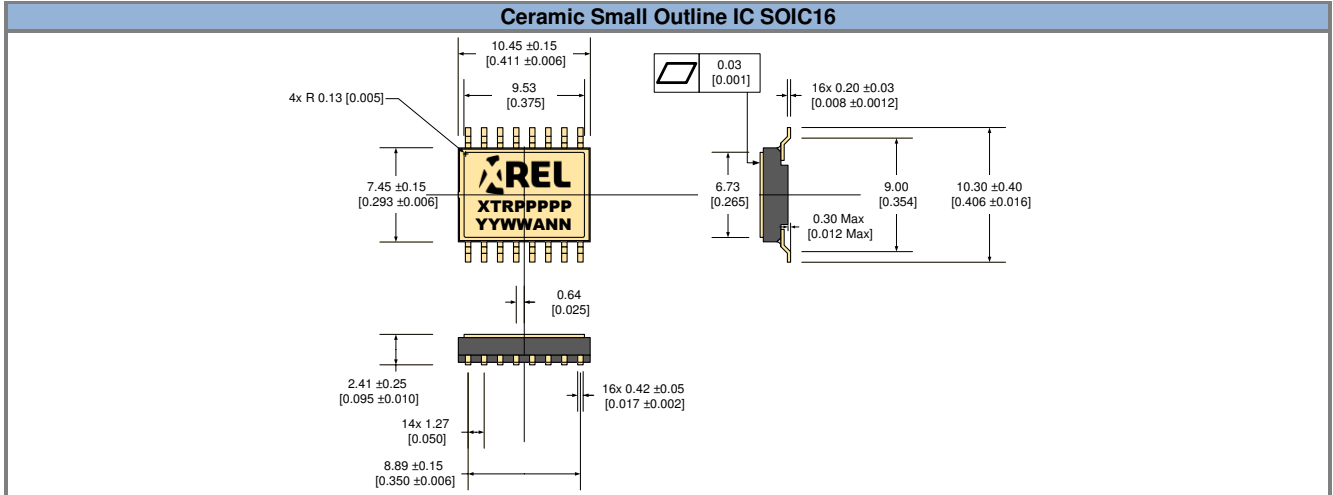
ELECTRICAL SPECIFICATIONS

Unless otherwise stated, specification applies for $V_{DD}=5V$, $-60^{\circ}C < T_{amb} < 230^{\circ}C$.

Parameter	Condition	Min	Typ	Max	Units
Supply					
Supply voltage V_{DD}		2.8		5.5	V
Supply quiescent current I_{DD}	SET_0=SET_1=VDD. $T_{amb}=230^{\circ}C$. $V_{DD}=2.8V$ $V_{DD}=5.5V$		3.5 4.3	10 15	μA
	SET_0=VDD and SET_1=0 or SET_0=0 and SET_1=VDD. $T_{amb}=230^{\circ}C$. $V_{DD}=2.8V$ $V_{DD}=5.5V$		10 18	20 30	μA
	SET_0=SET_1=0. $T_{amb}=230^{\circ}C$. $V_{DD}=2.8V$ $V_{DD}=5.5V$		17 30	35 50	μA
Pull-up strength (per input) I_{PU}	Pulled-up inputs SET_1 or SET_0 forced to GND. $T_{amb}=-60^{\circ}C$ $T_{amb}=230^{\circ}C$		6 12	12 20	μA
Schmitt Trigger Inputs					
Positive-going input threshold V_{T+}	$V_{DD}=2.8V$ $V_{DD}=5.5V$		2.0 3.3	2.3 3.7	V
Negative-going input threshold V_{T-}	$V_{DD}=2.8V$ $V_{DD}=5.5V$	0.7 1.2	1.1 1.9		V
Hystereris voltage ($V_{T+}-V_{T-}$) V_{Hys}	$V_{DD}=2.8V$ $V_{DD}=5.5V$	0.5 0.8	0.9 1.4		V
Outputs					
HIGH-level output voltage V_{OH}	$I_{OUT}=-4mA$ (device sourcing). $T_{amb}=230^{\circ}C$. $V_{DD}=2.8V$ $V_{DD}=5.5V$	2.35 5.20	2.58 5.38		V
	$I_{OUT}=-8mA$ (device sourcing). $T_{amb}=230^{\circ}C$. $V_{DD}=5.5V$	5.00	5.25		
LOW Level ouput voltage V_{OL}	$I_{OUT}=4mA$ (device sinking). $T_{amb}=230^{\circ}C$. $V_{DD}=2.8V$ $V_{DD}=5.5V$		0.21 0.11	0.35 0.25	V
	$I_{OUT}=8mA$ (device sinking). $T_{amb}=230^{\circ}C$. $V_{DD}=5.5V$		0.22	0.40	
Timing					
Propagation delay from inputs A or B to output Y t_{PHL}	$C_L=50pF$, $T_{amb}=25^{\circ}C$. $V_{DD}=2.8V$ $V_{DD}=5.5V$		24 13	43 22	ns
	$C_L=50pF$, $T_{amb}=230^{\circ}C$. $V_{DD}=2.8V$ $V_{DD}=5.5V$		32 15	60 26	
Propagation delay from inputs A or B to output Y t_{PLH}	$C_L=50pF$, $T_{amb}=25^{\circ}C$. $V_{DD}=2.8V$ $V_{DD}=5.5V$		33 11	60 19	ns
	$C_L=50pF$, $T_{amb}=230^{\circ}C$. $V_{DD}=2.8V$ $V_{DD}=5.5V$		39 14	70 25	
Output transition time. Any output Y. t_{THL} / t_{TLH}	$C_L=50pF$, $T_{amb}=25^{\circ}C$. $V_{DD}=2.8V$ $V_{DD}=5.5V$		9 / 6 4 / 4	18 / 12 8 / 8	ns
	$C_L=50pF$, $T_{amb}=230^{\circ}C$. $V_{DD}=2.8V$ $V_{DD}=5.5V$		10 / 7 5 / 4	20 / 14 10 / 8	

PACKAGE OUTLINES

Dimensions shown in mm [inches]. Tolerances ± 0.13 mm [± 0.005 in] unless otherwise stated.



Part Marking Convention	
Part Reference: XTRPPPPPP	
XTR	X-REL Semiconductor, high-temperature, high-reliability product (XTRM Series).
PPPPP	Part number (0-9, A-Z).
Unique Lot Assembly Code: YYWWANN	
YY	Two last digits of assembly year (e.g. 11 = 2011).
WW	Assembly week (01 to 52).
A	Assembly location code.
NN	Assembly lot code (01 to 99).

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