

## HIGH TEMPERATURE POWER GATE DRIVER

### FEATURES

- ▲ Supply voltage up to 40V.
- ▲ Operational beyond the -60°C to +230°C temperature range.
- ▲ Half-bridge driver.
- ▲ Integrated charge pump.
- ▲ Latch-up free.
- ▲ Ruggedized SMT packages.
- ▲ Also available as bare die.
- ▲ Up to 6A peak current drive strength.

### APPLICATIONS

- ▲ Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole.
- ▲ Intelligent Power Modules (IPM).
- ▲ Power inverters.
- ▲ Power conversion and motor drive.
- ▲ DC-DC converters and switched mode power supplies.

### DESCRIPTION

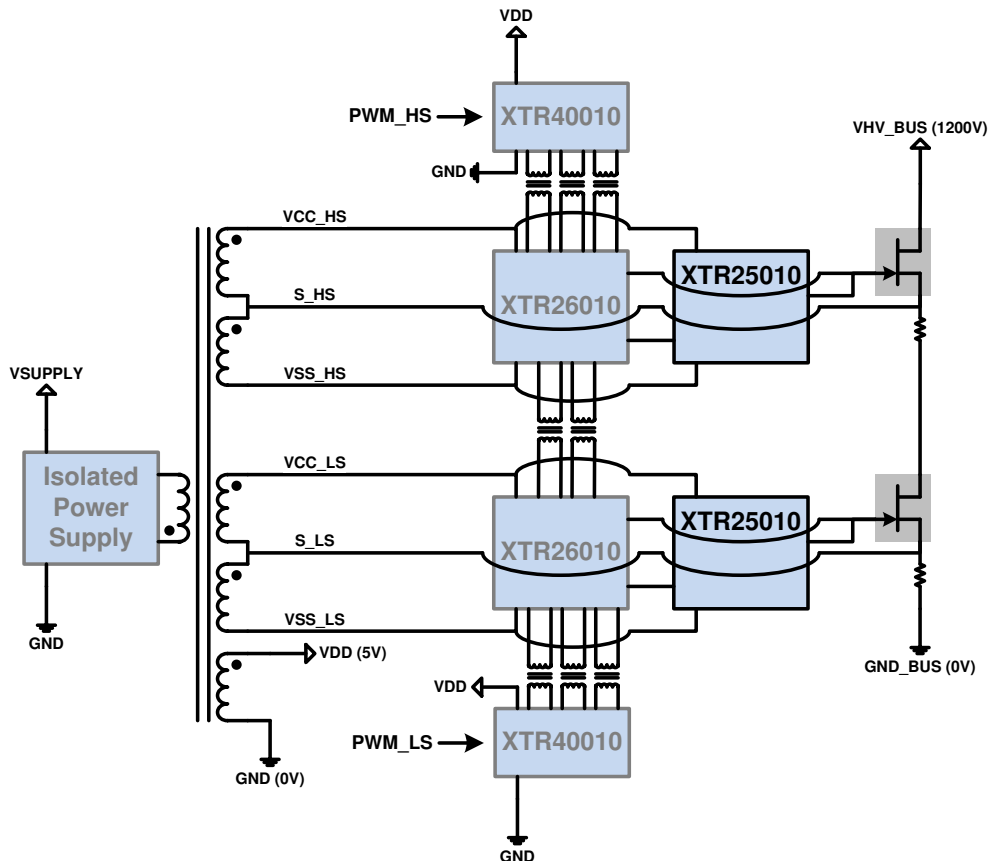
XTR25010 is a high-temperature, high reliability power transistor driver integrated circuit designed to drive normally ON and normally-OFF power transistors in Silicon Carbide (SiC), Gallium Nitride (GaN) and standard silicon, including JFETs, MOSFETs, BJTs, SJTs and MESFETs.

For turning on the power transistors, the XTR25010 includes two independent pull-up gate-drive-channels (PU\_DR1 and PU\_DR2) capable of sourcing 3A peak current each. For turning off the power transistors, the XTR25010 includes two pull-down gate-drive-channels capable of sinking 3A peak current each (PD\_DR and PD\_MC).

For driving wide bandgap transistors, it is recommended to use XTR25010 as a power stage extension for the XTR26010, which generates the needed control signals and additional protection functions (see XTR26010 datasheet and application note for more details).

XTR25010 can also be used standalone as a half-bridge driver for DC-DC converters and motor drive.

### PRODUCT HIGHLIGHT



### ORDERING INFORMATION

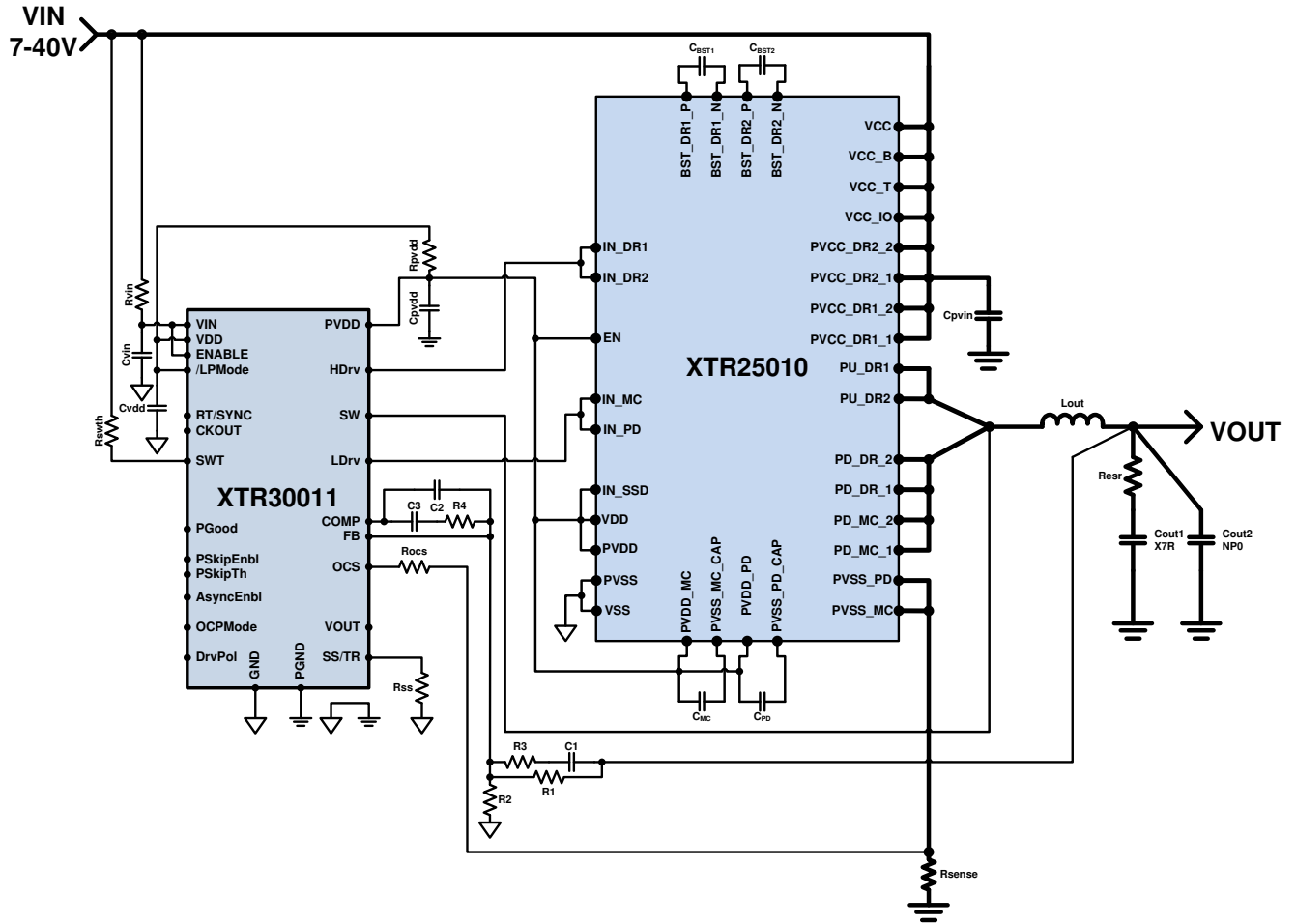
X ↓ Source: X = X-REL Semi	TR ↓ Process: TR = HiTemp, HiRel R = HiRel	25 ↓ Part family	010 ↓ Part number
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Product Reference	Temperature Range	Package	Pin Count	Marking
XTR25010-BD	-60°C to +230°C	Bare die		
XTR25011-LJ	-60°C to +230°C	Ceramic LJCC52	52	XTR25011

Other packages and packaging configurations possible upon request.

## TYPICAL APPLICATION

### Step-down (Buck) DC-DC Converter

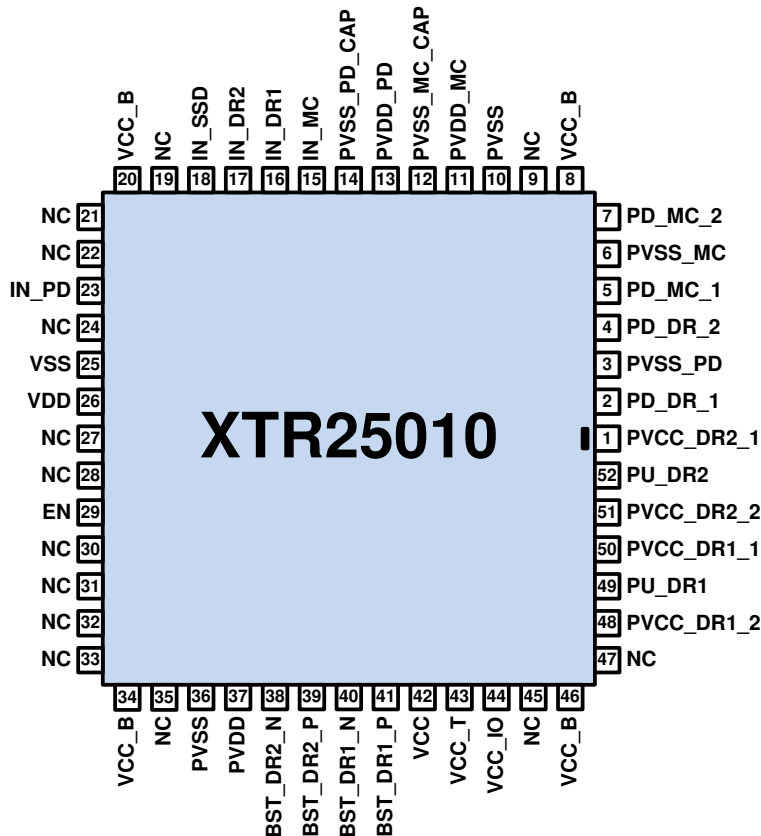


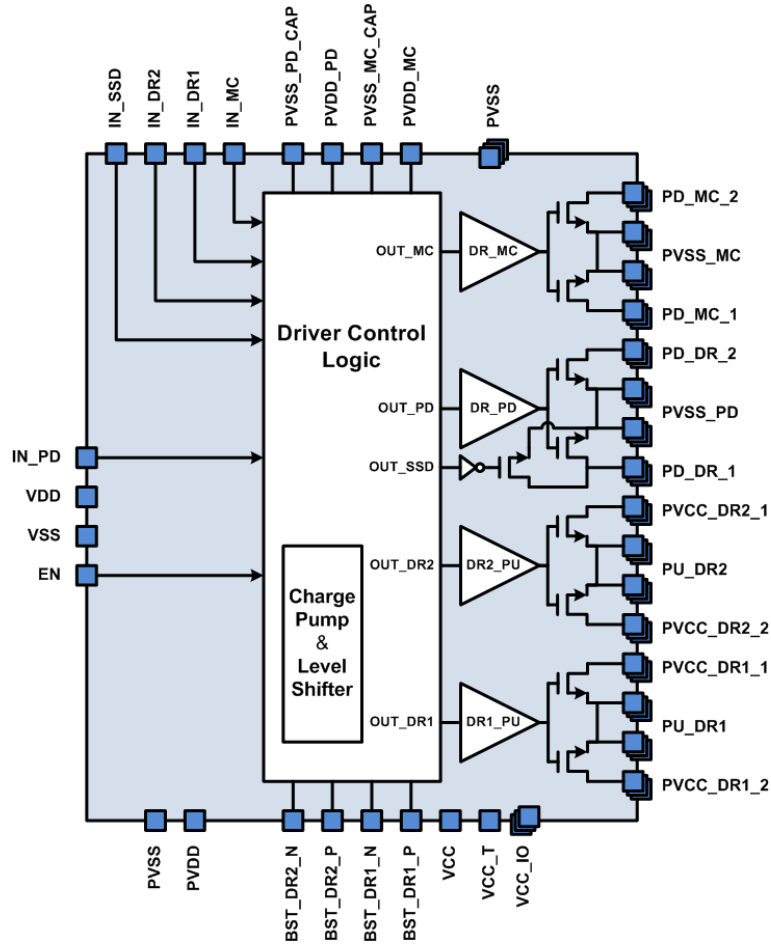
## ABSOLUTE MAXIMUM RATINGS

Supply voltage VCC_IO-PVSS	-0.5V to 44V
VCC, VCC_B, VCC_T, and PVCC_DRx_x	PVSS-0.5V to VCC_IO+0.5V
PVDD-PVSS	-0.5V to 5.5V
VDD, PVDD_PD and PVDD_MC	PVSS-0.5V to PVDD+0.5V
VSS, PVSS_MC, PVSS_PD	PVSS-0.5V to PVSS+0.5V
Inputs pins EN, IN_SSD, IN_DR1, IN_DR2, IN_MC and IN_PD	PVSS-0.5V to PVDD+0.5V
Outputs pins PD_MC_x and PD_DR_x	PVSS-0.5V to VCC_IO+0.5V
PU_DR1	PVSS-0.5V to PVCC_DR1+0.5V
PU_DR2	PVSS-0.5V to PVCC_DR2+0.5V
Storage Temperature Range	-70°C to +230°C
Operating Junction Temperature Range	-70°C to +300°C
ESD Classification	1kV HBM MIL-STD-883

**Caution:** Stresses beyond those listed in “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to “ABSOLUTE MAXIMUM RATINGS” conditions for extended periods may permanently affect device reliability.

## PACKAGING (LJCC52: J-FORMED LEADED CHIP CARRIER)



**BLOCK DIAGRAM (XTR25010-BD)**


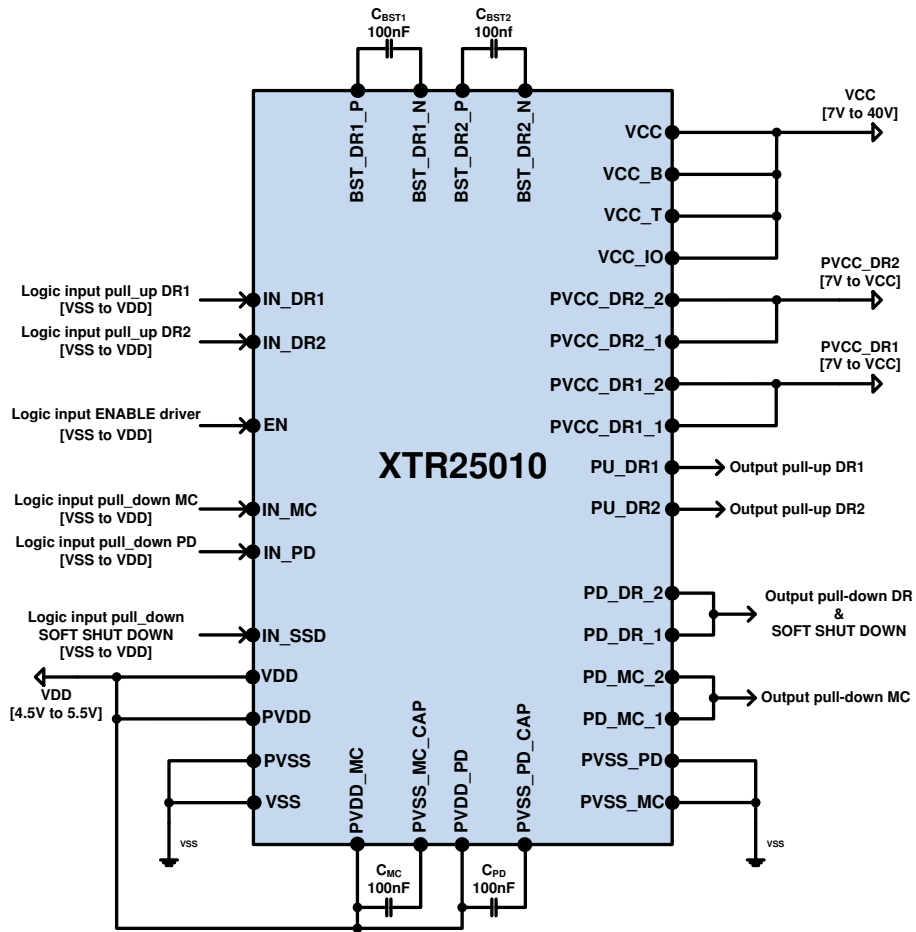
Die level block diagram showing all available functionalities and bond-pads.

**PIN DESCRIPTION (LJCC52: 52 LEAD J-SHAPED CHIP CARRIER)**

Pin number	Name	Description
1	<b>PVCC_DR2_1</b>	Connect to positive supply voltage of PU_DR2 driver (PVCC_DR2).
2	<b>PD_DR_1</b>	Connect to output of the pull-down driver PD_DR_2.
3	<b>PVSS_PD</b>	Power VSS of PD driver. Connect to PVSS plane.
4	<b>PD_DR_2</b>	Connect to output of the pull-down driver PD_DR_1.
5	<b>PD_MC_1</b>	Connect to Miller Clamp pull-down driver PD_MC_2
6	<b>PVSS_MC</b>	Power VSS of MC driver. Connect to PVSS plane.
7	<b>PD_MC_2</b>	Connect to Miller Clamp pull-down driver PD_MC_1
8	<b>VCC_B</b>	Connect to power VCC plane.
9	<b>NC</b>	No internal connection.
10	<b>PVSS</b>	Power VSS. Connect to VSS through a local plane.
11	<b>PVDD_MC</b>	Top plate of bypassing capacitor of the Miller clamp (MC) pre-driver. Connect to PVDD plane.
12	<b>PVSS_MC_CAP</b>	Bottom plate of bypassing capacitor (100nF) of the Miller clamp (MC) pre-driver. This pin is internally connected to PVSS_MC_1/PVSS_MC_2. Do not connect to VSS plane.
13	<b>PVDD_PD</b>	Top plate of bypassing capacitor of the pull-down (PD) pre-driver. Connect to PVDD plane.
14	<b>PVSS_PD_CAP</b>	Bottom plate of bypassing capacitor (100nF) of the pull-down (PD) pre-driver. This pin is internally connected to PVSS_PD_1/PVSS_PD_2. Do not connect to VSS plane.
15	<b>IN_MC</b>	Digital Schmidt triggered input control signal of Active Miller Clamp pull-down driver PD_MC (0/5V vs. VSS)
16	<b>IN_DR1</b>	Digital Schmidt triggered input control signal of pull-up driver PU_DR1 (0/5V vs. VSS).
17	<b>IN_DR2</b>	Digital Schmidt triggered input control signal of pull-up driver PU_DR2 (0/5V vs. VSS).
18	<b>IN_SSD</b>	Digital Schmidt triggered input control signal of soft-shutdown driver (0/5V vs. VSS).
19	<b>NC</b>	No internal connection.
20	<b>VCC_B</b>	Connect to power VCC plane.
21	<b>NC</b>	No internal connection.

Pin number	Name	Description
22	NC	No internal connection.
23	IN_PD	Digital Schmidt triggered input control signal of pull-down driver PD_DR (0/5V vs. VSS).
24	NC	No internal connection.
25	VSS	Negative supply voltage of the driver (its value depends on the power transistor to be driven). Connect to the reference ground plane of the circuit.
26	VDD	5V supply voltage versus VSS, supplying all logic except the output stage of the drivers. Connect to the VDD supply plane.
27	NC	No internal connection.
28	NC	No internal connection.
29	EN	Digital Schmidt triggered input enable signal for the driver outputs (0/5V vs. VSS).
30	NC	No internal connection.
31	NC	No internal connection.
32	NC	No internal connection.
33	NC	No internal connection.
34	VCC_B	Connect to power VCC plane.
35	NC	No internal connection.
36	PVSS	Power VSS. Connect to VSS through a local plane.
37	PVDD	5V supply voltage versus VSS, supplying the 5V IO cells of the circuit. Connect to the VDD supply plane through a local plane.
38	BST_DR2_N	Negative terminal of the (100nF) bootstrap capacitor of the PU_DR2 driver.
39	BST_DR2_P	Positive terminal of the (100nF) bootstrap capacitor of the PU_DR2 driver.
40	BST_DR1_N	Negative terminal of the (100nF) bootstrap capacitor of the PU_DR1 driver.
41	BST_DR1_P	Positive terminal of the (100nF) bootstrap capacitor of the PU_DR1 driver.
42	VCC	Positive supply voltage of the driver (its value depends on the power transistor to be driven). Connect to power VCC plane.
43	VCC_T	Connect to power VCC plane.
44	VCC_IO	Connect to power VCC plane.
45	NC	No internal connection.
46	VCC_B	Connect to power VCC plane.
47	NC	No internal connection.
48	PVCC_DR1_2	Connect to positive supply voltage of PU_DR1 driver (PVCC_DR1).
49	PU_DR1	Output of the pull-up driver with 3A peak drive capability.
50	PVCC_DR1_1	Connect to positive supply voltage of PU_DR1 driver (PVCC_DR1).
51	PVCC_DR2_2	Connect to positive supply voltage of PU_DR2 driver (PVCC_DR2).
52	PU_DR2	Output of the pull-up driver with 3A peak drive capability.

## RECOMMENDED OPERATING CONDITIONS

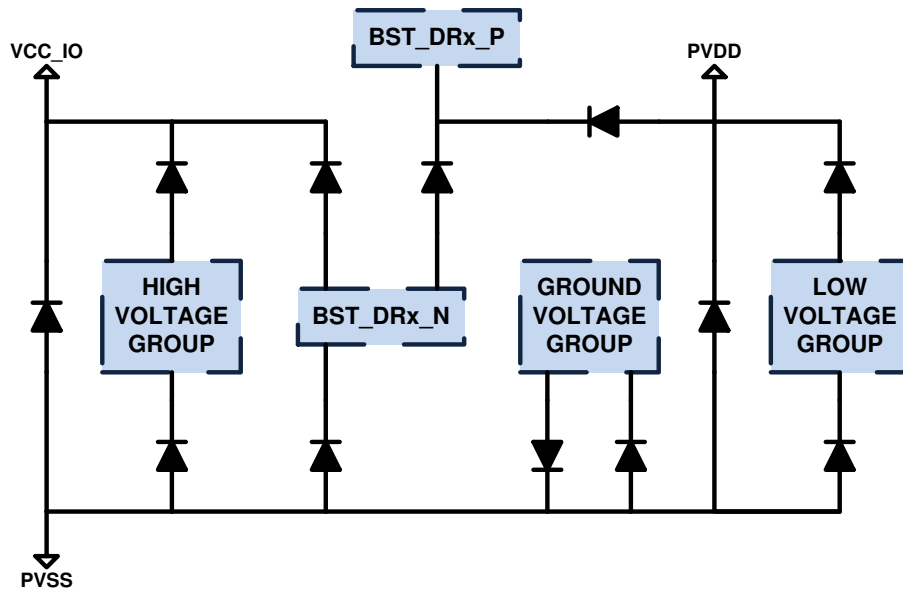


Parameter	Min	Typ	Max	Units
High voltage power supply VCC-VSS (VCC_B, VCC_T and VCC_IO connected to VCC)	7		40	V
High voltage driver power supplies: PVCC_DR1 (PVCC_DR1_1 connect to PVCC_DR1_2)	VSS+7		VCC	V
High voltage driver power supplies: PVCC_DR2 (PVCC_DR2_1 connect to PVCC_DR2_2)	VSS+7		VCC	V
Low voltage power supply VDD-VSS (PVDD, PVDD_PD and PVDD_MC connected to VDD)	4.5		5.5	V
Inputs: IN_DR1, IN_DR2, IN_MC, IN_PD, IN_SSD, EN	VSS		VDD	
Junction Temperature <sup>1</sup> T <sub>j</sub>	-60		230	°C

<sup>1</sup> Operation beyond the specified temperature range is achieved

**ESD CLAMPING SCHEME**

Pin Groups	Pins
High voltage power supply	VCC_IO-PVSS
High voltage group	PVCC_DR2_1, PD_DR_1, PD_DR_2, PU_DR2, PU_DR1, BST_DR1_N, BST_DR2_N, VCC_T, VCC_PD_MC_2, PD_MC_1, PVCC_DR1_2, PVCC_DR1_1, PVCC_DR2_2
Low voltage power supply	PVDD-PVSS
Low voltage group	IN_DR1, IN_DR2, IN_MC, IN_PD, IN_SSD, EN, PVDD_PD, PVDD_MC, VDD
Bootstrap voltages	BST_DRx N: BST_DRx P
Ground voltage group	VSS, PVSS_PD_CAP, PVSS_MC_CAP, PVSS_MC, PVSS_PD



**ELECTRICAL SPECIFICATIONS**

Unless otherwise stated, specification applies for VCC-VSS=25V (PVCC\_DR1 and PVCC\_DR2 connected to VCC) and  $-60^{\circ}\text{C} \leq T_j \leq 230^{\circ}\text{C}$ .

Parameter	Condition	Min	Typ	Max	Units
<b>Supply voltage</b>					
VCC-VSS		7		40	V
VDD-VSS		4.5		5.5	V
Quiescent current consumption	No PWM modulation		250		$\mu\text{A}$
			1.1		$\text{mA}$
<b>Driver</b>					
Propagation delay/channel	from digital inputs to driver outputs		150		ns
Rise time	1nF output capacitor per driver channel		15		ns
Fall time	1nF output capacitor per driver channel		15		ns
Minimum ON time $t_{\text{ON\_min}}$	1nF output capacitor per driver channel	0.5			$\mu\text{s}$
Minimum OFF time $t_{\text{OFF\_min}}$	1nF output capacitor per driver channel	0.5			$\mu\text{s}$
Peak output current of PU_DR1 driver	100nF output capacitor		3		A
Peak output current of PU_DR2 driver	100nF output capacitor		3		A
Continuous output current of PU_DR2	VCC-VSS=7V		0.5		A
Peak output current of PD_DR driver	100nF output capacitor		3		A
Peak output current of PD_MC driver	100nF output capacitor		3		A
Soft-shutdown transistor $R_{\text{ON}}$		50	100	150	$\Omega$
<b>Schmidt triggered inputs (IN_DR1, IN_DR2, IN_MC, IN_SSD)</b>					
$V_{\text{IH}}$	$V_{\text{IH}}$	4			V
$V_{\text{IL}}$	$V_{\text{IL}}$			1	V



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- ✓ Tel: +33 456 580 580
- ✓ Fax: +33 456 580 599
- ✓ Sales: [sales@x-relsemi.com](mailto:sales@x-relsemi.com)  
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- ✓ Information: [info@x-relsemi.com](mailto:info@x-relsemi.com)
- ✓ Support: [support@x-relsemi.com](mailto:support@x-relsemi.com)

**X-REL Semiconductor**

90, Avenue Léon Blum  
38100 Grenoble  
France