HIGH-TEMPERATURE CRYSTAL OSCILLATOR DRIVER

FEATURES

- ▲ Supply voltage from 2.5V to 5.5V.
- ▲ Operational beyond the -60℃ to +230℃ temperature range.
- ▲ Monolithic crystal oscillator driver controller.
- ▲ Operational from 32kHz to 50MHz.
- ▲ Automatically adapts to used crystal.
- ▲ Integrated capacitors for reduced Bill-of-Material
- ▲ Selectable low-power mode.
- ▲ Selectable 1/128 prescaler.
- ▲ Programmable Freq/1, Freq/2, Freq/4, Freq/8 divider.
- ▲ Stand-by functionality with output buffer in High-Z state.
- ▲ Separate oscillator and buffer supply pins for low-noise operation.
- ▲ Latch-up free.
- ▲ Ruggedized SMT and thru-hole packages.
- ▲ Also available as bare die.

APPLICATIONS

- ▲ Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole.
- ▲ Crystal oscillators, clock generation, clock buffering, clock frequency divider, time-base generator, precision timing.

DESCRIPTION

XTR60010 is a family of small footprint high-temperature, extended lifetime crystal oscillator drivers offering extended functional features and designed for extreme reliability applications such as crystal oscillators, clock and time-base generators. Being able to operate from supply voltages from 2.5V to 5.5V, the XTR60010 crystal oscillator driver can operate with crystals from 32kHz to 50MHz.

Functionality features include selectable prescaler (1/128), programmable frequency divider (1/2/4/8), operation in low-power mode for low frequency crystals, integrated capacitors for crystal loading and stand-by mode which stops oscillations and sets the output buffer to the high-Z state. Using the internal prescaler and frequency divider, division factors from 1 to 1024 can be obtained. The internal crystal driver has automatic gain control to be able to accommodate to the used crystal, with no intervention needed from the customer, as required by some competing products.

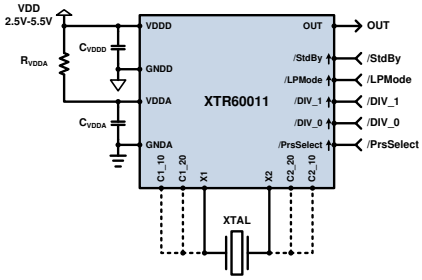
Special design techniques were used allowing the XTR60010 parts to offer a precise, robust and reliable operation in critical applications. Full functionality is guaranteed from -60℃ to +230℃, though operation well below and above this temperature range is achieved.

XTR60010 family parts have been designed to reduce system cost and ease adoption by reducing the learning curve and providing smart and easy to use features.

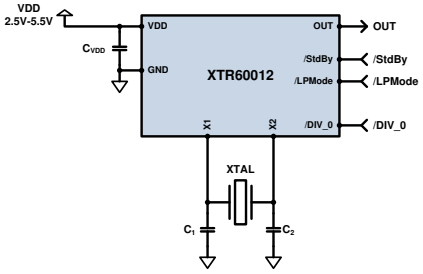
Parts from the XTR60010 family are available in ruggedized SMT and thru-hole packages. Parts are also available as bare dies.

PRODUCT HIGHLIGHT

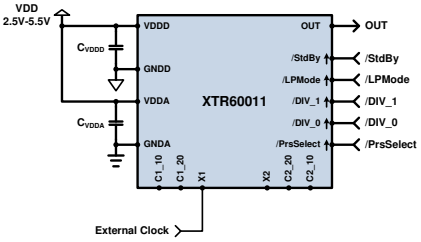
Full-featured Crystal Oscillator



Minimum Footprint Crystal Oscillator



Clock Buffering



ORDERING INFORMATION

X	TR	60	010
Source: X = X-REL Semi	Process: TR = HiTemp, HiRel R = HiRel	Part family	Part number

Product Reference	Temperature Range	Package	Pin Count	Marking
XTR60010-BD	-60℃ to +230℃	Bare die		XTR60010
XTR60010-TD	-60℃ to +230℃	Tested bare die		XTR60010
XTR60011-S	-60℃ to +230℃	Ceramic SOIC	16	XTR60011
XTR60011-D	-60℃ to +230℃	Ceramic side braze DIP	16	XTR60011
XTR60012-FE	-60℃ to +230℃	Gull-wing flat pack with ePad	8	XTR60012
XTR60012-D	-60℃ to +230℃	Ceramic side braze DIP	8	XTR60012

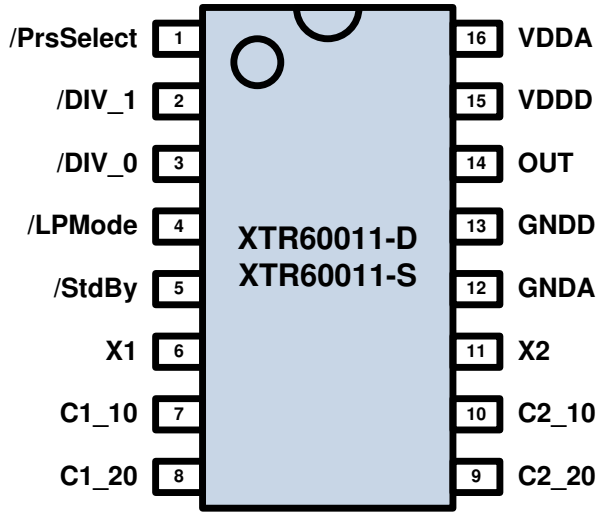
Other packages and packaging configurations possible upon request.

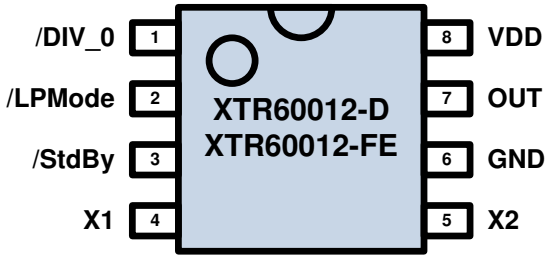
ABSOLUTE MAXIMUM RATINGS

Voltage on VDDA and VDD to GNDA and GNDD	-0.5 to 6.0V
Voltage on any pin to GNDA or GNDD	-0.5 to 6.0V
Maximum difference |VDDA - VDDD|	0.5V
Maximum difference |GNDA - GNDD|	0.5V
Storage Temperature Range	-70℃ to +230℃
Operating Junction Temperature Range	-70℃ to +300℃
ESD Classification	2kV HBM MIL-STD-883

Caution: Stresses beyond *those listed in "*ABSOLUTE MAXIMUM RATINGS*" may cause permanent damage to the device. These are* stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of *the specifications is not implied. Exposure to "*ABSOLUTE MAXIMUM RATINGS*" conditions for extended periods may permanently* affect device reliability.

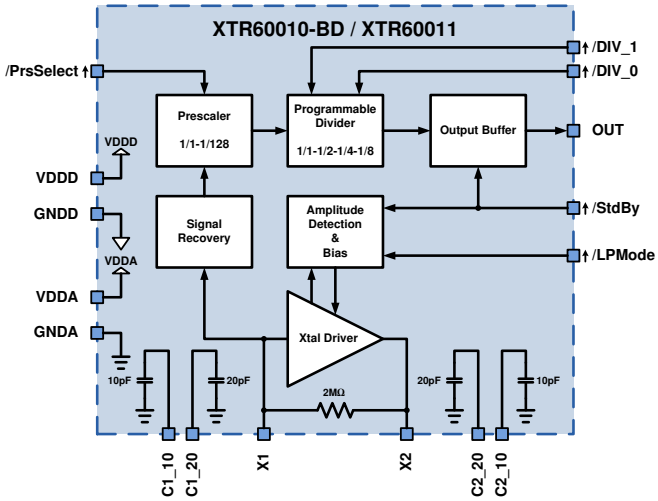
PRODUCT VARIANTS

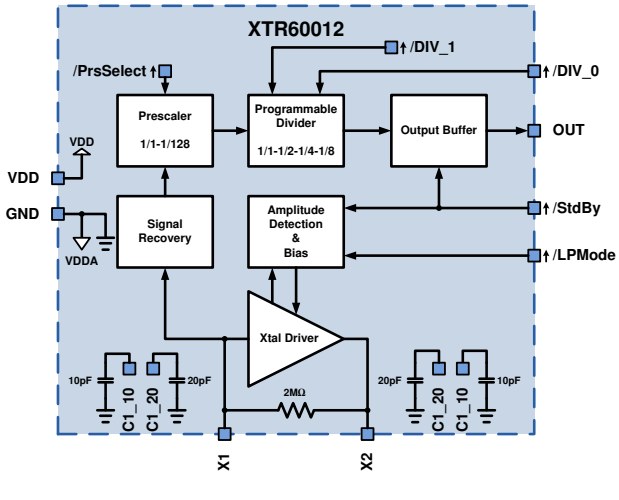




ePAD on bottom of package in "FE" option connected to VDD. ePAD can be left floating on the PCB.

BLOCK DIAGRAM





Arrows aside pin names indicate whether the input is internally pulled up or down.

PIN DESCRIPTION

XTR60011		
Pin Number	**Name**	**Description**
1	**/PrsSelect**	Selects prescaler division (128) when driven LOW.
2	**/DIV_1**	MSB of internal programmable divider. Negative logic. See Table 1.
3	**/DIV_0**	LSB of internal programmable divider. Negative logic. See Table 1.
4	**/LPMode**	Sets low-power operation mode when driven LOW.
5	**/StdBy**	Sets stand-by mode (oscillation stopped and high impedance output) when driven LOW.
6	**X1**	Input of crystal driver. It can also be used as input of an external clock.
7	**C1_10**	Top plate of a ground referenced, internal 10pF capacitor. To be used as crystal load.
8	**C1_20**	Top plate of a ground referenced, internal 20pF capacitor. To be used as crystal load.
9	**C2_20**	Top plate of a ground referenced, internal 20pF capacitor. To be used as crystal load.
10	**C2_10**	Top plate of a ground referenced, internal 10pF capacitor. To be used as crystal load.
11	**X2**	Output of crystal driver.
12	**GNDA**	Analog ground.
13	**GNDD**	Digital and output buffer ground.
14	**OUT**	Oscillator output.
15	**VDDD**	Digital and output buffer supply voltage.
16	**VDDA**	Analog supply voltage.

XTR60012		
Pin Number	**Name**	**Description**
1	**/DIV_0**	Controls internal programmable divider. Divides by 2 when driven LOW.
2	**/LPMode**	Sets low-power operation mode when driven LOW.
3	**/StdBy**	Sets stand-by mode (oscillation stopped and high impedance output) when driven LOW.
4	**X1**	Input of crystal driver. It can also be used as input of an external clock.
5	**X2**	Output of crystal driver.
6	**GND**	Ground.
7	**OUT**	Oscillator output.
8	**VDD**	Supply voltage.

Table 1. Function Table

/StdBy	/PrsSelect	/DIV_1	/DIV_0	Division Factor	OUT
0 (osc. stopped)	X	X	X	X	High Z
1	1	1	1	1	Freq
1	1	1	0	2	Freq/2
1	1	0	1	4	Freq/4
1	1	0	0	8	Freq/8
1	0	1	1	128	Freq/128
1	0	1	0	256	Freq/256
1	0	0	1	512	Freq/512
1	0	0	0	1024	Freq/1024

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Supply voltage V_{DDA}, V_{DDD}[1]	2.5[2]		5.5	V
Voltage on X1, X2, C1_xx and C2_xx to GNDA	0		V_{DDA}	V
Voltage on /DIV_0, /DIV_1, /PrsSelect, /LPMode, /StdBy to GNDD	0		V_{DDD}	V
Crystal Frequencies F_O	0.03[3]		50	MHz
Junction Temperature[4] T_j	-60		230	℃

[1] VDDA and VDDD must be the same voltage.
[2] For operation frequencies above 20MHz, minimum supply voltage is 2.8V.
[3] For operation frequencies below 1MHz, /LPMode must be LOW.
[4] Operation beyond the specified temperature range is achieved.

ELECTRICAL SPECIFICATIONS

Unless otherwise stated, specification applies for V_{DDA}=V_{DDD}=5V, -60℃<T_j<230℃.

Parameter	Condition	Min	Typ	Max	Units
Supply Current					
Analog stand-by supply current I_{VDDASB}	/StdBy=0V. No switching. T_j=-60℃ T_j=85℃ T_j=230℃		 43 47 60		µA
Digital stand-by supply current I_{VDDDSB}	/StdBy=0V. No switching. T_j=-60℃ T_j=85℃ T_j=230℃		 TBD		µA
Analog dynamic supply current I_{VDDA}	VDDA=VDDD=2.5V, F_O<1MHz, /LPMode=0 T_j=-60℃ T_j=85℃ T_j=230℃		 0.16 0.26 0.33		mA
	VDDA=VDDD=2.5V, F_O=1MHz, /LPMode=1 T_j=-60℃ T_j=85℃ T_j=230℃		 0.33 0.56 0.82		
	VDDA=VDDD=2.8V, F_O=40MHz, /LPMode=1 T_j=-60℃ T_j=85℃ T_j=230℃		 0.62 0.97 1.20		
	VDDA=VDDD=5.5V, F_O<1MHz, /LPMode=0 T_j=-60℃ T_j=85℃ T_j=230℃		 0.48 0.53 0.58		
	VDDA=VDDD=5.5V, F_O=1MHz, /LPMode=1 T_j=-60℃ T_j=85℃ T_j=230℃		 1.70 1.85 1.94		
	VDDA=VDDD=5.5V, F_O=40MHz, /LPMode=1 T_j=-60℃ T_j=85℃ T_j=230℃		 1.86 2.01 2.03		
Power dissipation capacitance C_{P_VDDD}	I_{VDDD} = (C_{P_VDDD} + C_L) x Freq x V_{DDD} C_L is the total load capacitance connected to OUT.		35.5		pF

ELECTRICAL SPECIFICATIONS (CONTINUED)

Unless otherwise stated, specification applies for V_{DDA}=V_{DDD}=5V, -60℃<T_j<230℃.

Digital Inputs (/LPMode, /PrsSelect, /StdBy, /DIV_0, /DIV_1)					
HIGH level input voltage **V_{T+}**		3.0	3.3	3.6	V
LOW level input voltage **V_{T-}**		1.6	1.9	2.2	V
Hystereris voltage (V_{T+}-V_{T-}) **V_{Hys}**		0.95	1.25	1.4	V
Input leakage current **I_{IL}**	Inputs connected to VDD for pulled-up inputs. T_j=25℃ T_j=230℃		0.01 3.2	0.05 3.8	µA
Pull-up strength **I_{PU}**	Pulled-up inputs connected to GND. T_j=25℃ T_j=230℃		10 14	10 14	µA
Output Buffer					
Peak output current **I_{OUT_peak}**	T_j=230℃.		±50		mA
HIGH level output voltage **V_{OH}**	I_{OUT}=20mA (sourcing), T_j=230℃.		4		V
LOW level output voltage **V_{OL}**	I_{OUT}=-20mA (sinking), T_j=230℃.		0.4		V
Output rise time **t_r**	0.1xVDDD to 0.9xVDDD; C_{load}=20pF, T_j=230℃.		5		ns
Output fall time **t_f**	0.9xVDDD to 0.1xVDDD; C_{load}=20pF, T_j=230℃.		3		ns
Crystal Driver Stage					
Driver transconductance **G_m**	VDDA=2.8V T_j=-60℃ T_j=230℃		TBD		mS
Driver output impedance **R_o**	VDDA=2.8V T_j=-60℃ T_j=230℃		TBD		Ω
Oscillation stable after VDDA goes up **$t_{power\_up\ 32KHz}$**	VDDA=2.8V for F_O=32kHz T_j=-60℃ T_j=230℃		50 70		ms
Oscillation stable after VDDA goes up **$t_{power\_up\ 50MHz}$**	VDDA=2.8V for F_O=50MHz T_j=-60℃ T_j=230℃		0.45 0.6		ms
Oscillation stable after /StdBy goes up **$t_{start\_up\ 32KHz}$**	VDDA=2.8V T_j=-60℃ T_j=230℃		TBD		ms
Oscillation stable after /StdBy goes up **$t_{start\_up\ 50MHz}$**	VDDA=2.8V T_j=-60℃ T_j=230℃		TBD		ms
Internal Load Capacitors					
Accuracy	T_j=25℃		±16		%
Linear temperature coefficient **TC1**	$C(T)=C(T_0) \times [1 + TC1 \times (T-T_0) + TC2 \times (T-T_0)^2]$		23		ppm/K
Quadratic temperature coefficient **TC2**			0.013		ppm/K²
Total variation with temperature **ΔC**	ΔT=290K (from -60℃ to 230℃)		0.8		%

TYPICAL PERFORMANCE

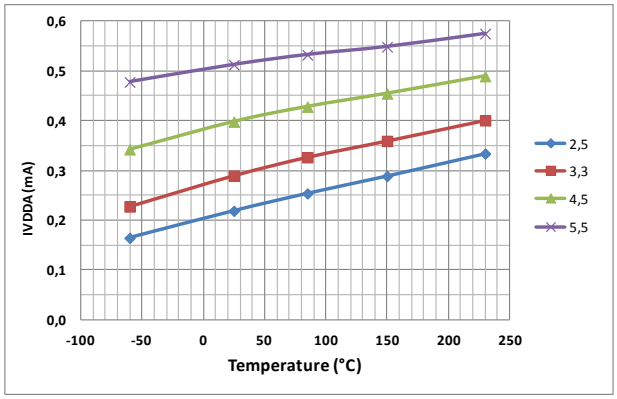


Figure 1. Current consumption through VDDA vs. temperature for different supply voltages in low-power mode (/LPMode=0). Freq=1MHz.

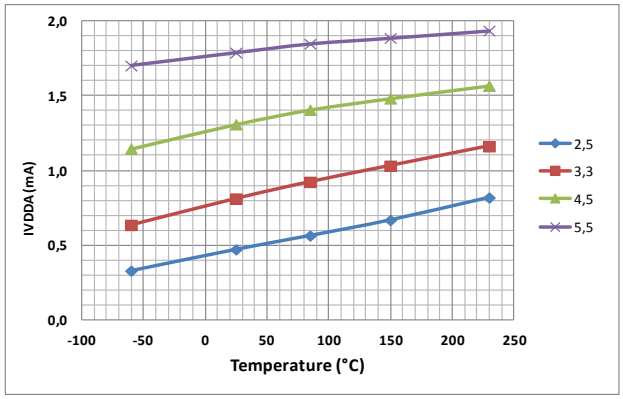


Figure 2. Current consumption through VDDA vs. temperature for different supply voltages in full-speed mode (/LPMode=1). Freq=1MHz.

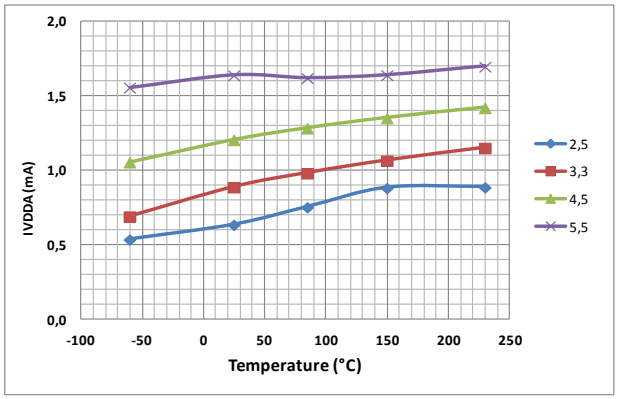


Figure 3. Current consumption through VDDA vs. temperature for different supply voltages in full-speed mode (/LPMode=1). Freq=20MHz.

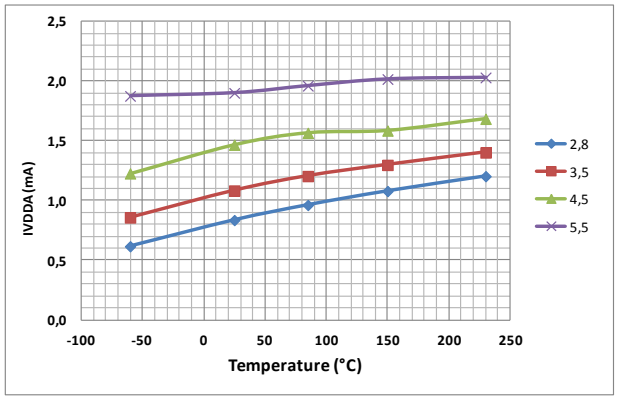


Figure 4. Current consumption through VDDA vs. temperature for different supply voltages in full-speed mode (/LPMode=1). Freq=40MHz.

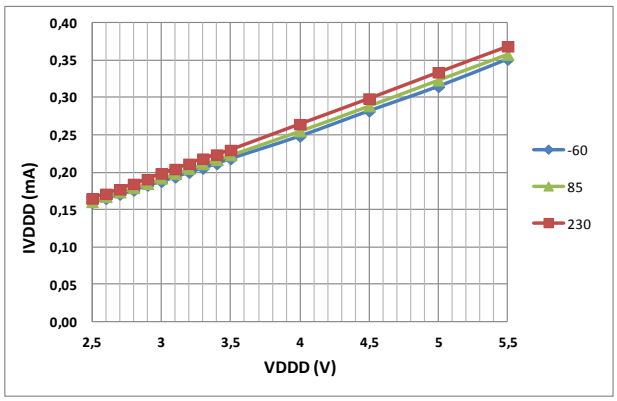


Figure 5. Current consumption through VDDD vs. supply voltage for different temperatures. Freq=1MHz, C_L=27pF.

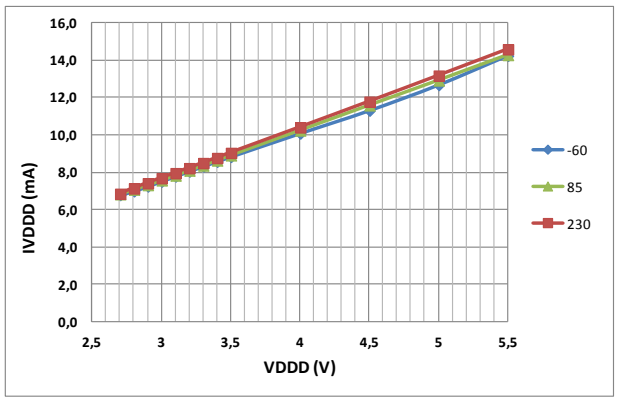


Figure 6. Current consumption through VDDD vs. supply voltage for different temperatures. Freq=40MHz, C_L=27pF.

THEORY OF OPERATION

Introduction

The XTR60010 is a family of high-temperature, extended lifetime crystal oscillator drivers. Operation is guaranteed from -60℃ to +230℃ and for supply voltages from 2.5V to 5.5V.

Integrated functional features include selectable prescaler (1/128), programmable frequency divider (1/2/4/8), operation in low-power mode for low frequency crystals, integrated capacitors for crystal loading and stand-by mode which stops oscillations and sets the output buffer to the high-Z state. Using the internal prescaler and frequency divider, division factors from 1 to 1024 can be obtained. The internal crystal driver has automatic gain control to be able to accommodate to the used crystal, with no intervention needed from the customer, as required by some competing products.

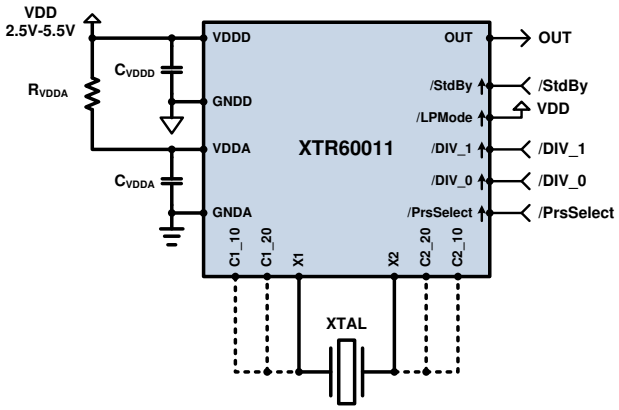
Operation Modes

Full speed mode

This mode, selected by setting /LPMode=1, is intended for oscillation frequencies in the range 1MHz to 50MHz.

In this case, the crystal driver adjusts its own gain so that the oscillation amplitude at X1 is constant at about 300-500mV.

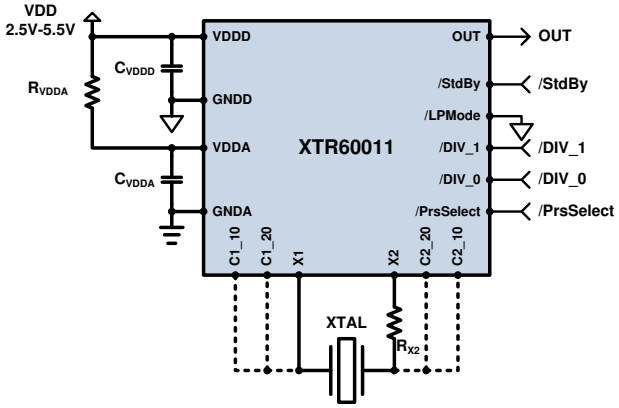
The following image shows a typical application schematic in full-speed mode. Separate decoupling capacitors are recommended on VDDA and VDDD in order to reduce any possible noise coupling from the digital part of the circuit onto the analog part.



Low-power mode

Low-power mode, selected by setting /LPMode=0, is intended for operation at frequencies below 10MHz. In particular, this mode should be selected to operate at 32.768kHz.

In this mode, the crystal driver operates at fixed gain.

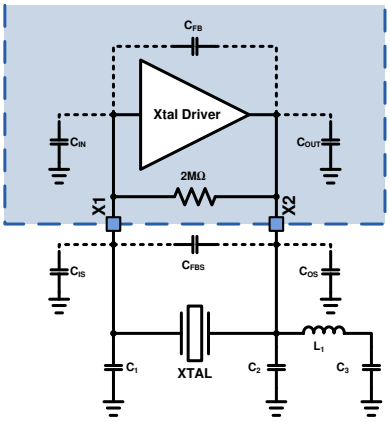


Operation with overtone crystals

XTR60010 products can also work with overtone crystals. Here below we expose the basic concepts when using a third overtone (3rd OT) crystal.

The basic oscillation schematic of the crystal oscillator must be modified in order to oscillate at the 3rd OT frequency (f_{OT}), otherwise the crystal will oscillate at about one third of the expected frequency.

The schematic below shows the crystal driver inside the XTR60010 parts, as well as external components to be added and stray capacitances present at die/package level and at substrate or PCB level. Capacitors connected by dashed lines are stray capacitances, whereas C_1, C_2, C_3 and L_1 are actual parts to be added at substrate or PCB level.



Capacitors C_1, C_2 and C_3 must have low loss dielectrics, such as NP0, with operating frequency beyond the expected OT frequency.

Inductor L_1 must have high quality factor Q at the OT frequency. As a rough rule, an inductor with Q>30, R_{DC}<1Ω and self resonant two or three times the OT frequency should be selected.

Inductor L_1 must be chosen to resonate with the total capacitance on terminal X2 in order to filter out the low frequencies of oscillation. This roll-off frequency is generally chosen at $2f_{OT}/3$.

$$f_R = \frac{2f_R}{3} = \frac{1}{2\pi\sqrt{(C_2 + C_{OUT} + C_{OS})L_1}}$$

At f_{OT}, the parallel of L_1 with C_2 provides an effective capacitance C_{2EFF} which must be considered together with C_1 in order to properly load the crystal. The reactance of C_{2EFF} at f_{OT} is provided by the following equation.

$$X_{C_{2EFF}} = \frac{1}{2\pi f_{OT} C_{2EFF}}$$

Capacitor C3 must be chosen so that its reactance at f_{OT} could be neglected when compared to that of L_1.

Under this assumption, the values of capacitor C_2 and inductor L_1 can be obtained as follows.

$$C_2 = \frac{9C_{2EFF} + 4(C_{OUT} + C_{OS})}{5}$$

$$L_1 = \frac{5}{4(2\pi f_{OT})^2(C_{2EFF} + C_{OUT} + C_{OS})}$$

To obtain the values of C_1 and C_2 in a practical case, the total stray capacitance in parallel with the crystal must be known. This total stray capacitance is given by

$$C_{ST} = C_{FB} + \frac{C_{IN}C_{OUT}}{(C_{IN}+C_{OUT})} + C_{FBS} + \frac{C_{IS}C_{OS}}{(C_{IS}+C_{OS})}$$

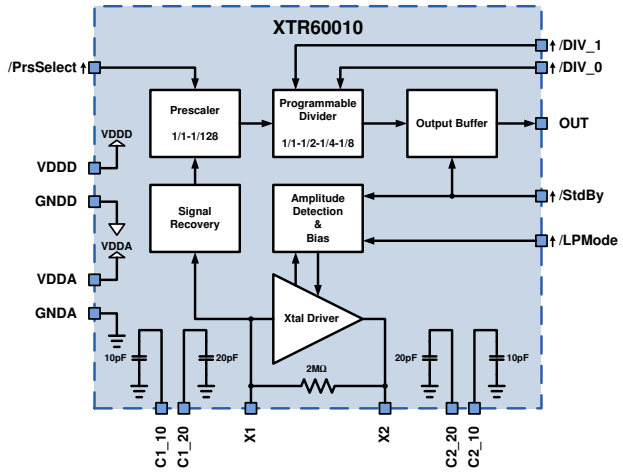
Considering a known load capacitance C_L provided by the crystal manufacturer and under the assumption that C_1=C_{2EFF}, it is obtained

$$C_L = C_{ST} + \frac{C_1 C_{2EFF}}{(C_1 + C_{2EFF})}$$

$$C_{2EFF} = 2(C_L - C_{ST})$$

Internal Blocks and Functional Features

The block diagram of the XTR60010 die is shown here below. Arrows aside input signal names indicate that the inputs are internally pulled up.



The XTR60010 has two power supply domains. The analog supply domain between VDDA and GNDA concerns the crystal driver, the amplitude detection block and the signal recovery block. The digital domain supplies the prescaler, frequency divider and output buffer.

Digital inputs

All digital inputs of the XTR60010 (/LPMode, /PrsSelect, /DIV_0, /DIV_1 and /StdBy) are Schmitt trigger type and are internally pulled up.

Crystal driver and amplitude detection block

The crystal driver operates in two different modes depending upon the status of /LPMode.
For /LPMode=1, the driver operates in full-speed mode and crystals up to 50MHz can be used. In this mode an amplitude detection block changes the driver gain so that a stable oscillation is obtained on X1 with amplitude between 300mV to 500mV depending on supply voltage and temperature.
When /LPMode=0, the driver operates in low-power mode, which is intended for low oscillation frequencies. In this mode the driver operates at fixed transconductance.
The /StdBy signal is used to stop the oscillation and to set the crystal driver and the amplitude detection block into a low quiescent current state. This also sets the output buffer of the circuit at hi-Z state.
Terminal X1 can also be used to receive an external clock signal in order to be buffered, using or not the internal prescaler and programmable divider. The external clock signal should have neat transitions without any bouncing from 10% to 90% of VDD.

Signal recovery block

The oscillation signal is recovered on terminal X1, which in general presents a much more symmetrical shape than the signal on X2. This fact is used in order to provide at the output a signal with a duty-ratio as close to 50% as possible.

Prescaler and programmable frequency divider

Two separate blocks are offered to the user in order to obtain eight possible division factors.
A prescaler, with a division factor of 1/128 can be inserted in the signal path by setting /PrsSelect=0.
Additionally to the prescaler, a programmable frequency divider can be used to obtain four binary weighted division factors.
The following table summarizes the total division factor obtained as a function of /PrsSelect, /DIV_0 and /DIV_1.

/PrsSelect	/DIV_1	/DIV_0	Division Factor
1	1	1	1
1	1	0	2
1	0	1	4
1	0	0	8
0	1	1	128
0	1	0	256
0	0	1	512
0	0	0	1024

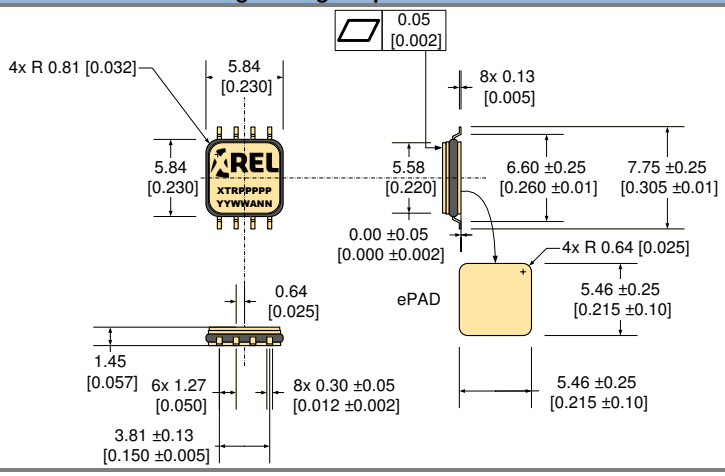
Output buffer

The output buffer provides a neat clock signal with duty-ratio close to 50% and is able to operate on loads of up to 50pF at 50MHz. A ruggedized architecture is used in order to be tolerant to impedance mismatches with respect to the load. However, for signal integrity reasons, good load matching is recommended.
The output buffer is responsible for the most of the digital current consumption of the part. In order to reduce the intrinsic current consumption, cross-conduction avoidance techniques were used in the output buffer. As a reminder, the digital current consumption can be written as $C.f.V_{DD}$, where C is the total equivalent capacitance (internal + load), f is the operating frequency and V_{DD} is the supply voltage.
When /StdBy=0, besides stopping oscillation of the crystal driver, the XTR60010 presents a hi-Z state on the output buffer.

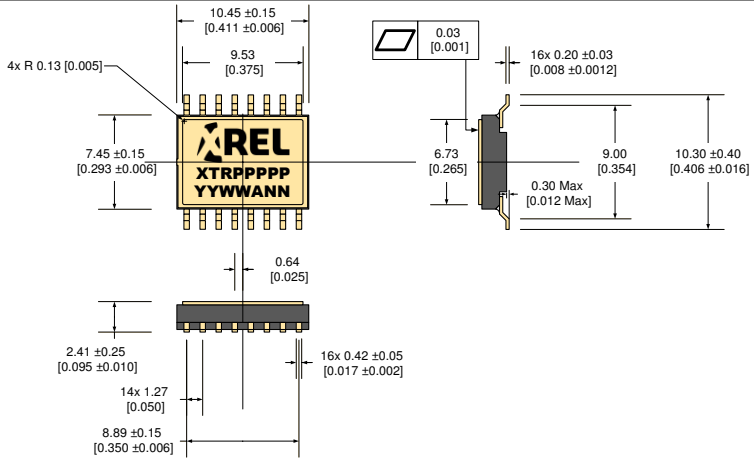
PACKAGE OUTLINES

Dimensions shown in mm [inches]. Tolerance ±0.13 mm [±.005 in], unless otherwise specified.

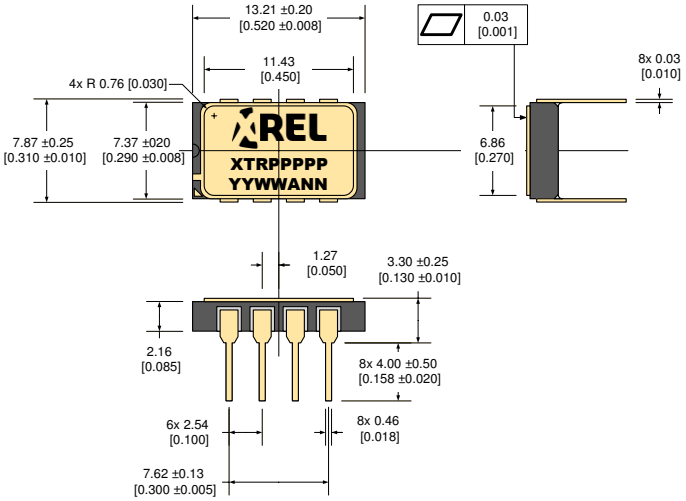
Ceramic gull-wing flat pack with ePad DFP8



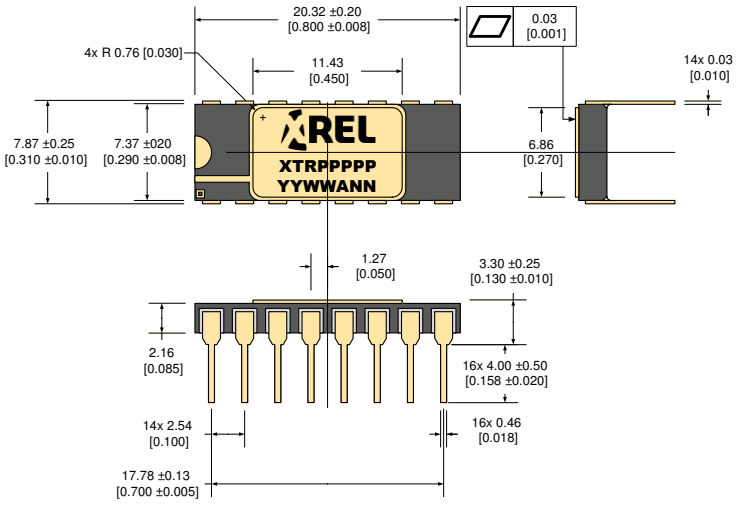
Ceramic Small Outline IC SOIC16



Ceramic Side Braze Dual In-line DIP8



Ceramic Side Braze Dual In-line DIP16



Part Marking Convention	
Part Reference: XTRPPPPPP	
XTR	X-REL Semiconductor, high-temperature, high-reliability product (XTRM Series).
PPPPP	Part number (0-9, A-Z).
Unique Lot Assembly Code: YYWWANN	
YY	Two last digits of assembly year (e.g. 11 = 2011).
WW	Assembly week (01 to 52).
A	Assembly location code.
NN	Assembly lot code (01 to 99).

IMPORTANT NOTICE & DISCLAIMER

CONTACT US

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