

HIGH-TEMPERATURE FAMILY OF 40V N-CANNEL POWER MOSFET WITH DRIVER

FEATURES

- ▲ Operational beyond the -60°C to +230°C temperature range.
- ▲ Robust operation as low-side or high-side switch.
- ▲ Input-to-output level shifting from -30V to +40V.
- ▲ Standard Schmitt-trigger CMOS input.
- ▲ Exists in inverting and non-inverting versions
- ▲ Plug-and-play with any digital 5V output.
- ▲ Over current (desaturation) protection.
- ▲ Under voltage lockout UVLO protection on the output stage.
- ▲ Low on-resistance :
 - XTR20411 : 890 mΩ @ 230°C
 - XTR20412 : 325 mΩ @ 230°C
- ▲ Large peak current capabilities:
 - XTR20411 : 2.9A @ 230°C
 - XTR20412 : 8.4A @ 230°C
- ▲ Low On- and Off-time (<170nsec @ 230°C)
- ▲ Monolithic design.
- ▲ Latch-up free.
- ▲ Ruggedized SMT and thru-hole packages.
- ▲ Also available as bare die.

APPLICATIONS

- ▲ Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole.
- ▲ DC/DC converters, motor drive, switching power supplies, switching control.

DESCRIPTION

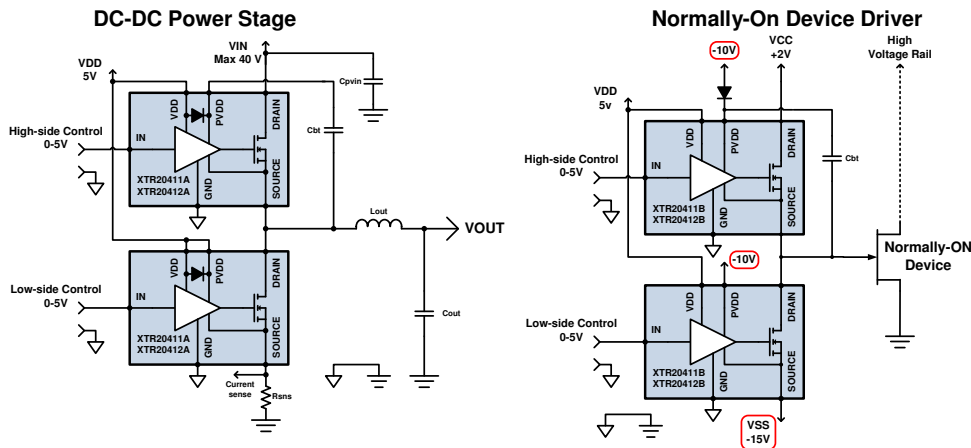
XTR20410 is a family of extremely flexible power N-channel MOSFETs with integrated driver designed for extreme reliability and high temperature applications such as DC/DC converters, motor control and power switching. XTR20410 parts can be used either as high-side (40V max), low-side, or low-side switch with negative offset (-30V max) on the output stage (SOURCE connected to a negative voltage), while receiving a control input signal referenced to GND. XTR20410 parts can be directly driven by any 5V digital output, making them fully plug-and-play devices, avoiding any time consuming optimization of the matching network between driver and power transistor.

The XTR20410 family is composed of two different dies each with different maximum output current.

XTR20410 parts are robust to usual spikes associated with parasitic inductors and fast transients in switching applications. Features of XTR20410 family parts include UVLO at the driver output, desaturation protection of the output transistor with soft shut-down functionality and possibility to select inversion of control signal.

Full functionality is guaranteed from -60°C to +230°C, though operation well beyond this temperature range is achieved. XTR20410 family parts have been designed to reduce system cost and ease adoption by reducing the learning curve and providing smart and easy to use features. The Parts from the XTR20410 family are available in ruggedized SMD and through hole hermetic packages, as well as bare die.

PRODUCT HIGHLIGHT



ORDERING INFORMATION



| Product Reference | Temperature Range | Package | Pin Count | Marking |
|-------------------|-------------------|------------------------------|-----------|-----------|
| XTR20411-BD | -60°C to +230°C | Bare die | | XTR20411 |
| XTR20412-BD | -60°C to +230°C | Bare die | | XTR20412 |
| XTR20411A-D | -60°C to +230°C | Ceramic side braze DIL | 8 | XTR20411A |
| XTR20411A-FE | -60°C to +230°C | Gull-wing flatpack with ePad | 8 | XTR20411A |
| XTR20414A-D | -60°C to +230°C | Ceramic side braze DIL | 8 | XTR20414A |
| XTR20411A-T | -60°C to +230°C | TO257 | 6 | XTR20411A |
| XTR20412A-T | -60°C to +230°C | TO257 | 6 | XTR20412A |
| XTR20411B-D | -60°C to +230°C | Ceramic side braze DIL | 8 | XTR20411B |
| XTR20411B-T | -60°C to +230°C | TO257 | 6 | XTR20411B |
| XTR20412B-T | -60°C to +230°C | TO257 | 6 | XTR20412B |

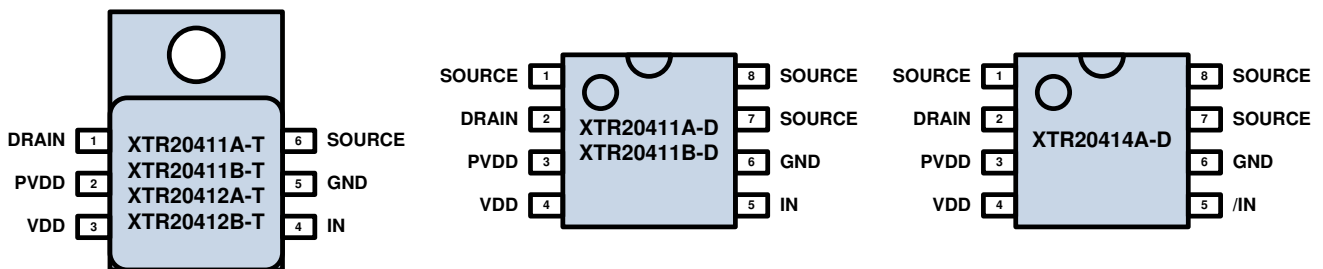
Other packages and packaging configurations possible upon request. For some packages or packaging configurations, MOQ may apply.

ABSOLUTE MAXIMUM RATINGS

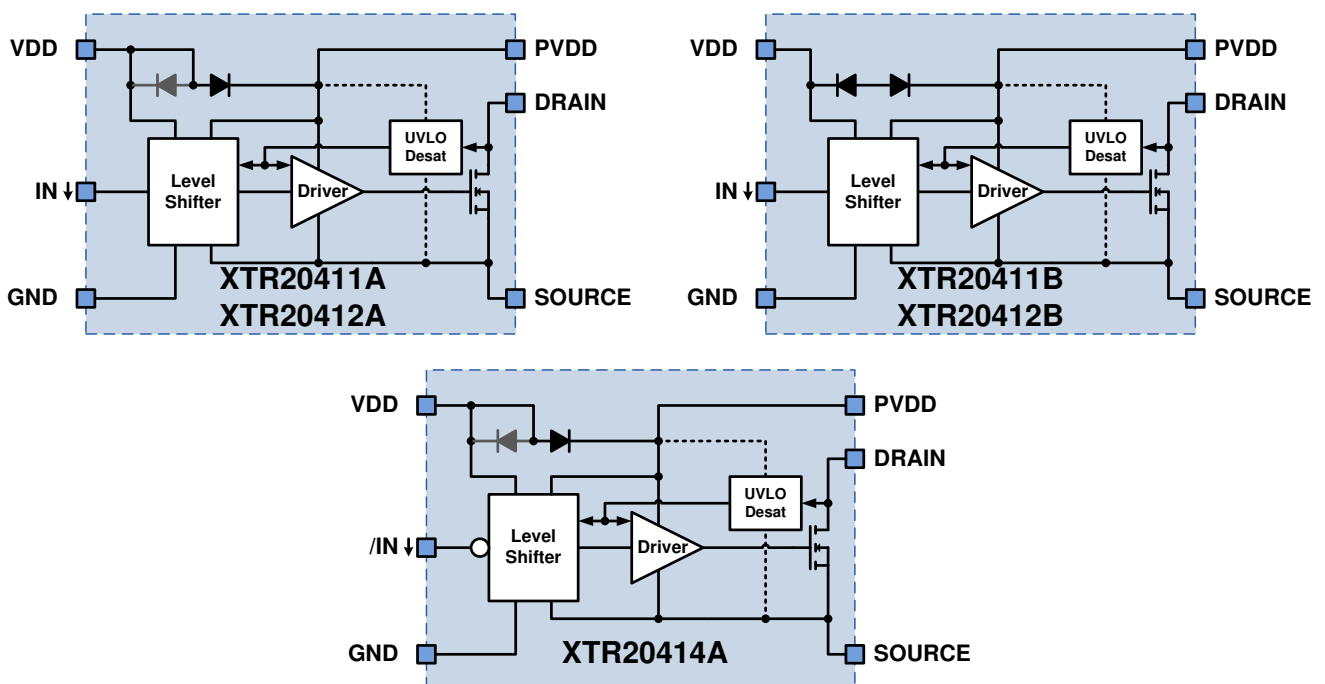
| | |
|--|---------------------|
| Voltage on DRAIN to SOURCE | -1.5 to 55V |
| Voltage on IN and VDD to GND | -0.5 to 6.0V |
| Voltage on PVDD to SOURCE | -0.5 to 7.5V |
| Voltage on SOURCE to GND for XTR20411A and XTR20412A | -1 to 50V |
| Voltage on SOURCE to GND for XTR20411B and XTR20412B | -35V to 55V |
| Storage Temperature Range | -70°C to +230°C |
| Operating Junction Temperature Range | -70°C to +300°C |
| ESD Classification | 1kV HBM MIL-STD-883 |

Caution: Stresses beyond those listed in “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to “ABSOLUTE MAXIMUM RATINGS” conditions for extended periods may permanently affect device reliability.

PRODUCT VARIANTS



BLOCK DIAGRAM



Arrows aside pin names indicate that pin is internally pulled down.
 XTR20414A is identical to XTR20411A except that the XTR20414A has inverted input /IN instead of IN.
 Different functionalities are available depending upon packaging configuration. Carefully read sections “Available Functionalities for Each Product Version” and “Theory of Operation” in order to select the packaging option that best fits your needs.

PIN DESCRIPTION
XTR20411A-T, XTR20411B-T, XTR20412A-T, XTR20412B-T

| Pin Number | Name | Description |
|------------|---------------|---|
| 1 | DRAIN | Drain of the power NMOS transistor. |
| 2 | PVDD | Supply voltage of power section. Referenced to SOURCE. |
| 3 | VDD | Supply voltage of the input section. Referenced to GND. |
| 4 | IN | Input signal. Referenced to GND. <u>Internally pulled down.</u> |
| 5 | GND | Circuit ground. |
| 6 | SOURCE | Source of the power NMOS transistor. |

XTR20411A-D, XTR20411B-D

| Pin Number | Name | Description |
|------------|---------------|---|
| 1 | SOURCE | Source of the power NMOS transistor. |
| 2 | DRAIN | Drain of the power NMOS transistor. |
| 3 | PVDD | Supply voltage of power section. Referenced to SOURCE. |
| 4 | VDD | Supply voltage of the input section. Referenced to GND. |
| 5 | IN | Input signal. Referenced to GND. <u>Internally pulled down.</u> |
| 6 | GND | Circuit ground. |
| 7 | SOURCE | Source of the power NMOS transistor. |
| 8 | SOURCE | Source of the power NMOS transistor. |

XTR20411A-FE

| Pin Number | Name | Description |
|------------|---------------|--|
| 1 | DRAIN | Drain of the power NMOS transistor. |
| 2 | DRAIN | Drain of the power NMOS transistor. |
| 3 | PVDD | Supply voltage of power section. Referenced to SOURCE. |
| 4 | VDD | Supply voltage of the input section. Referenced to GND. |
| 5 | IN | Input signal with inversion. Referenced to GND. <u>Internally pulled down.</u> |
| 6 | GND | Circuit ground. |
| 7 | SOURCE | Source of the power NMOS transistor. |
| 8 | SOURCE | Source of the power NMOS transistor. |

XTR20414A-D

| Pin Number | Name | Description |
|------------|---------------|--|
| 1 | SOURCE | Source of the power NMOS transistor. |
| 2 | DRAIN | Drain of the power NMOS transistor. |
| 3 | PVDD | Supply voltage of power section. Referenced to SOURCE. |
| 4 | VDD | Supply voltage of the input section. Referenced to GND. |
| 5 | /IN | Input signal with inversion. Referenced to GND. <u>Internally pulled down.</u> |
| 6 | GND | Circuit ground. |
| 7 | SOURCE | Source of the power NMOS transistor. |
| 8 | SOURCE | Source of the power NMOS transistor. |

RECOMMENDED OPERATING CONDITIONS

| Parameter | Min | Typ | Max | Units |
|---|--------------------|-----|-----|-------|
| Supply voltage VDD to GND | 4.5 | | 5.5 | V |
| Supply voltage PVDD to SOURCE | See UVLO threshold | | 5.5 | V |
| SOURCE to GND voltage XTR20411A, XTR20412A, XTR20414A | -1 | | 40 | V |
| SOURCE to GND voltage XTR20411B and XTR20412B | -30 | | 40 | V |
| Input voltage on IN to GND | -0.3 | | VDD | V |
| DRAIN-SOURCE voltage (V_{DS}) | -1 | | +40 | V |
| Junction Temperature ¹ T_j | -60 | | 230 | °C |

¹ Operation beyond the specified temperature range is achieved with little degradation on electrical parameters.

THERMAL CHARACTERISTICS

| Parameter | Condition | Min | Typ | Max | Units |
|--|-----------|-----|-----|-----|-------|
| XTR20411A/B-D, XTR20414A-D (Ceramic Side Brazed DIP8) | | | | | |
| Thermal Resistance: J-C $R_{Th\ J-C}$ | | | 30 | | °C/W |
| Thermal Resistance: J-A $R_{Th\ J-A}$ | | | 100 | | °C/W |
| XTR20411A/B-T (6-lead TO257) | | | | | |
| Thermal Resistance: J-C $R_{Th\ J-C}$ | | | 10 | | °C/W |
| Thermal Resistance: J-A $R_{Th\ J-A}$ | | | 50 | | °C/W |
| XTR20412A/B-T (6-lead TO257) | | | | | |
| Thermal Resistance: J-C $R_{Th\ J-C}$ | | | 5 | | °C/W |
| Thermal Resistance: J-A $R_{Th\ J-A}$ | | | 45 | | °C/W |

ELECTRICAL SPECIFICATIONS XTR20411A/B AND XTR20414A
STATIC CHARACTERISTICS

Unless otherwise stated, VDD=5V, PVDD=5V, GND=SOURCE, IN=0V, V_{DS}=20V, I_{DRAIN}=1A, -60°C<T_C<230°C. Except the inverted input logic, specifications of the **XTR20414A** are the same than the XTR20411A.

| Parameter | Condition | Min | Typ | Max | Units |
|--|--|-----|--------------------------|-------------|-------|
| Supply Current | | | | | |
| Static VDD Supply Current I _{VDD_Sta} | V _{IN} =GND or VDD T _C =25 °C T _C =230 °C | | 20 25 | | μA |
| Static PVDD Supply Current I _{PVDD_Sta} | V _{IN} =GND or VDD; Type A; T _C =25 °C Type A; T _C =230 °C Type B; T _C =25 °C Type B; T _C =230 °C | | 130 180 150 220 | | μA |
| Control INPUT | | | | | |
| Low Level Input voltage V _{IL} | T _C =25 °C | | 1.7 | | V |
| High Level Input voltage V _{IH} | T _C =25 °C | | 3.4 | | V |
| Input Current I _{IN} | V _{IN} =GND or VDD T _C =25 °C T _C =230 °C | | 3 4 | | μA |
| Under Voltage Lockout (UVLO) | | | | | |
| V _{PVDD} Start Voltage ¹ V _{UVLOR} | Rising PVDD threshold XTR20411A/XTR20414A XTR20411B | 3.2 | 3.5 4.1 | 3.8 4.5 | V |
| V _{PVDD} Start-stop Hysteresis V _{UVLOH} | XTR20411A/XTR20414A XTR20411B | | 300 400 | | mV |
| Output Transistor | | | | | |
| Drain-Source Breakdown Voltage V _{(BR)DSS} | T _C =25 °C | 55V | | | V |
| Off-State Drain Current I _{DSS} | Output transistor OFF and V _{DS} =40V T _C =25 °C T _C =230 °C | | | 0.002 25 | μA |
| Static ON Resistance R _{DSon} | I _{DRAIN} =1A, sied brazed DIP8 package (XTR20411-D) T _C =25 °C T _C =230 °C | | 450 890 | | mΩ |
| Source-Drain Body Diode | | | | | |
| Continuous Forward Current I _{FBD} | | 1 | | | A |
| Forward Voltage V _{FBD} | I _{FBD} =1A T _C =25 °C T _C =230 °C | | TBD TBD | | V |
| Bootstrap Diode (XTR20411A and XTR20414A) | | | | | |
| Continuous Forward Current I _{BSTD} | V _F =1.5V T _C =25 °C T _C =230 °C | | 0.55 0.50 | | A |
| Forward Voltage V _{BSTD} | I _{BSTD} =300mA T _C =25 °C T _C =230 °C | | 1.25 1.15 | | V |

¹ Below this threshold, the output nMOS is OFF, for PVDD rising.

¹ Once V_{GS} of the output transistor is high, a comparator checks if I_{DS}<I_{DESAT} after this blanking time.

ELECTRICAL SPECIFICATIONS XTR20411A/B AND XTR20414A (CONTINUED)
DYNAMIC CHARACTERISTICS

 Unless otherwise stated, VDD=5V, PVDD=5V, GND=SOURCE, IN=0V, V_{DS}=20V, I_{DRAIN}=1A, -60°C<T_C<230°C.

| Parameter | Condition | Min | Typ | Max | Units |
|--|---|-----|-----------------|-----|-------|
| Supply Current | | | | | |
| Dynamic VDD Supply Current I _{VDD_Dyn} | For Freq V _{IN} =1MHZ and duty cycle=50% | | | TBD | μA |
| Dynamic PVDD Supply Current I _{PVDD_Dyn} | For Freq V _{IN} =1MHZ and duty cycle=50% | | | 3 | mA |
| Max drain current and DESAT protection | | | | | |
| Peak Drain current I _{Dpeak} | 300ns pulse; V _{DS} =20V T _C =-60°C T _C =230°C | | 5.6 2.9 | | A |
| Max drain current after the blanking time I _{DESAT} | T _C =-60°C T _C =20°C T _C =230°C | | TBD 3 TBD | | A |
| Blanking Time ¹ t _{Blank} | | | 400 | | ns |
| Soft Turn-off Time t _{SSD} ² | T _C =230°C | | 260 | | ns |
| Switching Time 20411A/B and 20414A³ | | | | | |
| Delay ON Time ⁴ t _{d(ON)} | T _C =-60°C T _C =230°C | | 88 150 | | ns |
| Delay OFF Time t _{d(OFF)} | T _C =-60°C T _C =230°C | | 70 125 | | ns |

¹ Once V_{GS} of the output transistor is high, a comparator checks if I_{DS}<I_{DESAT} after this blanking time.

² If desaturation arises (I_{DS}>I_{DESAT}) after the blanking time, the output transistor is softly turned OFF during the t_{SSD} time.

³ Used as high side switch in a Buck converter configuration (40V supply, 300mA ON current)

⁴ From 50% input signal to 10% V_{DS} on the output transistor.

ELECTRICAL SPECIFICATIONS XTR20412
STATIC CHARACTERISTICS

 Unless otherwise stated, VDD=5V, PVDD=5V, GND=SOURCE, IN=0V, V_{DS}=20V, I_{DRAIN}=1A, -60 °C<T_C<230 °C.

| Parameter | Condition | Min | Typ | Max | Units |
|--|---|-----|--------------------------|-------------|-------|
| Supply Current | | | | | |
| Static VDD Supply Current I _{VDD_sta} | V _{IN} =GND or VDD T _C =25 °C T _C =230 °C | | 20 25 | | μA |
| Static PVDD Supply Current I _{PVDD_sta} | V _{IN} =GND or VDD Type A; T _C =25 °C Type A; T _C =230 °C Type B; T _C =25 °C Type B; T _C =230 °C | | 130 180 150 220 | | μA |
| Control INPUT | | | | | |
| Input Low voltage V _{IL} | T _C =25 °C | | 1.7 | | V |
| Input High voltage V _{IH} | T _C =25 °C | | 3.4 | | V |
| Input current I _{IN} | V _{IN} =GND or VDD T _C =25 °C T _C =230 °C | | 3 4 | | μA |
| Under Voltage Lockout (UVLO) | | | | | |
| V _{PVDD} start voltage ¹ V _{UVLOR} | Rising PVDD threshold XTR20412A XTR20412B | 3.2 | 3.5 4.1 | 3.8 4.5 | V |
| V _{PVDD} start-stop hysteresis V _{UVLOH} | XTR20412A XTR20412B | | 300 400 | | mV |
| Output Transistor | | | | | |
| Drain-Source Breakdown Voltage V _{(BR)DSS} | T _C =25 °C | 55V | | | V |
| Off-State Drain Current I _{DSS} | Output transistor OFF and V _{DS} =40V T _C =25 °C T _C =230 °C | | 18 | 0.006 75 | μA |
| Static ON Resistance R _{DSon} | I _{DRAIN} =100mA, TO257 package (XTR20412-T) T _C =25 °C T _C =230 °C | | 175 325 | | mΩ |
| Source-Drain Body Diode | | | | | |
| Continuous Forward Current I _{BD} | | 1 | | | A |
| Forward Voltage V _{BD} | I _{Body} =1A T _C =25 °C T _C =230 °C | | 0.95 0.75 | | V |
| Bootstrap Diode (XTR20412A only) | | | | | |
| Continuous Forward Current I _{BSTD} | V _F =1.5V T _C =25 °C T _C =230 °C | | 0.55 0.50 | | A |
| Forward Voltage V _{BSTD} | I _{BSTD} =300mA T _C =25 °C T _C =230 °C | | 1.25 1.15 | | V |

¹ Below this threshold, the output nMOS is OFF, for PVDD rising.

ELECTRICAL SPECIFICATIONS XTR20412 (CONTINUED)

DYNAMIC CHARACTERISTICS

Unless otherwise stated, VDD=5V, PVDD=5V, GND=SOURCE, IN=0V, VDS=20V, IDRAIN=1A, -60°C<Tc<230°C.

| Parameter | Condition | Min | Typ | Max | Units |
|---|--|-----|-----------------|-----|-------|
| Supply Current | | | | | |
| Dynamic VDD Supply Current IPVDD_Dyn | For Freq VIN=1MHZ and duty cycle=50% | | | TBD | µA |
| Dynamic PVDD Supply Current IPVDD_Dyn | For Freq VIN=1MHZ and duty cycle=50% | | | 5 | mA |
| Max drain current and DESAT protection | | | | | |
| Peak Drain current IDpeak | 150ns pulse; VDS=20V Tc=-60°C Tc=230°C | | 15.6 8.4 | | A |
| Max drain current after the blanking time IDESAT | Tc=-60°C Tc=20°C Tc=230°C | | TBD 8 TBD | | A |
| Blanking Time ¹ tBlank | | | 400 | | ns |
| Soft Turn-off Time tSSD ² | VDS=40V | | 260 | | ns |
| Switching Time 20412A/B³ | | | | | |
| Delay ON Time ⁴ td(ON) | Tj=-60°C Tj=230°C | | 108 170 | | ns |
| Delay OFF Time td(OFF) | Tj=-60°C Tj=230°C | | 90 145 | | ns |

¹ Once VGS of the output transistor is high, a comparator checks if ID<IDESAT after this blanking time.

² If desaturation arises (ID>IDESAT) after the blanking time, the output transistor is softly turned OFF during the tSSD time.

³ Used as high side switch in a Buck converter configuration (40V supply, 300mA ON current)

⁴ From 50% input signal to 10% VDS on the output transistor.

AVAILABLE FUNCTIONALITIES FOR EACH PRODUCT VERSION

| Functionality | Product Version | | | | | | |
|--------------------------------|-----------------------------|-------------|-----------------------------|-------------|-------------|-------------|-------------|
| | XTR20411A-D XTR20411A-FE | XTR20411A-T | XTR20411B-D XTR20411B-FE | XTR20411B-T | XTR20412A-T | XTR20412B-T | XTR20414A-D |
| Inverting input | | | | | | | ✓ |
| Operation as low-side switch | ✓ | ✓ | | | ✓ | | |
| Operation with negative offset | | | ✓ | ✓ | | ✓ | |
| Operation as high-side switch | ✓ | ✓ | | | ✓ | | ✓ |
| Integrated bootstrap diode | ✓ | ✓ | | | ✓ | | ✓ |
| Low power applications | ✓ | | ✓ | | | | ✓ |
| Mid power applications | | ✓ | | ✓ | | | |
| High power applications | | | | | ✓ | ✓ | |

THEORY OF OPERATION

Introduction

The XTR20410 is a family of 40V N-channel MOS transistors with integrated driver able to operate from -60°C to +230°C. Unique features of this product family make them an extremely flexible block when designing power switching applications.

Parts from the XTR20410 are divided into two variants depending upon the range of the common mode voltage of the output stage with respect to the input stage.

Devices with suffix "A" (XTR20411A, XTR20412A and XTR20414A) accept output common modes from -1V up to 40V and include a high-current diode from VDD (input stage) to PVDD (output stage) which can be used as bootstrap diode when using these parts as high-side drivers.

On the other side, devices with suffix "B" (XTR20411B and XTR20412B) accept output common modes from -30V up to 40V. In this case the PVDD supply voltage must be provided by an independent supply.

Level shifting is performed inside the XTR20410 parts.

The XTR20410 family includes several protection features offering enhanced robustness for operation in switching applications.

- Despite the recommended upper DC limit voltage on VDD and PVDD, the circuit can tolerate repetitive transient spike voltages up to 3V above the operation limits.

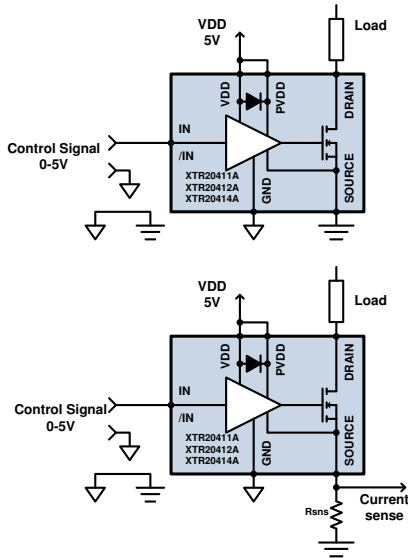
- A desaturation protection is implemented which softly turns off the output transistor whenever its current level exceeds a defined current threshold when in ON state (after a defined blanking time).
- Soft shut-down is implemented to prevent high dV/dt and di/dt on the application when the desaturation protection is activated.
- An UVLO on the floating output supply (PVDD to SOURCE) guarantees that below a defined threshold the output MOSFET is off.
- The recommended VDD range is between 4.5V and 5.5V. However, at lower VDD, the circuit could be functional as expected (with longer propagation delay). For very low VDD voltages (under 2-3V), it is guaranteed that the output MOSFET is off. Using this circuit below VDD=4.5V is however not recommended.

The XTR20410 family can also be packaged in such a way that the input signal logic is inverted (i.e. active low)

Operation Modes

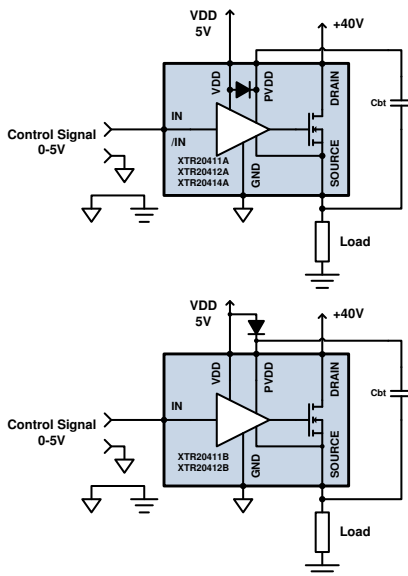
Low-side mode ($V_{SOURCE}=0V$)

In low-side mode operation, the SOURCE terminal is either directly tied to ground or through a small current sense resistor. For this operation mode, variant A is recommended. In this case, VDD and PVDD must be shorted or connected through a low pass RC filter from VDD to PVDD in order to filter out transient current spikes in VDD supply. Use a resistor up to 100 ohms and a capacitor of at least 100nF. Variant B could also be used, though turn-off delays of variant B with SOURCE close to ground are about twice those of variant A at the same conditions. The use of power and signal ground planes connected on a unique point as well as proper layout techniques is recommended.



High-side mode

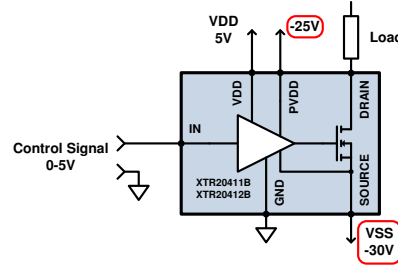
Operation in high-side mode can be obtained with both product variants (A and B). When using variant A, the bootstrap diode is already provided within the XTR20410 parts between VDD and PVDD terminals. For variant B, an external bootstrap diode must be used. In high-side mode the drain of the power transistor is directly tied to the bus voltage while the load is seen on the source of the output transistor.



Floating mode

This operation mode can only be achieved with the B variant, allowing the output stage to be shifted to negative as well as to

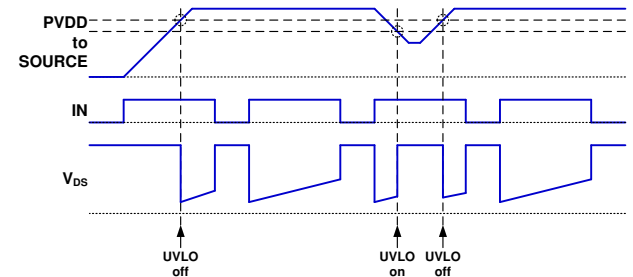
positive levels (from -30V to +40V) with respect to the input stage. In this case an external 5V floating source must be provided between PVDD and SOURCE.



Protections

Under Voltage Lockout (UVLO)

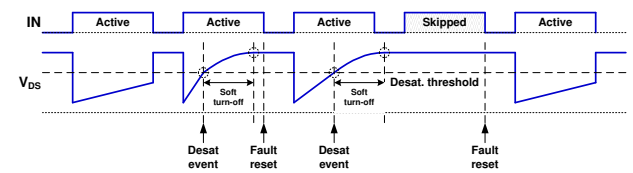
An UVLO detector continuously monitors the output stage supply voltage ($PVDD$ to $SOURCE$). During power-up, the UVLO protection guarantees that the output transistor is in off state for $V_{PVDD}-V_{SOURCE}$ below the V_{UVLOR} threshold for whichever state of IN (or /IN). Above the V_{UVLOR} threshold, the output MOSFET is controlled by the IN (or /IN) terminal. In case the UVLO protection is activated (UVLO on) while the output transistor is ON, this latter is immediately turned off. Once the UVLO event disappears (UVLO off), the output transistor state follows the input state.



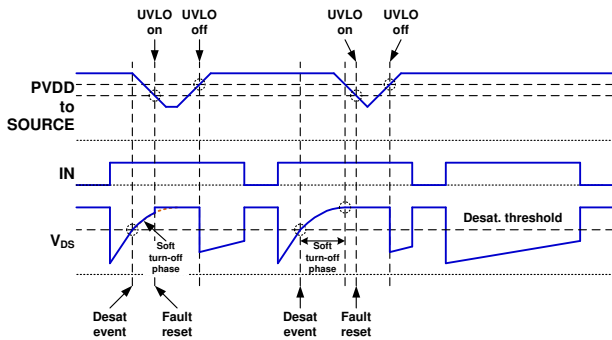
Note that due to internal ESD protections on the input pin (between GND and VDD), VDD could be self supplied if a 5V signal is applied on the input while VDD pin is floating. The recommended operation voltage for VDD is between 4.5V and 5.25V.

Desaturation (DESAT)

At each turn on of the output transistor, after a blanking time during which the desaturation protection is not allowed to react, the DRAIN to SOURCE voltage is continuously compared to an internal voltage threshold. For V_{DS} below this desaturation threshold, the output transistor still operates in its resistive regime (switch). If a desaturation event occurs after the blanking time, the output transistor is softly turned off and it remains off till the fault is cleared. If no UVLO event occurs during the soft shut down phase, the desaturation fault is cleared by the next falling edge of IN (rising edge for /IN) provided that the previous soft turn off is finished. If the soft shut down phase is not finished when the first falling edge arrives, the next input pulse is skipped and the output transistor remains off for one more period of the input signal.



If the UVLO is activated (V_{PVDD} too low) during a soft shut down phase, the UVLO protection takes over and immediately shuts down the output transistor. The activation of the UVLO protection also resets the desaturation fault, and the device can be turned on again as soon as the UVLO fault disappears.

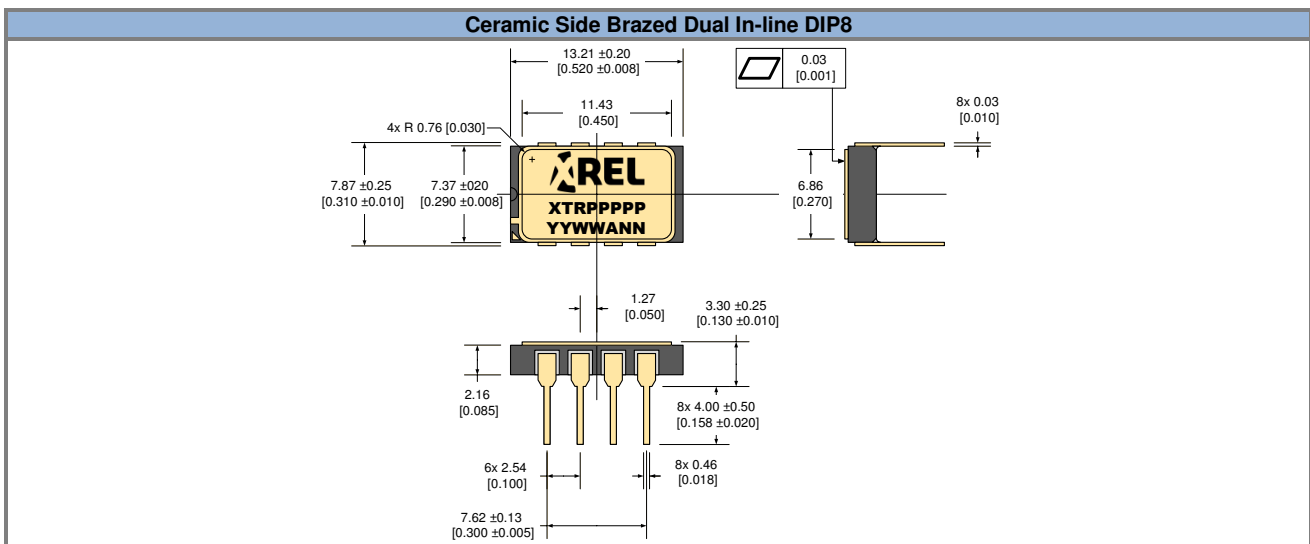
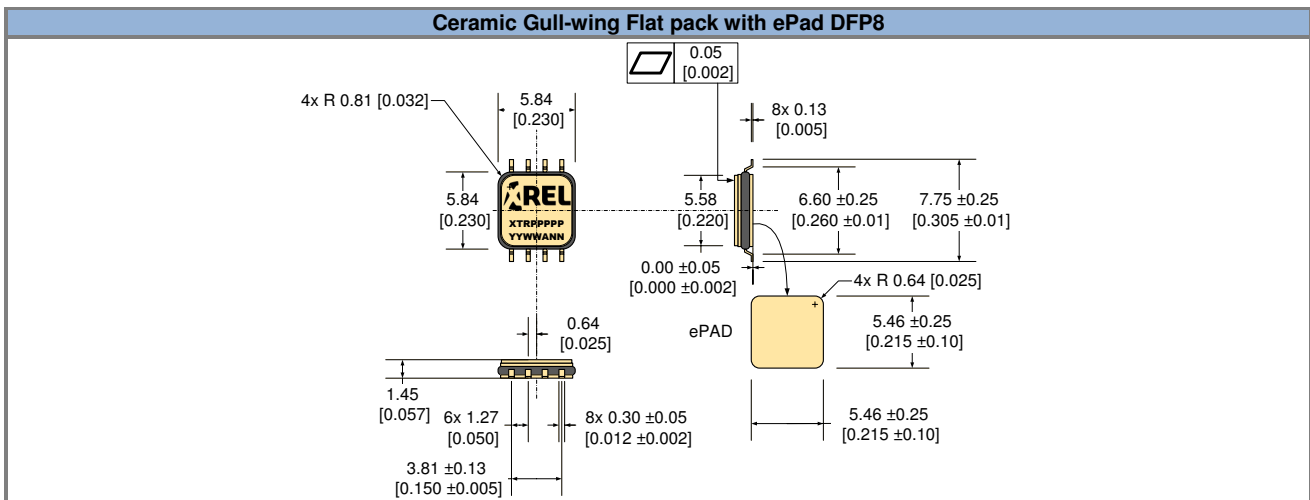


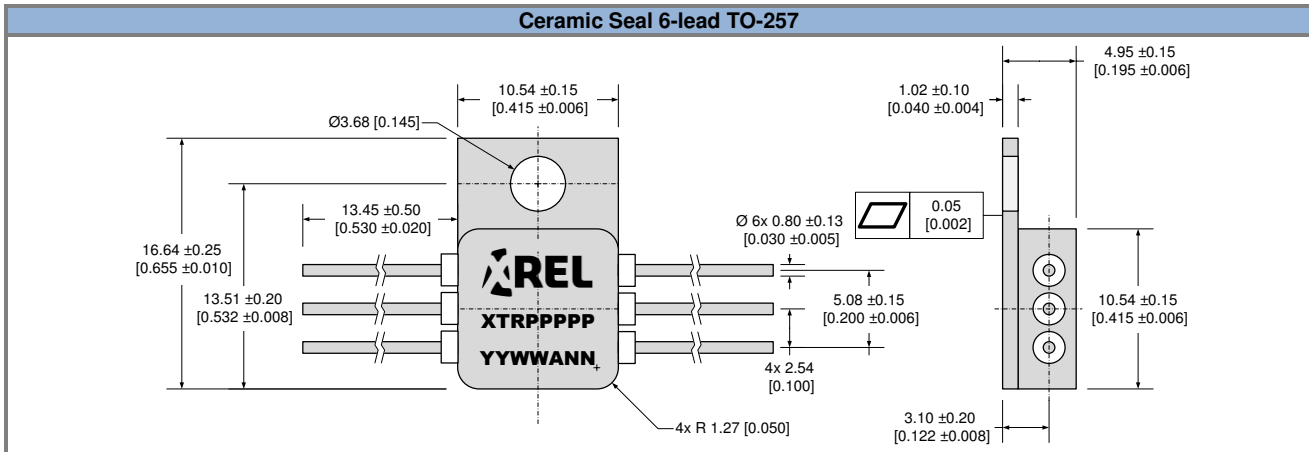
Robustness against over voltages

Though it is highly recommended to comply with the DC voltage limits of the part, in switching applications it is usually difficult to guarantee that aggressive spikes cannot occur in some cases due to fast dV/dt and di/dt. For these reasons, the XTR20410 products have been implemented in such a way that spikes of several volts over the recommended DC limits will not damage the device. For safe long term reliability, these spikes should however be reduced by correct PCB layout, ground planes and clean decoupling.

PACKAGE OUTLINES

Dimensions shown in mm [inches]. Tolerances ± 0.13 mm [± 0.005 in] unless otherwise stated.





| Part Marking Convention | |
|--|--|
| Part Reference: XTRPPPPP | |
| XTR | X-REL Semiconductor, high-temperature, high-reliability product (XTRM Series). |
| PPPPP | Part number (0-9, A-Z). |
| Unique Lot Assembly Code: YYWWANN | |
| YY | Two last digits of assembly year (e.g. 11 = 2011). |
| WW | Assembly week (01 to 52). |
| A | Assembly location code. |
| NN | Assembly lot code (01 to 99). |

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