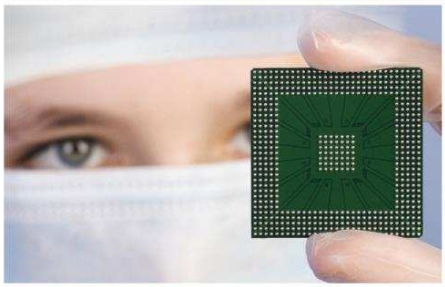
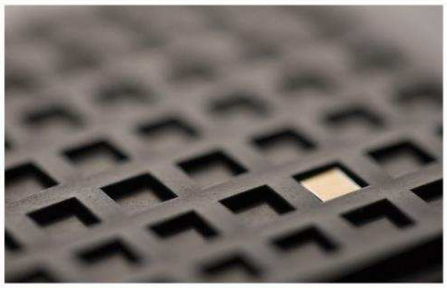
E16G301 EPIPHANY™ 16-CORE MICROPROCESSOR Datasheet



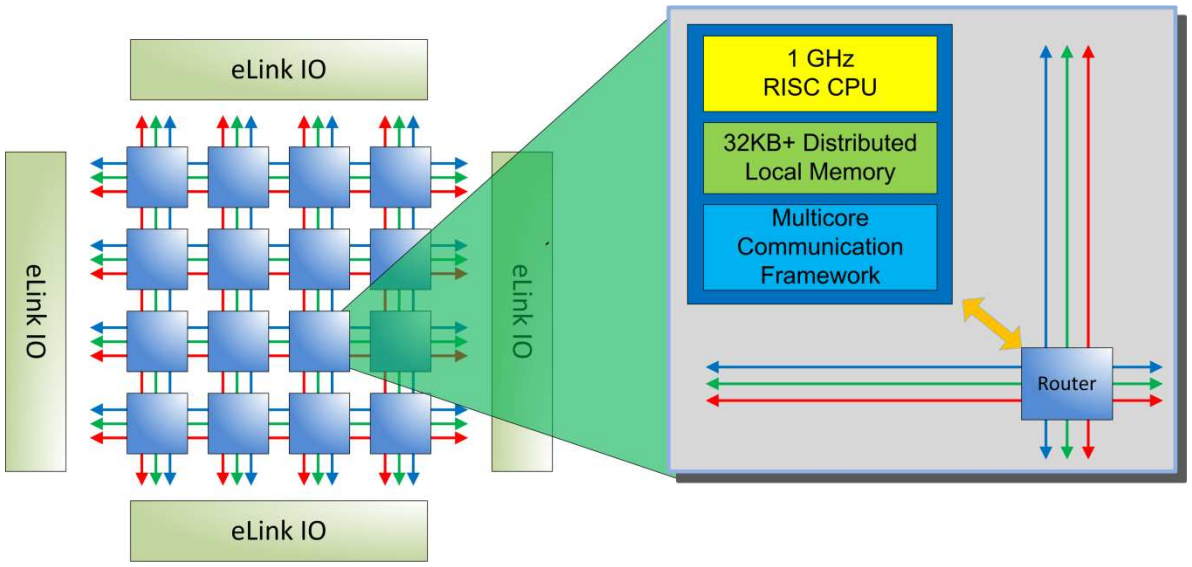


Epiphany - The world leader in microprocessor energy efficiency

The Epiphany is a scalable multicore architecture with up to 4,095 processors sharing a common 32 bit memory space. The Epiphany combines fully-featured floating point C/C++ programmable RISC processors, a high bandwidth distributed memory system, a low latency Network-On-Chip, and low overhead off-chip IO to bring an unprecedented level of processing to power constrained systems.

E16G301 Feature Summary

- 16 high performance RISC CPU cores
- C/C++ and OpenCL programmable
- 32-bit IEEE floating point support
- 512KB on-chip distributed shared memory
- 32 independent DMA channels
- Up to 1GHz operating frequency
- 32 GFLOPS peak performance
- 512 GB/s local memory bandwidth
- 64 GB/s Network-On-Chip bisection bandwidth
- 8 GB/s off-chip bandwidth
- 1.5ns network per-hop latency
- <2 Watt maximum chip power consumption
- 324-ball 15×15mm 0.8mm pitch BGA with built in heat sink



Revision	Changes
3.13.2.13	Initial Revision
3.13.6.14	General: Added electrical specs disclaimer notes Section 3.5: Added section on unused pins Section 6.3: Added new mechanical drawing (RevB) Section 6.4: Removed unused signals in pin mapping Section 6.4:Corrected incorrect pin map table Errata: Added Errata Section Ordering: Added part number methodology and ordering information Electrical: Changed minimum DVDD voltage to 1.8V
3.13.12.17	Section 2.2: Added Link Debug, Chip Start, and Chip Halt register. Section 2.2: Fixed the link register offsets.
14.2.21	Section 2: Added official register names to be used by SDK Added IO register access explanation Section3: Added eLink details Section 5: Added AC/DC timing specifications Added power consumption measurements Section 6: Added thermal data
14.03.11	Added missing 'NOT' in reset disclaimer

Table of Contents

Preface

This document describes the *E16G301* chip product. The document is written for system designers with a fundamental understanding of processor architectures and chip specifications.

Related Documents

- *Epiphany Architecture Reference*: The complete reference for the Epiphany multi-core computer architecture.
- *Epiphany SDK Reference*: The development tools and run-time library for the Epiphany architecture

1 Introduction

1.1 Overview

The E16G301 is a 16-core System-On-Chip implemented in a 65nm based on the 3rd generation of the Epiphany multicore IP. The Epiphany™ architecture is a scalable, distributed-shared-memory computing fabric comprised of a 2D array of processor nodes connected by a low-latency mesh network-on-chip. Here is a brief summary of the key components of the E16G301:

Processor:

The E16G301 includes 16 superscalar floating point RISC CPUs (eCore), each one capable of two floating point operations per clock cycle and one integer calculation per clock cycle. The CPU has an efficient general-purpose instruction set that excels at compute intensive applications while being efficiently programmable in C/C++.

Memory System:

The Epiphany memory architecture is based on a flat shared memory map in which each compute node has up to 1MB of local memory as a unique addressable slice of the total 32-bit address space. A processor can access its own local memory and other processors' memory through regular load/store instructions. The local memory system is comprised of 4 separate sub-banks, allowing for simultaneous memory accesses by the instruction fetch engine, local load-store instructions, and by memory transactions initiated by the DMA engine other processors within system.

Network-On-Chip:

The Epiphany Network-on-Chip (eMesh) is a 2D mesh network that handles all on-chip and off-chip communication. The eMesh network uses atomic 32-bit memory transactions and operates without the need for any special programming. The network consists of three separate and orthogonal mesh structures, each serving different types of transaction traffic: one network for on-chip write traffic, one network for off chip write traffic, and one network for all read traffic.

Off-Chip IO:

The eMesh network and memory architecture extends off-chip using source synchronous dual data rate LVDS links ("elinks"). Each E16G301 has 4 independent off-chip elinks, one in each physical

direction (north, east, west and south). The off chip links allows for glueless connection of multiple E16G301chips on a board and for interfacing to an FPGA.

For more detailed information about the Epiphany architecture, please refer to the *Epiphany Architecture Reference Manual.*

1.2 System Examples

The E16G301 product can be used in a number of different system configurations, some of which are shown in this section.

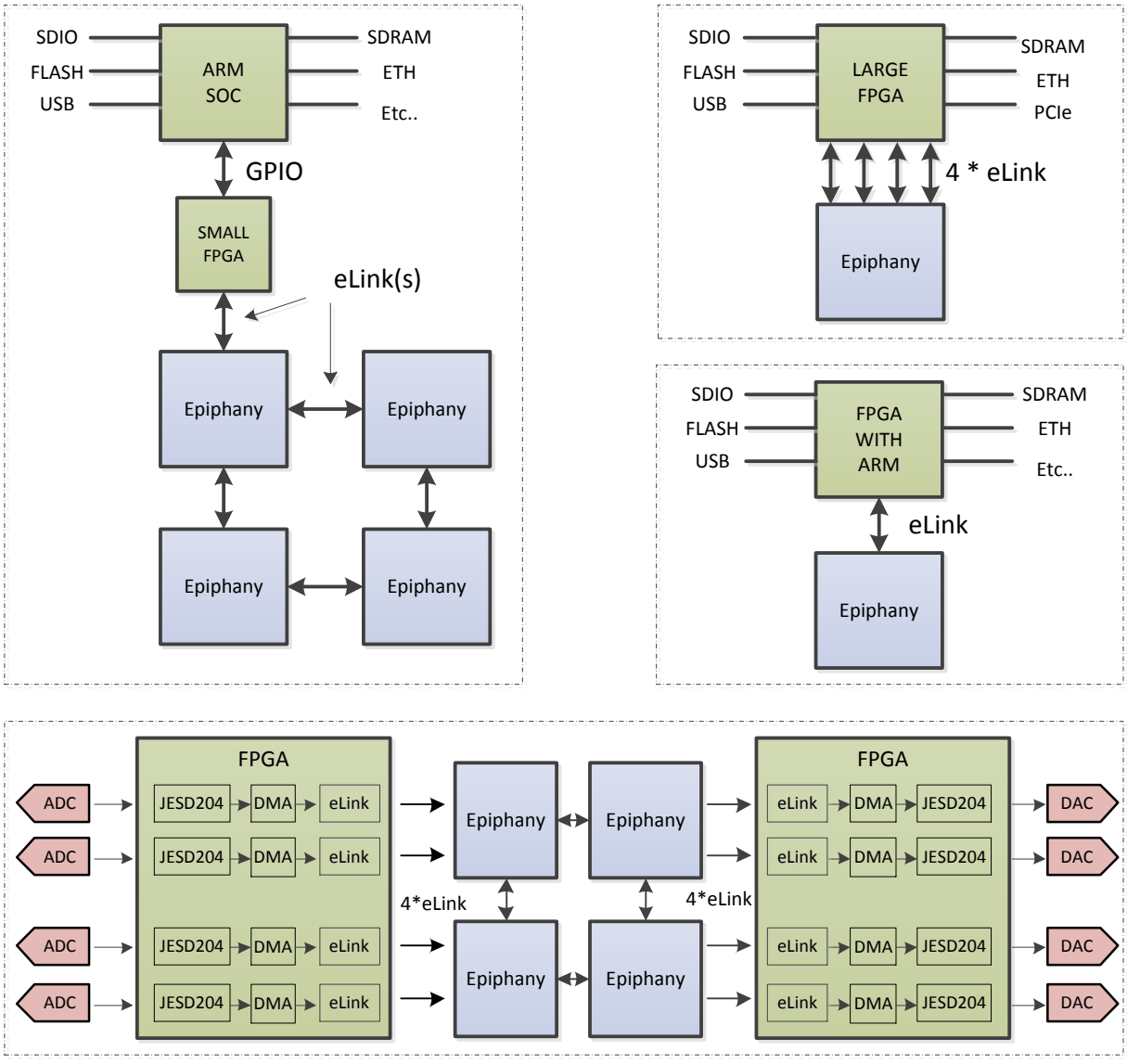


Figure 1: Epiphany System Architecture

1.3 Applications

The following list shows some applications for which the E16G301 is particularly well suited:

Consumer:

- Smart-phones and tablet application acceleration
- High end audio
- Computational photography
- Speech Recognition
- Face detection/recognition

Computing Infrastructure:

- Super Computers
- Big Data Analytics
- Software Defined Networking

Mil/Aero:

- Radar/Sonar
- Extremely Large Sensor Imaging
- Hyperspectral Imaging
- Military Radios

Medical:

- Ultrasound
- CT

Communication:

- Communication test-bed
- Software defined radio
- Adaptive Pre-distortion

Embedded Vision

- Machine Vision
- Autonomous Robots/Navigation
- Automotive Safety

Other:

- Compression
- Security Cameras
- Video Transcoding

2 Memory Architecture

2.1 Global Memory Map

The memory map configuration of the E16G301 within the 32 bit memory map is controlled with the ROWID[3:0] and COLID[3:0] chip input pins. The ROWID and COLID chip pins are sampled on the rising edge of RESET_N and are used to set the offset of the core's memory map. Figure 2 shows the distributed memory scheme of the Epiphany architecture. Table 1 shows the distribution of the SRAM within a specific E16G301 chip without the specific chip-ID offset. The complete core memory map of the local cores can be found in the Epiphany Architecture Reference Manual.

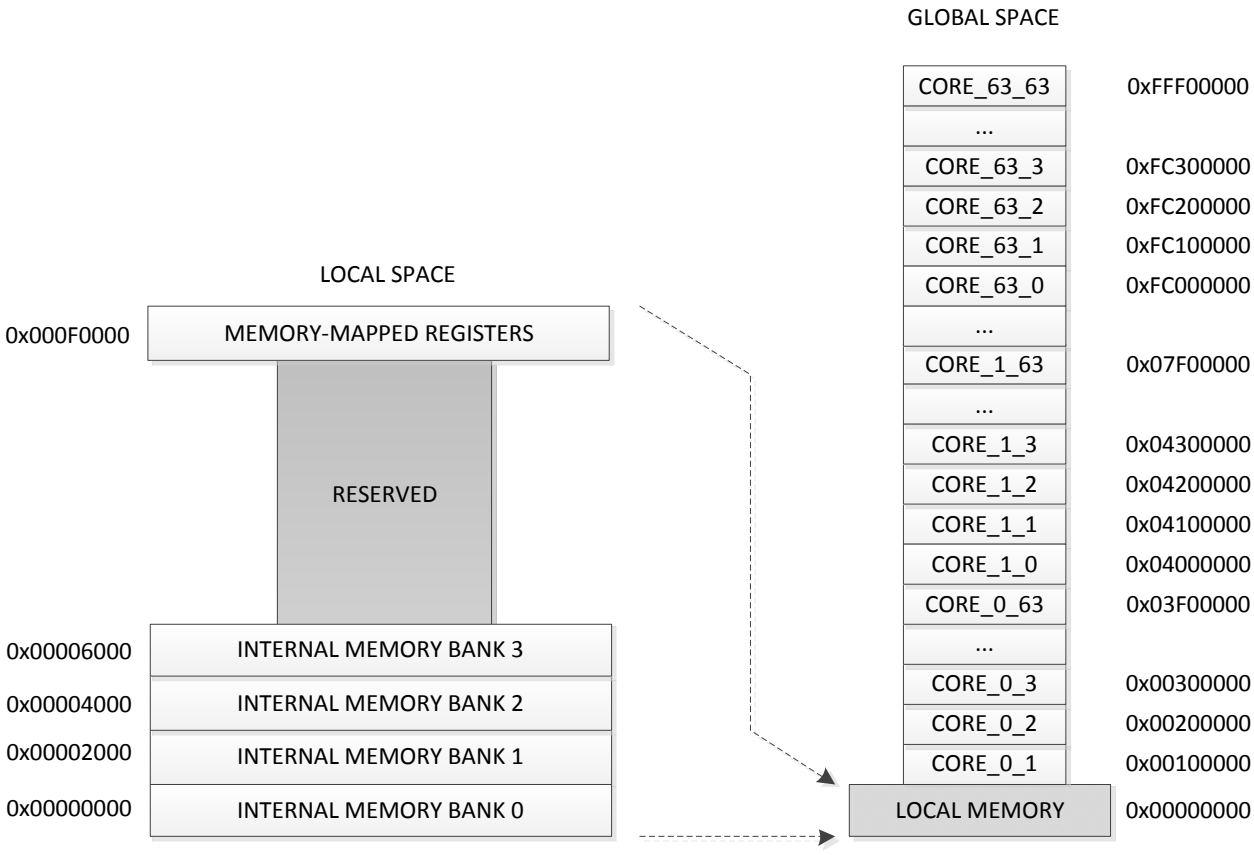


Figure 2: Epiphany Memory Architecture

Chip Core Number	Start Address	End Address	Size
(0,0)	00000000	00007FFF	32KB
(0,1)	00100000	00107FFF	32KB
(0,2)	00200000	00207FFF	32KB
(0,3)	00300000	00307FFF	32KB
(1,0)	04000000	04007FFF	32KB
(1,1)	04100000	04107FFF	32KB
(1,2)	04200000	04207FFF	32KB
(1,3)	04300000	04307FFF	32KB
(2,0)	08000000	08007FFF	32KB
(2,1)	08100000	08107FFF	32KB
(2,2)	08200000	08207FFF	32KB
(2,3)	08300000	08307FFF	32KB
(3,0)	0C000000	0C007FFF	32KB
(3,1)	0C100000	0C107FFF	32KB
(3,2)	0C200000	0C207FFF	32KB
(3,3)	0C300000	0C307FFF	32KB

Table 1: Relative Chip Memory Map

2.2 Memory Mapped Registers

The E16G301 has a set of chip IO registers used to configure the operating mode of the product. The memory locations of these configuration registers and their respective functions are shown in Table 2. These registers are cleared by asserting the chip RESET_N pin. The address entries below are relative to the ROWID and COLID chip address settings. In the table, the link registers additionally have an offset that is dependent on the link in question as follows:

- North link offset: **0x00200000**
- East link offset: **0x08300000**
- South link offset: **0x0c200000**
- West link offset: **0x08000000**

Register Name	Register Address	Bits	Description
ELINKCLKSO **ELINKCLKNO** **ELINKCLKEA** **ELINKCLKWE**	0xF0300 + link offset	[3:0]	LCLK Transmit Frequency control 0=Divide cclk by 2 1=Divide cclk by 4 2=Divide cclk by 8
ELINKTXSO **ELINKTXNO** **ELINKTXEA** **ELINKTXWE**	0xF0304 + link offset	[11:0]	Transmitter low power mode 0xFFF=turned off 0x000=turned on
ELINKRXSO **ELINKRXNO** **ELINKRXEA** **ELINKRXWE**	0xF0308 + link offset	[11:0]	Receiver lo power mode 0xFFF=turned off 0x000=turned on
ELINKDEBUGSO **ELINKDEBUGNO** **ELINKDEBUGEA** **ELINKDEBUGWE**	0xF0328 + link offset	[0] [1] [13:2] [14]	Set constant on link TX Loopback RX to TX Constant to drive on TX Force a chip transaction match on RX transactions
IOFLAG	0x006F0318	[5:0]	0=Sets MONITOR pin to 0 1=Sets MONITOR pin to 1
CHIPRESET	0x083F0324		Writing to register creates a three clock cycle long pulse that resets the rest of the chip.
CHIPSYNC	0x083F031C		Writing to register creates a chip wide “SYNC” interrupt
CHIPHALT	0x083F0320		Writing to register puts all cores in the HALT debug state.

Table 2: Memory Mapped Registers

In order to write to these memory mapped registers, the store transaction must be configured with a special control mode that allows the transaction to bypass the regular eMesh routing protocol.. The special routing mode is controlled through bits [15:12] of the CONFIG register of the core initiating the write transaction to the IO registers and should be set according to Table 3.

Register Name	CONFIG[15:12]
NORTH ELINK REGISTERS	0001
EAST ELINK REGISTERS	0101
SOUTH ELINK REGISTERS	1000
WEST ELINK REGISTERS	1101
IOFLAG, CHIPRESET, CHIPSYNC, CHIPHALT	1101

Table 3: CONFIG Register Routing Mode Selection

The CONFIG[15:12] register bits of a processor node are added to each outgoing on-chip write transactions as a CTRLMODE tag, overriding the default address matching algorithm of the cMesh. By default, when a write transaction arrives at a processor node, the write transaction is accepted into the node if the ROWID and COLID of the write transaction matches the node's coordinates exactly. By specifying a different matching direction in CONFIG[15:12], a matching write transaction can be directed to the south, north, east, or west instead of into the processor. To return the routing behavior to normal mode, CONFIG[15:12] should be reset to 0000. The safe method of writing to chip level IO register should use the following tightly coupled write sequence:

1. Set the CONFIG[15:12] appropriately according to Table 3 using a MOVTS instruction.
2. Write to the chip level register address as specified in Table 2
3. Reset CONFIG[15:12] to 0000 using a MOVTS instruction.

3 I/O Interfaces

3.1 Overview

The E16G301 includes the following basic signal groups:

- 1 core supply (VDD)
- 1 IO supply (DVDD)
- 1 differential input clock signal
- 1 single ended reset signal
- 8 single ended configuration strap pins
- 24 differential pairs for each one of the four different links (east/west/north/south)

NOTE: Chip input pins do NOT have on-chip pull-down resistors. To avoid erratic behavior, the input clock, reset and all eLink frame signals should not be left floating.

3.2 Supplies

The chip needs two separate and independent supplies for proper operation.

Signal Name	Signal Description	Direction	Signaling Type
DVDD	IO Supply	Input	Supply
VDD	Core Supply	Input	Supply
VSS	Common Ground	Input	Supply

Table 4: Chip Supplies

3.3 Reset and Clock

The E16G301 does not have an on-chip PLL and instead receives a high speed LVDS clock directly from a differential LVDS input signal.

Signal Name	Signal Description	Direction	Signaling Type
RESET_N	Active Low Reset	Input	LVCMOS
RXI_WE_CCLK_{P,N}	Chip Clock Input	Input	LVDS

Table 5: Chip Clock and Rest

NOTE: For correct reset sequencing, the RXI_WE_CCLK_{P/N} signal should be toggling during the rising edge of RESET_N.

3.4 Monitor Signals

The flag pin is a general purpose output pin that can be connected to an LED or routed to an FPGA or controller to be used as an interrupt or indicator. The pin is controlled by writing a 1 or 0 to the "Monitor Register" as described in Chapter 2.2.

Signal Name	Signal Description	Direction	Signaling Type
FLAG	Monitor Signal	Output	LVCMOS
MVDD	On-chip core voltage sensing pin	Output	Analog
MVSS	On-chip ground voltage sensing pin	Output	Analog

Table 6: Monitor Signals

3.5 Unused Input Signals

The following signal pairs should have the P/N pair pulled to a safe constant differential value. (i.e. if the _N signal is pulled low then the _P signal should be pulled high).

Signal Name	Signal Description	Direction	Signaling Type
RXI_EA_CCLK_{P,N}	Unimplemented signal	Input	LVDS
RXI_SO_CCLK_{P,N}	Unimplemented signal	Input	LVDS
RXI_NO_CCLK_{P,N}	Unimplemented signal	Input	LVDS

Table 7: Unused Signals

3.6 Chip Coordinate Signals

There are eight coordinate signals that are sampled at the rising edge of RESET_N to set the coordinate ID of the E16G301. The COLID[2:0] and ROWID[2:0] set bits [31:28] and [25:22] respectively of the chip's address map. The bits are needed to differentiate between chips in systems containing multiple E16G301 chips. Figure 3 shows an example system with four E16G401 chips with different COLID and ROWID input pin values.

Signal Name	Signal Description	Direction	Signaling Type
COLID[0]	Bit[28] of chip address map	Input	LVCMOS
COLID[1]	Bit[29] of chip address map	Input	LVCMOS
COLID[2]	Bit[30] of chip address map	Input	LVCMOS
COLID[3]	Bit[31] of chip address map	Input	LVCMOS
ROWID[0]	Bit[22] of chip address map	Input	LVCMOS
ROWID[1]	Bit[23] of chip address map	Input	LVCMOS
ROWID[2]	Bit[24] of chip address map	Input	LVCMOS
ROWID[3]	Bit[25] of chip address map	Input	LVCMOS

Table 8: Chip Coordinate Settings

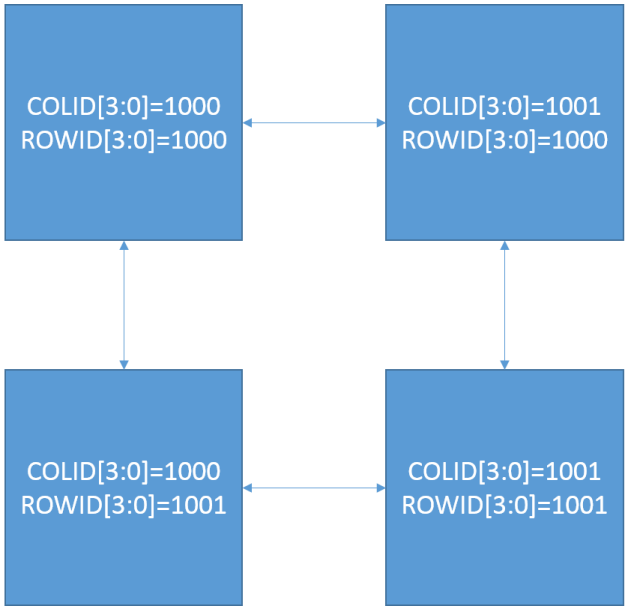


Figure 3: Chip coordinate configuration example

3.7 Chip-To-Chip Link Interface

The E16G301 has four identical source-synchronous bidirectional off chip LVDS links (eLink) that can be used to connect the E16G301 to other E16G301 chips, FPGAs, and/or ASICs. Interfacing the E16G301 with an FPGA should be done by instantiating the eLink HDL open source HDL code provided by Adapteva. The eLink enables glue-less chip to chip connections as illustrated in Figure 4.

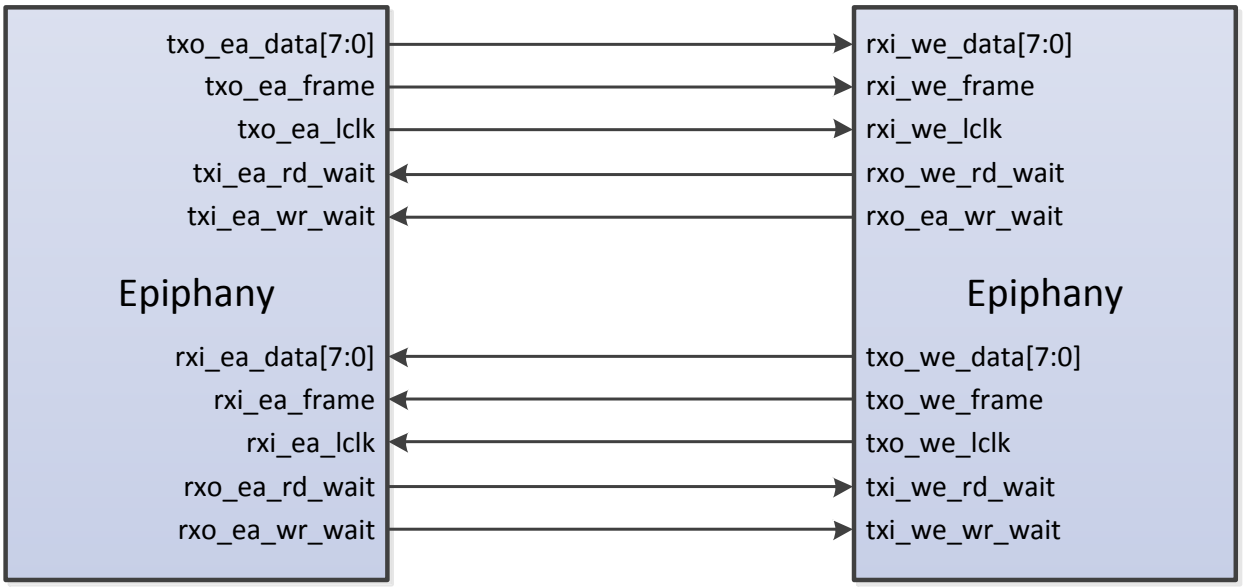


Figure 4: eLink Chip Interface

The eLink aggregates all read and write transactions from the eMesh Network-On Chip inside the E16G301 and sends them out as 104 bit memory mapped atomic transactions with the following sub-fields:

- Read indicator
- Write indicator
- Data size (2 bits)
- Control mode (4 bits)
- Destination address (32 bits)
- Lower data field (32 bits)
- Upper data field/source address (32 bits)

NOTE: The following eLink description is included to provide clarity. For a complete description, please refer to the open source eLink implementation at: http://github.com/parallella/parallella-hw

The eLink interface protocol is illustrated in Figure 5. The eLink data interface is 8 bits wide with a protocol specified in Table 9. The number of bytes to be received is determined by the data of the first "valid" byte (byte0) and the level of the FRAME signal. The data captured on the rising edge of the LCLK is considered to be byte0 if the FRAME control captured at the same cycle (rising edge) is high but was low at the rising edge of the previous LCLK cycle.

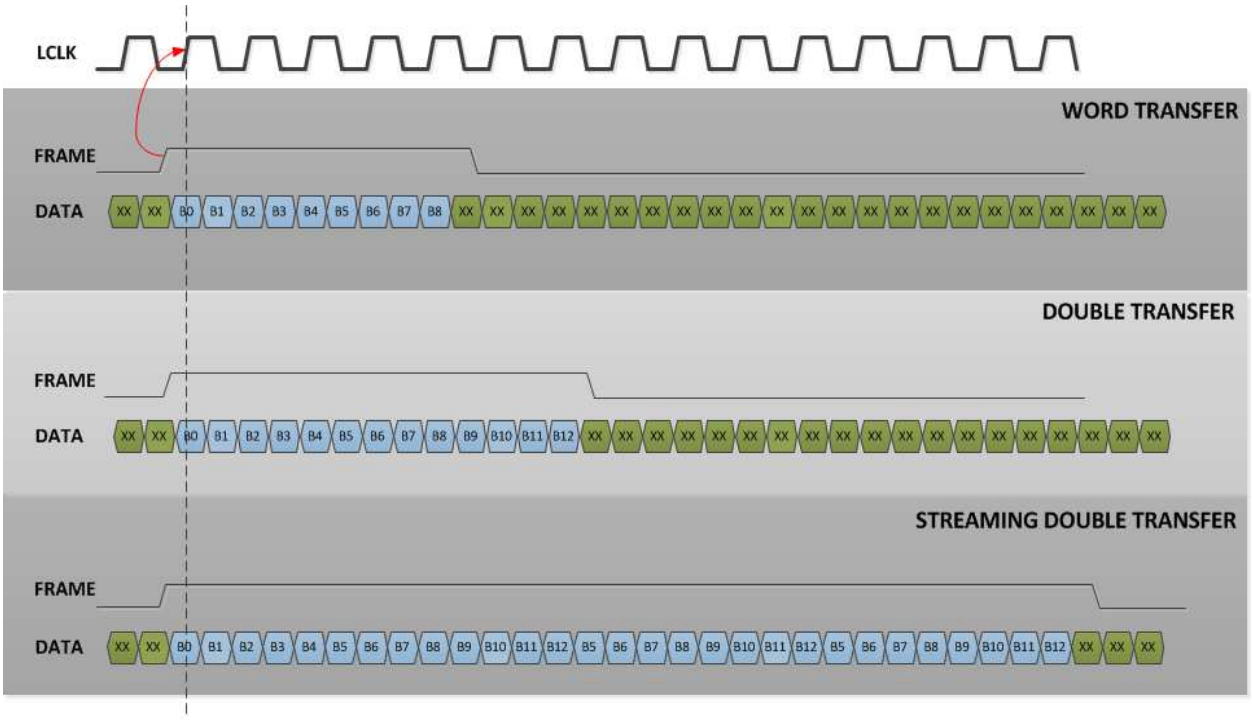


Figure 5: eLink Interface Illustration

The cycle after the last byte of the transaction (byte8 or byte12) will determine if the receiver should go into data streaming mode based on the level of the FRAME control signal. If the FRAME signal is low, the transaction is complete. If the FRAME control signal stays high, the eLink goes into "streaming mode", meaning that the last byte of the previous transaction (byte8 or byte12) will be followed by byte5 of the new transaction.

Byte	Content				
Byte0	{control mode[3:0], datamode[1:0], write, read}				
Byte1	dstaddr[7:0]				
Byte 2	dstaddr[15:8]				
Byte 3	dstadr[23:16]				
Byte 4	dstaddr[31:24]				
{datamode[1:0], read, write}	0X01	1001	1101	XX10	XX11
Byte 5	data[7:0]	data[7:0]	data[7:0]	srcaddr[7:0]	data[7:0]
Byte6	data[15:8]	data[15:8]	data[15:8]	srcaddr[15:8]	data[15:8]
Byte7	data[23:16]	data[23:16]	data[23:16]	srcaddr[23:16]	data[23:16]
Byte8	data[31:24]	data[31:24]	data[31:24]	srcaddr[31:24]	data[31:24]
Byte9	N/A	N/A	data[32:39]	N/A	srcaddr[7:0]
Byte10	N/A	N/A	data[47:40]	N/A	srcaddr[15:8]
Byte11	N/A	N/A	data[56:48]	N/A	srcaddr[23:16]
Byte12	N/A	N/A	data[63:57]	N/A	srcaddr[31:24]

Table 9: eLink Data Format

NOTE: Optimal eLink bandwidth utilization is achieved by transmitting a sequence of 64-bit write transactions with increasing address order (e.g 0x80800000, 0x80800008, 0x80800010, ..). Read transactions, non 64-bit transactions, and non-sequential 64-bit write transactions will result in a max bandwidth of 1/4th of peak.

The WAIT_RD and WAIT_WR signals are used to stall transmission when a receiver is unable to accept more transactions. This mechanism is shown in Figure 6. The receiver will raise its WAIT output signal on the second rising edge of LCLK input following the capturing rising edge of the last transaction byte (byte8 or byte12) but will be ready to accept one more full transaction (byte0 through byte8/byte12). The WAIT signal seen by the transmitter is assumed to be of the "unspecified" phase delay (while still of the LCLK clock period) and therefore has to be sampled with the two-cycle synchronizer. Once synchronized to the transmitter's LCLK clock domain, the WAIT control signals will prevent new transaction from being transmitted. If the transaction is in the middle of the transmission when the synchronized WAIT control goes high, the transmission process is to be completed without interruption.

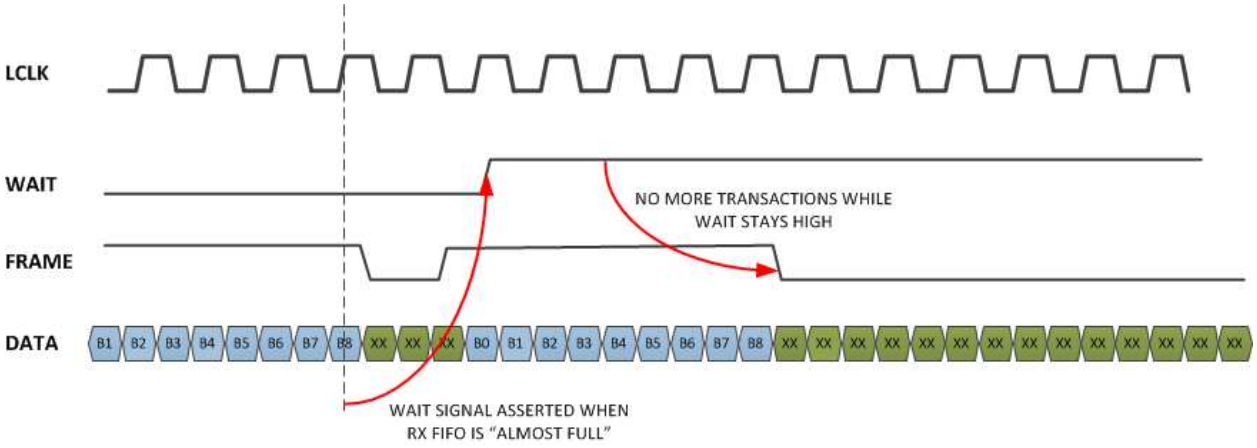


Figure 6: Transmitter Pushback Mechanism

The txo_* interface driven out from the E16G301 uses a divided version of the core cock frequency (RXI_WE_CCLK_{P,N}). The transmit clock is automatically aligned in the middle of the data eye by the eLink on chip transmit logic. The receiver logic assumes the clock is aligned at the center of the receiver data eye. The "wait" signals are used to indicate to the transmit logic that no more transactions can be received because the receiver buffer full.

For the sake of brevity the signal descriptions of the four links are merged in a single table below with each link having a unique modifier depending on the direction of the link. The modifier is: NO for north, SO for south, EA for east, and WE for west. The suffix P/N indicates positive or negative leg of the differential pair.

Signal Name	Direction	Signal Description
RXI_{NO,SO,EA,WE}_DATA_{P,N}[7:0]	Input	Receiver data
RXI_{NO,SO,EA,WE}_FRAME_{P,N}	Input	Receiver packet framing signal
RXI_{NO,SO,EA,WE}_LCLK_{P,N}	Input	Receiver clock
RXO_{NO,SO,EA,WE}_WR_WAIT_{P,N}	Output	Asynchronous push-back for transmitter indicating that device must hold off on sending another write packet.
RXO_{NO,SO,EA,WE}_RD_WAIT_{P,N}	Output	Asynchronous push-back for transmitter indicating that device must hold off on sending another read packet.
TXO_{NO,SO,EA,WE}_DATA_{P,N}[7:0]	Output	Transmitter data
TXO_{NO,SO,EA,WE}_FRAME_{P,N}	Output	Transmitter packet framing signal
TXO_{NO,SO,EA,WE}_LCLK_{P,N}	Output	Transmitter clock
TXI_{NO,SO,EA,WE}_WR_WAIT_{P,N}	Input	Asynchronous push-back from receiver indicating that transmitter must hold off on sending another write packet.
TXI_{NO,SO,EA,WE}_RD_WAIT_{P,N}	Input	Asynchronous push-back from transmitter indicating that transmitter must hold off on sending another read packet.

Table 10: eLink Signals

4 Electrical Specifications

NOTE: Absolute ratings are based on simulation results, process information, and initial testing. Final product qualification data not yet available, information provided without warranty.

4.1 Maximum Absolute Ratings

Parameter	Description	Value	Units
V_{DVDD}	IO Supply Voltage range	-0.5 to 2.75	V
V_{VDD}	Core supply voltage range	-0.3 to 1.3	V
V_{PAD}	Voltage range	-0.5 to (VDD+0.5)	V
T_{MAX}	Storage temperature	-65°C to 150	°C
T_J	Junction operating temperature	-40 to 125	°C

Table 11: Maximum Absolute Ratings

Charged devices and circuit boards can discharge without detection. Although this product features robust ESD protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

4.2 Recommended Operating Conditions

Parameter	Description	Min	Typical	Max	Unit
V_{DVDD}	IO Supply Voltage Range	1.8	2.5	2.75	V
V_{VDD}	Core Supply Voltage Range	0.90	1.0	1.2	V
V_{PAD}	Voltage at IO	-0.3		V_{DVDD} + 0.3	V
V_{IH}	High-level input voltage at IO	0.7 * V_{DVDD}		V_{DVDD} + 0.3	V
V_{IL}	Low-level input voltage at IO	V_{DVSS} - 0.3		V_{DVDD} + 0.3	V
T_J	Junction Temp	-40	25	125	°C
I_{VDD}	Core supply current at 800MHz		800		mA
I_{VDVDD}	IO supply current		320		mA

Table 12: Recommended Operating Conditions

4.3 Control Signal AC/DC Characteristics

The FLAG, ROWID, COLDID, and RESET_N pins use full swing LVCMOS signaling with AC/DC specifications given in the following table.

Parameter	Description	Min	Typical	Max	Unit
t_{rise}	Transmitter rise time (20pF load)	0.94	1.43	2.31	nS
t_{fall}	Transmitter fall time (20pF load)	0.96	1.39	2.19	nS
I_{OH}	Output drive current	16.4	24.5	35.7	mA
I_{OL}	Output drive current	16.9	27.0	39.1	mA
I_{SCH}	Output high short circuit	--	--	70	mA
I_{SCL}	Output low short circuit	--	--	72	mA
I_{L}	Input leakage	--	--	1	uA

Table 13: LVCMOS AC/DC Characteristics

4.4 eLink AC/DC Specifications

The E16G301 eLinks conform to the LVDS standard (IEEE Std 1596.3-1996, Low Voltage Differential Signaling). The driver design has all the necessary components for transmission of LVDS data and a temperature stable internal reference for setting of the LVDS signaling voltage and common mode level. The LVDS receiver does not comply with the hysteresis requirements of the TIA and IEEE standards for LVDS differential signaling at the specified rates.

Parameter	Description	Min	Typical	Max	Unit
V_{INPUT}	Common Mode Input Voltage	0	1.2	V_{DVDD} - 0.1	V
V_{IDT}	Input differential threshold	75			mV
V_{ID}	Input differential voltage	100		V_{DVDD}	mV
$V_{IA,IB}$	Input voltage	0	1.2	V_{DVDD}	V
$I_{IA,IA}$	Input leakage current			5	uA
$v_{psupply}$	Power supply sensitivity		0.15	0.3	ps/mV
t_{jps}	Total receiver pk-pk jitter		100	250	ps
t_{rise}	Output differential rise time	150		300	ps
t_{fall}	Output differential fall time	150		300	ps
v_{OH}	Output voltage high		1365	1485	mV
v_{OL}	Output voltage low	960	1035		mV
v_{OD}	Differential output voltage	250	325	410	mV
v_{OS}	Output offset voltage	1170	1200	1230	mV
$I_{SA,SB}$	Output short circuit current	-40	10	40	mA

Table 14: LVDS Electrical Specifications

4.5 Power Consumption

The following table shows the VDD power consumption of the E16G301 as a function of frequency and voltage with all 16 cores executing a heavy duty workload. The measurements were taken at room temperature without a heat sink and with 0 m/s airflow. The maximum operating frequency at each voltage level is specified next to the data point in the figure

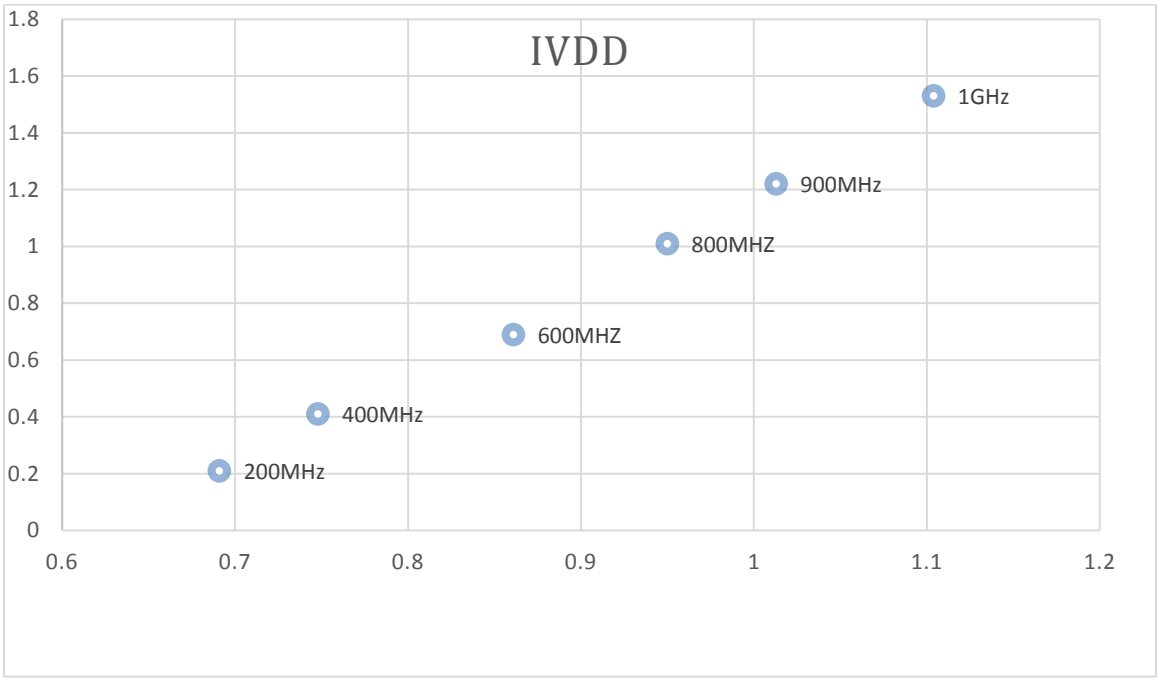


Figure 7: Power Consumption

5 Timing Specifications

5.1 Reset Sequence

The CCLK_N/CCLK_P should toggle at least 10 times while RESET_N is held low and should be held constant during the rising edge of RESET_N.

5.2 eLINK Timing

The following table gives recommended eLink timing constraints for E16G301 system integration.

Parameter	Value
Maximum skew between all rxi_* signals on one link	250ps
Maximum skew between all txo_* signals on one link	250ps
Maximum skew between nets of a p/n pair signal	50ps
Receiver clock min setup to data edge	250ps
Receiver clock min hold from data edge	250ps
Minimum receiver LCLK period	2ns

Table 15: eLink Timing Constraints

6 Device Package

6.1 Overview

The E16G301 uses a 324 ball 0.8 mm pitch wire-bond BGA package that measures 15×15mm.

6.2 Graphical Pin Mapping

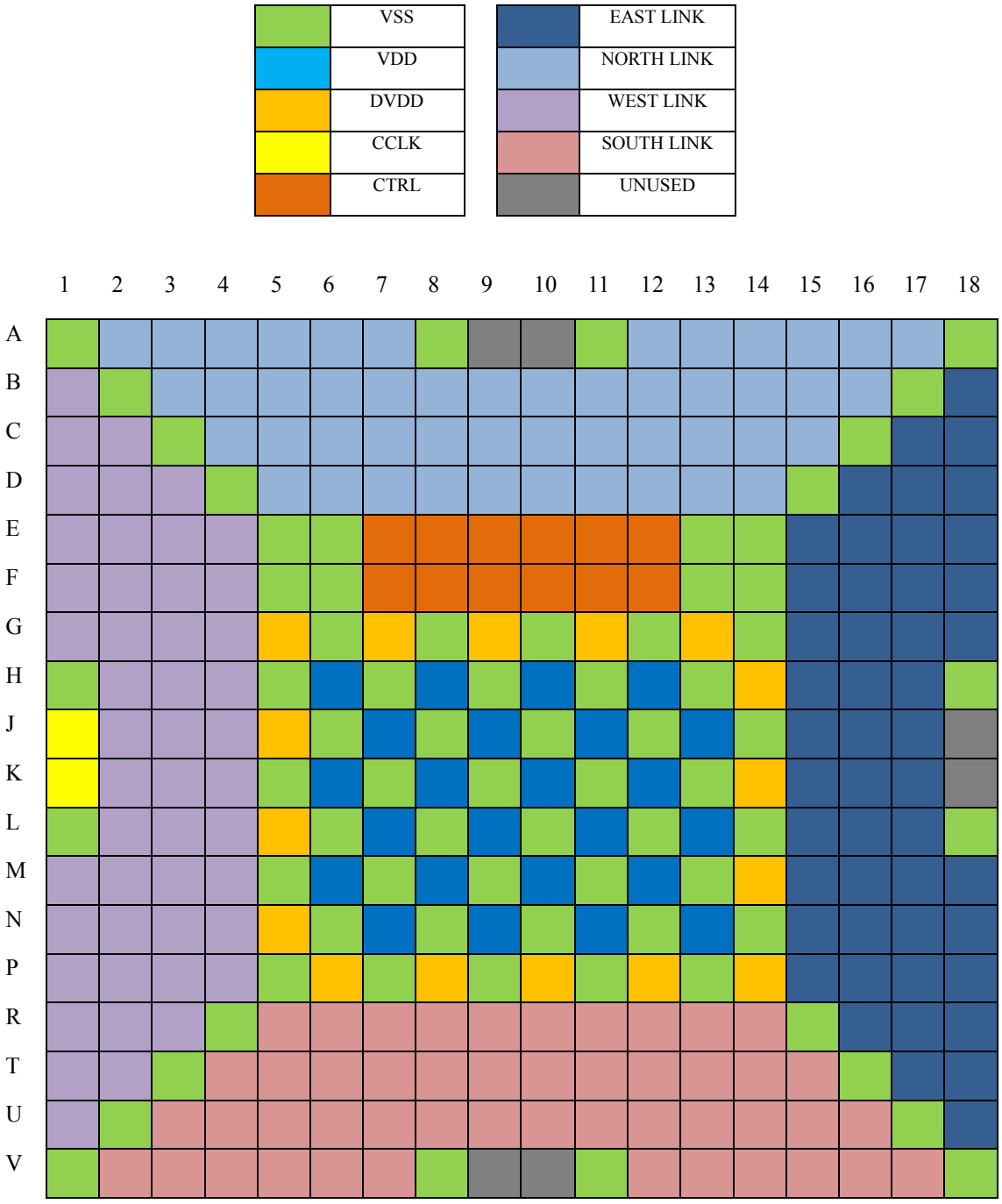
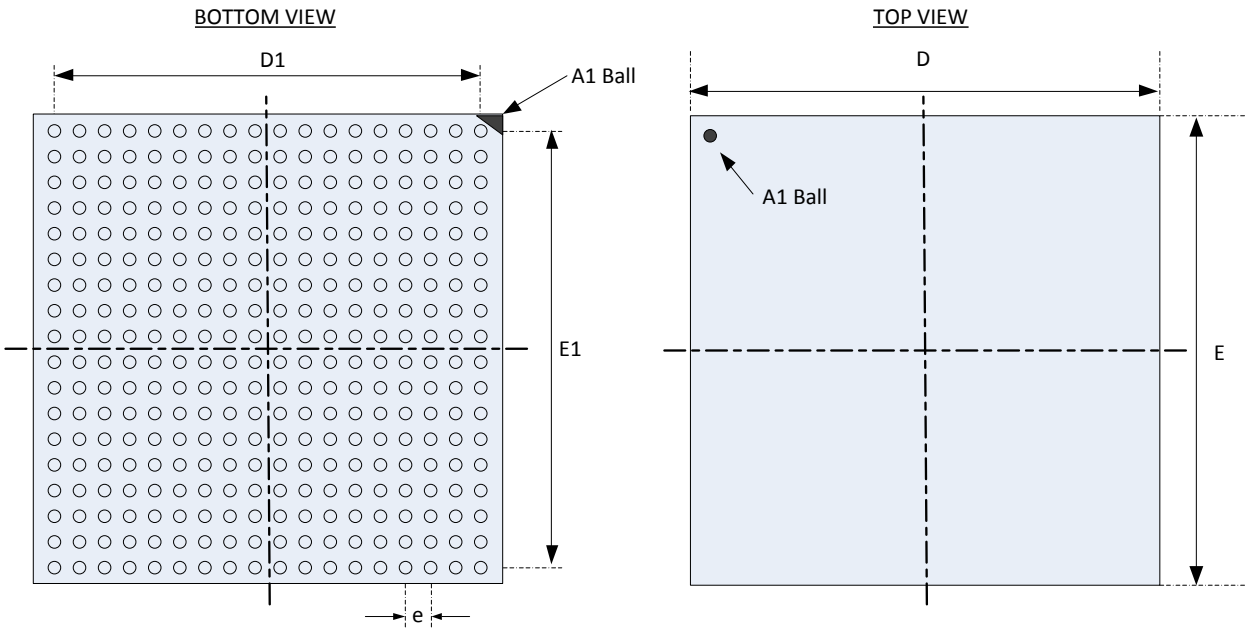


Figure 8: Pin Mapping Diagram

6.3 Mechanical Drawing



NOTES:
1. All dimensions and tolerances conform to ASME Y14.5M-1994
2. Symbol "M" is the pin matrix size
3. There shall be a minimum clearance of 0.25mm between edge of solder ball and body edge
4. Conforms to JEDEC MO-275-KKAB-1

	SYMBOL	MIN (mm)	NOM (mm)	MAX (mm)
Total Thickness	A	~	~	1.50
Standoff	A1	0.25	~	0.40
Substrate Height	A2	~	0.26	~
Mold+Heatslug	A3	~	0.8	~
Body Size	D/E		15.00	
Ball Array Size	D1/E1		13.60	
Ball Pitch	e		0.80	
Ball Size	b	0.40	0.45	0.50

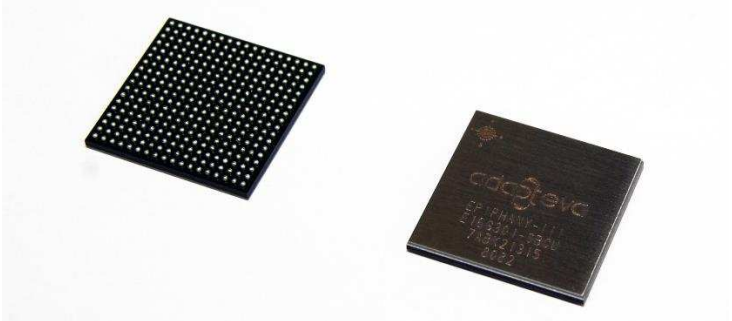


Figure 9: Mechanical Drawing

6.4 Thermal Characteristics

The following table shows simulated thermal data for the E16G301 package with a total chip power consumption of 2 Watts with the E16G301 mounted on a 12 layer PCB of dimensions 86mm x 54mm.

Theta ja (C/W)			Psi jt	Theta jc
0 m/s	1 m/s	2 m/s	(C/W)	(C/W)
22.6	20.0	19.1	7.88	10.4

Table 16: Thermal Characteristics of Device Package

6.5 Complete Package Pin-out

PIN	BGA BALL
VSS (72)	A1,A8,A11,A18, B2,B17, C3,C16,D4,D15, E5,E6,E13,E14, F5,F6,F13,F14, G6,G8,G10,G12,G14, H1,H5,H7,H9,H11,H13,H18, J6,J8,J10,J12,J14, K5,K7,K9,K11,K13, L1,L6,L8,L10,L12,L14,L18, M5,M7,M9,M11,M13, N6,N8,N10,N12,N14, P5,P7, P9, P11,P13, R4,R15, T3,T16, U2,U17, V1, V8, V11,V18
VDD (24)	H6,H8,H10,H12,J7,J9,J11,J13,K6,K8,K10,K12,L7,L9,L11,L13,M6 ,M8,M10,M12,N7,N9,N11,N13
DVDD (16)	G5,G7,G9,G11,G13,H14,J5,K14,L5,M14,N5,P6,P8,P10,P12,P14

PIN	BGA BALL
COLID[0]	F12
COLID[1]	E8
COLID[2]	F10
COLID[3]	E7
ROWID[0]	E10
ROWID[1]	E11
ROWID[2]	E9
ROWID[3]	F9
FLAG	E12
MVDD	F8
MVSS	F7
RESET_N	F11
RXI_EA_CCLK_N	J18
RXI_EA_CCLK_P	K18
RXI_EA_DATA_N[0]	T18
RXI_EA_DATA_N[1]	R17
RXI_EA_DATA_N[2]	P16
RXI_EA_DATA_N[3]	N15

RXI_EA_DATA_N[4]	P18
RXI_EA_DATA_N[5]	N17
RXI_EA_DATA_N[6]	M16
RXI_EA_DATA_N[7]	L15
RXI_EA_DATA_P[0]	U18
RXI_EA_DATA_P[1]	T17
RXI_EA_DATA_P[2]	R16
RXI_EA_DATA_P[3]	P15
RXI_EA_DATA_P[4]	R18
RXI_EA_DATA_P[5]	P17
RXI_EA_DATA_P[6]	N16
RXI_EA_DATA_P[7]	M15
RXI_EA_FRAME_N	L17
RXI_EA_FRAME_P	M17
RXI_EA_LCLK_N	M18
RXI_EA_LCLK_P	N18
RXO_EA_RD_WAIT_N	J17
RXO_EA_RD_WAIT_P	K17
RXO_EA_WR_WAIT_N	K16
RXO_EA_WR_WAIT_P	L16
RXI_NO_CCLK_N	A9
RXI_NO_CCLK_P	A10
RXI_NO_DATA_N[0]	A2
RXI_NO_DATA_N[1]	B3
RXI_NO_DATA_N[2]	C4
RXI_NO_DATA_N[3]	D5
RXI_NO_DATA_N[4]	A4
RXI_NO_DATA_N[5]	B5
RXI_NO_DATA_N[6]	C6
RXI_NO_DATA_N[7]	D7
RXI_NO_DATA_P[0]	A3
RXI_NO_DATA_P[1]	B4
RXI_NO_DATA_P[2]	C5
RXI_NO_DATA_P[3]	D6
RXI_NO_DATA_P[4]	A5
RXI_NO_DATA_P[5]	B6
RXI_NO_DATA_P[6]	C7
RXI_NO_DATA_P[7]	D8

RXI_NO_FRAME_N	B7
RXI_NO_FRAME_P	B8
RXI_NO_LCLK_N	A6
RXI_NO_LCLK_P	A7
RXO_NO_RD_WAIT_N	B9
RXO_NO_RD_WAIT_P	B10
RXO_NO_WR_WAIT_N	C8
RXO_NO_WR_WAIT_P	C9
RXI_SO_CCLK_N	V10
RXI_SO_CCLK_P	V9
RXI_SO_DATA_N[0]	V3
RXI_SO_DATA_N[1]	U4
RXI_SO_DATA_N[2]	T5
RXI_SO_DATA_N[3]	R6
RXI_SO_DATA_N[4]	V5
RXI_SO_DATA_N[5]	U6
RXI_SO_DATA_N[6]	T7
RXI_SO_DATA_N[7]	R8
RXI_SO_DATA_P[0]	V2
RXI_SO_DATA_P[1]	U3
RXI_SO_DATA_P[2]	T4
RXI_SO_DATA_P[3]	R5
RXI_SO_DATA_P[4]	V4
RXI_SO_DATA_P[5]	U5
RXI_SO_DATA_P[6]	T6
RXI_SO_DATA_P[7]	R7
RXI_SO_FRAME_N	U8
RXI_SO_FRAME_P	U7
RXI_SO_LCLK_N	V7
RXI_SO_LCLK_P	V6
RXI_SO_RD_WAIT_N	U10
RXI_SO_RD_WAIT_P	U9
RXI_SO_WR_WAIT_N	T9
RXI_SO_WR_WAIT_P	T8
RXI_WE_CCLK_N	K1
RXI_WE_CCLK_P	J1
RXI_WE_DATA_N[0]	U1
RXI_WE_DATA_N[1]	T2

RXI_WE_DATA_N[2]	R3
RXI_WE_DATA_N[3]	P4
RXI_WE_DATA_N[4]	R1
RXI_WE_DATA_N[5]	P2
RXI_WE_DATA_N[6]	N3
RXI_WE_DATA_N[7]	M4
RXI_WE_DATA_P[0]	T1
RXI_WE_DATA_P[1]	R2
RXI_WE_DATA_P[2]	P3
RXI_WE_DATA_P[3]	N4
RXI_WE_DATA_P[4]	P1
RXI_WE_DATA_P[5]	N2
RXI_WE_DATA_P[6]	M3
RXI_WE_DATA_P[7]	L4
RXI_WE_FRAME_N	M2
RXI_WE_FRAME_P	L2
RXI_WE_LCLK_N	N1
RXI_WE_LCLK_P	M1
RXO_WE_RD_WAIT_N	K2
RXO_WE_RD_WAIT_P	J2
RXO_WE_WR_WAIT_N	L3
RXO_WE_WR_WAIT_P	K3
TXO_EA_DATA_N[0]	G15
TXO_EA_DATA_N[1]	F16
TXO_EA_DATA_N[2]	E17
TXO_EA_DATA_N[3]	D18
TXO_EA_DATA_N[4]	E15
TXO_EA_DATA_N[5]	D16
TXO_EA_DATA_N[6]	C17
TXO_EA_DATA_N[7]	B18
TXO_EA_DATA_P[0]	H15
TXO_EA_DATA_P[1]	G16
TXO_EA_DATA_P[2]	F17
TXO_EA_DATA_P[3]	E18
TXO_EA_DATA_P[4]	F15
TXO_EA_DATA_P[5]	E16
TXO_EA_DATA_P[6]	D17
TXO_EA_DATA_P[7]	C18

TXO_EA_FRAME_N	J15
TXO_EA_FRAME_P	K15
TXO_EA_LCLK_N	F18
TXO_EA_LCLK_P	G18
TXO_EA_RD_WAIT_N	G17
TXO_EA_RD_WAIT_P	H17
TXO_EA_WR_WAIT_N	H16
TXO_EA_WR_WAIT_P	J16
TXO_NO_DATA_N[0]	D11
TXO_NO_DATA_N[1]	C12
TXO_NO_DATA_N[2]	B13
TXO_NO_DATA_N[3]	A14
TXO_NO_DATA_N[4]	D13
TXO_NO_DATA_N[5]	C14
TXO_NO_DATA_N[6]	B15
TXO_NO_DATA_N[7]	A16
TXO_NO_DATA_P[0]	D12
TXO_NO_DATA_P[1]	C13
TXO_NO_DATA_P[2]	B14
TXO_NO_DATA_P[3]	A15
TXO_NO_DATA_P[4]	D14
TXO_NO_DATA_P[5]	C15
TXO_NO_DATA_P[6]	B16
TXO_NO_DATA_P[7]	A17
TXO_NO_FRAME_N	D9
TXO_NO_FRAME_P	D10
TXO_NO_LCLK_N	A12
TXO_NO_LCLK_P	A13
TXO_NO_RD_WAIT_N	B11
TXO_NO_RD_WAIT_P	B12
TXO_NO_WR_WAIT_N	C10
TXO_NO_WR_WAIT_P	C11
TXO_SO_DATA_N[0]	R12
TXO_SO_DATA_N[1]	T13
TXO_SO_DATA_N[2]	U14
TXO_SO_DATA_N[3]	V15
TXO_SO_DATA_N[4]	R14
TXO_SO_DATA_N[5]	T15

TXO_SO_DATA_N[6]	U16
TXO_SO_DATA_N[7]	V17
TXO_SO_DATA_P[0]	R11
TXO_SO_DATA_P[1]	T12
TXO_SO_DATA_P[2]	U13
TXO_SO_DATA_P[3]	V14
TXO_SO_DATA_P[4]	R13
TXO_SO_DATA_P[5]	T14
TXO_SO_DATA_P[6]	U15
TXO_SO_DATA_P[7]	V16
TXO_SO_FRAME_N	R10
TXO_SO_FRAME_P	R9
TXO_SO_LCLK_N	V13
TXO_SO_LCLK_P	V12
TXO_SO_RD_WAIT_N	U12
TXO_SO_RD_WAIT_P	U11
TXO_SO_WR_WAIT_N	T11
TXO_SO_WR_WAIT_P	T10
TXO_WE_DATA_N[0]	H4
TXO_WE_DATA_N[1]	G3
TXO_WE_DATA_N[2]	F2
TXO_WE_DATA_N[3]	E1
TXO_WE_DATA_N[4]	F4
TXO_WE_DATA_N[5]	E3
TXO_WE_DATA_N[6]	D2
TXO_WE_DATA_N[7]	C1
TXO_WE_DATA_P[0]	G4
TXO_WE_DATA_P[1]	F3
TXO_WE_DATA_P[2]	E2
TXO_WE_DATA_P[3]	D1
TXO_WE_DATA_P[4]	E4
TXO_WE_DATA_P[5]	D3
TXO_WE_DATA_P[6]	C2
TXO_WE_DATA_P[7]	B1
TXO_WE_FRAME_N	K4
TXO_WE_FRAME_P	J4
TXO_WE_LCLK_N	G1
TXO_WE_LCLK_P	F1

TXO_WE_RD_WAIT_N	H2
TXO_WE_RD_WAIT_P	G2
TXO_WE_WR_WAIT_N	J3
TXO_WE_WR_WAIT_P	H3

7 System Integration

7.1 FPGA/ASIC Interfacing

The E16G301 can be directly interfaced to an FPGA or ASIC by instantiating the eLink interface provided by Adapteva. The eLink interface block is used to convert the high speed serial link I/O interface to a lower speed parallel interface. To the system, the eLink interface looks like a simple memory mapped interface.

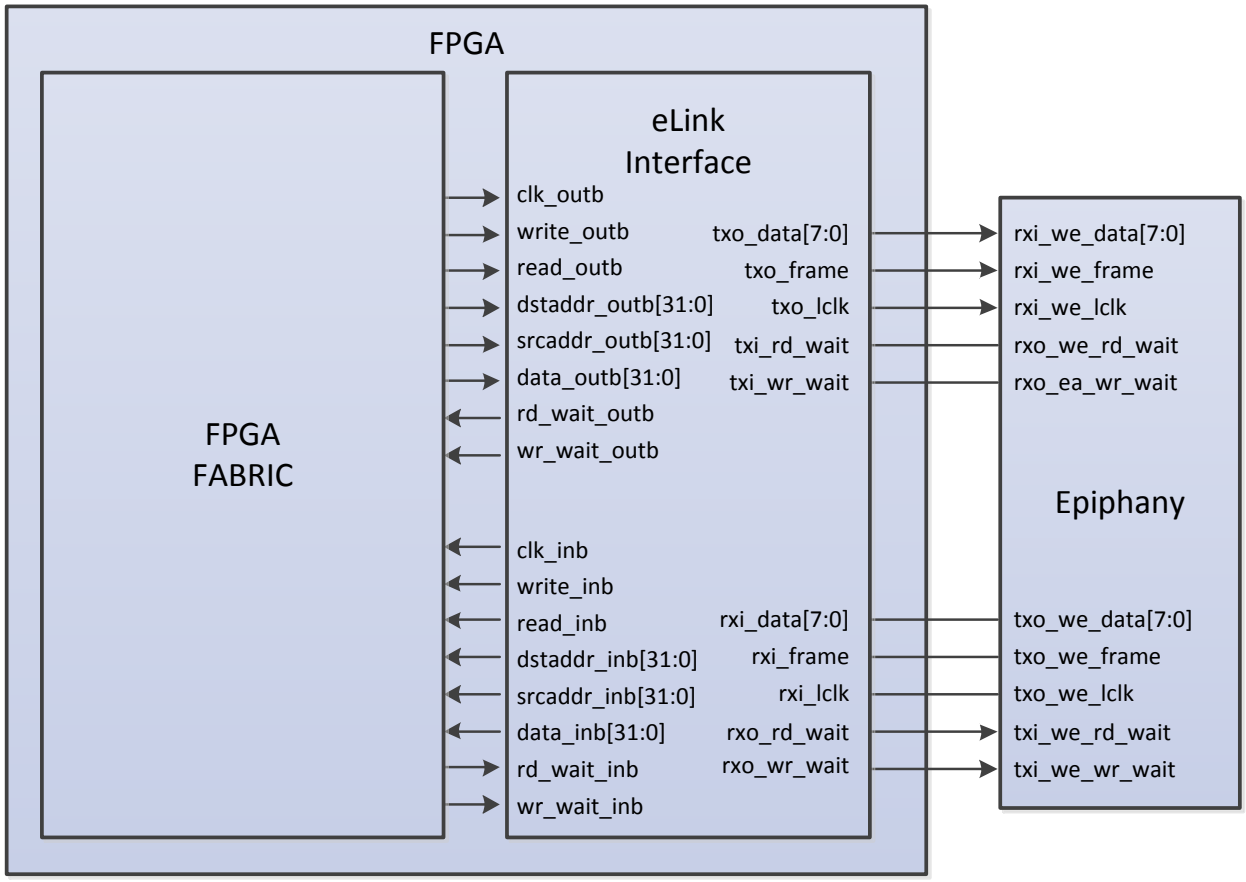


Figure 10: FPGA eLink Integration Example

The following table documents the signal description of the eLink interface as seen by the FPGA internal logic.

Signal Name	Width	Direction	Description
clk_inb	1	In	Clock used to write to transaction FIFO in eMesh interface
access_inb	1	In	Assert high and stays keep until read or write transaction has completed
write_inb	1	In	Asserted high to indicate a write transaction
datamode_inb	2	In	Datasize of transaction. 00=8-bit, 01=16-bit, 10=32-bit, 11=64-bit
ctrlmode_inb	4	In	Reserved, should be tied to 0
dstaddr_inb	32	In	Address of memory mapped transaction
data_inb	32	In	For write transaction: Data to be written For read transaction: Value ignored
srcaddr_inb	32	In	For write transaction: Upper data of 64 bit transaction in case of double write transaction, otherwise ignored For read transaction: Returning address to send data to once the data has been read from the address in the dstaddr field.
wr_wait_inb	1	Out	Pushback indicating that eMesh write transaction receiving FIFO is full
rd_wait_inb	1	Out	Pushback indicating that eMesh read transaction receiving FIFO is full

Table 17: Incoming Transaction (TO FPGA/ASIC)

Signal Name	Width	Direction	Description
clk_outb	1	Out	Clock to be used to sample transaction from eMesh
access_outb	1	Out	Asserted high and stays keep until read or write transaction has completed
write_outb	1	Out	Asserted high to indicate a write transaction
datamode_outb	2	Out	Data size of transaction. 00=8-bit, 01=16-bit, 10=32-bit, 11=64-bit
ctrlmode_outb	4	Out	Reserved, should be tied to 0
dstaddr_outb	32	Out	Address of memory mapped transaction
data_outb	32	Out	For write transaction: Data to write to dstaddr_out For read transaction: Value can be ignored
srcaddr_outb	32	Out	For write transaction: Upper data of 64 bit transaction in case of double write transaction, otherwise ignored For read transaction: Returning address to send data to once the data has been read from the address in the dstaddr field.
wr_wait_outb	1	In	Driven high to stop eMesh from sending more write transactions
rd_wait_outb	1	In	Driven high to stop eMesh from sending more read transactions

Table 18: Outgoing Transaction (FROM FPGA/ASIC)

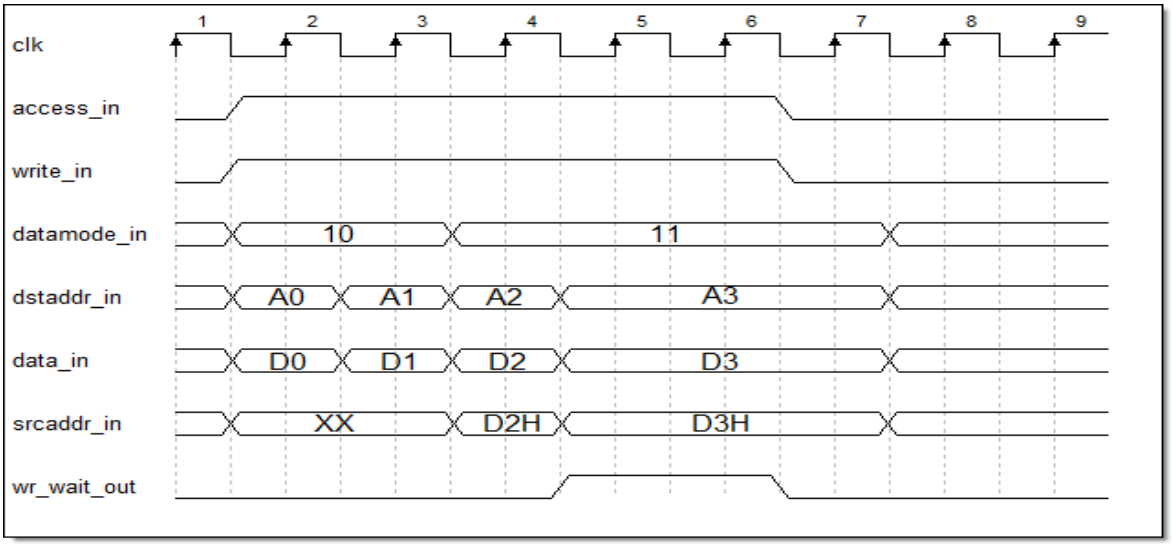


Figure 11: eLink Write Transaction Timing Diagram

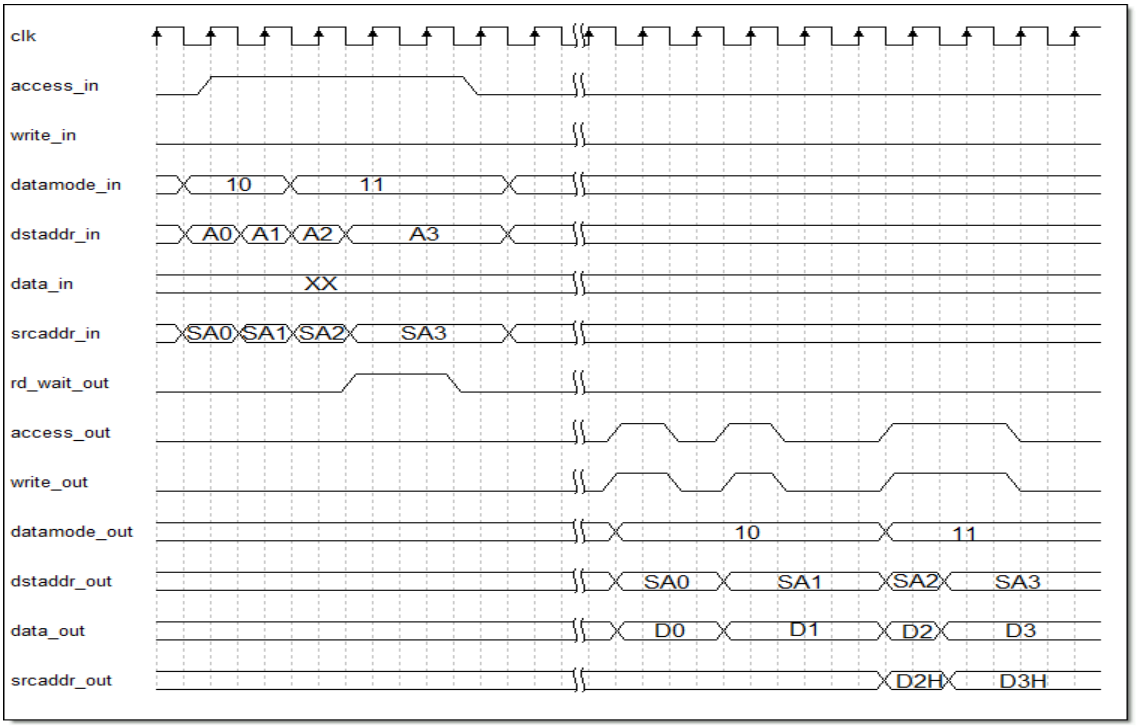


Figure 12: eLink Read Transaction Timing Diagram

8 Ordering Information

8.1 Part Number Naming Methodology

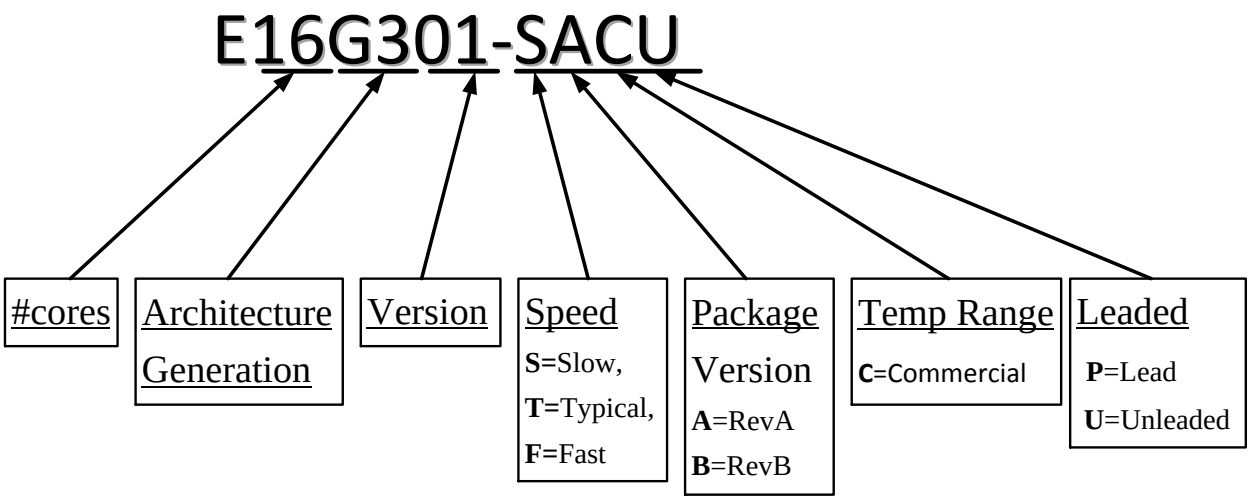


Figure 13: Part Numbering Methodology

8.2 Product Availability

Part Number	Temp Range	Speed Grade	Comment
E16G301-SACP	–40°C to +85°C	700MHz	End-Of-Life
E16G301-SBCU	–40°C to +85°C	700MHz	Sampling Q3, 2013
E16G301-TBCU	–40°C to +85°C	800MHz	Planned for Q3, 2014
E16G301-FBCU	–40°C to +85°C	1 GHz	Planned for Q3, 2014

Table 19: Product Ordering Table

9 Errata

This table contains all the known errata for the E16G301 product. System designers and software developers should consider these items as a part of the current product but they should also beware that that the behavior of the errata items is likely to change in future versions of the Epiphany products.

Errata #	Errata Item	Chip Version	Type	Explanation
0	Reset sensitivity	E16G301	Functional	To guarantee a correct and repeatable reset wakeup sequencing, the RXI_WE_CCLK_{P/N} signal must be held stable for the duration of the rising edge of RESET_N.
1	DMA Throttle	E16G301	Performance	The DMA engine bandwidth per channel is stuck at 50% throttle, meaning that each DMA channel can transfer at most 1 double word every two clock cycles.
2	NOC FIFO Full	E16G301	Performance	The FIFO interface between the compute node and the Network-On-Chip currently indicates FIFO full too early, causing a degradation in peak outgoing transfer bandwidth from the Epiphany processor node to the eMesh NOC.
3	Software Exception	E16G301	Functional	On a software exception, the PC jumps to address 0x4 and halts instead of continuing with the exception service routine.

Table 20: Errata List

10 Copyright Information

Adapteva Inc.

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Lexington, MA 02420

USA

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