DDR3 VLP-Registered/ECC DIMM Module

2GB based on 1Gbit component

FBGA with Pb-Free

Revision 1.0 (May. 2008)
-Initial Release

240-Pin DDR3-VLP-Reg/ECC-DIMM DDR3 SDRAM

1.0 Feature

- JEDEC standard V_{DDQ}=1.5V +/- 0.075V Power Supply
- VDDQ = 1.5V ± 0.075V
- Programmable CAS Latency: 6,7,8,9,10,11
- Programmable Additive Latency(Posted CAS) : 0, CL - 2, or CL - 1 clock
- 400MHz fCK for 800Mb/sec/pin, 533MHz fCK for 1066Mb/sec/pin, 667MHz fCK for 1333Mb/sec/pin, 800MHz fCK for 1600Mb/sec/pin
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address "000" only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm ± 1%)
- Bi-directional Differential Data Strobe
- Asynchronous Reset
- On-Die termination using ODT pin
- 8 independent internal bank
- Average Refresh Period 7.8us at lower than a TCASE 85°C, 3.9us at 85°C < TCASE < 95 °C
- Serial presence detect with EEPROM
- VLP-RDIMM Dimension (Nominal) 18.75 mm high, 133.35 mm wide
- Based on JEDEC standard reference Raw Cards Lay out.
- Halogen-Free compliant
- Gold plated contacts

2.0 Ordering Information

Part number	Density	Module Organization	Component composition	Component PKG	Module Rank	Description
W13VB2G8x	2GB	256Mx72	128Mx8*18	FBGA	2	PC3-10600

Note: Last Character x of the Part Number stand for DRAM vendor
S=Samsung; M=Micron; H=Hynix

3.0 Operating Frequencies

	DDR3-1333	Unit
CL-tRCD-tRP	9-9-9	tCK
CAS Latency	9	tCK
tCK(min)	1.5	ns
tRCD(min)	13.5	ns
tRP(min)	13.5	ns
tRAS(min)	36	ns
tRC(min)	49.5	ns

4.0 Absolute Maximum DC Rating

Symbol	Parameter	Rating	Units
V_{in}, Vout	Voltage on any pin relative to V_{SS}	-0.4 ~ 1.975	V
V_{DD}	Voltage on V_{DD} & V_{DDQ} supply relative to V_{ss}	-0.4 ~ 1.975	V
V_{DDQ}	Short circuit current	-0.4 ~ 1.975	V
V_{DDL}	Power dissipation	-0.4 ~ 1.975	V
T_{STG}	Storage Temperature	-55 ~ + 100	°C

5.0 DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	$V_{REF}DQ$	121	V_{SS}	31	DQ25	151	V_{SS}	61	A2	181	A1	91	DQ41	211	V_{SS}
2	V_{SS}	122	DQ4	32	V_{SS}	152	DQS12	62	V_{DD}	182	V_{DD}	92	V_{SS}	212	DQS14,NC
3	DQ0	123	DQ5	33	$\overline{DQS3}$	153	$\overline{DQS12}$	63	NC,CK1	183	V_{DD}	93	$\overline{DQS5}$	213	$\overline{DQS14,NC}$
4	DQ1	124	V_{SS}	34	DQS3	154	V_{SS}	64	NC,$\overline{CK1}$	184	CK0	94	DQS5	214	V_{SS}
5	V_{SS}	125	DQS9	35	V_{SS}	155	DQ30	KEY				95	V_{SS}	215	DQ46
6	$\overline{DQS0}$	126	$\overline{DQS9}$	36	DQ26	156	DQ31	65	V_{DD}	185	$\overline{CK0}$	DQ47	DQ42	216	DQ47
7	DQS0	127	V_{SS}	37	DQ27	157	V_{SS}	66	V_{DD}	186	V_{DD}	97	DQ43	217	V_{SS}
8	V_{SS}	128	DQ6	38	V_{SS}	158	CB4,NC	67	$V_{REF}CA$	187	$\overline{EVENT,NC}$	98	V_{SS}	218	DQ52
9	DQ2	129	DQ7	39	CB0,NC	159	CB5,NC	68	NC/Par_in	188	A0	99	DQ48	219	DQ53
10	DQ3	130	V_{SS}	40	CB1,NC	160	V_{SS}	69	V_{DD}	189	V_{DD}	100	DQ49	220	V_{SS}
11	V_{SS}	131	DQ12	41	V_{SS}	161	DQS17,NC	70	A10/AP	190	BA1	101	V_{SS}	221	DQS15,NC
12	DQ8	132	DQ13	42	$\overline{DQS8}$	162	$\overline{DQS17,NC}$	71	BA0	191	V_{DD}	102	$\overline{DQS6}$	222	$\overline{DQS15,NC}$
13	DQ9	133	V_{SS}	43	DQS8	163	V_{SS}	72	V_{DD}	192	$\overline{RAS}$	103	DQS6	223	V_{SS}
14	V_{SS}	134	DQS10	44	V_{SS}	164	CB6,NC	73	$\overline{WE}$	193	$\overline{S0}$	104	V_{SS}	224	DQ54
15	$\overline{DQS1}$	135	$\overline{DQS10}$	45	CB2,NC	165	CB7,NC	74	$\overline{CAS}$	194	V_{DD}	105	DQ50	225	DQ55
16	DQS1	136	V_{SS}	46	CB3,NC	166	V_{SS}	75	V_{DD}	195	ODT0	106	DQ51	226	V_{SS}
17	V_{SS}	137	DQ14	47	V_{SS}	167	NC	76	NC	196	A13	107	V_{SS}	227	DQ60
18	DQ10	138	DQ15	48	V_{TT},NC	168	$\overline{RESET}$	77	NC	197	V_{DD}	108	DQ56	228	DQ61
19	DQ11	139	V_{SS}	49	V_{TT},NC	169	CKE1,NC	78	V_{DD}	198	NC	109	DQ57	229	V_{SS}
20	V_{SS}	140	DQ20	50	CKE0	170	V_{DD}	79	NC	199	V_{SS}	110	V_{SS}	230	DQS16,NC
21	DQ16	141	DQ21	51	V_{DD}	171	A15	80	V_{SS}	200	DQ36	111	$\overline{DQS7}$	231	$\overline{DQS16,NC}$
22	DQ17	142	V_{SS}	52	BA2	172	A14	81	DQ32	201	DQ37	112	DQS7	232	V_{SS}
23	V_{SS}	143	DQS11	53	$\overline{E_{RR}\_O_{UT}}$	173	V_{DD}	82	DQ33	202	V_{SS}	113	V_{SS}	233	DQ62
24	$\overline{DQS2}$	144	$\overline{DQS11}$	54	V_{DD}	174	A12	83	V_{SS}	203	$\overline{DQS13,NC}$	114	DQ58	234	DQ63
25	DQS2	145	V_{SS}	55	A11	175	A9	84	$\overline{DQS4}$	204	DQS13,NC	115	DQ59	235	VSS
26	V_{SS}	146	DQ22	56	A7	176	V_{DD}	85	DQS4	205	V_{SS}	116	V_{SS}	236	$V_{DD}SPD$
27	DQ18	147	DQ23	57	V_{DD}	177	A8	86	V_{SS}	206	DQ38	117	SA0	237	SA1
28	DQ19	148	V_{SS}	58	A5	178	A6	87	DQ34	207	DQ39	118	SCL	238	SDA
29	V_{SS}	149	DQ28	59	A4	179	V_{DD}	88	DQ35	208	V_{SS}	119	SA2	239	V_{SS}
30	DQ24	150	DQ29	60	V_{DD}	180	A3	89	V_{SS}	209	DQ44	120	V_{TT}	240	V_{TT}
								90	DQ40	210	DQ45				

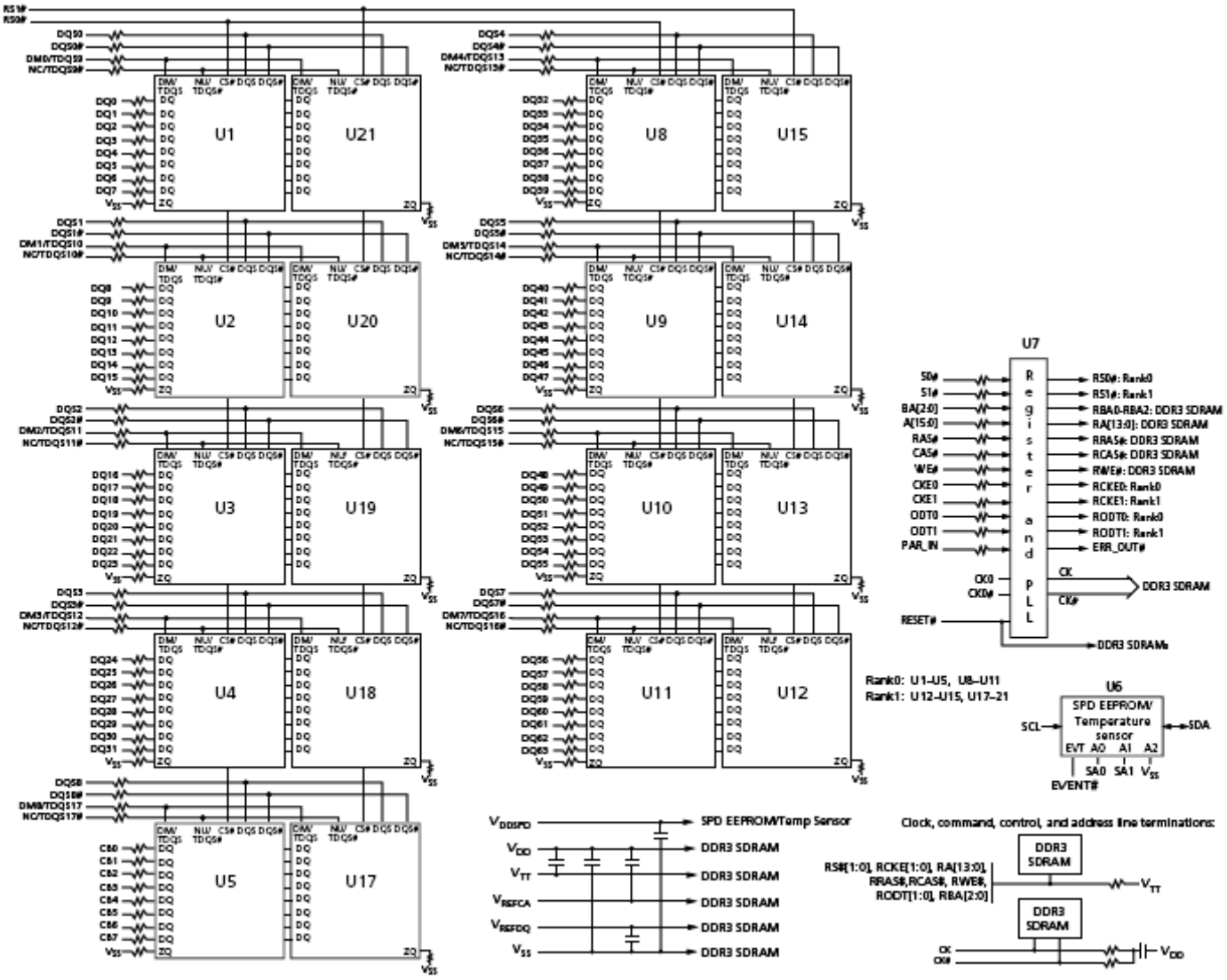
6.0 DIMM Pin Description

Pin Name	Function	Pin Name	Function
A0 ~ A15	Address input (Multiplexed)	ODT0~ODT1	On Die Termination
A10/AP	Address Input/Auto pre-charge	CB0~CB7	ECC Data check bits Input/Output
BA0 ~ BA2	Bank Select	DQ0~DQ63	Data Input/Output
$\overline{CK0}$ ~ $\overline{CK2}$, CK0~CK2	Clock input	$\overline{DQS0}$~$\overline{DQS8}$	Data strobes, negative line
CKE0, CKE1	Clock enable input	DM (0~8),	Data Masks/Data strobes (Read)
$\overline{S0}$, $\overline{S1}$	Chip select input	DQS0~DQS8	Data Strobes
$\overline{RAS}$	Row address strobe	RFU	Reserved for future used
$\overline{CAS}$	Column address strobe	V_{TT}	SDRAM I/O termination power supply
$\overline{WE}$	Write Enable	TEST	Memory bus test tool
SCL	SPD Clock Input	V_{DD}	Core Power
SDA	SPD Data Input/Output	V_{DDQ}	I/O Power
SA0~SA2	SPD Address	V_{SS}	Ground
Par_In	Parity bit for address & Control bus	V_{REF}DQ	SDRAM Input/Output Reference Supply
$\overline{EVENT}$	EVENT pin on TS/SPD part, Temperature event	V_{DD}SPD	Serial EEPROM Power Supply
Reset	Register and PLL control pin	V_{REF}CA	Command Address Reference Supply

7.0 Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Pre-charge
128Mx8(1Gb)base	A0-A13	A0-A9	BA0-BA2	A10

8.0 Functional Block Diagram: 2GB; 256x72 Module (Populated as 2 ranks of x8 SDRAM Module)



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1 percent resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

9.0 AC & DC Operating Conditions

Recommended operating conditions (Voltage referenced to Vss=0V, TA=0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	1.425	1.5	1.575	V
V_{DDQ}	Supply Voltage for Output	1.425	1.5	1.575	V
$V_{REF}DQ_{(DC)}$	I/O Reference Voltage (DQ)	0.49*V_{DDQ}	0.50*V_{DDQ}	0.51*V_{DDQ}	V
$V_{REF}CA_{(DC)}$	I/O Reference Voltage (CMD/Add)	0.49*V_{DDQ}	0.50*V_{DDQ}	0.51*V_{DDQ}	V
V_{TT}	Termination Voltage	0.49*V_{DDQ}	0.50*V_{DDQ}	0.51*V_{DDQ}	V

10.0 Capacitance (Max.)

Symbol	Parameter/Condition	Min	Max	Unit
CCK	Input capacitance, CK and $\overline{CK}$	-	11	pF
CI1	Input capacitance, CKE and $\overline{CS}$	-	12	pF
CI2	Input capacitance, Addr, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	-	12	pF
CIO	Input capacitance, DQ, DM, DQS, $\overline{DQS}$	-	10	pF

11.1 AC Timing Parameters & Specifications

(AC operating conditions unless otherwise noted)

Parameter	Symbol	DDR3-1333		Units
		min	max	
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	ns
Average Clock Period	tCK(avg)	-		ps
Clock Period	tCK(abs)	tCK(avg) min +tJIT (per)min	tCK(avg) max +tJIT (per)max	ps
Average high pulse width	tCH(avg)	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	tCK(avg)
Clock Period Jitter	tJIT(per)	-80	80	ps
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-80	80	ps
Cycle to Cycle Period Jitter	tJIT(cc)	160	-	ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	140	-	ps
Cumulative error across 2 cycles	tERR(2per)	- 118	118	ps
Cumulative error across 3 cycles	tERR(3per)	- 140	140	ps
Cumulative error across 4 cycles	tERR(4per)	- 155	155	ps
Cumulative error across 5 cycles	tERR(5per)	- 168	168	ps
Cumulative error across 6 cycles	tERR(6per)	- 177	177	ps
Cumulative error across 7 cycles	tERR(7per)	- 186	186	ps
Cumulative error across 8 cycles	tERR(8per)	- 193	193	ps
Cumulative error across 9 cycles	tERR(9per)	- 200	200	ps
Cumulative error across 10 cycles	tERR(10per)	- 205	205	ps

11.2 AC Timing Parameters & Specifications (con't)

Parameter	Symbol	DDR3-1333		Units
		min	max	
Cumulative error across 11 cycles	tERR(11per)	- 210	210	ps
Cumulative error across 12 cycles	tERR(12per)	- 215	215	ps
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min tERR(nper)max = (1 = 0.68ln(n))*tJIT(per)max		ps
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	tCK(avg)
Absolute clock Low pulse width	tCL(abs)	0.43	-	tCK(avg)
Data Timing				
DQS, /DQS to DQ skew, per group, per access	tDQSQ	-	125	ps
DQ output hold time from DQS, /DQS	tQH	0.38	-	tCK(avg)
DQ low-impedance time from CK, /CK	tLZ(DQ)	-500	250	ps
DQ high-impedance time from CK, /CK	tHZ(DQ)	-	250	ps
Data setup time to DQS, /DQS referenced to Vih(ac)Vil(ac) levels	tDS(base)	TBD	-	ps
Data hold time to DQS, /DQS referenced to Vih(ac)Vil(ac) levels	tDH(base)	TBD	-	ps
DQ and DM Input pulse width for each input	tDIPW	400	-	ps
Data Strobe Timing				
DQS, /DQS READ Preamble	tRPRE	0.9	-	tCK
DQS, /DQS differential READ Postamble	tRPST	0.3	-	tCK
DQS, /DQS output high time	tQSH	0.4	-	tCK(avg)
DQS, /DQS output low time	tQSL	0.4	-	tCK(avg)
DQS, /DQS WRITE Preamble	tWPRE	0.9	-	tCK
DQS, /DQS WRITE Postamble	tWPST	0.3	-	tCK
DQS, /DQS rising edge output access time from rising CK, /CK	tDQSCK	-255	255	ps
DQS, /DQS low-impedance time (Referenced from RL-1)	tLZ(DQS)	-500	250	ps
DQS, /DQS high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	250	-	ps
DQS, DQS differential input low pulse width	tDQSL	0.45	0.55	tCK
DQS, DQS differential input high pulse width	tDQSH	0.45	0.55	tCK
DQS, DQS rising edge to CK, CK rising edge	tDQSS	-0.25	0.25	tCK(avg)
DQS,DQS faling edge setup time to CK, CK rising edge	tDSS	0.2	-	tCK(avg)
DQS,DQS faling edge hold time to CK, CK rising edge	tDSH	0.2	-	tCK(avg)
DLL locking time	tDLLK	512	-	nCK
internal READ Command to PRECHARGE Command delay	tRTP	max (4tCK,7.5ns)	-	
Delay from start of internal write transaction to internal read command	tWTR	max (4tCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	nCK
Mode Register Set command update delay	tMOD	max (12tCK,15ns)	-	
CAS# to CAS# command delay	tCCD	4	-	nCK
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP / tCK(AVG))		nCK

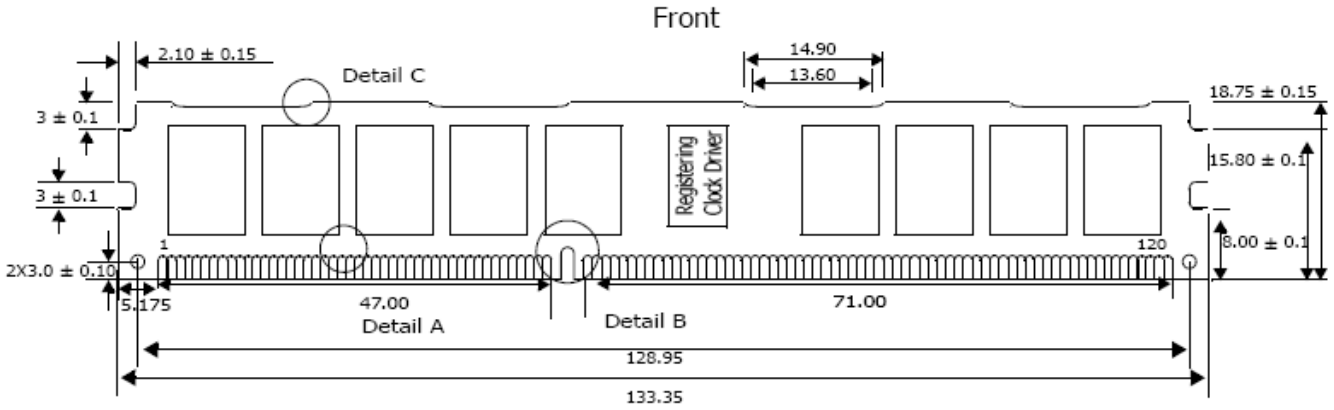
11.3 AC Timing Parameters & Specifications (con't)

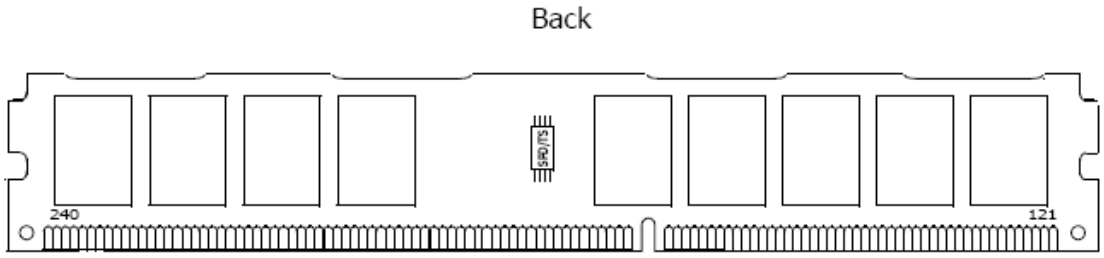
Parameter	Symbol	DDR3-1333		Units
		min	max	
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK
ACTIVE to PRECHARGE command period	tRAS	36	70,000	ns
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max (4tCK,6ns)	-	
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4tCK,7.5ns)	-	
Four activate window for 1KB page size	tFAW	30	-	ns
Four activate window for 2KB page size	tFAW	45	-	ns
Command and Address setup time to CK, CK referenced to Vih(ac) / Vil(ac) levels	tIS(base)	65	-	ps
Command and Address hold time from CK, CK referenced to Vih(ac) / Vil(ac) levels	tIH(base)	140	-	ps
Command and Address setup time to CK, CK referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC150	65+125	-	ps
Control & Address Input pulse width for each input	tIPW	620	-	ps
Calibration Timing				
Power-up and RESET calibration time	tZQinitI	512	-	tCK
Normal operation Full calibration time	tZQoper	256	-	tCK
Normal operation short calibration time	tZQCS	64	-	tCK
Reset Timing				
Exit Reset from CKE HIGH to a valid command	tXPR	max(5tCK, tRFC+ 10ns)	-	
Self Refresh Timing				
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5tCK,tRFC+ 10ns)	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	nCK
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1tCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE)	tCKSRE	max(5tCK, 10ns)	-	
Valid Clock Requirement before Self Refresh Exit (SRX)	tCKSRX	max(5tCK, 10ns)	-	
Power Down Timing				
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (3tCK,6ns)	-	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max(10tCK, 24ns)	-	
CKE minimum pulse width	tCKE	max(3tCK, 5.625ns)	-	
Command pass disable delay	tCPDED	1	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCK
Timing of ACT command to Power Down entry	tACTPDEN	1	-	nCK
Timing of PRE command to Power Down entry	tPRPDEN	1	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 +1	-	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRPDEN	WL + 4 +(tWR/tCK)	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRAPDEN	WL + 4 +WR+1	-	nCK
Timing of WR command to Power Down entry (BL4MRS)	tWRPDEN	WL + 2 +(tWR/ tCK(avg))	-	nCK

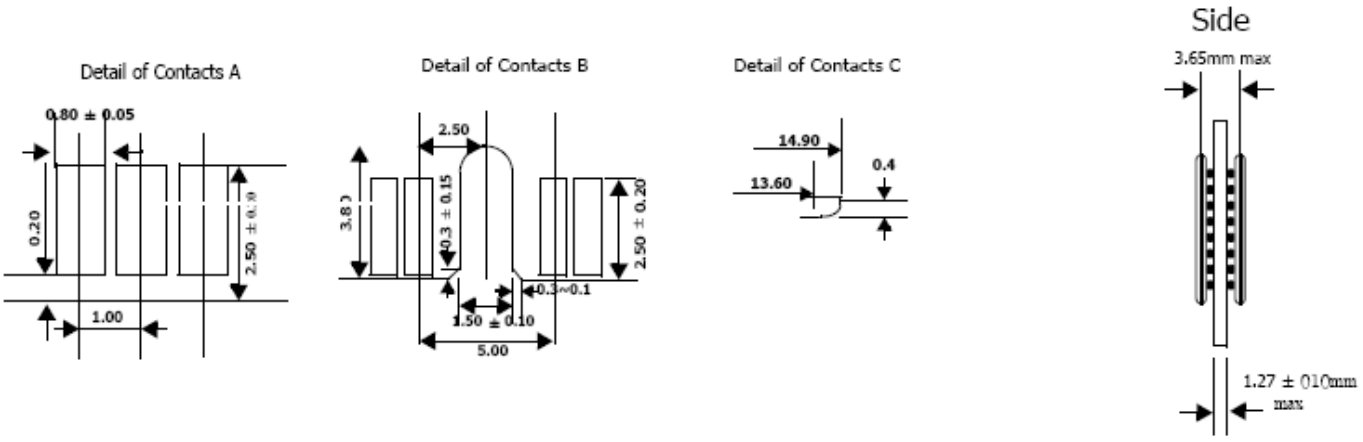
11.4 AC Timing Parameters & Specifications (con't)

Parameter	Symbol	DDR3-1333		Units
		min	max	
Timing of WRA command to Power Down entry (BL4MRS)	tWRAPDEN	WL +2 +WR +1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	1	-	
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	
ODT Timing				
ODT high time without write command or with wirte commandand BC4	ODTH4	4	-	nCK
ODT high time with Write command and BL8	ODTH8	6	-	nCK
Asynchronous RTT tum-on delay (Power-Down with DLL frozen)	tAONPD	1	9	ns
Asynchronous RTT tum-off delay (Power-Down with DLL frozen)	tAOFPD	1	9	ns
ODT turn-on	tAON	-250	250	ps
RTT_NOM and RTT_WR turn-off time from ODTL off reference	tAOF	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)
Write Leveling Timing				
First DQS pulse rising edge after tDQSS margining mode is programmed	tWLMRD	40	-	tCK
DQS/DQS delay after tDQS margining mode is programmed	tWLDQSEN	25	-	tCK
Setup time for tDQSS latch	tWLS	195	-	ps
Hold time of tDQSS latch	tWLH	195	-	ps
Write leveling output delay	tWLO	0	9	ns
Write leveling output error	tWLOE	0	2	ns

12.0 Physical Dimensions: (128Mx8 Based)
256Mx72 (2Rank)







Tolerances: ± 0.005(.13) unless otherwise specified