DDR3 Unbuffered DIMM Module

2GB based on 2Gbit component

TFBGA with Pb-Free

Revision 1.0 (MAY. 2007)
-Initial Release

1.0 Feature

- JEDEC standard 1.5V ± 0.075V Power Supply
- VDDQ = 1.5V ± 0.075V
- Programmable CAS latencies 6,7,8,9,10,11,13
- Programmable Additive Latency(Posted CAS) : 0, CL - 2, or CL - 1 clock
- Programmable CAS Write Latency(CWL) = 5 (DDR3-800), 6 (DDR3-1066), 7 (DDR3-1333), 8 (DDR3-1600) and 9 (DDR3-1866)
- 400MHz fCK for 800Mb/sec/pin, 533MHz fCK for 1066Mb/sec/pin, 667MHz fCK for 1333Mb/sec/pin, 800MHz fCK for 1600Mb/sec/pin, 900MHz fCK for 1866Mb/sec/pin
- Bi-directional Differential Data Strobe
- Burst Length: 8 (Interleave without any limit, sequential with starting address "000" only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- On-Die termination using ODT pin
- 8 independent internal bank
- Asynchronous Reset
- Average Refresh Period 7.8us at lower than a TCASE 85°C, 3.9us at 85°C < TCASE < 95 °C
- Serial presence detect with EEPROM
- DIMM Dimension (Nominal) 30.00 mm high, 133.35 mm wide
- Based on JEDEC standard reference Raw Cards Lay out.
- RoHS compliant
- Gold plated contacts

2.0 Ordering Information

Part number	Density	Module Organization	Component composition	Component PKG	Module Rank	Description
W1333UA2GV	2GB	256Mx64	256Mx8*8	TFBGA	1	2GB 1Rx8 PC3-10600U

3.0 Key Timing Parameters

	DDR3-1333	Unit
CL-tRCD-tRP	9-9-9	tCK
CAS Latency	9	tCK
tCK(min)	1.5	ns
tRCD(min)	13.5	ns
tRP(min)	13.5	ns
tRAS(min)	36	ns
tRC(min)	49.5	ns

4.0 Absolute Maximum DC Rating

Symbol	Parameter	Rating	Units
Vin , Vout	Voltage on any pin relative to V_{SS}	-0.4 ~ 1.975	V
V_{DD}	Voltage on V_{DD} & V_{DDQ} supply relative to V_{ss}	-0.4 ~ 1.975	V
V_{DDQ}	Short circuit current	-0.4 ~ 1.975	V
V_{DDL}	Power dissipation	-0.4 ~ 1.975	V
T_{STG}	Storage Temperature	-55 ~ + 100	°C

5.0 DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}DQ	121	Vss	41	Vss	161	*DM8/DQS17_P*	81	DQ32	201	DQ37
2	Vss	122	DQ4	42	NC	162	*DQS17_N*	82	DQ33	202	Vss
3	DQ0	123	DQ5	43	NC	163	Vss	83	Vss	203	*DM4/DQS13_P*
4	DQ1	124	Vss	44	Vss	164	NC	84	*DQS4_N*	204	*DQS13_N*
5	Vss	125	*DM0/DQS9_P*	45	NC	165	NC	85	*DQS4_P*	205	Vss
6	*DQS0_N*	126	*NC/DQS9_N*	46	NC	166	Vss	86	Vss	206	DQ38
7	*DQS0_P*	127	Vss	47	Vss	167	NC/TEST	87	DQ34	207	DQ39
8	Vss	128	DQ6	48	NC	168	RESET_N	88	DQ35	208	Vss
9	DQ2	129	DQ7	KEY				89	Vss	209	DQ44
10	DQ3	130	Vss	49	NC	169	CKE1	90	DQ40	210	DQ45
11	Vss	131	DQ12	50	CKE0	170	V_{DD}	91	DQ41	211	Vss
12	DQ8	132	DQ13	51	V_{DD}	171	A15	92	Vss	212	*DM5/DQS14_P*
13	DQ9	133	Vss	52	BA2	172	A14	93	*DQS5_N*	213	*DQS14_N*
14	Vss	134	*DM1/DQS10_P*	53	NC/Err-Out	173	V_{DD}	94	*DQS5_P*	214	Vss
15	*DQS1_N*	135	*DQS10_N*	54	V_{DD}	174	A12	95	Vss	215	DQ46
16	*DQS2_P*	136	Vss	55	A11	175	A9	96	DQ42	216	DQ47
17	Vss	137	DQ14	56	A7	176	V_{DD}	97	DQ43	217	Vss
18	DQ10	138	DQ15	57	V_{DD}	177	A8	98	Vss	218	DQ52
19	DQ11	139	Vss	58	A5	178	A6	99	DQ48	219	DQ53
20	Vss	140	DQ20	59	A4	179	V_{DD}	100	DQ49	220	Vss
21	DQ16	141	DQ21	60	V_{DD}	180	A3	101	VSS	221	*DM6_DQS15_P*
22	DQ17	142	Vss	61	A2	181	A1	102	*DQS6_N*	222	*DQS15_N*
23	Vss	143	*DQS11_P*	62	V_{DD}	182	V_{DD}	103	*DQS6_P*	223	Vss
24	*DQS2_N*	144	*DQS11_N*	63	*CK1_P/NC*	183	V_{DD}	104	Vss	224	DQ54
25	*DQS2_P*	145	Vss	64	*CK1_N/NC*	184	*CK0_P*	105	DQ50	225	DQ55
26	Vss	146	DQ22	65	V_{DD}	185	*CK0_N*	106	DQ51	226	Vss
27	DQ18	147	DQ23	66	V_{DD}	186	VDD	107	Vss	227	DQ60
28	DQ19	148	Vss	67	V_{REF}CA	187	NC/EVENT	108	DQ56	228	DQ61
29	Vss	149	DQ28	68	NC, Par_In	188	A0	109	DQ57	229	Vss
30	DQ24	150	DQ29	69	V_{DD}	189	V_{DD}	110	Vss	230	*DM7/DQS16_P*
31	DQ25	151	Vss	70	A10/AP	190	BA1	111	*DQS7_N*	231	*DQS16_N*
32	Vss	152	*DM3/DQS12_P*	71	BA0	191	VDD	112	*DQS7_P*	232	Vss
33	*DQ3_N*	153	*DQS12_N*	72	V_{DD}	192	RAS_N	113	Vss	233	DQ62
34	*DQ3_P*	154	Vss	73	WE	193	S0_N	114	DQ58	234	DQ63
35	Vss	155	DQ30	74	CAS	194	VDD	115	DQ59	235	Vss
36	DQ26	156	DQ31	75	V_{DD}	195	ODT0	116	Vss	236	V_{DD}SPD
37	DQ27	157	Vss	76	S1	196	A13	117	SA0	237	SA1
38	Vss	158	NC	77	ODT1	197	V_{DD}	118	SCL	238	SDA
39	NC	159	NC	78	V_{DD}	198	NC	119	SA2	239	Vss
40	NC	160	Vss	79	S2/NC	199	Vss	120	V_{TT}	240	V_{TT}
				80	Vss	200	DQ36				

1. NC = No Connect, RFU = Reserved for Future Use
2. Par_in and Err_out pins are intended for register control functions.

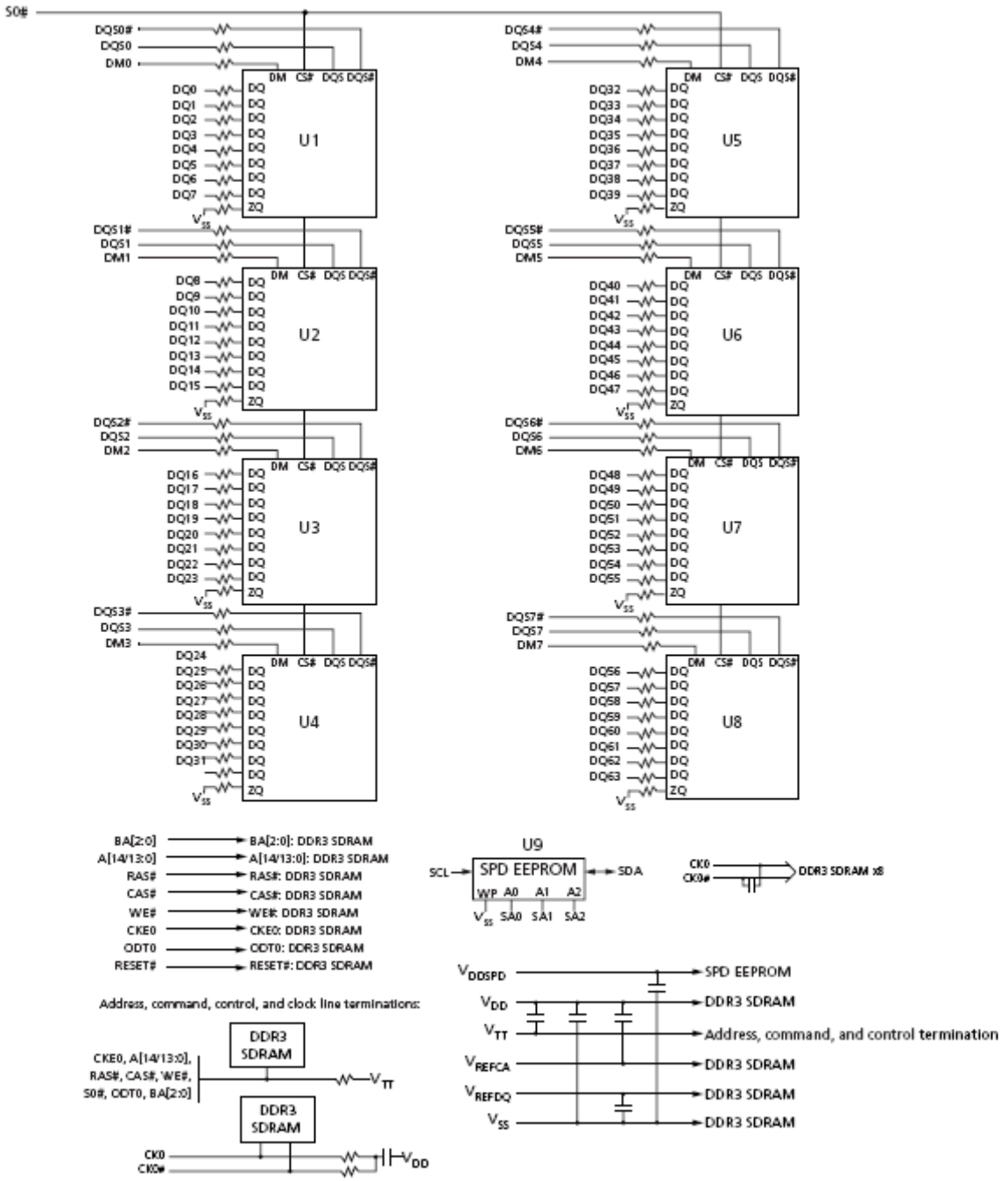
6.0 DIMM Pin Description

Pin Name	Function	Pin Name	Function
A0 ~ A15	Address input (Multiplexed)	ODT0~ODT1	On Die Termination
A10/AP	Address Input/Auto pre-charge	CB0~CB7	ECC Data check bits Input/Output
BA0 ~ BA2	Bank Select	DQ0~DQ63	Data Input/Output
$\overline{CK0}$ ~ $\overline{CK2}$, CK0~CK2	Clock input	$\overline{DQS0}$~$\overline{DQS8}$	Data strobes, negative line
CKE0, CKE1	Clock enable input	DM(0~8),	Data Masks/Data strobes (Read)
$\overline{S0}$, $\overline{S1}$	Chip select input	DQS0~DQS8	Data Strobes
$\overline{RAS}$	Row address strobe	RFU	Reserved for future used
$\overline{CAS}$	Column address strobe	V_{TT}	SDRAM I/O termination power supply
$\overline{WE}$	Write Enable	TEST	Memory bus test tool
SCL	SPD Clock Input	V_{DD}	Core Power
SDA	SPD Data Input/Output	V_{DDQ}	I/O Power
SA0~SA2	SPD Address	V_{SS}	Ground
Par_In	Parity bit for address & Control bus	V_{REF}DQ	SDRAM Input/Output Reference Supply
Err_Out	Parity error found in the Address and Control bus	V_{DD}SPD	Serial EEPROM Power Supply
/RESET	Register and PLL control pin	V_{REF}CA	Command Address Reference Supply

7.0 Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Pre-charge
256Mx8(2Gb) base	A0-A14	A0-A9	BA0-BA2	A10/AP

8.0 Functional Block Diagram: 2GB, 256Mx64 Module (Populated as 1 ranks of x8)



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

9.0 AC & DC Operating Conditions

Recommended operating conditions (Voltage referenced to Vss=0V, TA=0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	1.425	1.5	1.575	V
V_{DDQ}	Supply Voltage for Output	1.425	1.5	1.575	V
$V_{REF}DQ_{(DC)}$	I/O Reference Voltage (DQ)	$0.49*V_{DDQ}$	$0.50*V_{DDQ}$	$0.51*V_{DDQ}$	V
$V_{REF}CA_{(DC)}$	I/O Reference Voltage (CMD/Add)	$0.49*V_{DDQ}$	$0.50*V_{DDQ}$	$0.51*V_{DDQ}$	V
V_{TT}	Termination Voltage	$0.49*V_{DDQ}$	$0.50*V_{DDQ}$	$0.51*V_{DDQ}$	V

10.0 Capacitance (Max.)

Symbol	Parameter/Condition	Min	Max	Unit
CCK	Input capacitance, CK and $\overline{CK}$	-	11	pF
CI1	Input capacitance, CKE and $\overline{CS}$	-	12	pF
CI2	Input capacitance, Addr, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	-	12	pF
CIO	Input capacitance, DQ, DM, DQS, $\overline{DQS}$	-	10	pF

11.1 AC Timing Parameters & Specifications

(AC operating conditions unless otherwise noted)

Parameter	Symbol	DDR3-1333		Units
		min	max	
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	ns
Average Clock Period	tCK(avg)	-		ps
Clock Period	tCK(abs)	tCK(avg) min +tJIT (per)min	tCK(avg) max +tJIT (per)max	ps
Average high pulse width	tCH(avg)	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	tCK(avg)
Clock Period Jitter	tJIT(per)	-80	80	ps
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-80	80	ps
Cycle to Cycle Period Jitter	tJIT(cc)	160	-	ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	140	-	ps
Cumulative error across 2 cycles	tERR(2per)	- 118	118	ps
Cumulative error across 3 cycles	tERR(3per)	- 140	140	ps
Cumulative error across 4 cycles	tERR(4per)	- 155	155	ps
Cumulative error across 5 cycles	tERR(5per)	- 168	168	ps
Cumulative error across 6 cycles	tERR(6per)	- 177	177	ps
Cumulative error across 7 cycles	tERR(7per)	- 186	186	ps
Cumulative error across 8 cycles	tERR(8per)	- 193	193	ps
Cumulative error across 9 cycles	tERR(9per)	- 200	200	ps
Cumulative error across 10 cycles	tERR(10per)	- 205	205	ps

11.2 AC Timing Parameters & Specifications (con't)

Parameter	Symbol	DDR3-1333		Units
		min	max	
Cumulative error across 11 cycles	tERR(11per)	- 210	210	ps
Cumulative error across 12 cycles	tERR(12per)	- 215	215	ps
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min tERR(nper)max = (1 = 0.68ln(n))*tJIT(per)max		ps
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	tCK(avg)
Absolute clock Low pulse width	tCL(abs)	0.43	-	tCK(avg)
Data Timing				
DQS, /DQS to DQ skew, per group, per access	tDQSQ	-	125	ps
DQ output hold time from DQS, /DQS	tQH	0.38	-	tCK(avg)
DQ low-impedance time from CK, /CK	tLZ(DQ)	-500	250	ps
DQ high-impedance time from CK, /CK	tHZ(DQ)	-	250	ps
Data setup time to DQS, /DQS referenced to Vih(ac)Vil(ac) levels	tDS(base)	TBD	-	ps
Data hold time to DQS, /DQS referenced to Vih(ac)Vil(ac) levels	tDH(base)	TBD	-	ps
DQ and DM Input pulse width for each input	tDIPW	400	-	ps
Data Strobe Timing				
DQS, /DQS READ Preamble	tRPRE	0.9	-	tCK
DQS, /DQS differential READ Postamble	tRPST	0.3	-	tCK
DQS, /DQS output high time	tQSH	0.4	-	tCK(avg)
DQS, /DQS output low time	tQSL	0.4	-	tCK(avg)
DQS, /DQS WRITE Preamble	tWPRE	0.9	-	tCK
DQS, /DQS WRITE Postamble	tWPST	0.3	-	tCK
DQS, /DQS rising edge output access time from rising CK, /CK	tDQSCK	-255	255	ps
DQS, /DQS low-impedance time (Referenced from RL-1)	tLZ(DQS)	-500	250	ps
DQS, /DQS high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	250	-	ps
DQS, DQS differential input low pulse width	tDQSL	0.45	0.55	tCK
DQS, DQS differential input high pulse width	tDQSH	0.45	0.55	tCK
DQS, DQS rising edge to CK, CK rising edge	tDQSS	-0.25	0.25	tCK(avg)
DQS,DQS faling edge setup time to CK, CK rising edge	tDSS	0.2	-	tCK(avg)
DQS,DQS faling edge hold time to CK, CK rising edge	tDSH	0.2	-	tCK(avg)
DLL locking time	tDLLK	512	-	nCK
internal READ Command to PRECHARGE Command delay	tRTP	max (4tCK,7.5ns)	-	
Delay from start of internal write transaction to internal read command	tWTR	max (4tCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	nCK
Mode Register Set command update delay	tMOD	max (12tCK,15ns)	-	
CAS# to CAS# command delay	tCCD	4	-	nCK
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP / tCK(AVG))		nCK

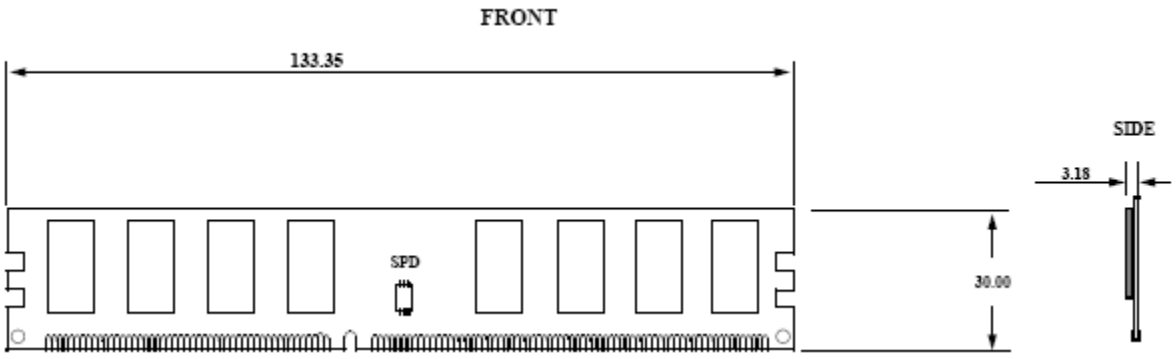
11.3 AC Timing Parameters & Specifications (con't)

Parameter	Symbol	DDR3-1333		Units
		min	max	
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK
ACTIVE to PRECHARGE command period	tRAS	36	70,000	ns
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max(4tCK,6ns)	-	
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max(4tCK,7.5ns)	-	
Four activate window for 1KB page size	tFAW	30	-	ns
Four activate window for 2KB page size	tFAW	45	-	ns
Command and Address setup time to CK, CK referenced to Vih(ac) / Vil(ac) levels	tIS(base)	65	-	ps
Command and Address hold time from CK, CK referenced to Vih(ac) / Vil(ac) levels	tIH(base)	140	-	ps
Command and Address setup time to CK, CK referenced to Vih(ac) / Vil(ac) levels	tIS(base)AC150	65+125	-	ps
Control & Address Input pulse width for each input	tIPW	620	-	ps
Calibration Timing				
Power-up and RESET calibration time	tZQinitI	512	-	tCK
Normal operation Full calibration time	tZQoper	256	-	tCK
Normal operation short calibration time	tZQCS	64	-	tCK
Reset Timing				
Exit Reset from CKE HIGH to a valid command	tXPR	max(5tCK, tRFC+10ns)	-	
Self Refresh Timing				
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5tCK,tRFC+ 10ns)	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	nCK
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1tCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE)	tCKSRE	max(5tCK, 10ns)	-	
Valid Clock Requirement before Self Refresh Exit (SRX)	tCKSRX	max(5tCK, 10ns)	-	
Power Down Timing				
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLLfrozen to commands not requiring a locked DLL	tXP	max(3tCK,6ns)	-	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max(10tCK, 24ns)	-	
CKE minimum pulse width	tCKE	max(3tCK, 5.625ns)	-	
Command pass disable delay	tCPDED	1	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCK
Timing of ACT command to Power Down entry	tACTPDEN	1	-	nCK
Timing of PRE command to Power Down entry	tPRPDEN	1	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 +1	-	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRPDEN	WL + 4 +(tWR/tCK)	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRAPDEN	WL + 4 +WR+1	-	nCK
Timing of WR command to Power Down entry (BL4MRS)	tWRPDEN	WL + 2 +(tWR/ tCK(avg))	-	nCK

11.4 AC Timing Parameters & Specifications (con't)

Parameter	Symbol	DDR3-1333		Units
		min	max	
Timing of WRA command to Power Down entry (BL4MRS)	tWRAPDEN	WL +2 +WR +1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	1	-	
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	
ODT Timing				
ODT high time without write command or with wirte commandand BC4	ODTH4	4	-	nCK
ODT high time with Write command and BL8	ODTH8	6	-	nCK
Asynchronous RTT tum-on delay (Power-Down with DLL frozen)	tAONPD	1	9	ns
Asynchronous RTT tum-off delay (Power-Down with DLL frozen)	tAOFPD	1	9	ns
ODT turn-on	tAON	-250	250	ps
RTT_NOM and RTT_WR turn-off time from ODTL off reference	tAOF	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)
Write Leveling Timing				
First DQS pulse rising edge after tDQSS margining mode is programmed	tWLMRD	40	-	tCK
DQS/DQS delay after tDQS margining mode is programmed	tWLDQSEN	25	-	tCK
Setup time for tDQSS latch	tWLS	195	-	ps
Hold time of tDQSS latch	tWLH	195	-	ps
Write leveling output delay	tWLO	0	9	ns
Write leveling output error	tWLOE	0	2	ns

12.0 Physical Dimensions: (256Mbx8 Based, 256MBx64, 1 Rank)



Tolerances: ± 0.005(.13) unless otherwise specified