

BUK9K29-100E

Dual N-channel TrenchMOS logic level FET

28 August 2012

Product data sheet

1. Product profile

1.1 General description

Dual logic level N-channel MOSFET in a LFPAK56D package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

1.2 Features and benefits

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with $V_{GS(th)} > 0.5 \text{ V @ } 175 \text{ °C}$

1.3 Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25 \text{ °C}; T_j \leq 175 \text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 5 \text{ V}; T_{mb} = 25 \text{ °C}; \text{Fig. 1}$	-	-	30	A
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ °C}; \text{Fig. 2}$	-	-	68	W
T_j	junction temperature		-55	-	175	°C
Static characteristics FET1 and FET2						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ °C}; \text{Fig. 12}$	-	25.1	29	mΩ
Dynamic characteristics FET1 and FET2						
$Q_{G(tot)}$	total gate charge	$I_D = 10 \text{ A}; V_{DS} = 80 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ °C}; \text{Fig. 14}; \text{Fig. 15}$	-	54	-	nC
Q_{GD}	gate-drain charge		-	10.9	-	nC

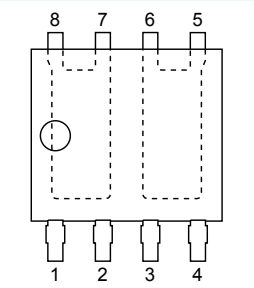
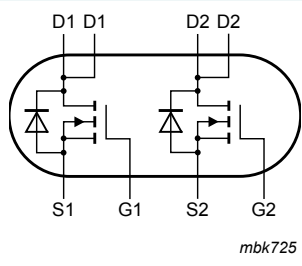


Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche Ruggedness FET1 and FET2						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 40\text{ A}$; $V_{sup} \leq 100\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; Fig. 3	[1][2]	-	63	mJ

- [1] Refer to application note AN10273 for further information
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>LFAK56D (SOT1205)</p>	 <p style="text-align: right;"><i>mbk725</i></p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK9K29-100E	LFAK56D	Plastic single ended surface mounted package (LFAK56D); 8 leads	SOT1205

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$; $T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	100	V
V_{GS}	gate-source voltage		-10	10	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 1	-	30	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 1	-	21	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 4	-	118	A

Symbol	Parameter	Conditions	Min	Max	Unit
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 2	-	68	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode FET1 and FET2					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	30	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	118	A
Avalanche Ruggedness FET1 and FET2					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 40\text{ A}$; $V_{sup} \leq 100\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; Fig. 3	[1][2]	-	63 mJ

[1] Refer to application note AN10273 for further information

[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C

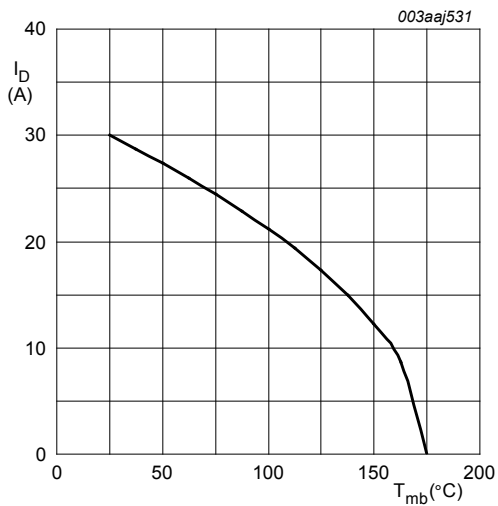


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10V$$

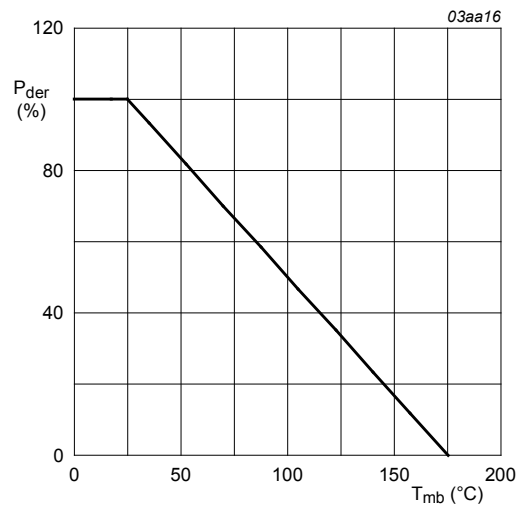


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

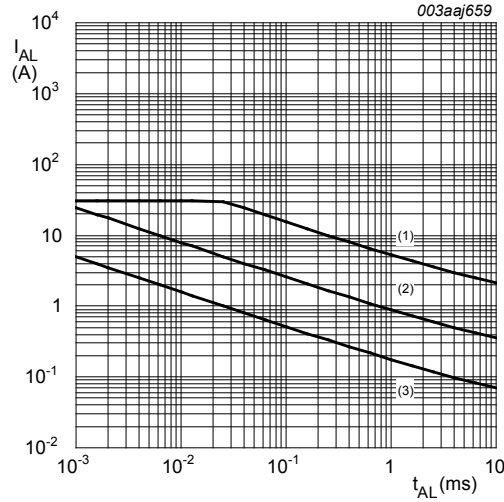


Fig. 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2

- (1) Single-pulse; $T_j = 25^\circ\text{C}$.
- (2) Single-pulse; $T_j = 175^\circ\text{C}$.
- (3) Repetitive.

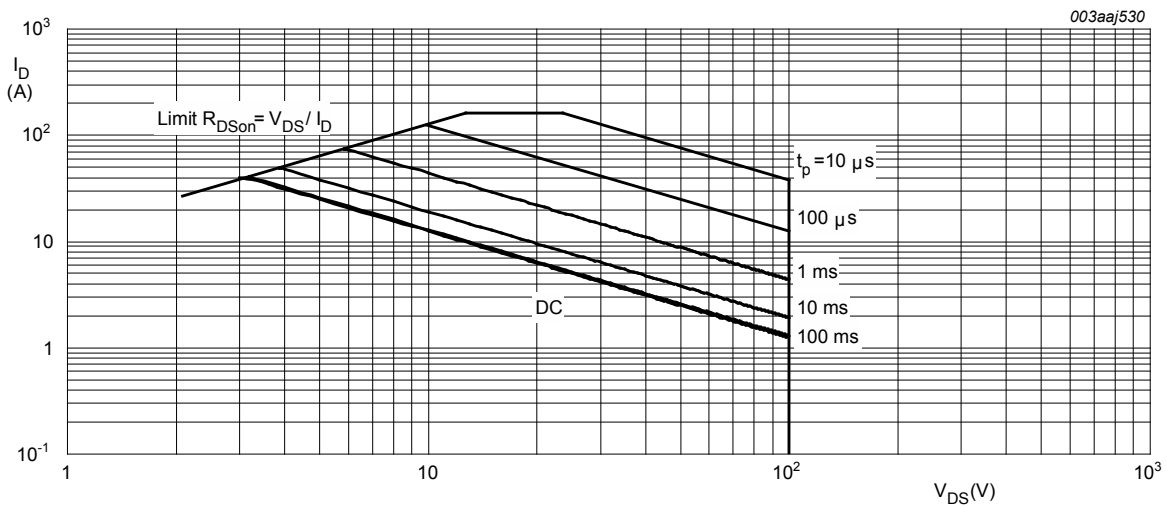


Fig. 4. Safe operating area; continuous and peak drain current as a function of drain-source voltage

$T_{mb} = 25^\circ\text{C}$; I_{DM} is single pulse

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	2.21	K/W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

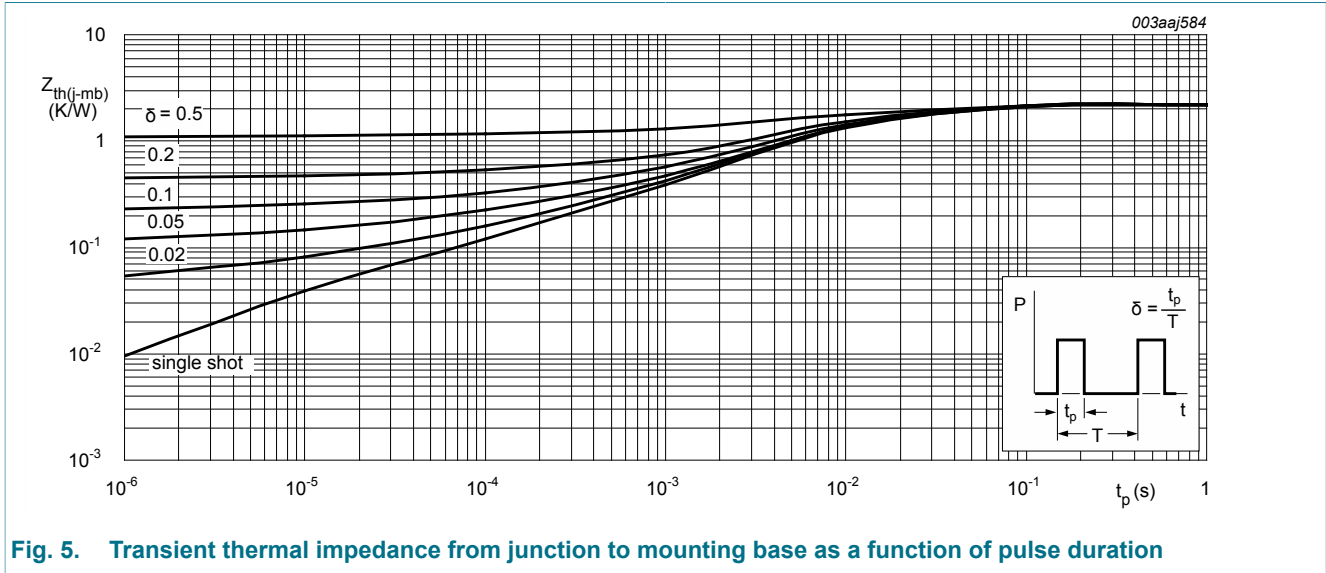


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics FET1 and FET2						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 10; Fig. 11	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ Fig. 10; Fig. 11	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ Fig. 10; Fig. 11	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.02	1	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 12	-	25.1	29	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 175 \text{ }^\circ C;$ Fig. 12; Fig. 13	-	68.02	78.6	m Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_{GS} = 10\text{ V}; I_D = 10\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 12	-	22.7	27	mΩ
Dynamic characteristics FET1 and FET2						
$Q_{G(\text{tot})}$	total gate charge	$I_D = 10\text{ A}; V_{DS} = 80\text{ V}; V_{GS} = 10\text{ V};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 14 ; Fig. 15	-	54	-	nC
Q_{GS}	gate-source charge	$I_D = 10\text{ A}; V_{DS} = 80\text{ V}; V_{GS} = 10\text{ V};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 15 ; Fig. 14	-	5.6	-	nC
Q_{GD}	gate-drain charge	$I_D = 10\text{ A}; V_{DS} = 80\text{ V}; V_{GS} = 10\text{ V};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 14 ; Fig. 15	-	10.9	-	nC
$Q_{GS(\text{th})}$	pre-threshold gate-source charge	$I_D = 10\text{ A}; V_{DS} = 80\text{ V}; V_{GS} = 10\text{ V};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 14 ; Fig. 15	-	4.2	-	nC
$Q_{GS(\text{th-pl})}$	post-threshold gate-source charge		-	1.4	-	nC
$V_{GS(\text{pl})}$	gate-source plateau voltage	$I_D = 10\text{ A}; V_{DS} = 80\text{ V}; T_j = 25\text{ }^\circ\text{C};$ $T_j = 25\text{ }^\circ\text{C}$	-	2.3	-	V
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 16	-	2618	3491	pF
C_{oss}	output capacitance		-	172	206	pF
C_{rss}	reverse transfer capacitance		-	90	123	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 80\text{ V}; R_L = 8\text{ }^\Omega; V_{GS} = 10\text{ V};$ $R_{G(\text{ext})} = 5\text{ }^\Omega; T_j = 25\text{ }^\circ\text{C}; I_D = 10\text{ A}$	-	6.1	-	ns
t_r	rise time		-	6.4	-	ns
$t_{d(\text{off})}$	turn-off delay time		-	67.3	-	ns
t_f	fall time		-	35.1	-	ns
Source-drain diode FET1 and FET2						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 17	-	0.78	1.2	V
t_{rr}	reverse recovery time	$I_S = 10\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 80\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	32.7	-	ns
Q_r	recovered charge		-	50.1	-	nC

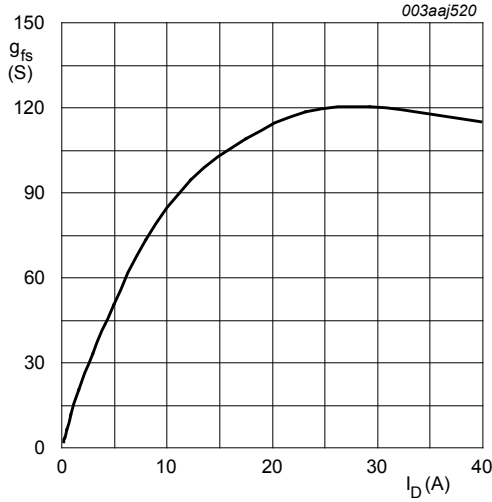


Fig. 6. Forward transconductance as a function of drain current; typical values

$T_j = 25^\circ\text{C}; V_{DS} = 15\text{ V}$

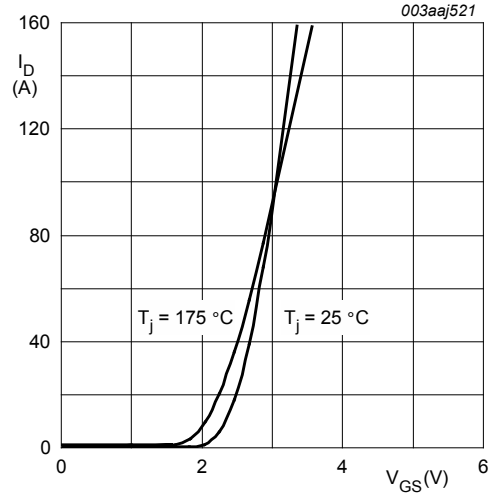


Fig. 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} > I_D \times R_{DS(on)}$

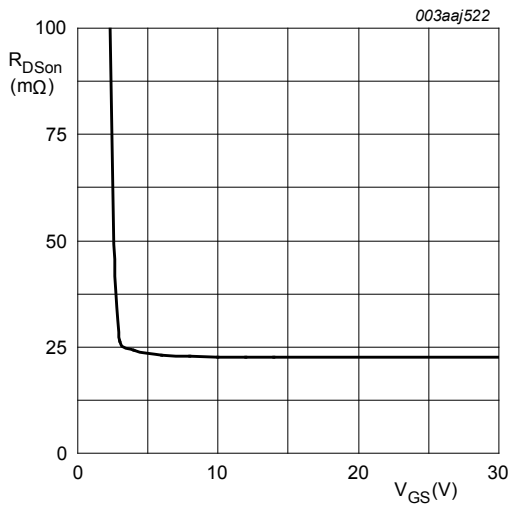


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^\circ\text{C}; I_D = 10\text{ A}$

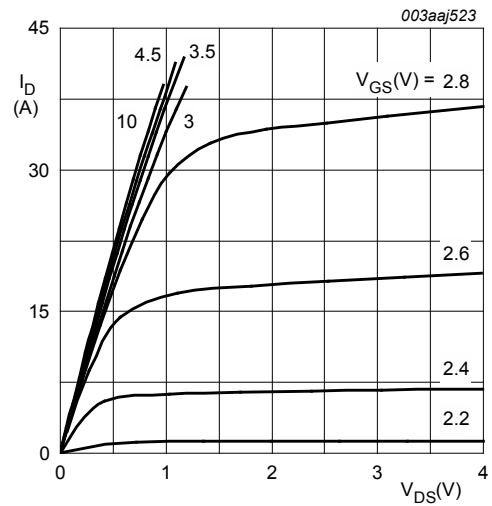


Fig. 9. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25^\circ\text{C}$

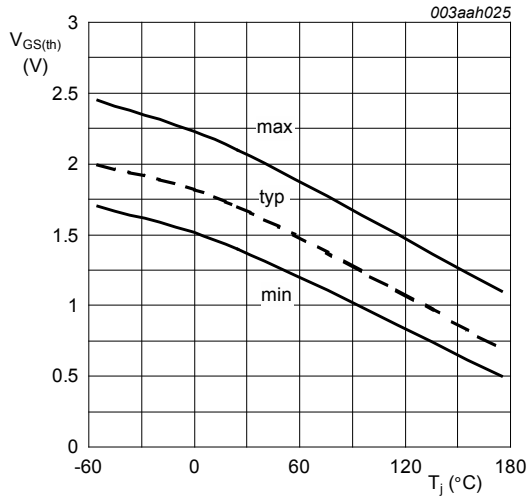


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

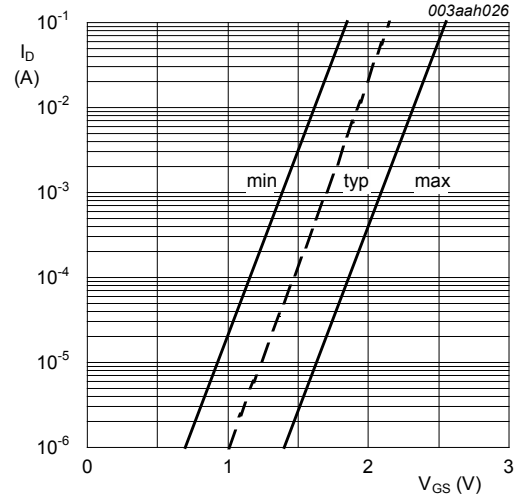


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$$

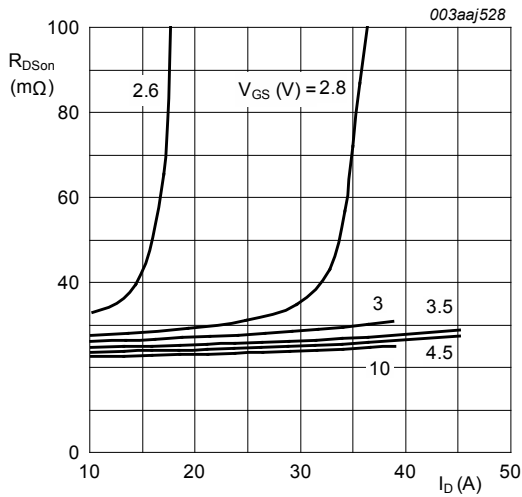


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}$$

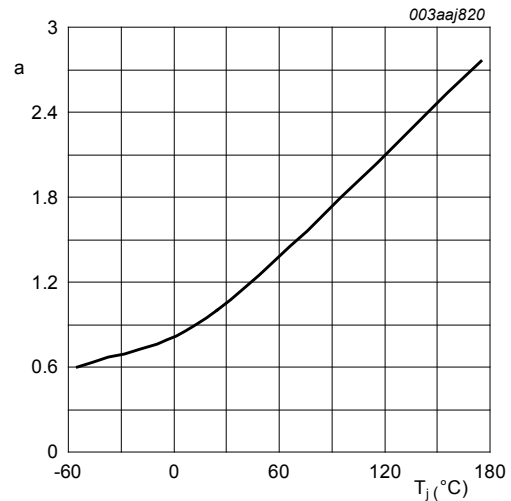


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^\circ\text{C})}$$

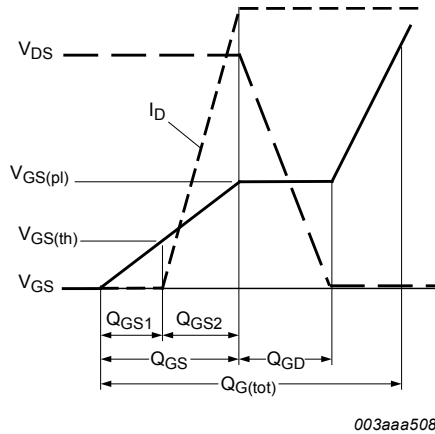


Fig. 14. Gate charge waveform definitions

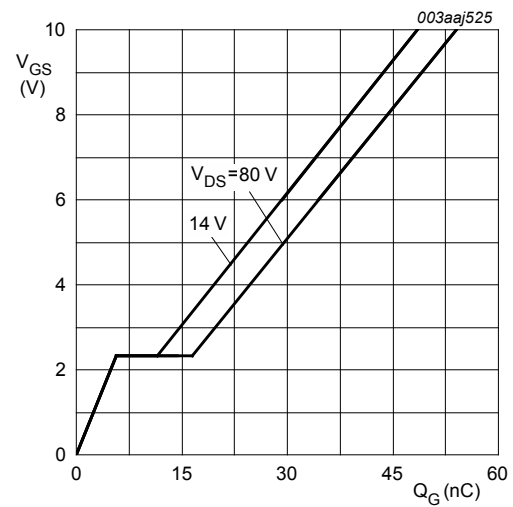


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^\circ\text{C}; I_D = 10\text{ A}$$

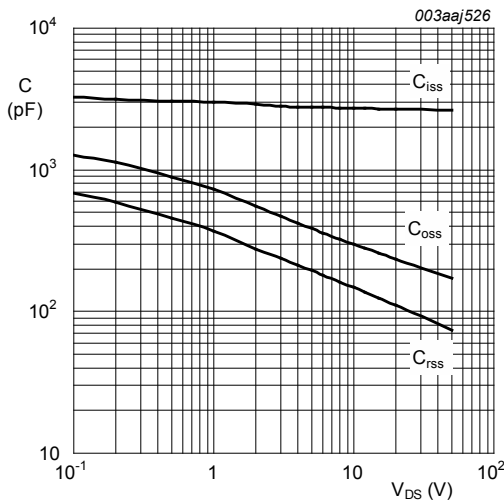


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$$

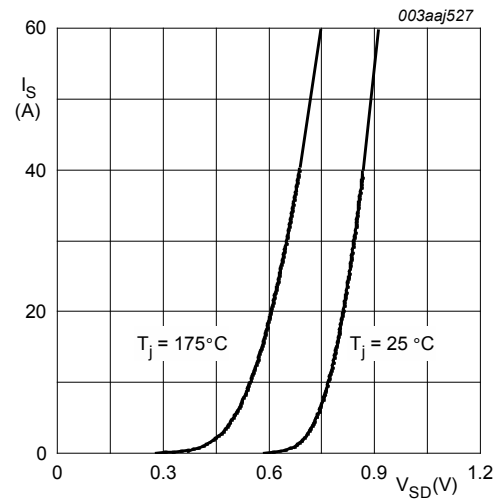
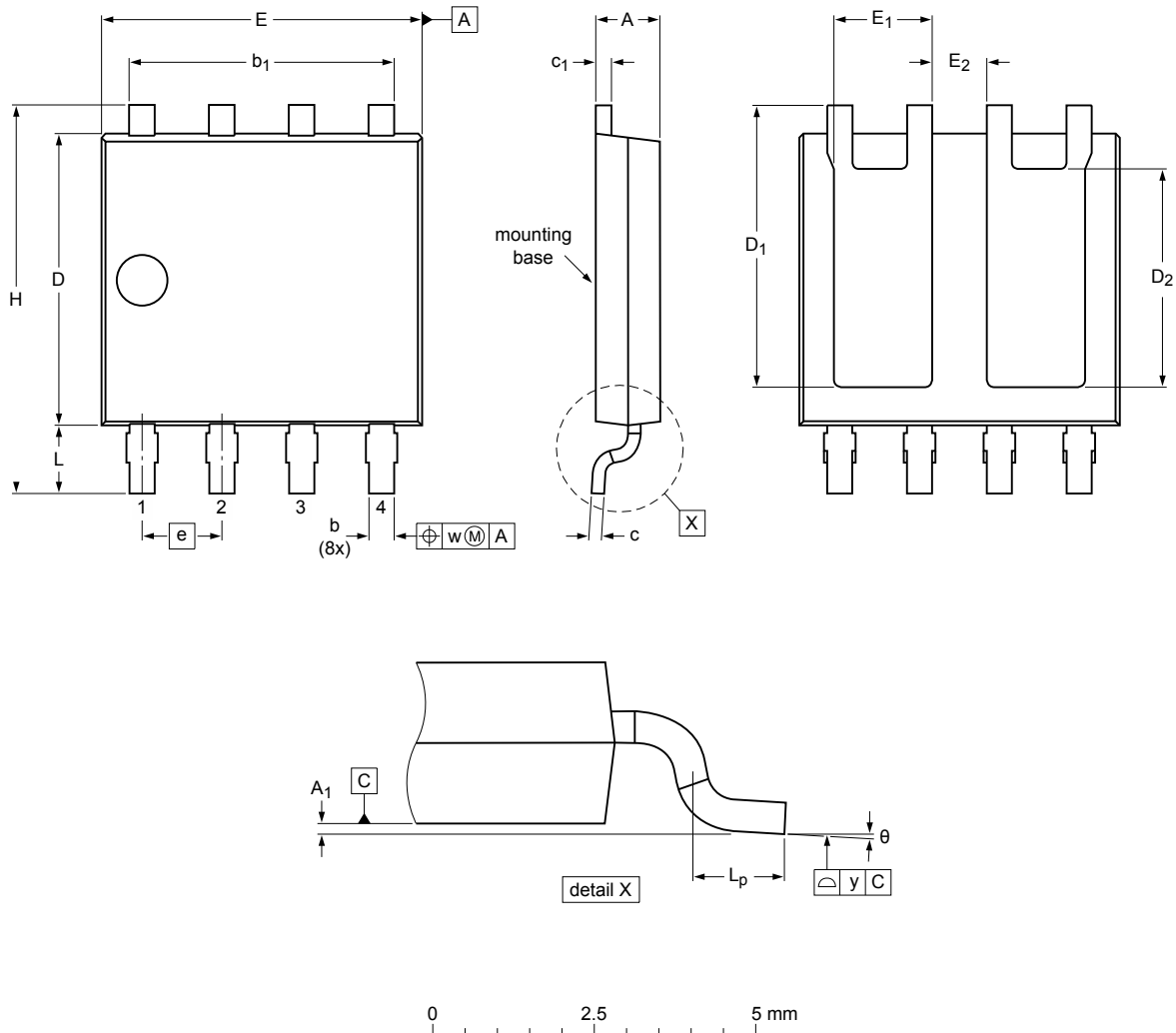


Fig. 17. Source current as a function of source-drain voltage; typical values

$$V_{GS} = 0\text{ V}$$

7. Package outline

Plastic single ended surface mounted package (LPAK56D); 8 leads SOT1205



Dimensions

Unit	A	A ₁	b	b ₁	c	c ₁	D ⁽¹⁾	D ₁ ⁽¹⁾	D ₂ ^(ref)	E ⁽¹⁾	E ₁ ⁽¹⁾	E ₂	e	H	L	L _p	w	y	θ
max	1.05	0.1	0.50	4.4	0.25	0.30	4.70	4.8	3.3	5.30	1.6	0.85		6.2	1.3	0.85			8°
nom													1.27				0.25	0.1	
min		0.0	0.35	4.1	0.19	0.24	4.45			4.95	1.5			5.9	0.8	0.40			0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot1205_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1205					11-12-07 12-02-28

Fig. 18. Package outline LPAK56D (SOT1205)

8. Legal information

8.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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