

Nutaq PicoDigitizer 250-Series

Wideband IQ Processor
PRODUCT SHEET



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Nutaq PicoDigitizer 250-Series

The PicoDigitizer 250-Series is a wideband IQ processor solution which combines the power of a large FPGA with high sampling speeds, while accelerating the development cycle by eliminating the need for hand-coding.

At the core is a Virtex-6 FPGA, which interfaces with a dual channel 250 MSPS A/D and dual channel 1 GSPS D/A.

A model-based development environment allows for rapid deployment and testing of algorithms without hand-coding of the FPGA.

To maximize the power and flexibility of this small table top solution, the PicoDigitizer 250-Series is available in a dual channel, dual channel embedded, or quad channel configuration.

Key Features

- Choose either one or two high speed dual channel processor nodes, each capable of processing up to 250 MHz of baseband signal
- 2 x 250 MSPS 14-bit A/D per dual channel processor node
- 2 x 1 GSPS 16-bit D/A per dual channel processor node
- One large Virtex-6 FPGA per dual channel processor node
- Optional Intel Quad-Core i7 (Available in the 1 x dual channel embedded configuration)
- 14 x high speed LVDS user I/Os per dual channel processor node
- One trigger input per dual channel processor node for event-based recording/playback
- One PPS input per node for a GPS-disciplined sampling clock
- GigE and PCIe 4x high speed interfaces

Configurations

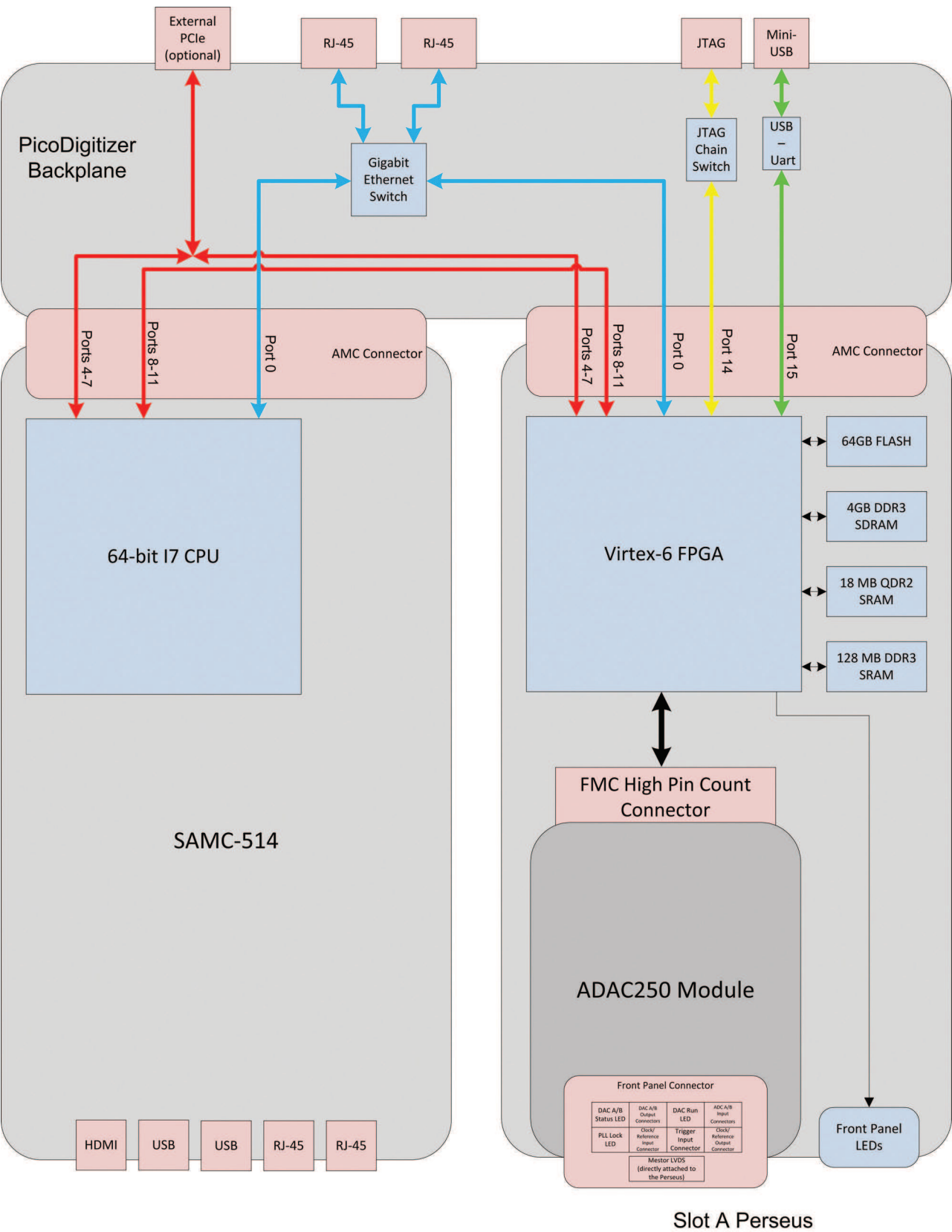
	PicoDigitizer 250-Series 1 x Dual Channel Processor Node	PicoDigitizer 250-Series 1 x Dual Channel Processor Node (Embedded)	PicoDigitizer 250-Series 2 x Dual Channel Processor Node
250 MHz Dual Channel Processor Nodes	1	1	2
A/D Converters	2	2	4
Maximum Input Sampling Frequency	250 MSPS	250 MSPS	250 MSPS
Input Resolution	14 bits	14 bits	14 bits
D/A Converters	2	2	4
Maximum Output Sampling Frequency	1 GSPS	1 GSPS	1 GSPS
Output Resolution	16 bits	16 bits	16 bits
FPGA*	1 x Virtex-6	1 x Virtex-6	2 x Virtex-6
Remote Host Interface	1x GigE 1x PCIe-4x	1x GigE Dual PCIe 4x (between embedded Intel Quad-Core i7 and Virtex-6) Or Single PCIe 4x (between embedded Intel Quad-Core i7 and Virtex-6) + Single PCIe 4x external	1x GigE 1x PCIe-4x
Embedded CPU	None	Intel Quad-Core i7- 2715QE	None
Embedded Storage **	N.A.	64 GB SSD +1x SATA external +1x 200 GB SATA internal (optional)	N.A.

* Virtex-6 options available: LX240T, LX550T, SX315T or SX475T

** 1x eSATA connection Rear PicoDigitizer panel, 1x SATA for internal 1.8" SSD Drive.

Sample Block Diagram

PicoDigitizer 250-Series: 1 x Dual Channel Processor Node, Embedded Version



Model-Based Design Flow

Rapid System Level FPGA Development in MATLAB and Xilinx System Generator for DSP

Built on top of Nutaq's board software development kit (BSDK), Nutaq's model-based design kit (MBDK) enables rapid design, simulation, testing, and deployment of applications from the Simulink graphical environment without requiring hand-coding in either VHDL or C.

Some of the benefits presented by Nutaq's model-based design approach include:

- A significant reduction in the time spent on low value-add tasks such as programming I/O interfaces, adjusting FPGA constraints, debugging drivers etc.
- Providing host co-simulation tools which enables:
 - o I/O integration within simulations
 - o Step-by-step FPGA fabric design migration
 - o Easy FPGA-to-host interaction
 - o Data logging
- Tools such as record/playback, host IO control and data streaming libraries.

FPGA Recording/Playback IP Core

The FPGA SDRAM recording/playback IP core enables storage and playback of very high speed multichannel bursts of data in the FPGA-attached SDRAM.

This data can then be transferred to a host device for storage and/or real-time analysis. It can also be loaded in memory for looped playback transmission over the high speed D/A converters.

The FPGA recording/playback IP core comes with standard trigger mechanisms (single shot, normal, and software defined). The trigger sources can either come from the host processor, a user-defined FPGA signal, or from the PicoDigitizer 250-Series trigger front panel input.

The user can define the number of channels to record/playback, as well as the acquisition rate, so that the available recording memory bandwidth is efficiently used. Note that FPGA pre/post-processing on the channels can be performed before recording or after playback, to potentially reduce recording/playback bandwidth needs.

- DDR3 FPGA memory size = 4 GB
- Maximum data throughput = 5.7 GBps

Application Example:

FPGA-based filtering on 2 channels sampled at 250 MSPS on the FPGA (decimation by 16), then recording of both channels. Each channel can be recorded for 64 seconds.

RTDEx (Real Time Data Exchange)

Nutaq's RTDEx IP core provides users with a framework to exchange data with a host device through either the GigE or PCIe links, yielding the highest bandwidth and lowest possible latency.

Built to complement our "snapshot" FPGA recording/playback capabilities, the RTDEx IP core provides a continuous data flow from the acquisition/transmission to the host computer, for further real-time computing or real-time PC recording/playback.

HOST - FPGA Streaming	GigE	PCIe 1x	PCIe 4x
Data BW	1 Gbps	2.5 Gbps	10 Gbps
Sustained Data Throughput	900 Mbps	1.5 Gbps	6 Gbps

Specifications

FPGA

Supports LX240T, LX550T, SX315T and SX475T FPGA devices
Supports GigE interface; Supports single PCIe (4x) non-embedded;
Supports up to 2 PCIe (4x) embedded;
4 GB SODIMM DDR3
18 MB QDR2 SRAM
64 MB NOR Flash
128 MB DDR3 SRAM (Dedicated to Nutaq Central Communication Engine and Microblaze Embedded Linux OS)

Embedded CPU Section

Intel Quad-Core i7 Gen2 CPU, 2.1 GHz processor
8 GB DDR3 SDRAM
64 GB SSD + 1 x SATA external + 1 x 200 GB internal (optional)
GigE & Dual PCIe 4x support
SATA -II/III support
Embedded throughput (FPGA-CPU) : 1x PCIe 4x - 6 Gbps

A/D Sampler Coupling

AC coupled
Single-ended

A/D Sampler Characteristics

14 bit
250 MSPS maximum
2 or 4 channels

A/D Sampler Coupling

AC coupled
Single-ended

A/D Sampler Characteristics

16 bit
1000 MSPS maximum
2 or 4 channels

Sampling Clock

Equipped with an onboard, low-jitter reference clock and synchronization PLL (AD9511)
Input PPS signal for GPS-disciplined on-board reference clock
Input External CLK or External Reference
Output CLK or Reference

A/D Performance

Analog input bandwidth: 470 MHz (-3dB)
SNR (dB): 70.5 (@ 30 MHz) , 70 (@ 70 MHz), 65 (@ 150 MHz)
SFDR (dBc): 75 (@ 30 MHz) , 85 (@ 70 MHz), 74 (@ 150 MHz)
THD (dBc): 74 (@ 30 MHz) , 84 (@ 70 MHz), 74 (@ 150 MHz)

A/D Performance

Analog output bandwidth : 500 MHz (1 GSPS DAC)
Phase Noise (1MHz; dBc/Hz): 125 (@ 30 MHz) , 122 (@ 70 MHz), 121 (@ 150 MHz)
2nd harmonic (dBc): 63 (@ 30 MHz) , 57 (@ 70 MHz), 54 (@ 150 MHz)
3rd harmonic (dBc): 69 (@ 30 MHz) , 61 (@ 70 MHz), 52 (@ 150 MHz)

Front Panel Connectors

Analog Inputs, CLK & Triggers (All PicoDigitizer 250-Series Models)

Each IQ Processor Node

- 2 x A/D MMCX inputs
- 2 x D/A MMCX outputs
- 1 x external trigger/PPS input
- 1 x external sampling or reference CLK input
- 1 x sampling or reference CLK output

Digital Inputs & Outputs (All PicoDigitizer 250-Series Models)

Each IQ Processor Node

- 1x VHDCI connector

VHDCI Connector Signal Map

- 14 x user LVDS I/O data
- 1 x LVDS clock

Additional Front Panel Connectors (PicoDigitizer 250-Series 1x Dual Channel Processor Node, Embedded Version Only)

- 1 x HDMI
- 2 x GigE
- 1 x Mini USB port
- 1 x COM-port
- 1 x USB 2.0 ports

Rear Panel Connectors

- 2 x GigE ports
- 1 x USB UART FPGA console port
- 1 x external universal power supply
- 1 x SATA (Embedded models only)
- 1 x PCIe 4x cable interface connector

Ordering Information

PicoDigitizer250-A-B-C-D-E

A (Dual Channel Processors)	0 = No Embedded CPU, 1 x Virtex-6 Dual Channel Processor	1 = Embedded CPU, 1 x Virtex-6 Dual Channel Processor	2 = No Embedded CPU, 2 x Virtex-6 Dual Channel Processors	
B (FPGA Option)	0 = LX240T	1 = LX550T	2 = SX315T	3= SX475T
C (Additional Embedded Storage)	0 = None	1 = 200 GB SSD (172 MBytes/s)		
D (External PCIe)	0 = No external PCIe	1 = PCIe 4x external link to FPGA		
E (Model-Based Design Software License)	0 = No external license	1 = 1x MBDK Workstation License)		

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2150 Cyrille-Duquet, Quebec City (Quebec) G1N 2G3 CANADA
T. 418-914-7484 | 1-855-914-7484 | F. 418-914-9477
info@nutaq.com