

# BLF7G24L-160P; BLF7G24LS-160P

Power LDMOS transistor

Rev. 4 — 25 July 2012

Product data sheet

## 1. Product profile

### 1.1 General description

160 W LDMOS power transistor for base station applications at frequencies from 2300 MHz to 2400 MHz.

**Table 1. Typical performance**

Typical RF performance at  $T_{case} = 25\text{ °C}$  in a common source class-AB production test circuit.

Test signal	f (MHz)	$I_{Dq}$ (mA)	$V_{DS}$ (V)	$P_{L(AV)}$ (W)	$G_p$ (dB)	$\eta_D$ (%)	ACPR <sub>885k</sub> (dBc)
IS-95	2300 to 2400	1200	28	30	18.5	27.5	-45.5 <sup>[1]</sup>

[1] Single carrier IS-95 with pilot, paging, sync and 6 traffic channels (Walsh codes 8 - 13). PAR = 9.7 dB at 0.01 % probability on the CCDF. Channel bandwidth is 1.2288 MHz.

### 1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low  $R_{th}$  providing excellent thermal stability
- Designed for broadband operation (2300 MHz to 2400 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

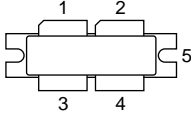
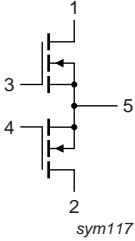
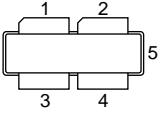
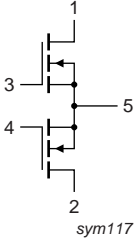
### 1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 2300 MHz to 2400 MHz frequency range



## 2. Pinning information

**Table 2. Pinning**

Pin	Description	Simplified outline	Graphic symbol
<b>BLF7G24L-160P (SOT539A)</b>			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source		
<b>BLF7G24LS-160P (SOT539B)</b>			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source		

[1] Connected to flange.

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
BLF7G24L-160P	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF7G24LS-160P	-	earless flanged balanced ceramic package; 4 leads	SOT539B

## 4. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-0.5	+13	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	200	°C

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}$ ; $P_L = 30\text{ W}$ ; $V_{DS} = 28\text{ V}$ ; $I_{Dq} = 1200\text{ mA}$	0.2	K/W

## 6. Characteristics

**Table 6. Characteristics**

$T_j = 25\text{ °C}$  per section, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ ; $I_D = 1\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$ ; $I_D = 102\text{ mA}$	1.5	1.9	2.3	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 28\text{ V}$	-	-	2.8	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$ ; $V_{DS} = 10\text{ V}$	-	19	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}$ ; $V_{DS} = 0\text{ V}$	-	-	280	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}$ ; $I_D = 3.57\text{ A}$	-	6.9	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$ ; $I_D = 3.57\text{ A}$	-	0.15	0.23	$\Omega$

## 7. Test information

**Remark:** All testing performed in a class-AB production test circuit.

**Table 7. Functional test information**

Test signal: single carrier IS-95 with pilot, paging, sync and 6 traffic channels (Walsh codes 8 - 13). PAR = 9.7 dB at 0.01 % probability on the CCDF, channel bandwidth is 1.2288 MHz;  $f_1 = 2300\text{ MHz}$ ;  $f_2 = 2400\text{ MHz}$ ; RF performance at  $V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 1200\text{ mA}$ ;  $T_{case} = 25\text{ °C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_{L(AV)} = 30\text{ W}$	17.8	18.5	-	dB
$RL_{in}$	input return loss	$P_{L(AV)} = 30\text{ W}$	-	-13.5	-9	dB
$\eta_D$	drain efficiency	$P_{L(AV)} = 30\text{ W}$	25	27.5	-	%
$ACPR_{885k}$	adjacent channel power ratio (885 kHz)	$P_{L(AV)} = 30\text{ W}$	-	-45.5	-41.5	dBc

### 7.1 Ruggedness in class-AB operation

The BLF7G24L-160P and BLF7G24LS-160P are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 1200\text{ mA}$ ;  $P_L = 160\text{ W}$ ;  $f = 2300\text{ MHz}$ .

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data. Typical values per section.  
 $I_{Dq} = 600 \text{ mA}$ ; main transistor  $V_{DS} = 28 \text{ V}$ .  $Z_S$  and  $Z_L$  defined in Figure 1.

f (MHz)	$Z_S$ ( $\Omega$ )	$Z_L$ ( $\Omega$ )
2300	$2.5 - j5.9$	$3.1 - j4.3$
2400	$4.6 - j7.2$	$2.9 - j4.2$

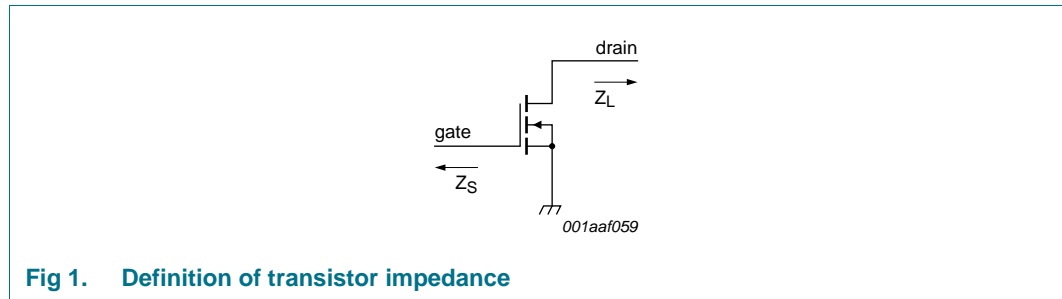
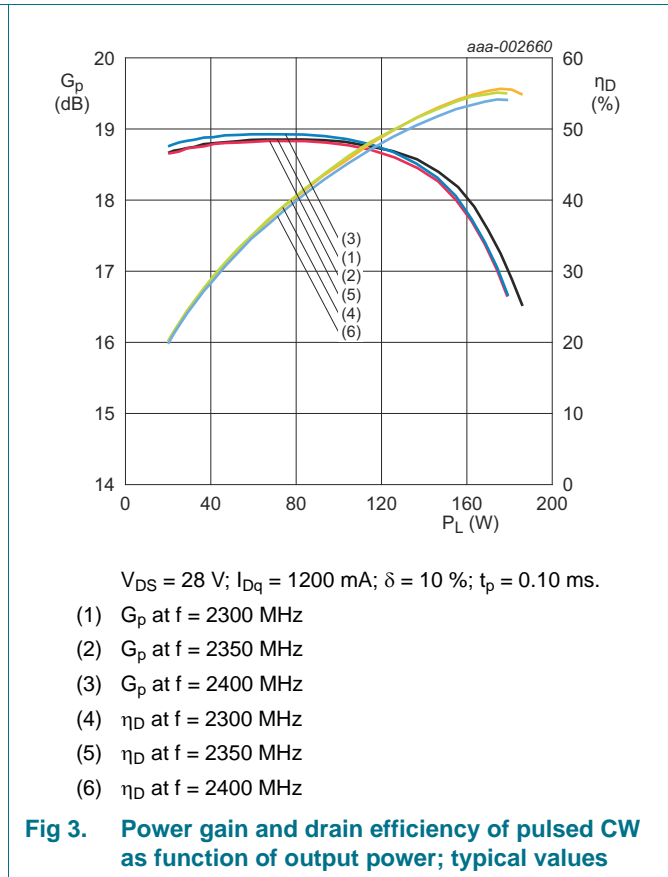
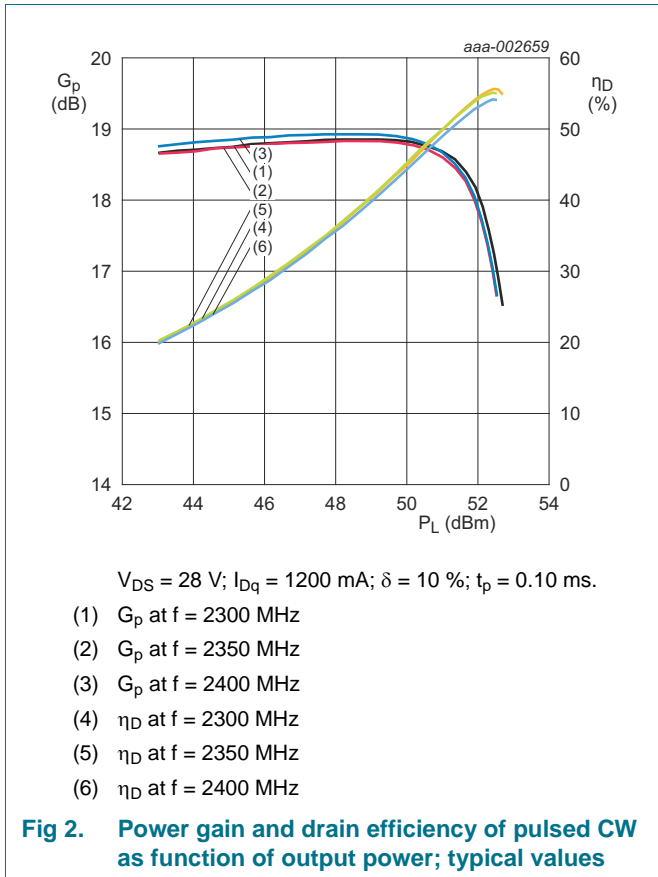
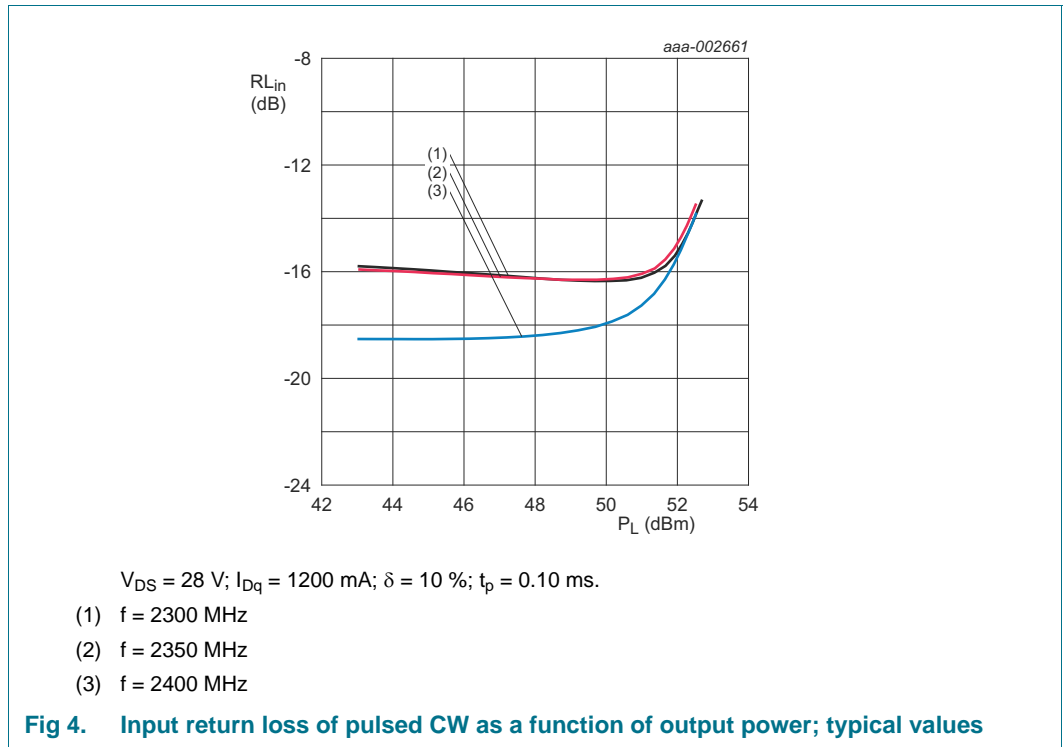


Fig 1. Definition of transistor impedance

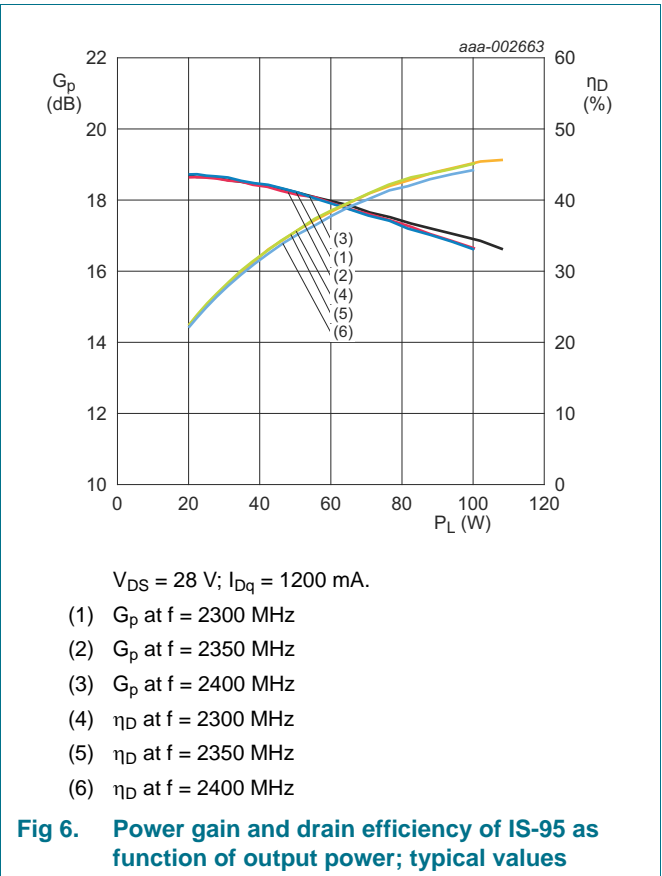
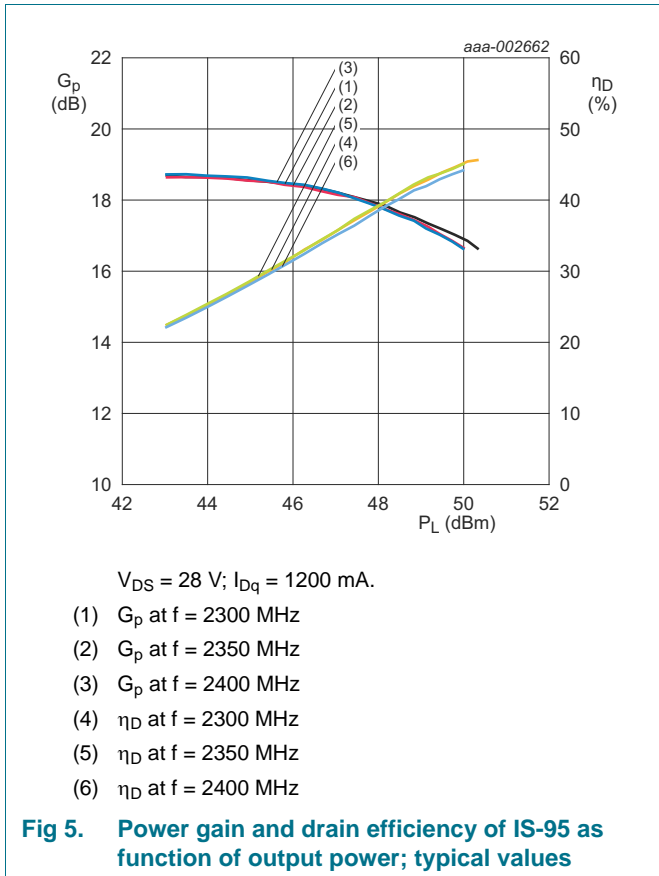
7.3 Graphs

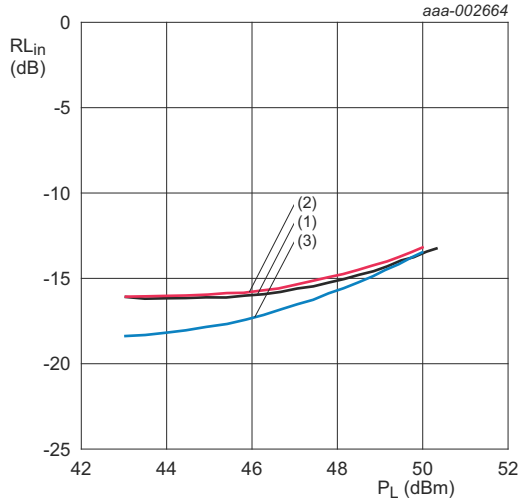
7.3.1 Pulsed CW





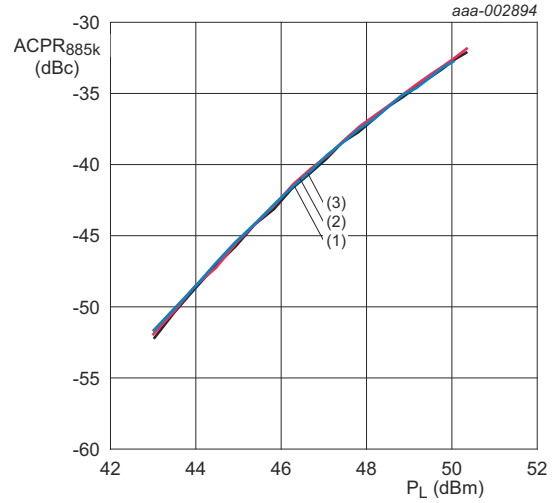
7.3.2 IS-95





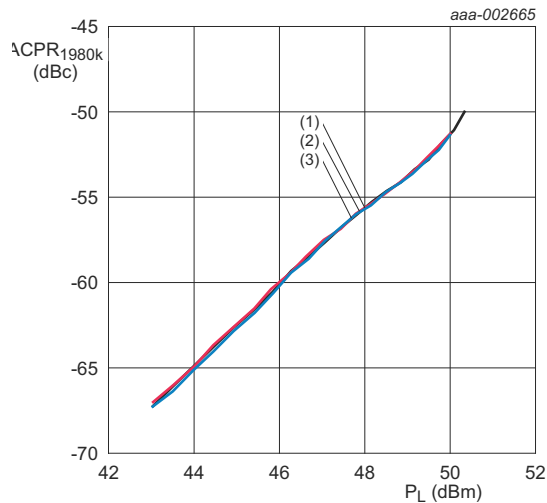
$V_{DS} = 28\text{ V}; I_{Dq} = 1200\text{ mA}.$   
 (1)  $f = 2300\text{ MHz}$   
 (2)  $f = 2350\text{ MHz}$   
 (3)  $f = 2400\text{ MHz}$

**Fig 7. Input return loss of IS-95 as a function of output power; typical values**



$V_{DS} = 28\text{ V}; I_{Dq} = 1200\text{ mA}.$   
 (1)  $f = 2300\text{ MHz}$   
 (2)  $f = 2350\text{ MHz}$   
 (3)  $f = 2400\text{ MHz}$

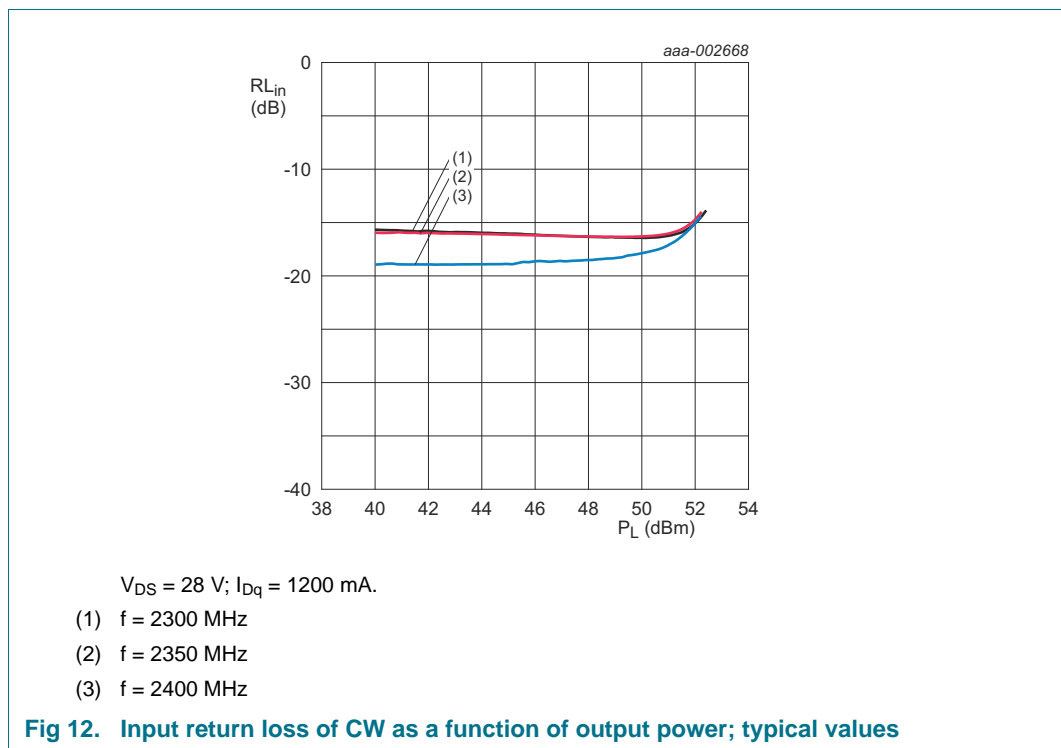
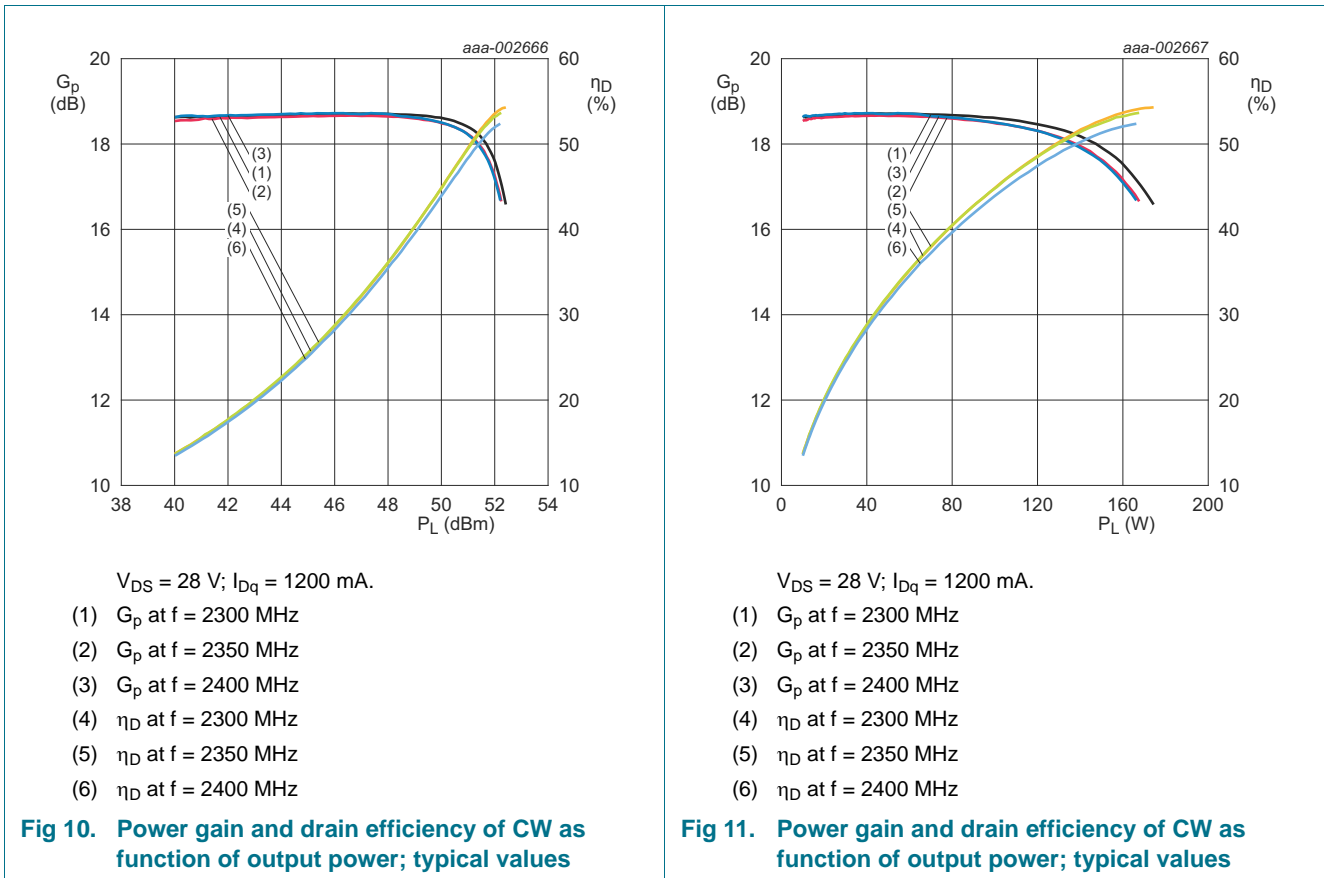
**Fig 8. Adjacent channel power ratio (885 kHz) of IS-95 as a function of output power; typical values**



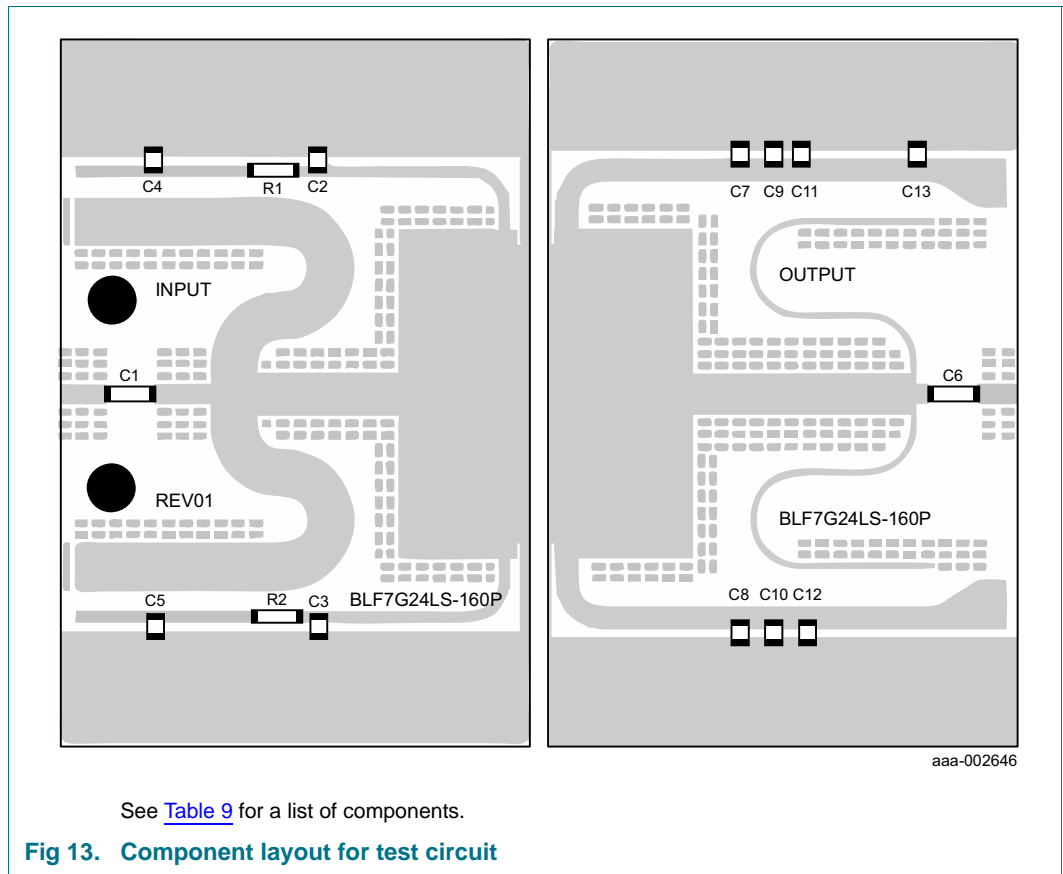
$V_{DS} = 28\text{ V}; I_{Dq} = 1200\text{ mA}.$   
 (1)  $f = 2300\text{ MHz}$   
 (2)  $f = 2350\text{ MHz}$   
 (3)  $f = 2400\text{ MHz}$

**Fig 9. Adjacent channel power ratio (1980 kHz) of IS-95 as a function of output power; typical values**

7.3.3 CW



7.4 Test circuit



**Table 9. List of components**

For test circuit, see [Figure 13](#).

Component	Description	Value	Remarks
C1, C6	multilayer ceramic chip capacitor	7.5 pF	[1]
C2, C3, C7, C8	multilayer ceramic chip capacitor	16 pF	[2]
C4, C5, C9, C10	multilayer ceramic chip capacitor	20 nF	[1]
C11, C12	multilayer ceramic chip capacitor	10 $\mu$ F	[3]
C13	electrolytic capacitor	220 $\mu$ F; 63 V	
R1, R2	chip resistor	2 $\Omega$ ; SMD 805	

[1] American technical ceramics type 100B or capacitor of same quality.

[2] American technical ceramics type 100A or capacitor of same quality.

[3] TDK or capacitor of same quality.

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads

SOT539A

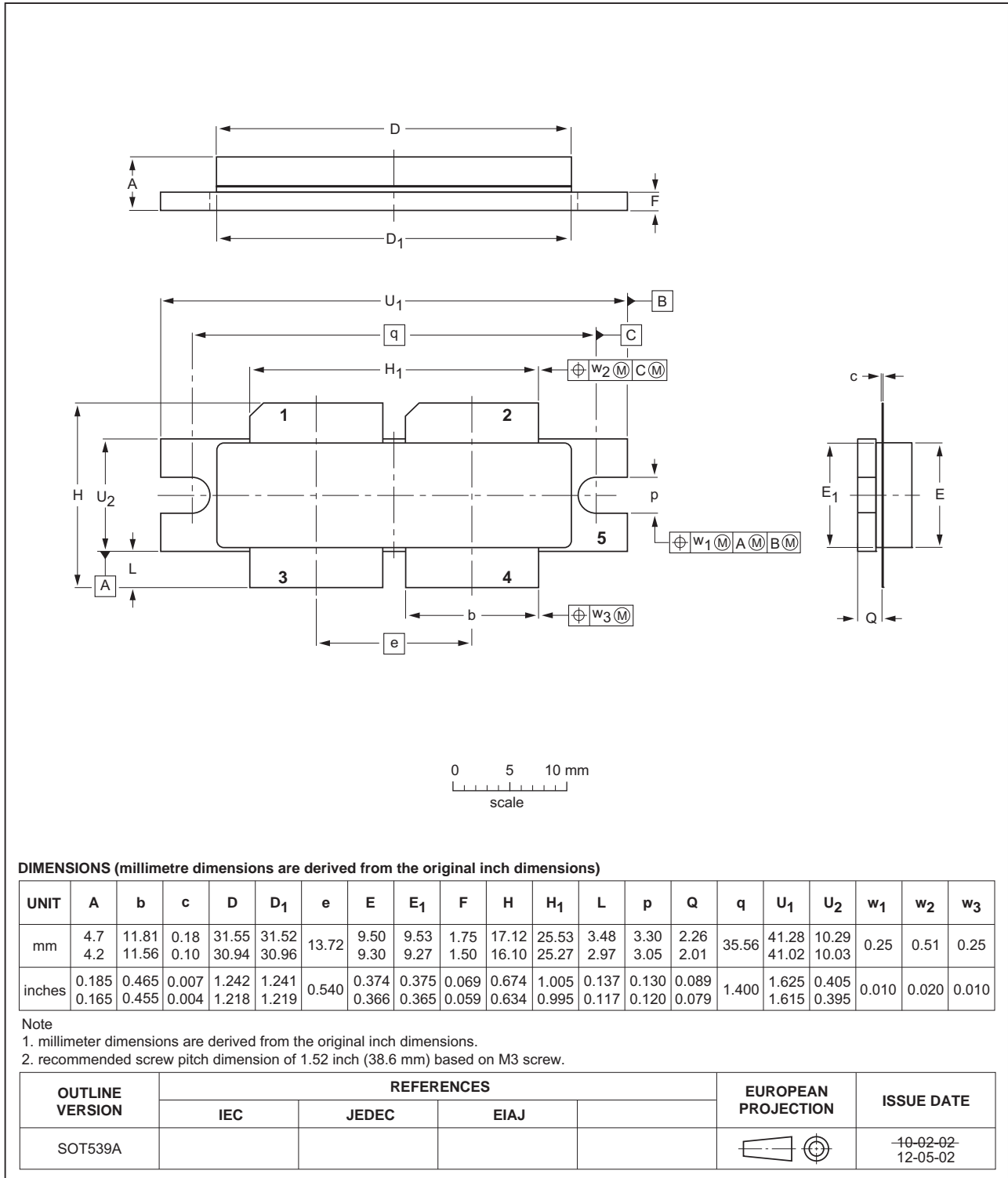


Fig 14. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads

SOT539B

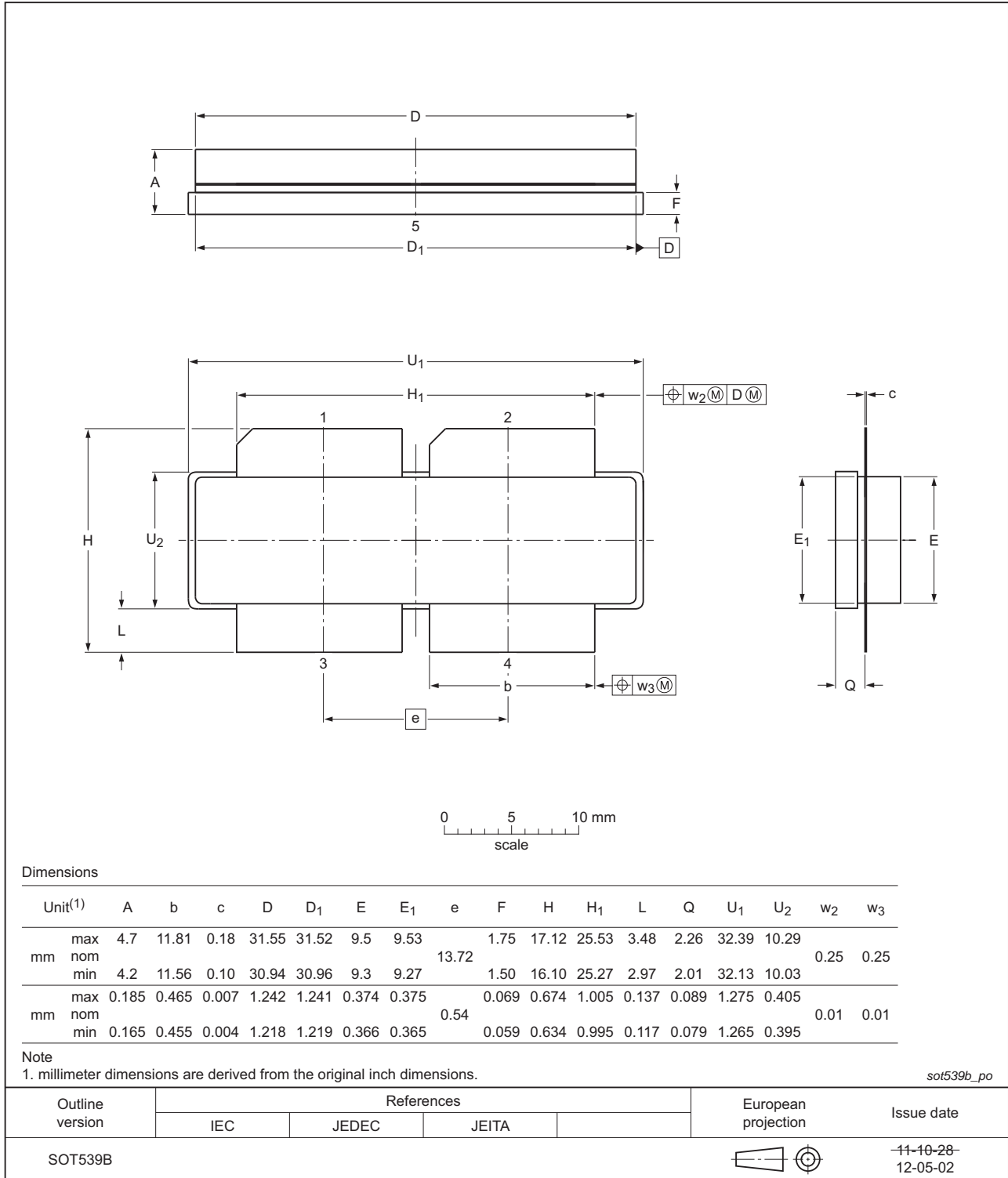


Fig 15. Package outline SOT539B

## 9. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CCDF	Complementary Cumulative Distribution Function
IS-95	Interim Standard 95
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
PAR	Peak-to-Average Ratio
RF	Radio Frequency
VSWR	Voltage Standing Wave Ratio

## 10. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF7G24L-160P_7G24LS-160P v.4	20120725	Product data sheet	-	BLF7G24L-160P_7G24LS-160P v.3
Modifications:		<ul style="list-style-type: none"> <li>The status of this document has been changed to Product data sheet</li> <li><a href="#">Table 6 on page 3</a>: added max. value <math>R_{DS(on)}</math>.</li> <li><a href="#">Table 7 on page 3</a>: modified max. value of <math>RL_{in}</math>.</li> </ul>		
BLF7G24L-160P_7G24LS-160P v.3	20120420	Preliminary data sheet	-	BLF7G24L-160P_7G24LS-160P v.2
BLF7G24L-160P_7G24LS-160P v.2	20120301	Objective data sheet	-	BLF7G24L-160P_7G24LS-160P v.1
BLF7G24L-160P_7G24LS-160P v.1	20120210	Objective data sheet	-	-

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
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