BLF6G22L-40BN

Power LDMOS transistor

Rev. 1 — 30 August 2010 Product data sheet

1. Product profile

1.1 General description

40 W LDMOS power transistor for base station applications at frequencies from 2000 MHz to 2200 MHz.

Table 1. Typical performance

RF performance at T_{case} = 25 °C in a common source class-AB production test circuit.

Mode of operation	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	2110 to 2170	28	2.5	19	16	–50[1]

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF per carrier; carrier spacing 5 MHz

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features and benefits

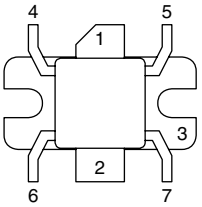
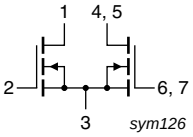
- Typical 2-carrier W-CDMA performance at frequencies of 2110 MHz and 2170 MHz, a supply voltage of 28 V and an I_{Dq} of 345 mA:
  - Average output power = 2.5 W
  - Power gain = 19 dB (typ)
  - Efficiency = 16 %
  - ACPR = –50 dBc
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (2000 MHz to 2200 MHz)
- Internally matched for ease of use
- Integrated current sense
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 2000 MHz to 2200 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source [1]		
4, 5	sense drain		
6, 7	sense gate		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF6G22L-40BN	-	flanged ceramic package; 2 mounting holes; 6 leads	SOT1112A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
$V_{GS(sense)}$	sense gate-source voltage		–0.5	+9	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 12.5 W (CW)	1.7	K/W

6. Characteristics

Table 6. Characteristics

T_j = 25 °C per section; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.5 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 59 mA	1.4	1.9	2.4	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.5	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	8.8	10	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	150	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 2.9 A	-	4.3	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 2.1 A	-	0.25	-	Ω
I_{Dq}	quiescent drain current	main transistor: V_{DS} = 28 V sense transistor: I_{DS} = 7.43mA; V_{DS} = 26.7 V	310	345	380	mA

7. Test information

Table 7. Application information

Mode of operation: 2-carrier W-CDMA; PAR 8.4 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1 to 64 PDPCH; f_1 = 2112.5 MHz; f_2 = 2117.5 MHz; f_3 = 2162.5 MHz; f_4 = 2167.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 345 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit

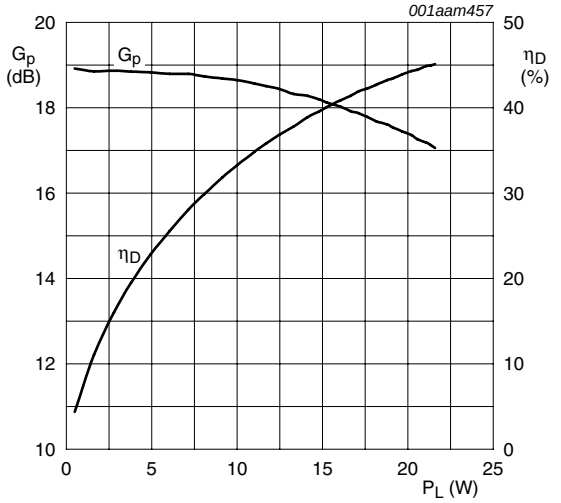
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 2.5 W		17.8	19	21.0	dB
η_D	drain efficiency	$P_{L(AV)}$ = 2.5 W		13	16	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 2.5 W		–57	–50	–45	dBc
PAR_O	output peak-to-average ratio	$P_{L(AV)}$ = 20 W	[1]	3.6	4.0	4.8	dB

[1] Mode of operation: 1-carrier W-CDMA; PAR 7.2 dB at 0.01 % probability on CCDF; f = 2167.5 MHz.

7.1 Ruggedness in class-AB operation

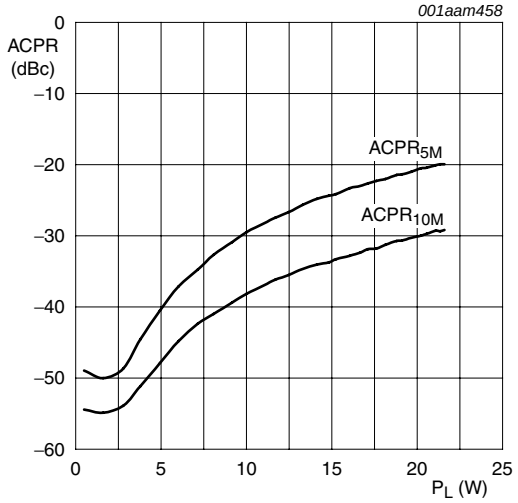
The BLF6G22L-40BN is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 345 mA; P_L = 40 W (CW); f = 2140 MHz.

7.2 2-Carrier W-CDMA with 5 MHz carrier spacing



V_{DS} = 28 V; I_{Dq} = 345 mA; f = 2140 MHz.

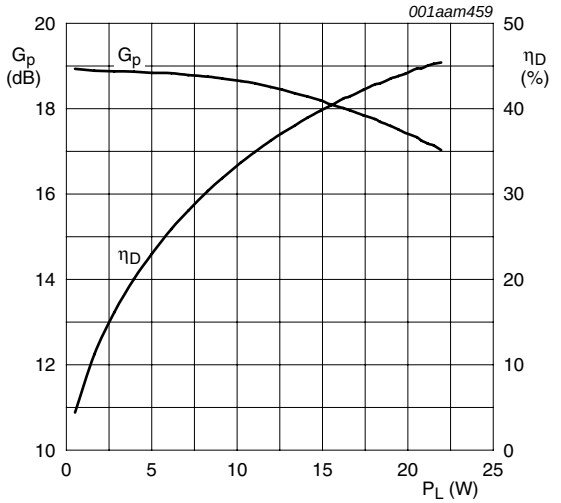
Fig 1. Power gain and drain efficiency as function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 345 mA; f = 2140 MHz.

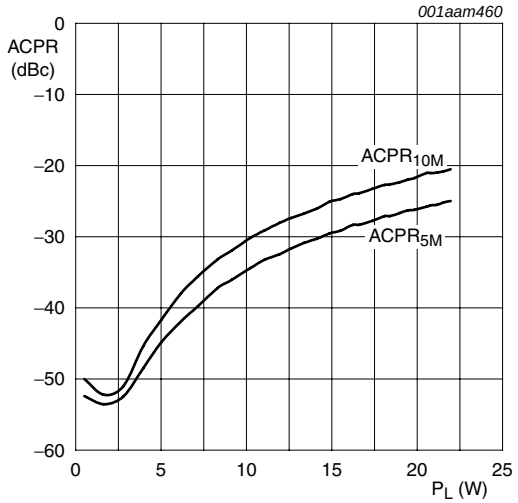
Fig 2. ACPR at 5 MHz and at 10 MHz as function of load power; typical values

7.3 2-Carrier W-CDMA with 10 MHz carrier spacing



V_{DS} = 28 V; I_{Dq} = 345 mA; f = 2140 MHz.

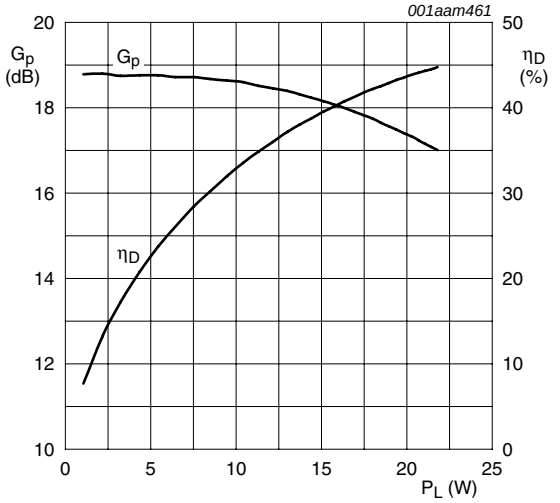
Fig 3. Power gain and drain efficiency as function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 345 mA; f = 2140 MHz.

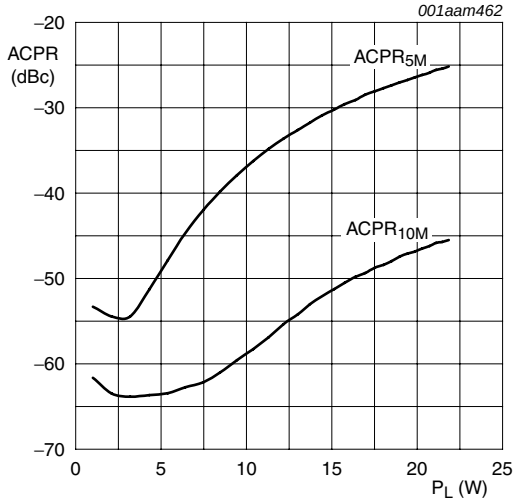
Fig 4. ACPR at 5 MHz and at 10 MHz as function of load power; typical values

7.4 1-Carrier W-CDMA



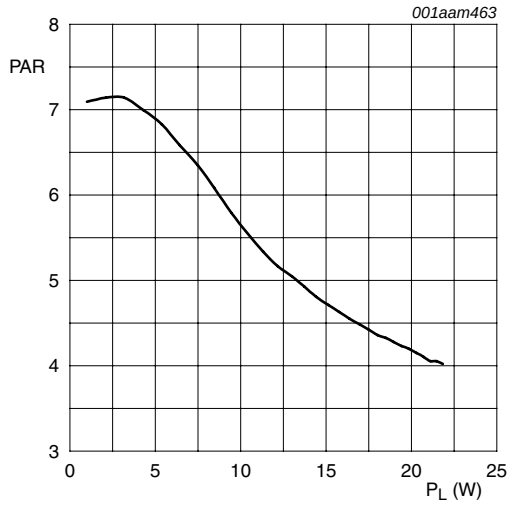
V_{DS} = 28 V; I_{Dq} = 345 mA; f = 2140 MHz.

Fig 5. Power gain and drain efficiency as function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 345 mA; f = 2140 MHz.

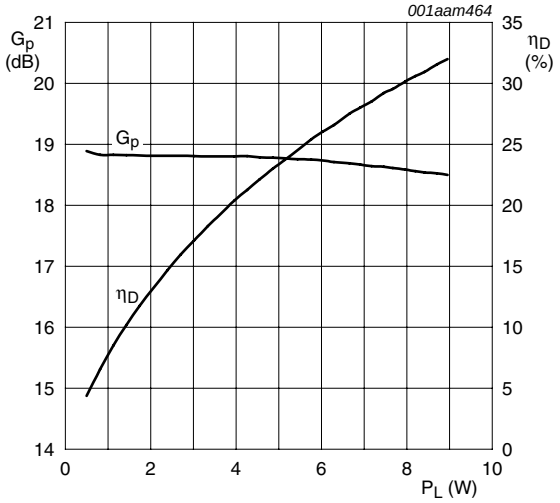
Fig 6. ACPR at 5 MHz and at 10 MHz as function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 345 mA; f = 2140 MHz.

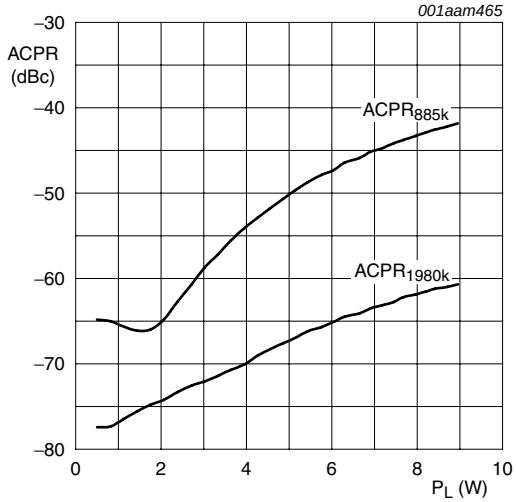
Fig 7. Peak-to-average power ratio as a function of load power; typical values

7.5 1-Carrier IS-95



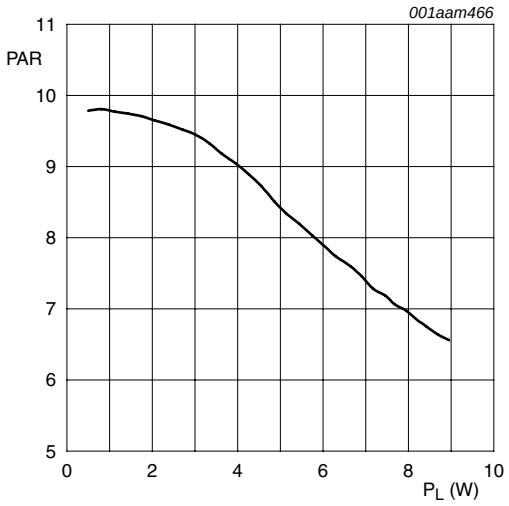
V_{DS} = 28 V; I_{Dq} = 345 mA; f = 2140 MHz.

Fig 8. Power gain and drain efficiency as function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 345 mA; f = 2140 MHz.

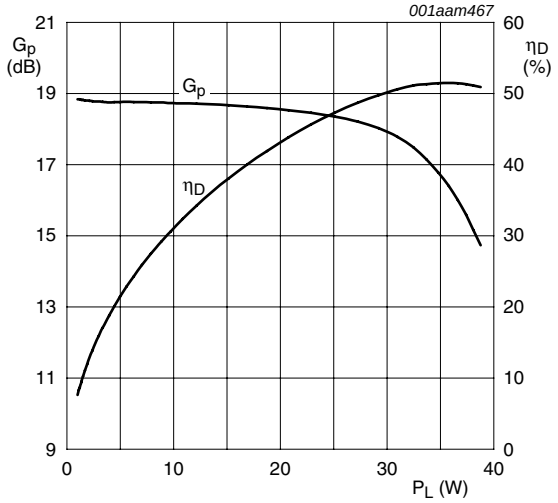
Fig 9. ACPR at 885 kHz and at 1980 kHz as function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 345 mA; f = 2140 MHz.

Fig 10. Peak-to-average power ratio as a function of load power; typical values

7.6 1-Tone CW



V_{DS} = 28 V; I_{Dq} = 345 mA; f = 2140 MHz.

Fig 11. Power gain and drain efficiency as function of load power; typical values

7.7 Test circuit

Table 8. List of components

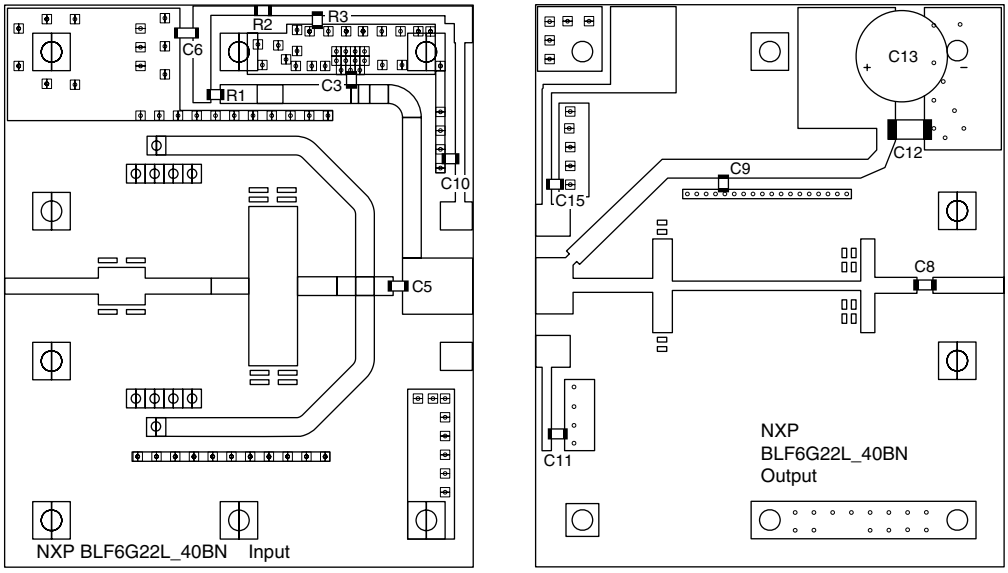
For test circuit see Figure 12.

Component	Description	Value		Remarks
C3, C8, C9	multilayer ceramic chip capacitor	33 pF	[1]	
C5	multilayer ceramic chip capacitor	1.0 pF	[1]	
C6	multilayer ceramic chip capacitor	100 nF	[2]	
C10	multilayer ceramic chip capacitor	33 pF	[3]	
C11, C15	multilayer ceramic chip capacitor	47 pF	[3]	
C12	multilayer ceramic chip capacitor	10 μF	[2]	
C13	electrolytic capacitor	470 μF; 63 V		
R1	SMD resistor	10 Ω		Philips 0603
R2	SMD resistor	820 Ω		Philips 0603
R3	SMD resistor	1.8 kΩ		Philips 0603

[1] American Technical Ceramics type 800B or capacitor of same quality.

[2] TDK or capacitor of same quality.

[3] American Technical Ceramics type 100A or capacitor of same quality.



Printed-Circuit Board (PCB): Taconic RF-35A; ε_r = 3.5 F/m; thickness = 0.765 mm; thickness copper plating = 35 μm.

See Table 8 for a list of components.

Fig 12. Component layout for class-AB production test circuit

7.8 Impedance information

Table 9. Typical impedance

Typical values valid for both section in parallel unless otherwise specified.

f	Z_S	Z_L
(MHz)	(Ω)	(Ω)
2050	3.3 – j12.2	13 – j11.2
2140	4.5 – j12.8	12.2 – j6.9
2230	10 – j15.3	13.3 – j5.5

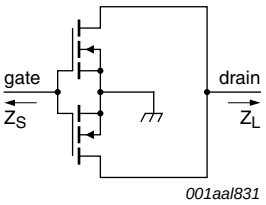
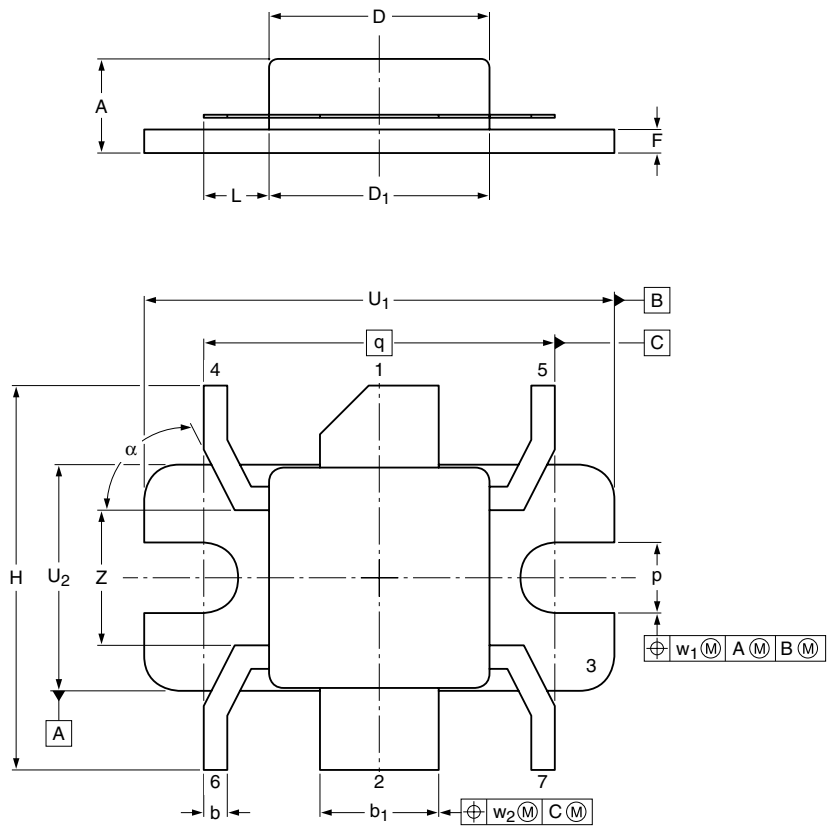


Fig 13. Definition of transistor impedance

8. Package outline

Flanged ceramic package; 2 mounting holes; 6 leads **SOT1112A**



Dimensions

Unit[1]		A	b	b_1	c	D	D_1	E	E_1	F	H	L	p	Q[2]	q	U_1	U_2	w_1	w_2	Z	α
mm	max	4.65	1.14	5.26	0.18	9.65	9.65	9.65	9.65	1.14	17.12	3.00	3.30	1.70		20.45	9.91			5.97	64°
	nom														15.24			0.25	0.51		
	min	3.76	0.89	5.00	0.10	9.40	9.40	9.40	9.40	0.89	16.10	2.69	2.92	1.45		20.19	9.65			5.72	62°
inches	max	0.183	0.045	0.207	0.007	0.38	0.38	0.38	0.38	0.045	0.674	0.118	0.130	0.067		0.805	0.39			0.235	64°
	nom														0.6			0.01	0.02		
	min	0.148	0.035	0.197	0.004	0.37	0.37	0.37	0.37	0.035	0.634	0.106	0.115	0.057		0.795	0.38			0.225	62°

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1112a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1112A						~~09-10-12~~ 10-02-02

Fig 14. Package outline SOT1112A

9. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Waveform
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
IMD	InterModulation Distortion
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
PAR	Peak-to-Average power Ratio
PDPCH	transmission Power of the Dedicated Physical CHannel
RF	Radio Frequency
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

10. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF6G22L-40BN v.1	20100830	Product data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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13. Contents

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