BLF6G15L-250PBRN

Power LDMOS transistor

Rev. 2 — 3 November 2010 | Product data sheet

1. Product profile

1.1 General description

250 W LDMOS power transistor for base station applications at frequencies from 1450 MHz to 1550 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a class-AB production test circuit.

Mode of operation	f (MHz)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR (dBc)
2C-WCDMA	1476 to 1511	28	60	18.5	33.0	–32[1]

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF per carrier. Carrier spacing 5 MHz.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features and benefits

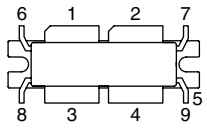
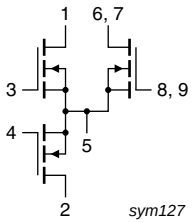
- Typical 2C-WCDMA performance at frequencies of 1476 MHz and 1511 MHz, a supply voltage of 28 V and an I_{Dq} of 1410 mA:
  - Average output power = 60 W
  - Power gain = 18.5 dB
  - Efficiency = 33.0 %
  - ACPR = –32 dBc
- Easy power control
- Integrated ESD protection
- Enhanced ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1450 MHz to 1550 MHz)
- Internally matched for ease of use
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC
- Integrated current sense

1.3 Applications

- RF power amplifiers for GSM, GSM EDGE, CDMA and W-CDMA and multi carrier applications in the 1450 MHz to 1550 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		
6, 7	sense drain		
8, 9	sense gate		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF6G15L-250PBRN	-	flanged LDMOST ceramic package; 2 mounting holes; 8 leads	SOT1110A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+11	V
I_D	drain current		-	64	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 60 W (CW)	0.29	K/W

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6. Characteristics

Table 6. Characteristics

T_j = 25 °C per section; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.8 mA	65	75	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 180 mA	1.4	1.9	2.4	V
I_{Dq}	quiescent drain current	sense transistor: I_{DS}= 20.1 mA; V_{DS} = 12 V main transistor: V_{DS} = 28 V	1.31	1.41	1.51	A
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	25.3	29	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 9 A	8.1	11.3	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 6.3 A	0.03	0.1	0.16	Ω

7. Application information

Table 7. RF performance

Mode of operation: 2-carrier W-CDMA; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 64 DPCH; f_1 = 1473.4 MHz; f_2 = 1478.4 MHz; f_3 = 1508.4 MHz; f_4 = 1513.4 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 1410 mA; T_{case} = 25 °C; unless otherwise specified in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(AV)}$	average output power		-	60	-	W
G_p	power gain	$P_{L(AV)}$ = 60 W	16.5	18.5	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 60 W	8	12	-	dB
η_D	drain efficiency	$P_{L(AV)}$ = 60 W	30	33	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 60 W	-	–32	–27	dBc

Table 8. PAR performance

Mode of operation; 1-carrier W-CDMA; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 64 DPCH; f_1 = 1510.9 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 1410 mA; T_{case} = 25 °C; unless otherwise specified in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR_O	output peak-to-average ratio	$P_{L(AV)}$ = 120 W at 0.01 % probability on CCDF	3.4	4.2	-	dB

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Table 9. Phase binning

Off state S_{11} measurement; V_{DS} = 28 V; V_{GS} = 0 V

Marking code	Input Resonance Frequency (GHz)	
	Min	Max
1	1.85	1.89
2	1.89	1.93
3	1.93	1.97

Table 10. Gain binning

Mode of operation: 2-carrier W-CDMA; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 64 DPCH; f_1 = 1473.4 MHz, f_2 = 1478.4 MHz; $P_{L(AV)}$ = 60 W; V_{DS} = 28 V; I_{Dq} = 1410 mA

Marking code	Gain at a center frequency of 1475.9 MHz in dB	
	Min	Max
BT	17.0	17.5
BU	17.5	18.0
BW	18.0	18.5
BX	18.5	19.0

7.1 Ruggedness in class-AB operation

The BLF6G15L-250PBRN is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 1410 mA; P_L = 200 W; f = 1475 MHz.

7.2 Impedance information

Table 11. Typical impedance per section

I_{Dq} = 950 mA; main transistor V_{DS} = 28 V

f (MHz)	Z_S[1] (Ω)	Z_L[1] (Ω)
1480	1.1 – j2.8	2.3 – j3.2
1510	1.3 – j2.8	2.1 – j2.8

[1] Z_S and Z_L defined in Figure 1.

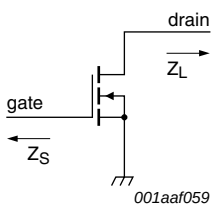

Fig 1. Definition of transistor impedance

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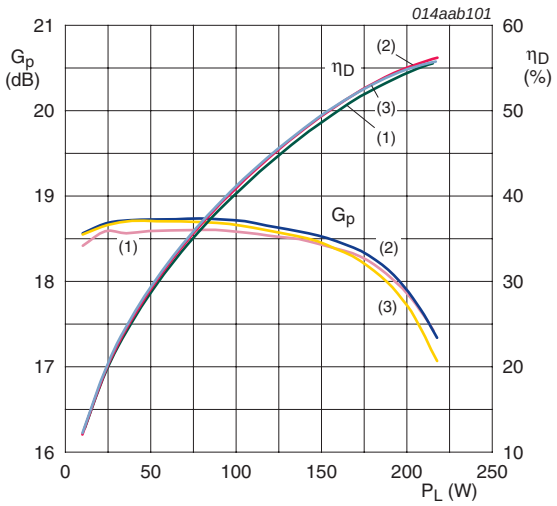
7.3 Graphs

7.3.1 CW

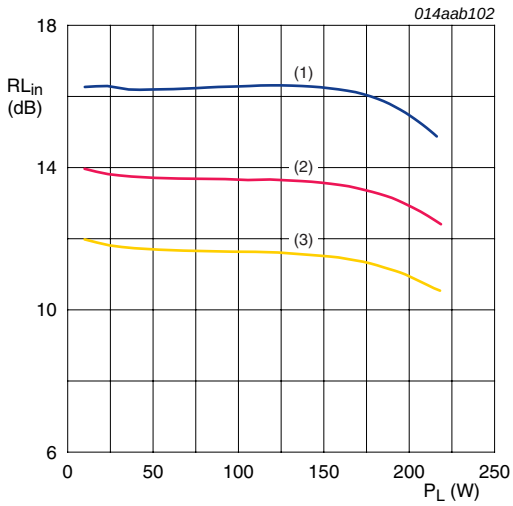


(1) f = 1475 MHz

(2) f = 1493 MHz

(3) f = 1511 MHz

Fig 2. Power gain and drain efficiency as function of output power; typical values



(1) f = 1475 MHz

(2) f = 1493 MHz

(3) f = 1511 MHz

Fig 3. Input return loss as a function of output power; typical values

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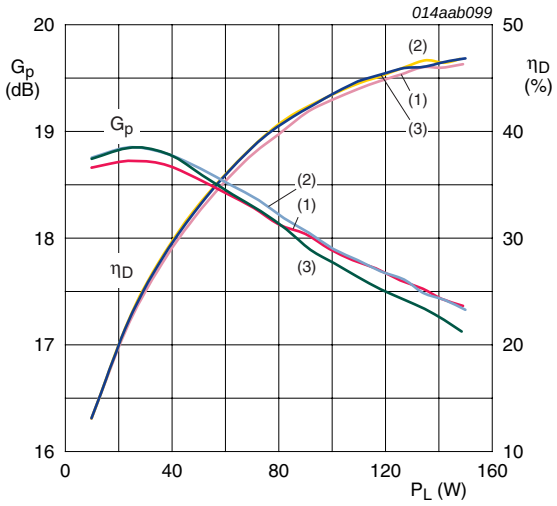
7.3.2 IS-95



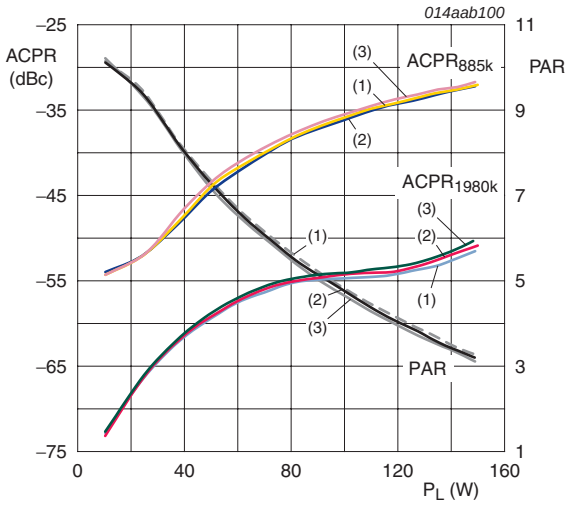
IS-95: PAR = 9.8 dB at 0.01 % probability of the CCDF.

(1) f = 1475 MHz

(2) f = 1493 MHz

(3) f = 1511 MHz

Fig 4. Power gain and drain efficiency as function of output power; typical values



IS-95: PAR = 9.8 dB at 0.01 % probability of the CCDF.

(1) f = 1475 MHz

(2) f = 1493 MHz

(3) f = 1511 MHz

Fig 5. Adjacent channel power ratio and peak-to-average power ratio as function of output power; typical values

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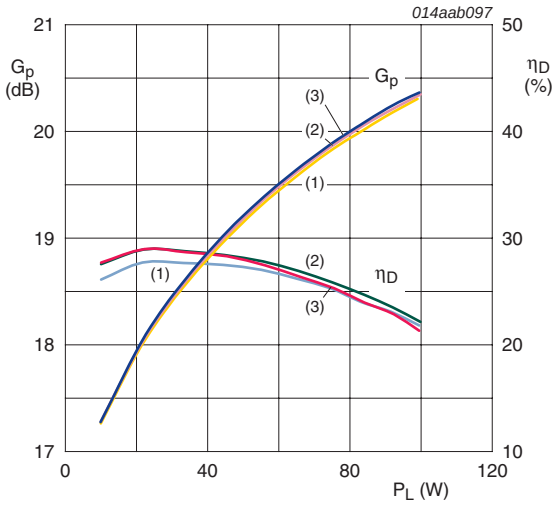
7.3.3 2C-WCDMA (5 MHz spacing)



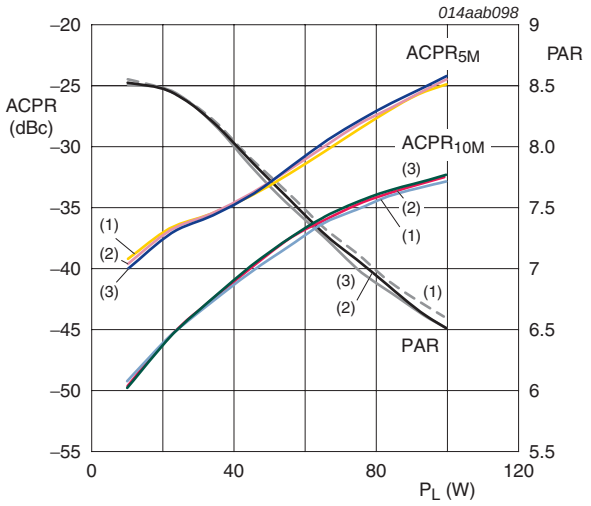
3GPP: Test Model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability per carrier; 5 MHz carrier spacing.

(1) f = 1475 MHz

(2) f = 1493 MHz

(3) f = 1511 MHz

Fig 6. Power gain and drain efficiency as function of output power; typical values



3GPP: Test Model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability per carrier; 5 MHz carrier spacing.

(1) f = 1475 MHz

(2) f = 1493 MHz

(3) f = 1511 MHz

Fig 7. Adjacent channel power ratio and peak-to-average power ratio as function of output power; typical values

8. Test information

Table 12. List of components

See Figure 8 for component layout.

Component	Description	Value		Remarks
C1, C2, C3, C4	multi layer ceramic chip capacitor	100 pF	[1]	
C5, C6	multi layer ceramic chip capacitor	10 μF	[2]	
C7	multi layer ceramic chip capacitor	10 nF	[2]	on input gate line as shown
C8	multi layer ceramic chip capacitor	100 nF	[2]	
C10	multi layer ceramic chip capacitor	2.4 pF	[1]	
C11	multi layer ceramic chip capacitor	3.6 pF	[3]	
C12	electrolytic capacitor	470 μF; 63 V		
C13, C14, C15, C16	multi layer ceramic chip capacitor	33 pF	[3]	
R1	chip resistor	3.9 kΩ		Philips 0603
R2	chip resistor	2.2 kΩ		Philips 0603
R3	chip resistor	10 Ω		Philips 0603
R4	chip resistor	0 Ω		Philips 0603

[1] American Technical Ceramics type 800B or capacitor of same quality.

[2] TDK or capacitor of same quality.

[3] American Technical Ceramics type 100B or capacitor of same quality.

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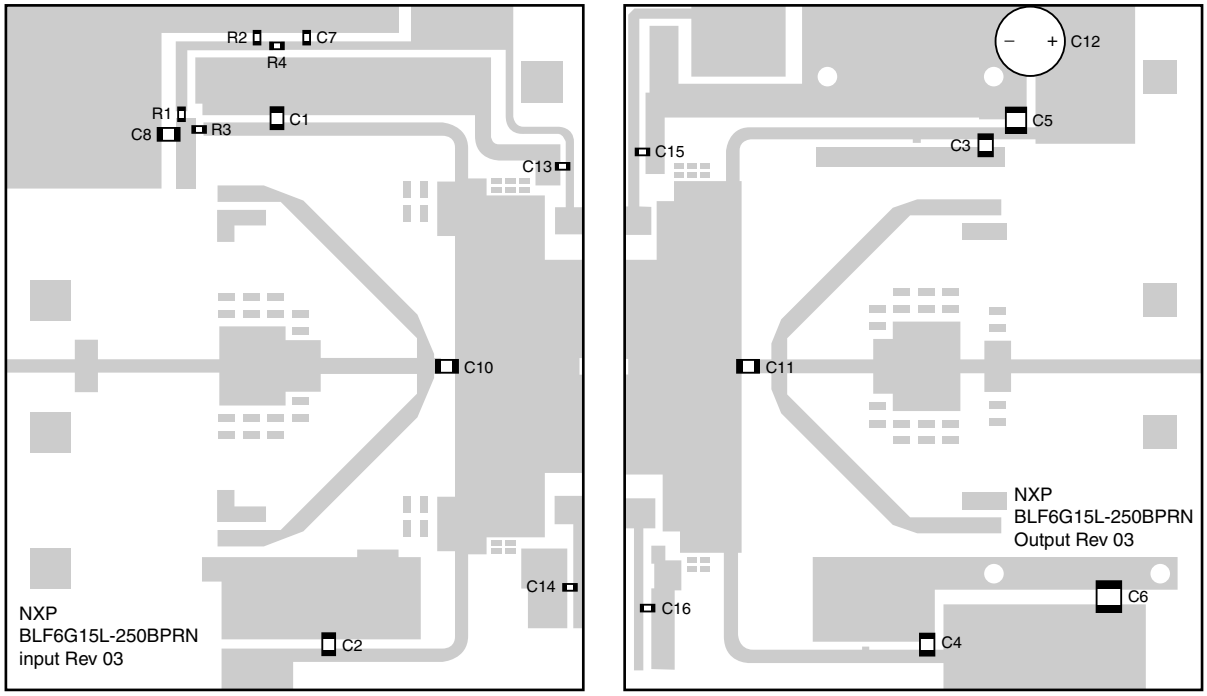

014aab104

Printed-Circuit Board (PCB): Taconic RF-35A2; ε_r = 3.5 F/m; thickness = 0.762 mm; thickness copper plating = 35 μm.

The vias can be as a reference to place components.

The above layout shows the test circuit used to measure the devices in production. A more appropriate application demonstration for specific customer needs can be provided.

See Table 12 for list of components.

Fig 8. Component layout

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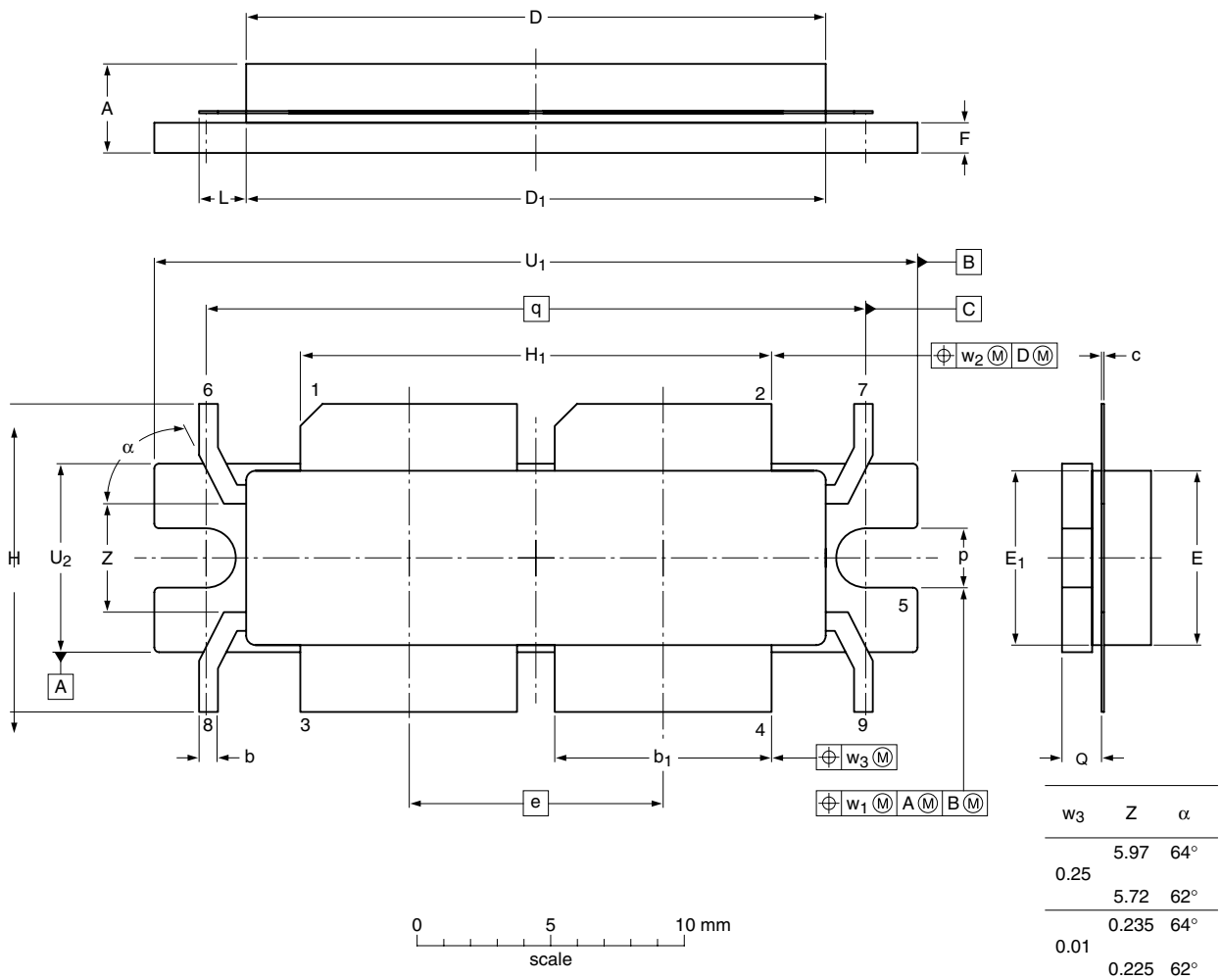
9. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 8 leads **SOT1110A**



w3	Z	α
0.25	5.97	64°
	5.72	62°
0.01	0.235	64°
	0.225	62°

Dimensions

Unit(1)		A	b	b_1	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q(2)	q	U_1	U_2	w_1	w_2
mm	max	5.36	1.14	11.81	0.18	31.55	31.52		9.50	9.53	1.75	17.12	25.53	2.67	3.30	2.26		41.28	10.29		
	nom							13.72									35.56			0.25	0.51
	min	3.99	0.89	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.41	3.05	2.01		41.02	10.03		
inches	max	0.211	0.045	0.465	0.007	1.242	1.241		0.374	0.375	0.069	0.674	1.005	0.105	0.13	0.089		1.625	0.405		
	nom							0.540									1.4			0.01	0.02
	min	0.157	0.035	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.095	0.12	0.079		1.615	0.395		

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.
3. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

sot1110a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1110A						~~09-11-20~~ 10-02-02

Fig 9. Package outline SOT1110A

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10. Abbreviations

Table 13. Abbreviations

Acronym	Description
CCDF	Complementary Cumulative Distribution Function
CDMA	Code Division Multiple Access
CW	Continuous Wave
EDGE	Enhanced Data rates for GSM Evolution
DPCH	Dedicated Physical CHannel
GSM	Global System for Mobile communications
IS-95	Interim Standard 95
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
RF	Radio Frequency
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF6G15L-250PBRN v.2	20101103	Product data sheet	-	BLF6G15L-250PBRN v.1
BLF6G15L-250PBRN v.1	20100914	Preliminary data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

1 Product profile 1
1.1 General description 1
1.2 Features and benefits 1
1.3 Applications 2
2 Pinning information 2
3 Ordering information 2
4 Limiting values 2
5 Thermal characteristics 2
6 Characteristics 3
7 Application information 3
7.1 Ruggedness in class-AB operation 4
7.2 Impedance information 4
7.3 Graphs 5
7.3.1 CW 5
7.3.2 IS-95 6
7.3.3 2C-WCDMA (5 MHz spacing) 7
8 Test information 7
9 Package outline 9
10 Abbreviations 10
11 Revision history 10
12 Legal information 11
12.1 Data sheet status 11
12.2 Definitions 11
12.3 Disclaimers 11
12.4 Trademarks 12
13 Contact information 12
14 Contents 13

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