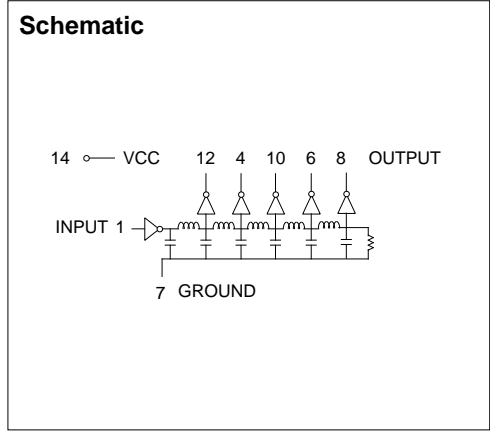


# 14 Pin DIP 5 Tap Fast-TTL Logic Compatible Active Delay Lines

TAP DELAYS ±5% or ±2 nS†	TOTAL DELAYS ±5% or ±2 nS†	PART NUMBER	TAP DELAYS ±5% or ±2 nS†	TOTAL DELAYS ±5% or ±2 nS†	PART NUMBER
*3±1, 1±.5, 2±.5, 3±.5	4	EPA1145-4	35, 70, 105, 140	175	EPA1145-175
*3±1, 1.5±.5, 3±.5, 4.5±.5	6	EPA1145-6	40, 80, 120, 160	200	EPA1145-200
*3±1, 2±.5, 4±.5, 6±.5	8	EPA1145-8	45, 90, 135, 180	225	EPA1145-225
*3±1, 6±1.5, 9, 12	15	EPA1145-15	50, 100, 150, 200	250	EPA1145-250
4, 8, 12, 16	20	EPA1145-20	60, 120, 180, 240	300	EPA1145-300
5, 10, 15, 20	25	EPA1145-25	70, 140, 210, 280	350	EPA1145-350
6, 12, 18, 24	30	EPA1145-30	80, 160, 240, 320	400	EPA1145-400
8, 16, 24, 32	40	EPA1145-40	90, 180, 270, 360	450	EPA1145-450
10, 20, 30, 40	50	EPA1145-50	100, 200, 300, 400	500	EPA1145-500
12, 24, 36, 48	60	EPA1145-60	120, 240, 360, 480	600	EPA1145-600
15, 30, 45, 60	75	EPA1145-75	140, 280, 420, 560	700	EPA1145-700
20, 40, 60, 80	100	EPA1145-100	160, 320, 480, 640	800	EPA1145-800
25, 50, 75, 100	125	EPA1145-125	180, 360, 540, 720	900	EPA1145-900
30, 60, 90, 120	150	EPA1145-150	200, 400, 600, 800	1000	EPA1145-1000

† Whichever is greater. Delay times referenced from input to leading edges at 25°C, 5.0V, with no load.  
 \* First tap is inherent delay (3 ± 1 nS), all other taps are measured referenced from first tap.

DC Electrical Characteristics					
Parameter	Test Conditions	Min	Max	Unit	
V <sub>OH</sub>	High-Level Output Voltage	V <sub>CC</sub> = min. V <sub>IL</sub> = max. I <sub>OH</sub> = max	2.7		V
V <sub>OL</sub>	Low-Level Output Voltage	V <sub>CC</sub> = min. V <sub>IH</sub> = min. I <sub>OL</sub> = max		0.5	V
V <sub>IK</sub>	Input Clamp Voltage	V <sub>CC</sub> = min. I <sub>I</sub> = I <sub>IK</sub>		-1.2	V
I <sub>IH</sub>	High-Level Input Current	V <sub>CC</sub> = max. V <sub>IN</sub> = 2.7V		50	µA
		V <sub>CC</sub> = max. V <sub>IN</sub> = 5.25V		1.0	mA
I <sub>IL</sub>	Low-Level Input Current	V <sub>CC</sub> = max. V <sub>IN</sub> = 0.5V		-0.6	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = max. V <sub>OUT</sub> = 0. (One output at a time)	-40	-150	mA
I <sub>CCH</sub>	High-Level Supply Current	V <sub>CC</sub> = max. V <sub>IN</sub> = OPEN		15	mA
I <sub>CCL</sub>	Low-Level Supply Current	V <sub>CC</sub> = max. V <sub>IN</sub> = 0		50	mA
T <sub>RO</sub>	Output Rise Time	T <sub>d</sub> ≤ 500 nS (0.75 to 2.4 Volts) T <sub>d</sub> > 500 nS		3	nS
N <sub>H</sub>	Fanout High-Level Output	V <sub>CC</sub> = max. V <sub>OH</sub> = 2.7V		20 TTL LOAD	
N <sub>L</sub>	Fanout Low-Level Output	V <sub>CC</sub> = max. V <sub>OL</sub> = 0.5V		10 TTL LOAD	



Recommended Operating Conditions				
		Min	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.25	V
V <sub>IH</sub>	High-Level Input Voltage	2.0		V
V <sub>IL</sub>	Low-Level Input Voltage		0.8	V
I <sub>IK</sub>	Input Clamp Current		-18	mA
I <sub>OH</sub>	High-Level Output Current		-1.0	mA
I <sub>OL</sub>	Low-Level Output Current		20	mA
PW*	Pulse Width of Total Delay	40		%
d*	Duty Cycle		40	%
T <sub>A</sub>	Operating Free-Air Temperature	-55	+125	°C

\*These two values are inter-dependent.

Input Pulse Test Conditions @ 25° C			
		Unit	
E <sub>IN</sub>	Pulse Input Voltage	3.2	Volts
PW	Pulse Width % of Total Delay	110	%
T <sub>RI</sub>	Pulse Rise Time (0.75 - 2.4 Volts)	2.0	nS
PRR	Pulse Repetition Rate @ T <sub>d</sub> ≤ 200 nS	1.0	MHz
	Pulse Repetition Rate @ T <sub>d</sub> > 200 nS	100	KHz
V <sub>CC</sub>	Supply Voltage	5.0	Volts

