Institut für angewandte Funksystemtechnik GmbH

IAF GmbH
Berliner Straße 52j
38104 Braunschweig
Germany

Phone: ++49 531 379 88-0
Fax: ++49 531 37988-30
e-mail: info@iaf-bs.de
www.iaf-bs.de

2x2 RF-TRANSCEIVER (Rev. 1.0)

(Data Sheet Rev. 1. March 2011)

1. Overview

Key facts:

- **2 antenna full duplex transmitter and receiver**
- **20 MHz bandwidth**
- **2,6 GHz and 800 MHz frequency frontends**
- **several digital interfaces (CPRI, PCIe, LVDS)**

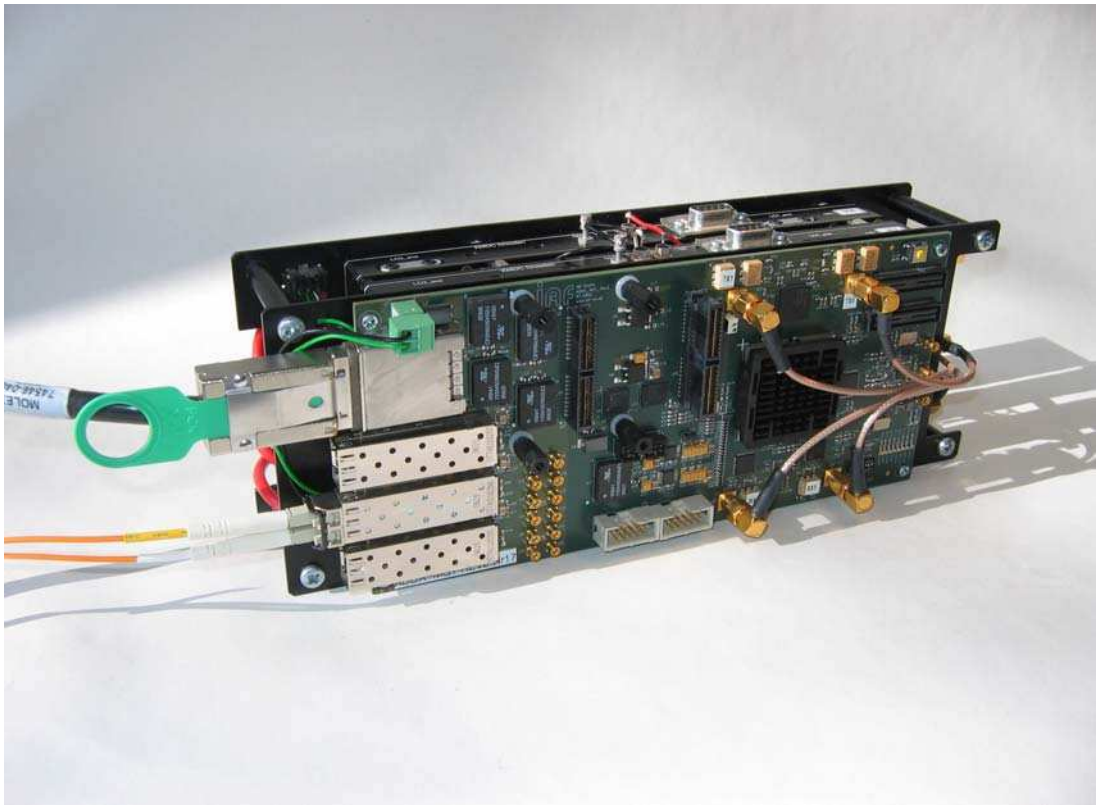

Figure 1: 2x2 RF-Transceiver

The 2x2 RF-Transceiver is designed for **3G-LTE** prototyping systems as well as for software defined radio development purposes. It supports simultaneous transmission and receiption of two antennas in frequency-duplex-mode.

The 2x2 RF-Transceiver includes 2 main components: analog RF unit and digital module.

The RF unit is available for two frequency bands, 2.6GHz or 800MHz and up to 20MHz bandwidth.

The digital module (ADDA_MGT board) is designed for A/D conversion, D/A conversion and for pre- and post-processing of data streams like digital I/Q modulation and demodulation. In this application the Xilinx Virtex-5-SXT chip is used for pre- and post-processing of DAC and ADC data streams and for controlling of the connected analog RF circuits.

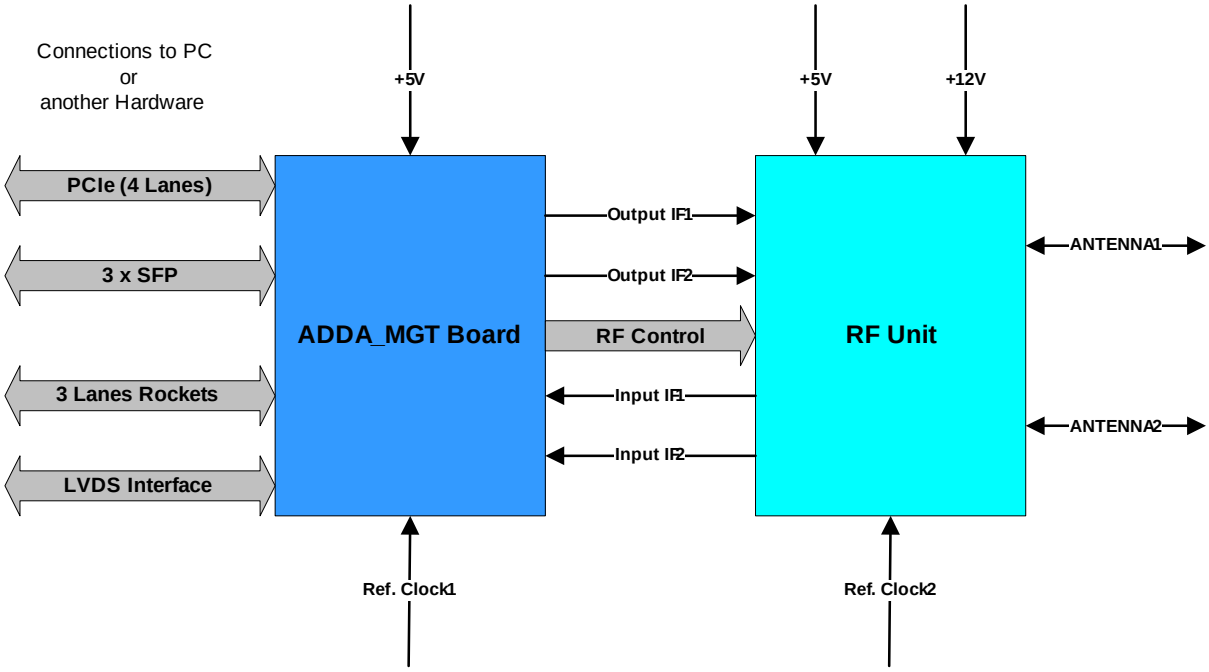

Figure 2: 2x2 RF-Transceiver block diagram.

2. RF Unit.

The RF unit is a flexible and reconfigurable dual transmitter and dual receiver unit for LTE test applications. The RF unit is produced in two different versions: 2.6 GHz frequency band (UL 2.53GHz / DL 2.68GHz) and 800 MHz frequency band (UL 816MHz / DL 856.8MHz). Other frequency configurations are possible. The maximal bandwidth of the RF unit is 20 MHz. The LO frequency and AGC is configurable via RF control interface from ADDA_MGT board. The input and output impedance is 50 Ohm. Maximal transmitter power is +26dBm.

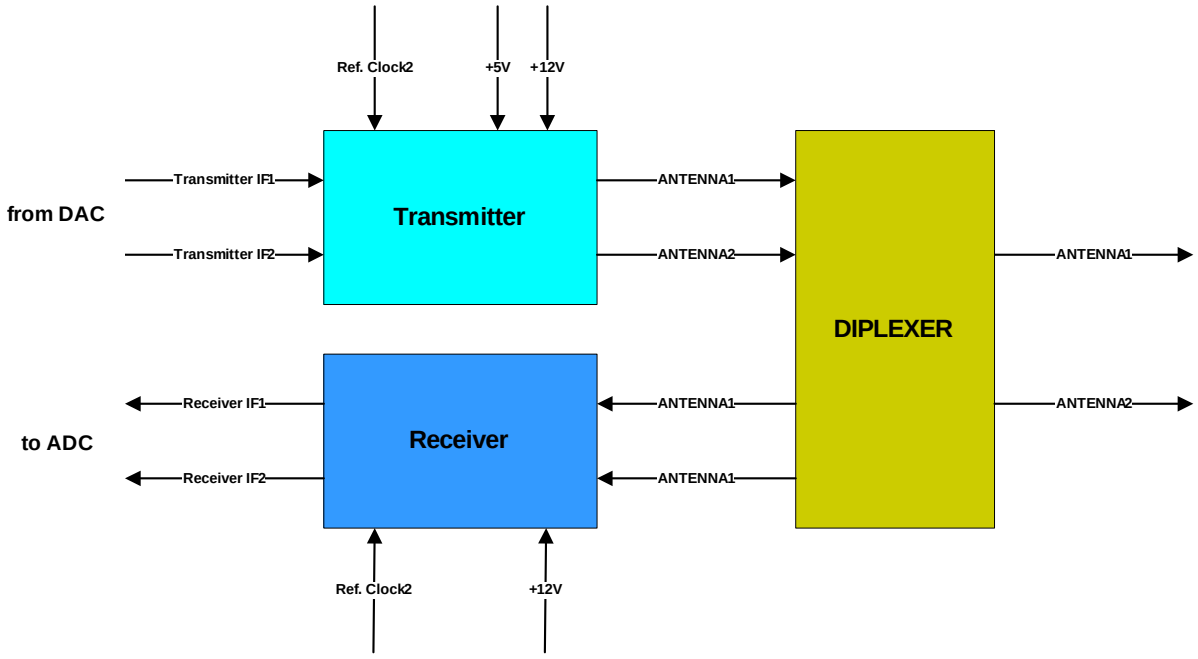

Figure 3: RF unit block diagramm.

3. ADDA_MGT Board.

The ADDA_MGT-Board is designed for A/D conversion, D/A conversion as well as for pre- and post-processing of data streams like digital I/Q modulation and demodulation. In this application the Xilinx Virtex-5SXT chip is used for pre- and post-processing of DAC and ADC data streams and for controlling of the connected analog RF circuits. The digital interface logic for PCIe and CPRI are also integrated in the Virtex-5 SX95T FPGA.

This board includes four digital data interfaces for connection to PC or any baseband processing platform:

- PCI Express Interface (4 Lanes)
- Rocket I/O Interfaces
- Parallel LVDS Interface
- 3 SFP Interfaces (CPRI,OBSAI, Ethernet etc.)

The complete clock generation and power supply is integrated on board (see Figure 4).

The Virtex5 chip can either be configured directly via JTAG-Interface or via an integrated flash ROM configuration memory.

ADDA_MGT-Board Overview

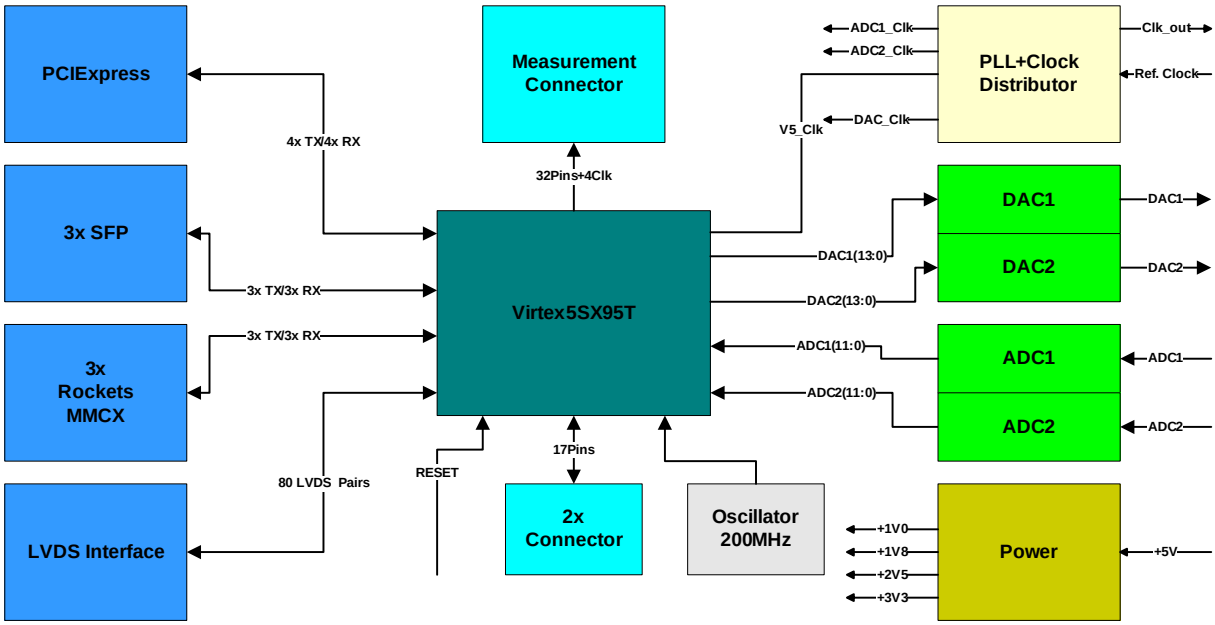

Figure 4: ADDA_MGT-Board block diagram