

2GSPlus-DAC-Board Rev.2 Overview

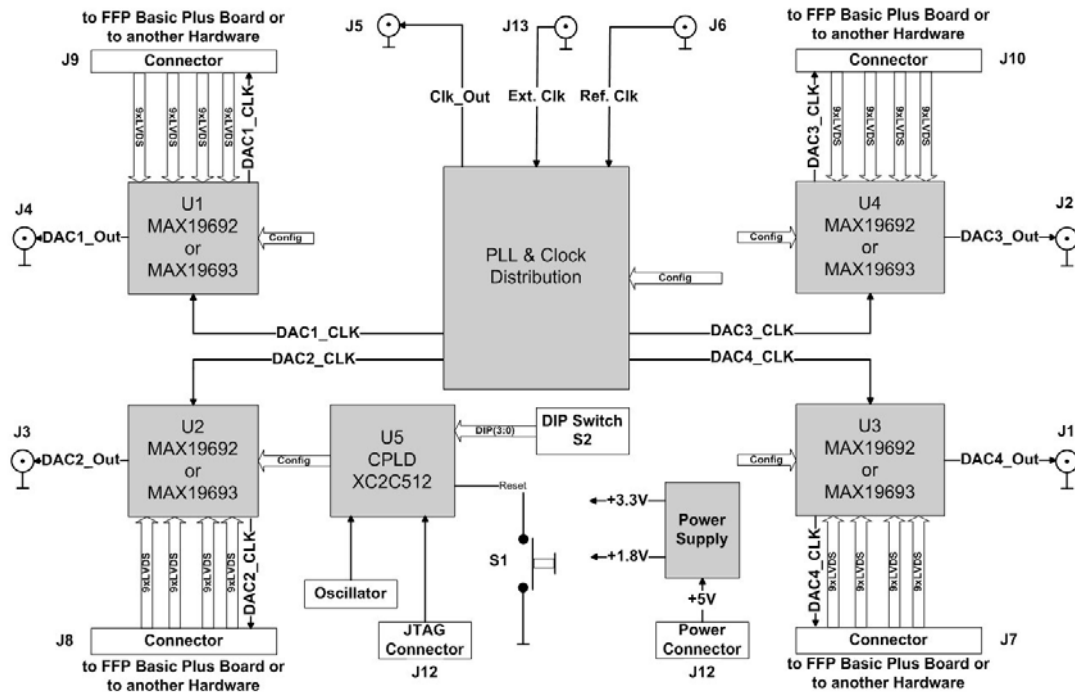


Figure 2: Overview

2. Power Section.

The 2GSPlus-DAC-Board includes the complete power generation on board and needs only +5V voltage input. The supply voltages are generated with linear voltage regulators (see Figure 2). The +5V input voltage can be connected on two different ways: from connector J11 or from power pins of connectors J7, J8, J9 and J10. The last case is recommended to use with FFP-Plus board.

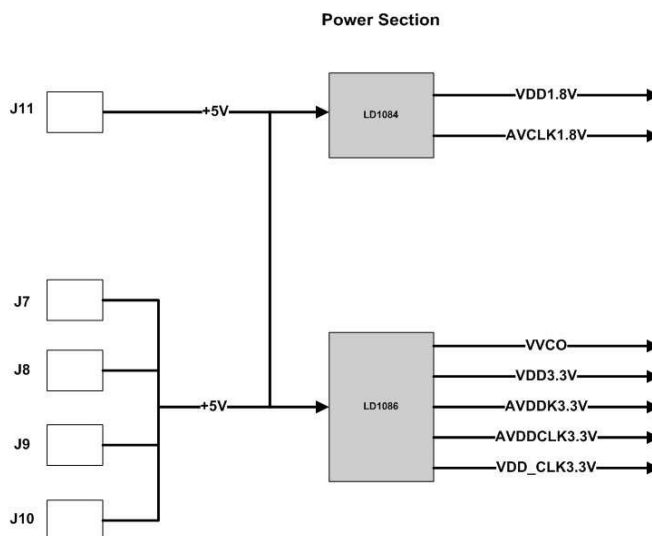


Figure 3: Power Section

3. PLL and clock distribution.

The board includes the complete clock generation and distribution. The PLL can generate clocks in range from 500MHz to 2.725GHz. The output frequency range depends on the onboard placed chip (see Table1 and ADF4360-x datasheet). The AD4360-x works with input reference clock from 10 to 250MHz. The LED3 indicated PLL is locked. The SY5802U works as clock distributor and SY8987 as clock divider for FPGA clock. For MAX19692 must be generated the full sample frequency, MAX19693 need the half of sample frequency as input clock. The PLL is programmable from CPLD via SPI interface (see Table2).

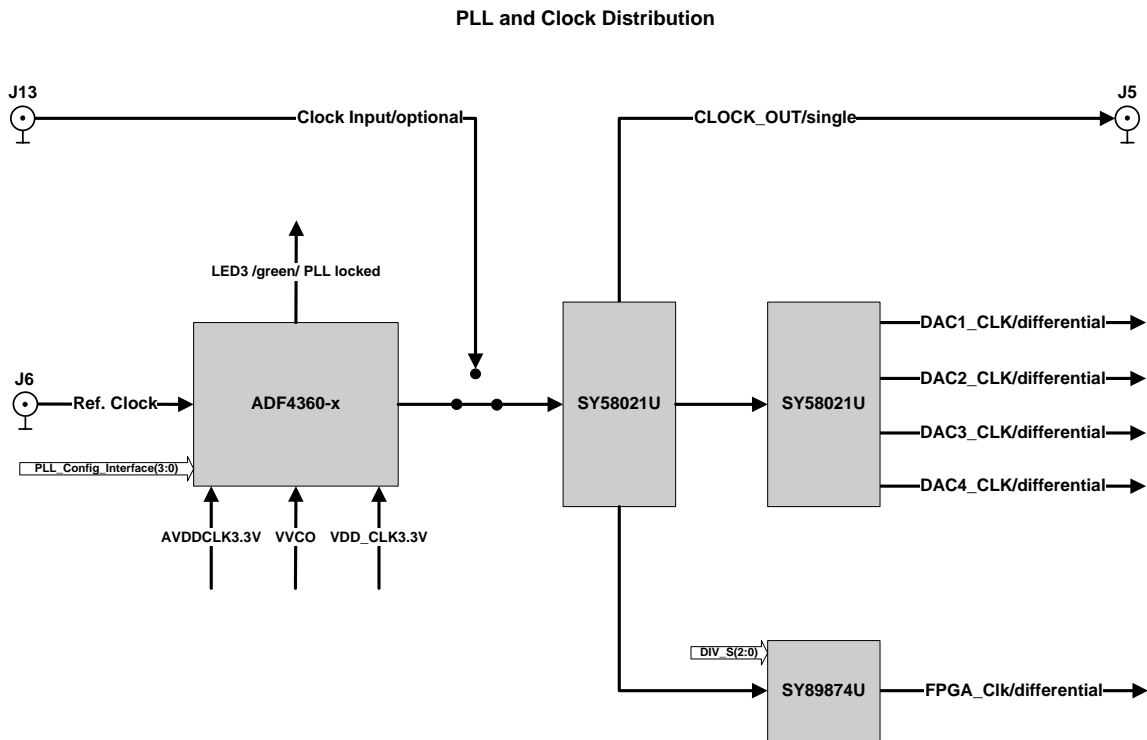


Figure 4: Clock generation and distribution.

Chip	Frequency range
ADF4360-0	2400-2725MHz
ADF4360-1	2050-2450MHz
ADF4360-2	1850-2150MHz
ADF4360-3	1600-1950MHz
ADF4360-4	1450-1750MHz
ADF4360-5	1200-1400MHz
ADF4360-6	1050-1250MHz

Table 1: Frequency range.

4. DC-Specification:

	Min	Typ	Max
Power Supply Voltage Range	+4,5 V	+5 V	+5,5 V
Power Supply Current		5.1A	

5. AC-Specification.

	Min	Typ	Max
Reference input frequency range	10 MHz	-	250MHz
Analog output range	-	-	-2.6dBm/50Ohm

6. Board Dimensions.

