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ADDA-MGT-Board (Rev. 2.0)

(Data Sheet Rev. 2. March 2011)

1. Overview

The ADDA_MGT-Board is designed for A/D conversion, D/A conversion and for pre- and post-processing of data streams like digital I/Q modulation and demodulation. In this application the Xilinx Virtex-5-SXT chip is used for pre- and post-processing of DAC and ADC data streams and for controlling of the connected analog RF circuits.

This board includes four digital data interfaces:

- 4x PCI Express Interface
- Rocket I/O Interface
- Parallel LVDS Interface
- SFP Interface

The complete clock generation and power supply is integrated on board (see Figure 1).

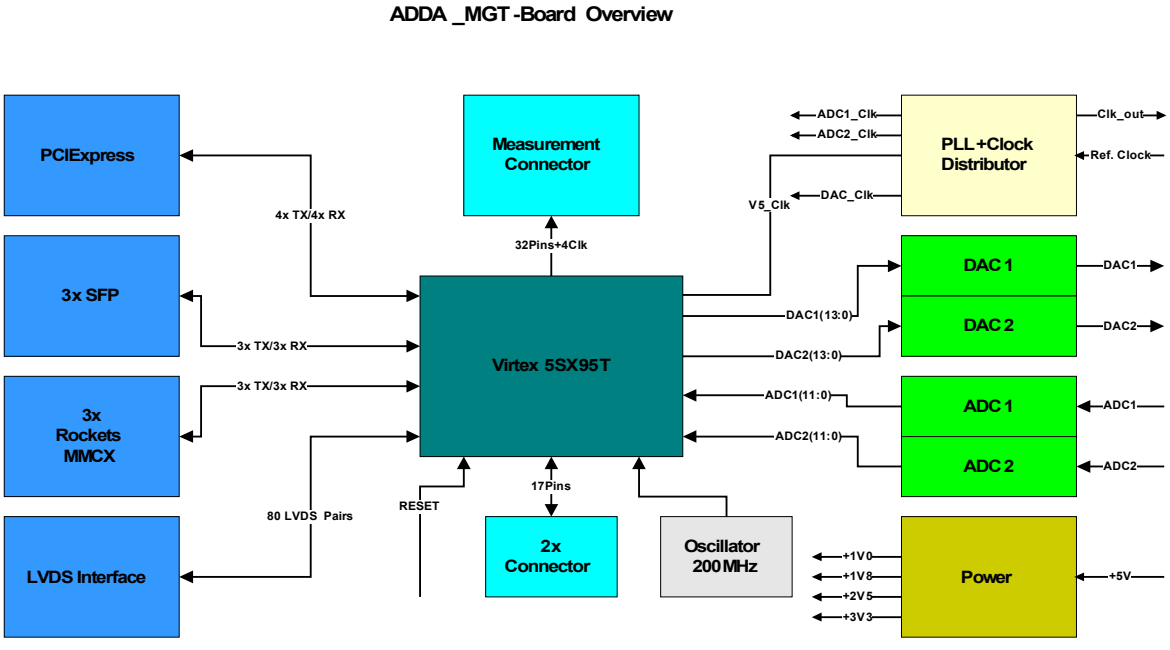

Figure 1: Overview

The ADDA-MGT-Board can also operate standalone.

The Virtex5 chip can either be configured directly via JTAG-Interface or via an integrated flash ROM configuration memory.

This data sheet describes the hardware and function of the ADDA-MGT-Board.

2. Power Section.

The ADDA-MGT-Board includes the complete power generation on board and needs only +5V voltage input. The analog domain supply voltage for A/D and D/A conversion is generated separately with linear voltage regulators (see Figure 2).

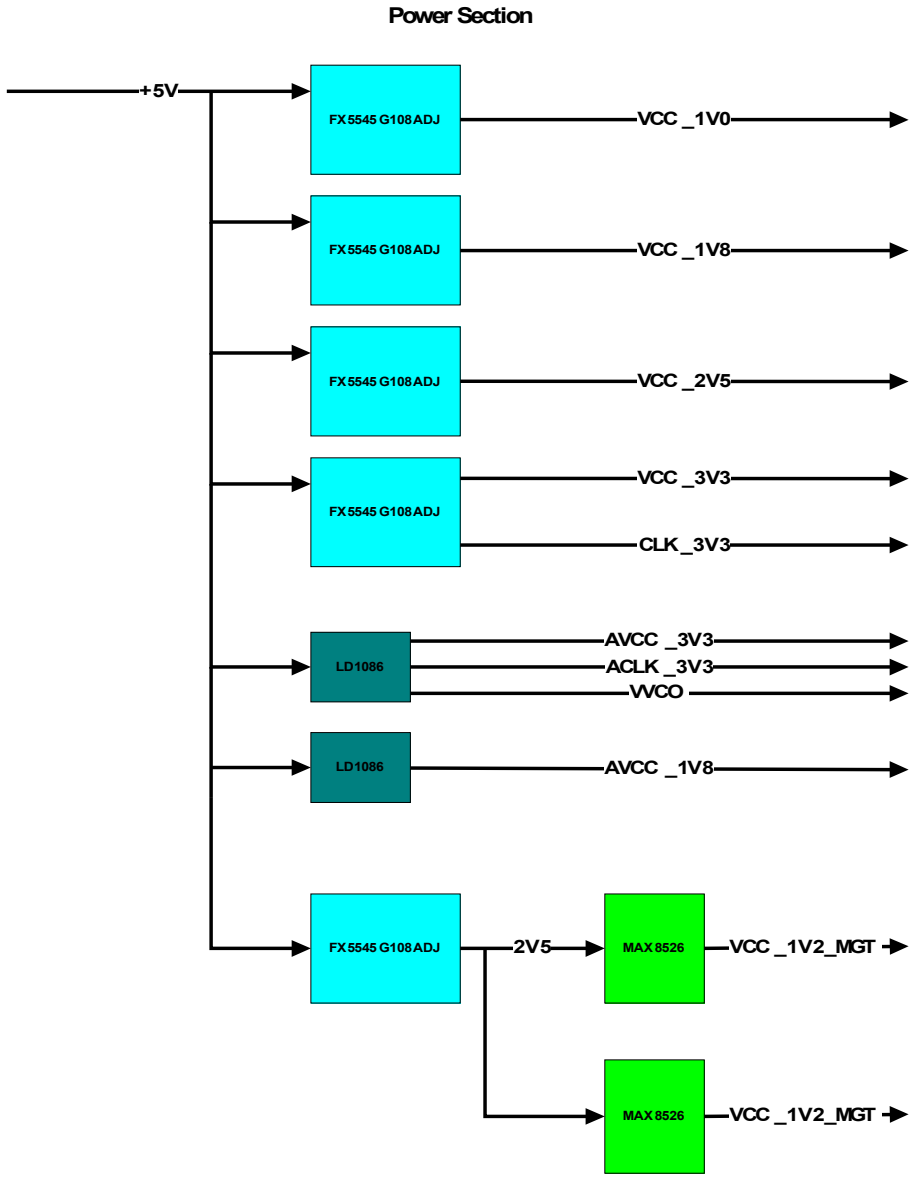

Figure 2: Power Section

3. PLL and clock distribution.

The board includes the complete clock generation and distribution. The PLL1 can generate clocks in range from 350MHz to 1.8GHz. The AD4360-7 works with input reference clock from 10 to 250MHz. The output frequency range depends on the values of L19 and L20. For output frequency change L19 and L20 must be replaced by other values.(see AD4360-7 data sheet). The AD9510 works as clock distributor and divider. Both chips are programmable via SPI interface (see Table 1).

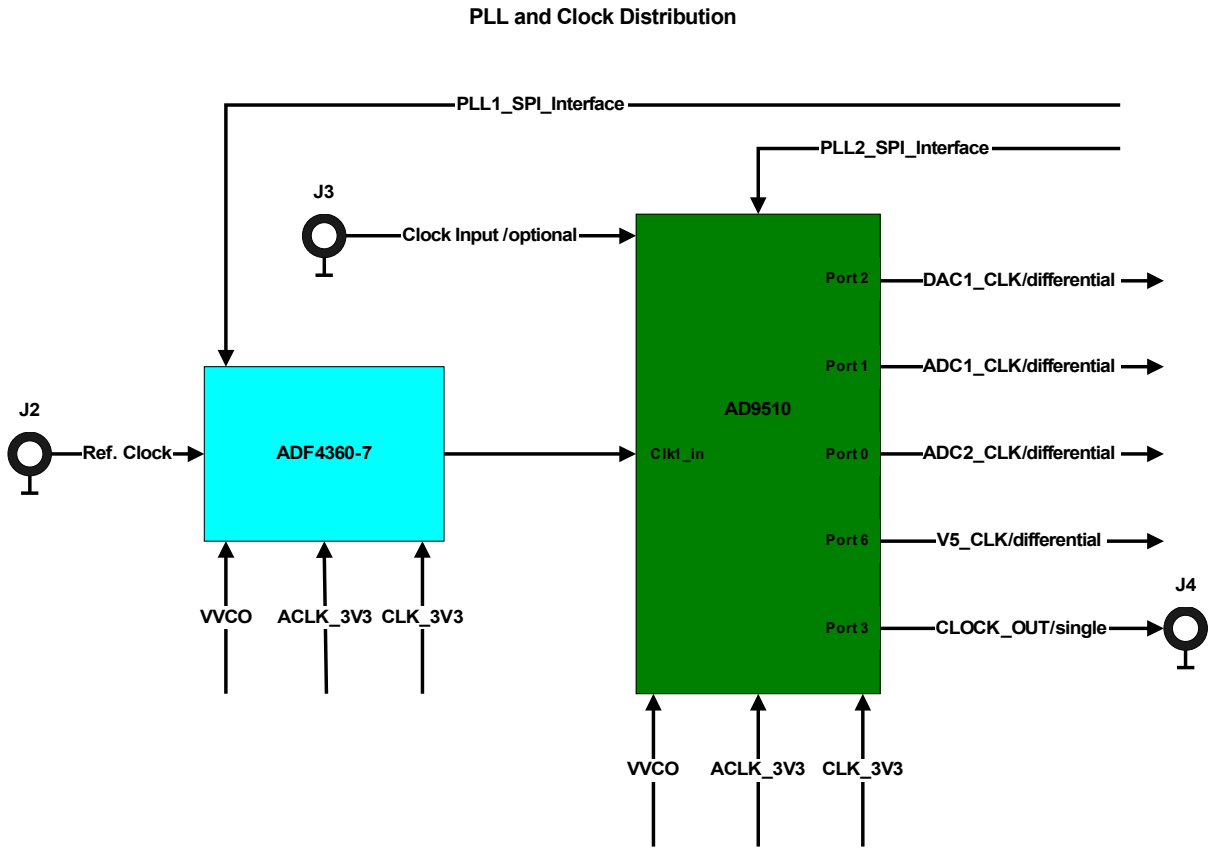

Figure 3: PLL and clock distribution.

SPI Interface for PLL's				
PLL's			Virtex5	
Signal	Part	Pin Nr.	IO-Standard	Function
EN_PROG_PLL1	U7/19	K12	LVCMOS18	latch enable
PLL1_CE	U7/23	G23	LVCMOS18	chip enable; activ high
SCLK_PLL1	U7/17	H23	LVCMOS18	serial clock
SDATA_PLL1	U7/18	K13	LVCMOS18	serial data
Signal	Part			
EN_PROG_PLL2	U8/21	H18	LVCMOS25	latch enable
RESET_PLL2	U8/16	H17	LVCMOS25	Reset; activ low
SCLK_PLL2	U8/18	K17	LVCMOS25	serial clock
SDATA_PLL2	U8/19	L18	LVCMOS25	serial data

Table1: SPI Interface.

4. Reset, LED's, Clock and Configurations Pins.

The ADDA-MGT-Board provides on board clock oscillator, reset and dip-switch. The oscillator generates a 200MHz clock. The reset signal is generated with button S1. This signal is active low.

The dip switch can be used to generate different user configurations on the Virtex5 chip (see Table2). Note: switch ON results to a low signal level, switch OFF results to a high signal level.

		User Interface		
			Virtex5	
Signal	Part	Pin Nr.	IO-Standard	Function
RESET	S1	AF5	LVCMOS_25	Reset/active low
CLK_200_P	X1/Pin4	H19	LVTTL	User Clock 200MHz
CLK_200_N	X1/Pin5	H20	LVTTL	inv. User Clock 200MHz
CONF0	SW1/Switch1	K18	LVCMOS_25	User Config/ON=low
CONF1	SW1/Switch2	J19	LVCMOS_25	User Config/ON=low
CONF2	SW1/Switch3	J14	LVCMOS_25	User Config/ON=low
CONF3	SW1/Switch4	H13	LVCMOS_25	User Config/ON=low
CONF4	SW1/Switch5	F6	LVCMOS_25	User Config/ON=low
CONF5	SW1/Switch6	T10	LVCMOS_25	User Config/ON=low
CONF6	SW1/Switch7	T11	LVCMOS_25	User Config/ON=low
CONF7	SW1/Switch8	G6	LVCMOS_25	User Config/ON=low
LED1	LED6	AE14	LVTTL	User LED/blue
LED2	LED7	AF14	LVTTL	User LED/blue
LED3	LED8	AF20	LVTTL	User LED/green
LED4	LED9	AF29	LVTTL	User LED/green
LED5	LED10	AF30	LVTTL	User LED/yellow
LED6	LED11	V8	LVCMOS_25	User LED/yellow
LED7	LED12	U8	LVCMOS_25	User LED/red
LED8	LED13	AK7	LVCMOS_25	User LED/red

Table2.

5. Digital to analog conversion.

Digital to Analog Conversion

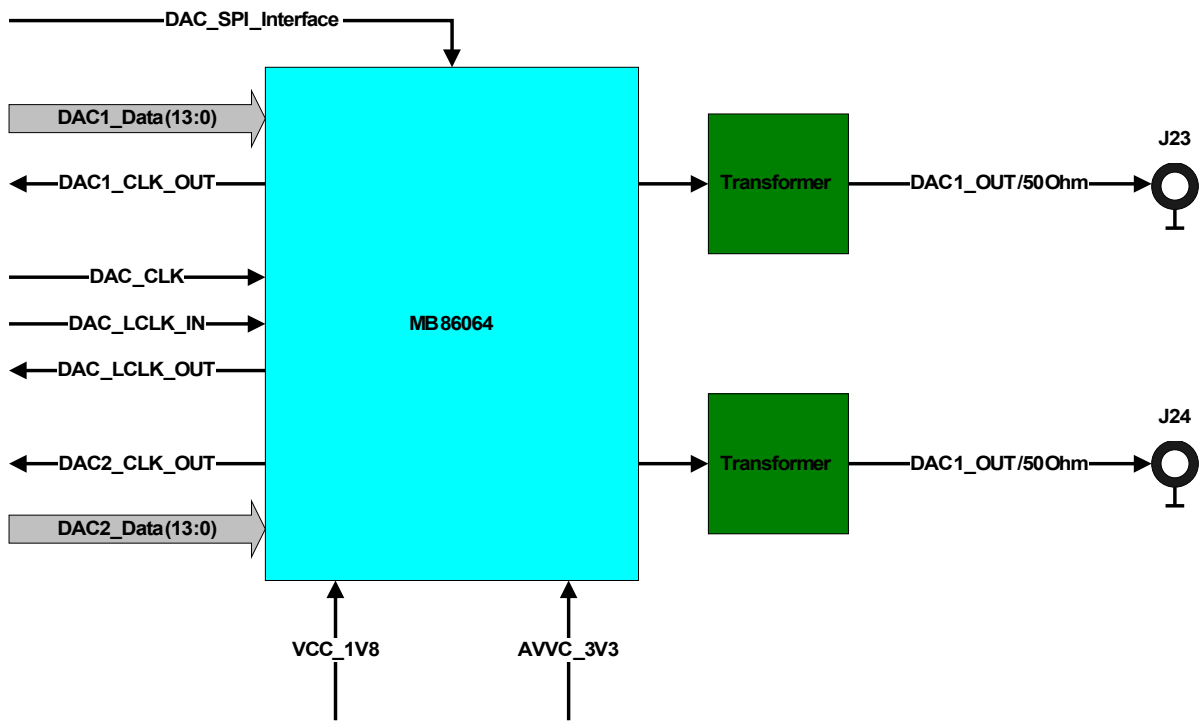

Figure 4: Digital to analog conversion.

DAC1			
	DAC	Virtex	
Signal	Pin Nr.	Pin Nr.	IO-Standard
DAC1_P0	H20	AC34	LVDS_25
DAC1_N0	J21	AD34	LVDS_25
DAC1_P1	H22	AC32	LVDS_25
DAC1_N1	J23	AB32	LVDS_25
DAC1_P2	K20	AC33	LVDS_25
DAC1_N2	L21	AB33	LVDS_25
DAC1_P3	K22	AF33	LVDS_25
DAC1_N3	L23	AE33	LVDS_25
DAC1_P4	N23	AF34	LVDS_25
DAC1_N4	P22	AE34	LVDS_25
DAC1_P5	N21	AK34	LVDS_25
DAC1_N5	P20	AK33	LVDS_25
DAC1_P6	R23	AG32	LVDS_25
DAC1_N6	T22	AH32	LVDS_25
DAC1_P7	R21	AJ32	LVDS_25
DAC1_N7	T20	AK32	LVDS_25
DAC1_P8	V22	AL34	LVDS_25
DAC1_N8	W23	AL33	LVDS_25
DAC1_P9	V20	AM33	LVDS_25
DAC1_N9	W21	AM32	LVDS_25
DAC1_P10	AA19	AA34	LVDS_25
DAC1_N10	Y18	Y34	LVDS_25
DAC1_P11	AC19	Y33	LVDS_25
DAC1_N11	AB18	AA33	LVDS_25
DAC1_P12	Y16	W34	LVDS_25
DAC1_N12	AA15	V34	LVDS_25
DAC1_P13	AB16	V32	LVDS_25
DAC1_N13	AC15	V33	LVDS_25
DAC1_CLK_OUT_P	AC13	AD32	LVDS_25
DAC1_CLK_OUT_N	AB14	AE32	LVDS_25

Table3. DAC1 data interface.

DAC2			
	DAC	Virtex	
Signal	Pin Nr.	Pin Nr.	IO-Standard
DAC2_P0	H4	B32	LVDS_25
DAC2_N0	J3	A33	LVDS_25
DAC2_P1	H2	B33	LVDS_25
DAC2_N1	J1	C33	LVDS_25
DAC2_P2	K4	C32	LVDS_25
DAC2_N2	L3	D32	LVDS_25
DAC2_P3	K2	C34	LVDS_25
DAC2_N3	L1	D34	LVDS_25
DAC2_P4	N1	G32	LVDS_25
DAC2_N4	P2	H32	LVDS_25
DAC2_P5	N3	F33	LVDS_25
DAC2_N5	P4	E34	LVDS_25
DAC2_P6	R1	E32	LVDS_25
DAC2_N6	T2	E33	LVDS_25
DAC2_P7	R3	G33	LVDS_25
DAC2_N7	T4	F34	LVDS_25
DAC2_P8	V2	J32	LVDS_25
DAC2_N8	W1	H33	LVDS_25
DAC2_P9	V4	L34	LVDS_25
DAC2_N9	W3	K34	LVDS_25
DAC2_P10	AA5	K33	LVDS_25
DAC2_N10	Y6	K32	LVDS_25
DAC2_P11	AC5	L33	LVDS_25
DAC2_N11	AB6	M32	LVDS_25
DAC2_P12	Y8	P32	LVDS_25
DAC2_N12	AA9	N32	LVDS_25
DAC2_P13	AB8	T33	LVDS_25
DAC2_N13	AC9	R34	LVDS_25
DAC2_CLK_OUT_P	AC11	H34	LVDS_25
DAC2_CLK_OUT_N	AB10	J34	LVDS_25

Table4: DAC2 data interface.

DAC1 and DAC2				
	DAC	Virtex		
Signal	Pin Nr.	Pin Nr.	IO-Standard	Descryption
ENABLE_PROG_DAC	D6	K23	LVCMOS18	serial programing enable; activ high
SCLK_DAC	B6	H12	LVCMOS18	serial programing clk
SDATA_DAC	C5	J12	LVCMOS18	serial programing data
RESET_DAC	B18	K22	LVCMOS18	Reset; activ low
DAC_LPCLK_IN_P	AA11	U33	LVDS_25_DCI	Loop clock input
DAC_LPCLK_IN_N	Y10	T34	LVDS_25_DCI	Loop clock input
DAC_LPCLK_OUT_P	AA13	AH34	LVDS_25	Loop clock output
DAC_LPCLK_OUT N	Y14	AJ34	LVDS_25	Loop clock output

Table5: DAC1 and DAC2 control interface.

6. Analog to digital conversion.

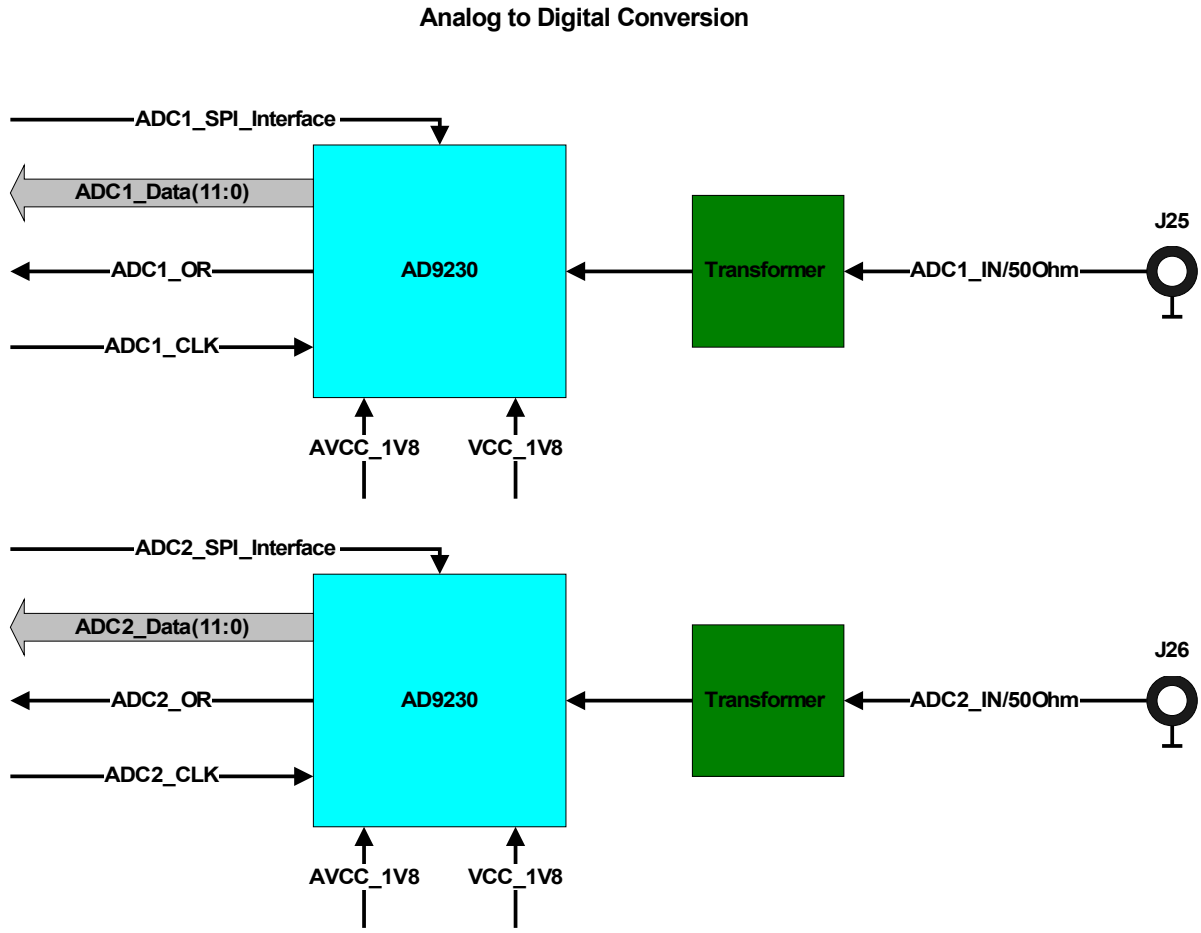

Figure 5: Analog to digital conversion.

		ADC1		
	DAC		Virtex	
Signal	Pin Nr.	Pin Nr.	IO-Standard	Function
ADC1_P0	52	M6	LVDS_25_DCI	data input
ADC1_N0	51	M5	LVDS_25_DCI	data input
ADC1_P1	53	N8	LVDS_25_DCI	data input
ADC1_N1	55	N7	LVDS_25_DCI	data input
ADC1_P2	56	M7	LVDS_25_DCI	data input
ADC1_N2	55	L6	LVDS_25_DCI	data input
ADC1_P3	2	N5	LVDS_25_DCI	data input
ADC1_N3	1	P5	LVDS_25_DCI	data input
ADC1_P4	4	L4	LVDS_25_DCI	data input
ADC1_N4	3	L5	LVDS_25_DCI	data input
ADC1_P5	6	P7	LVDS_25_DCI	data input
ADC1_N5	5	P6	LVDS_25_DCI	data input
ADC1_P6	10	K7	LVDS_25_DCI	data input
ADC1_N6	9	K6	LVDS_25_DCI	data input
ADC1_P7	12	R6	LVDS_25_DCI	data input
ADC1_N7	11	T6	LVDS_25_DCI	data input
ADC1_P8	14	J6	LVDS_25_DCI	data input
ADC1_N8	13	J5	LVDS_25_DCI	data input
ADC1_P9	16	R7	LVDS_25_DCI	data input
ADC1_N9	15	R8	LVDS_25_DCI	data input
ADC1_P10	18	T8	LVDS_25_DCI	data input
ADC1_N10	17	U7	LVDS_25_DCI	data input
ADC1_P11	20	H5	LVDS_25_DCI	data input
ADC1_N11	19	G5	LVDS_25_DCI	data input
ADC1_OR_P	22	E6	LVDS_25_DCI	out of range input
ADC1_OR_N	21	E7	LVDS_25_DCI	out of range input
ADC1_P_CO	50	H7	LVDS_25_DCI	clock input
ADC1_N_CO	49	J7	LVDS_25_DCI	clock input
ADC1_CSB	27	L16	LVCMOS18	chip select output
ADC1_PWDN	29	J22	LVCMOS18	power down
ADC1_RESET	28	L21	LVCMOS18	reset
ADC1_SCLK	26	L15	LVCMOS18	serial programing clock
ADC1_SDIO	25	L20	LVCMOS18	serial programing data in/out

Table6: ADC1 interface.

		ADC2		
	DAC		Virtex	
Signal	Pin Nr.	Pin Nr.	IO-Standard	Function
ADC2_P0	52	AC4	LVDS_25_DCI	data input
ADC2_N0	51	AC5	LVDS_25_DCI	data input
ADC2_P1	53	AB6	LVDS_25_DCI	data input
ADC2_N1	55	AB7	LVDS_25_DCI	data input
ADC2_P2	56	AA5	LVDS_25_DCI	data input
ADC2_N2	55	AB5	LVDS_25_DCI	data input
ADC2_P3	2	AC7	LVDS_25_DCI	data input
ADC2_N3	1	AD7	LVDS_25_DCI	data input
ADC2_P4	4	Y8	LVDS_25_DCI	data input
ADC2_N4	3	Y9	LVDS_25_DCI	data input
ADC2_P5	6	AD4	LVDS_25_DCI	data input
ADC2_N5	5	AD5	LVDS_25_DCI	data input
ADC2_P6	10	AA6	LVDS_25_DCI	data input
ADC2_N6	9	Y7	LVDS_25_DCI	data input
ADC2_P7	12	AD6	LVDS_25_DCI	data input
ADC2_N7	11	AE6	LVDS_25_DCI	data input
ADC2_P8	14	W6	LVDS_25_DCI	data input
ADC2_N8	13	Y6	LVDS_25_DCI	data input
ADC2_P9	16	AE7	LVDS_25_DCI	data input
ADC2_N9	15	AF6	LVDS_25_DCI	data input
ADC2_P10	18	AG5	LVDS_25_DCI	data input
ADC2_N10	17	AF5	LVDS_25_DCI	data input
ADC2_P11	20	Y11	LVDS_25_DCI	data input
ADC2_N11	19	W11	LVDS_25_DCI	data input
ADC2_OR_P	22	W10	LVDS_25_DCI	out of range input
ADC2_OR_N	21	W9	LVDS_25_DCI	out of range input
ADC2_P_CO	50	W7	LVDS_25_DCI	clock input
ADC2_N_CO	49	V7	LVDS_25_DCI	clock input
ADC2_CSB	27	G22	LVCMOS18	chip select output
ADC2_PWDN	29	H22	LVCMOS18	power down
ADC2_RESET	28	K21	LVCMOS18	reset
ADC2_SCLK	26	J15	LVCMOS18	serial programing clock
ADC2_SDIO	25	K16	LVCMOS18	serial programing data in/out

Table7: ADC2 interface.

7. LVDS interface.

LVDS Interface

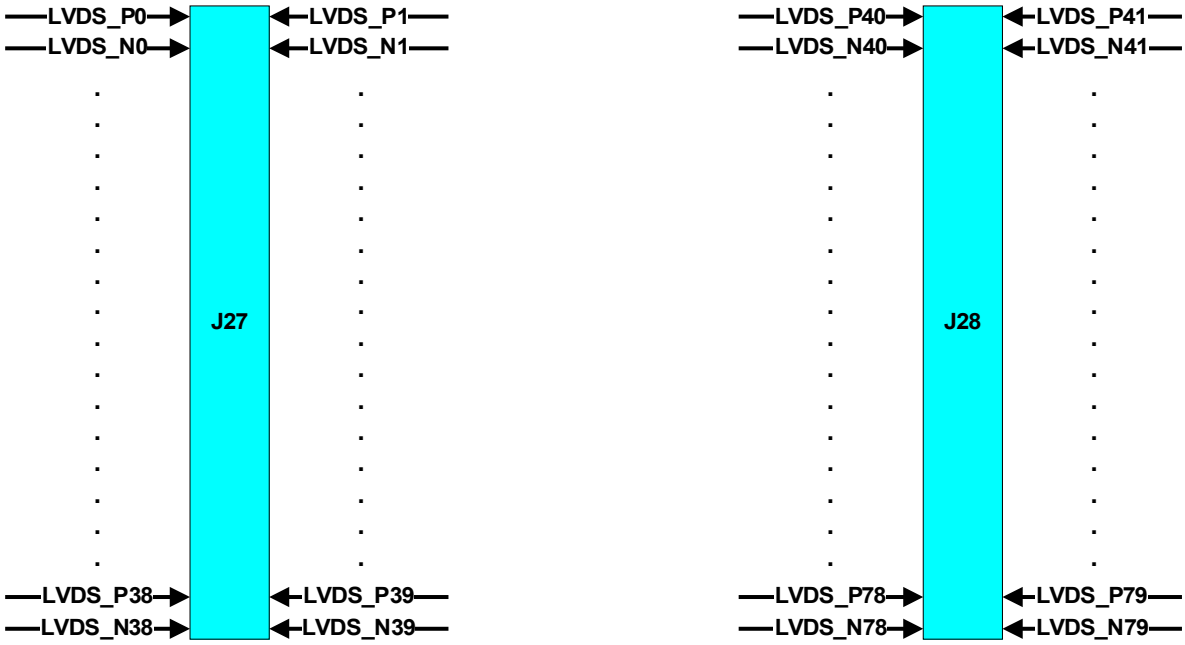

Figure 6: LVDS interface.

Connector J27							
Pin Nr.	Signal	Virtex Pin	IO-Standard	Pin Nr.	Signal	Virtex Pin	IO-Standard
1	LVDS_P0	E9	LVDS_25	41	LVDS_P20	L25	LVDS_25
2	LVDS_P1	F9	LVDS_25	42	LVDS_P21	J24	LVDS_25
3	LVDS_N0	E8	LVDS_25	43	LVDS_N20	L26	LVDS_25
4	LVDS_N1	F8	LVDS_25	44	LVDS_N21	J25	LVDS_25
5	LVDS_P2	F10	LVDS_25	45	LVDS_P22	M25	LVDS_25
6	LVDS_P3	G8	LVDS_25	46	LVDS_P23	J27	LVDS_25
7	LVDS_N2	G10	LVDS_25	47	LVDS_N22	M26	LVDS_25
8	LVDS_N3	H8	LVDS_25	48	LVDS_N23	J26	LVDS_25
9	LVDS_P4	D11	LVDS_25	49	LVDS_P24	G25	LVDS_25
10	LVDS_P5	K11	LVDS_25	50	LVDS_P25	H25	LVDS_25
11	LVDS_N4	D10	LVDS_25	51	LVDS_N24	G26	LVDS_25
12	LVDS_N5	J11	LVDS_25	52	LVDS_N25	H24	LVDS_25
13	LVDS_P6	D12	LVDS_25	53	LVDS_P26	F25	LVDS_25
14	LVDS_P7	H10	LVDS_25	54	LVDS_P27	G27	LVDS_25
15	LVDS_N6	C12	LVDS_25	55	LVDS_N26	F26	LVDS_25
16	LVDS_N7	H9	LVDS_25	56	LVDS_N27	H27	LVDS_25
17	LVDS_P8	A13	LVDS_25	57	LVDS_P28	H28	LVDS_25
18	LVDS_P9	J10	LVDS_25	58	LVDS_P29	E28	LVDS_25
19	LVDS_N8	B12	LVDS_25	59	LVDS_N28	G28	LVDS_25
20	LVDS_N9	J9	LVDS_25	60	LVDS_N29	F28	LVDS_25
21	LVDS_P10	K8	LVDS_25	61	LVDS_P30	E26	LVDS_25
22	LVDS_P11	B13	LVDS_25	62	LVDS_P31	K28	LVDS_25
23	LVDS_N10	K9	LVDS_25	63	LVDS_N30	E27	LVDS_25
24	LVDS_N11	C13	LVDS_25	64	LVDS_N31	L28	LVDS_25
25	LVDS_P12	G11	LVDS_25	65	LVDS_P32	K27	LVDS_25
26	LVDS_P13	M8	LVDS_25	66	LVDS_P33	M28	LVDS_25
27	LVDS_N12	G12	LVDS_25	67	LVDS_N32	K26	LVDS_25
28	LVDS_N13	L8	LVDS_25	68	LVDS_N33	N28	LVDS_25
29	LVDS_P14	F11	LVDS_25	69	LVDS_P34	P26	LVDS_25
30	LVDS_P15	M10	LVDS_25	70	LVDS_P35	N24	LVDS_25
31	LVDS_N14	E11	LVDS_25	71	LVDS_N34	P27	LVDS_25
32	LVDS_N15	L9	LVDS_25	72	LVDS_N35	P24	LVDS_25
33	LVDS_P16	E12	LVDS_25	73	LVDS_P36	P25	LVDS_25
34	LVDS_P17	N10	LVDS_25	74	LVDS_P37	R24	LVDS_25
35	LVDS_N16	E13	LVDS_25	75	LVDS_N36	N25	LVDS_25
36	LVDS_N17	N9	LVDS_25	76	LVDS_N37	T24	LVDS_25
37	LVDS_P18	F13	LVDS_25	77	LVDS_P38	AN14	LVDS_25
38	LVDS_P19	K24	LVDS_25	78	LVDS_P39	AB10	LVDS_25
39	LVDS_N18	G13	LVDS_25	79	LVDS_N38	AP14	LVDS_25
40	LVDS_N19	L24	LVDS_25	80	LVDS_N39	AA10	LVDS_25

Table 8: LVDS connector J27.

			Connector J28				
Pin Nr.	Signal	Virtex Pin	IO-Standard	Pin Nr.	Signal	Virtex Pin	IO-Standard
1	LVDS_P40	AN13	LVDS_25	41	LVDS_P60	J20	LVDS_25
2	LVDS_P41	AA8	LVDS_25	42	LVDS_P61	AA25	LVDS_25
3	LVDS_N40	AM13	LVDS_25	43	LVDS_N60	J21	LVDS_25
4	LVDS_N41	AA9	LVDS_25	44	LVDS_N61	AA26	LVDS_25
5	LVDS_P42	AP12	LVDS_25	45	LVDS_P62	AB27	LVDS_25
6	LVDS_P43	AC8	LVDS_25	46	LVDS_P63	Y24	LVDS_25
7	LVDS_N42	AN12	LVDS_25	47	LVDS_N62	AC27	LVDS_25
8	LVDS_N43	AB8	LVDS_25	48	LVDS_N63	AA24	LVDS_25
9	LVDS_P44	AM12	LVDS_25	49	LVDS_P64	AB25	LVDS_25
10	LVDS_P45	AC10	LVDS_25	50	LVDS_P65	AC28	LVDS_25
11	LVDS_N44	AM11	LVDS_25	51	LVDS_N64	AB26	LVDS_25
12	LVDS_N45	AC9	LVDS_25	52	LVDS_N65	AD27	LVDS_25
13	LVDS_P46	AL11	LVDS_25	53	LVDS_P66	AB28	LVDS_25
14	LVDS_P47	AE8	LVDS_25	54	LVDS_P67	AG28	LVDS_25
15	LVDS_N46	AL10	LVDS_25	55	LVDS_N66	AA28	LVDS_25
16	LVDS_N47	AD9	LVDS_25	56	LVDS_N67	AH28	LVDS_25
17	LVDS_P48	AD10	LVDS_25	57	LVDS_P68	AE28	LVDS_25
18	LVDS_P49	AK11	LVDS_25	58	LVDS_P69	AK26	LVDS_25
19	LVDS_N48	AD11	LVDS_25	59	LVDS_N68	AF28	LVDS_25
20	LVDS_N49	AJ11	LVDS_25	60	LVDS_N69	AJ27	LVDS_25
21	LVDS_P50	AK8	LVDS_25	61	LVDS_P70	AK29	LVDS_25
22	LVDS_P51	AF9	LVDS_25	62	LVDS_P71	AK28	LVDS_25
23	LVDS_N50	AK9	LVDS_25	63	LVDS_N70	AJ29	LVDS_25
24	LVDS_N51	AF10	LVDS_25	64	LVDS_N71	AK27	LVDS_25
25	LVDS_P52	AJ9	LVDS_25	65	LVDS_P72	AH27	LVDS_25
26	LVDS_P53	AF11	LVDS_25	66	LVDS_P73	AF24	LVDS_25
27	LVDS_N52	AJ10	LVDS_25	67	LVDS_N72	AJ26	LVDS_25
28	LVDS_N53	AE11	LVDS_25	68	LVDS_N73	AG25	LVDS_25
29	LVDS_P54	AH9	LVDS_25	69	LVDS_P74	AG27	LVDS_25
30	LVDS_P55	AG8	LVDS_25	70	LVDS_P75	AF25	LVDS_25
31	LVDS_N54	AH10	LVDS_25	71	LVDS_N74	AG26	LVDS_25
32	LVDS_N55	AH8	LVDS_25	72	LVDS_N75	AF26	LVDS_25
33	LVDS_P56	AG10	LVDS_25	73	LVDS_P76	AE27	LVDS_25
34	LVDS_P57	J16	LVDS_25	74	LVDS_P77	AC25	LVDS_25
35	LVDS_N56	AG11	LVDS_25	75	LVDS_N76	AE26	LVDS_25
36	LVDS_N57	J17	LVDS_25	76	LVDS_N77	AC24	LVDS_25
37	LVDS_P58	L19	LVDS_25	77	LVDS_P78	AD26	LVDS_25
38	LVDS_P59	H14	LVDS_25	78	LVDS_P79	AD24	LVDS_25
39	LVDS_N58	K19	LVDS_25	79	LVDS_N78	AD25	LVDS_25
40	LVDS_N59	H15	LVDS_25	80	LVDS_N79	AE24	LVDS_25

Table 9: LVDS connector J28.

8. PCI Express interface.

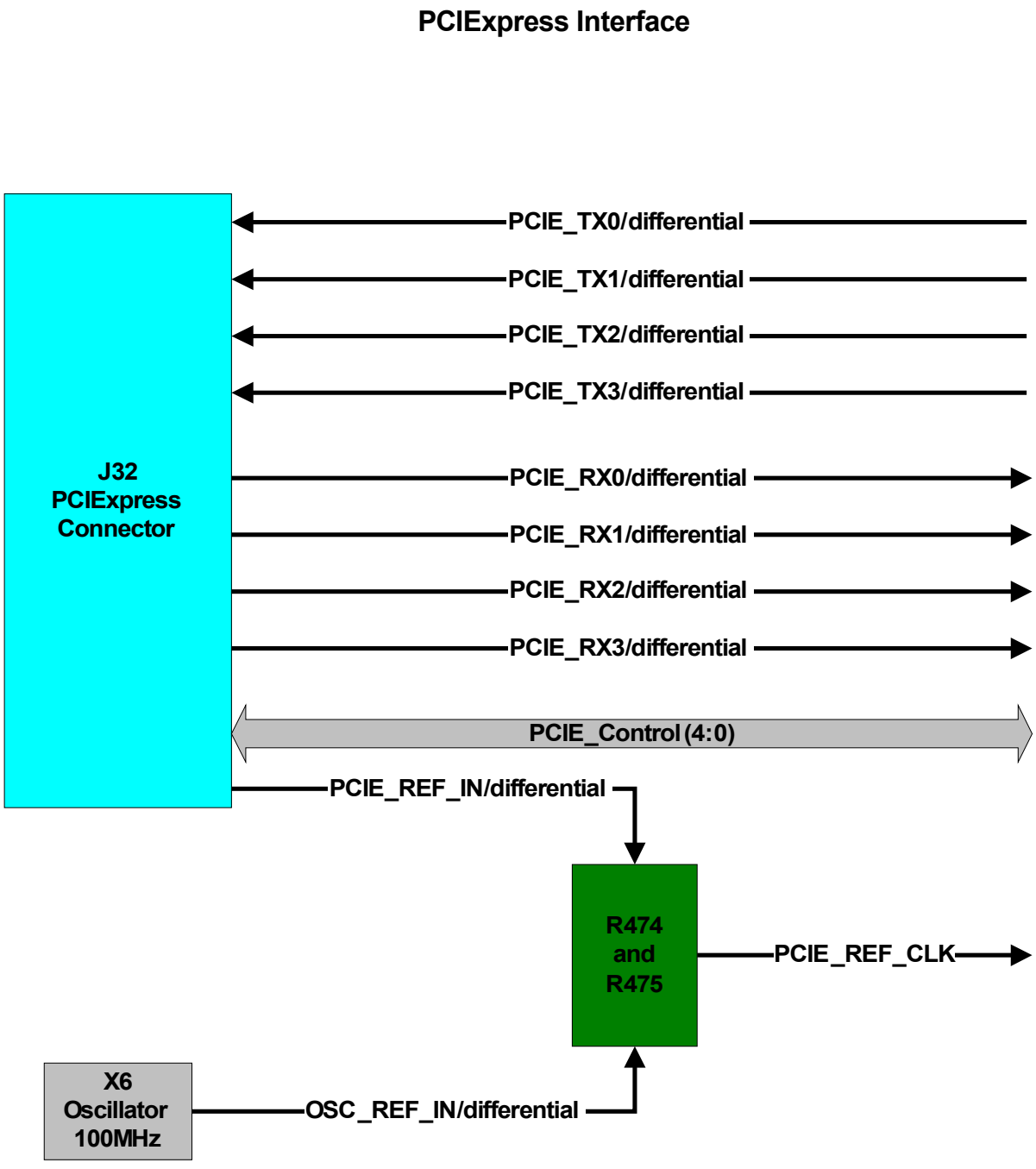

Figure 7: PCIExpress interface.

PCIE_RX_P0	A2	A3		Receiver Lane 0
PCIE_RX_N0	A3	A2		inv. Receiver Lane 0
PCIE_RX_P1	A5	D1		Receiver Lane 1
PCIE_RX_N1	A6	C1		inv. Receiver Lane 1
PCIE_RX_P2	A8	G1		Receiver Lane 2
PCIE_RX_N2	A9	H1		inv. Receiver Lane 2
PCIE_RX_P3	A11	K1		Receiver Lane 3
PCIE_RX_N3	A12	J1		inv. Receiver Lane 3
PCIE_REF_CLK_P	A14	E4		reference clock input
PCIE_REF_CLK_N	A15	D4		reference clock input
PCIE_CTRL0	A17	AG23		PCIE-Control
PCIE_CTRL1	A18	AF13		PCIE-Control
PCIE_CTRL2	A19	AG12		PCIE-Control
PCIE_TX_P0	B2	B4		Transmitter Lane 0
PCIE_TX_N0	B3	B3		inv. Transmitter Lane 0
PCIE_TX_P1	B5	E2		Transmitter Lane 1
PCIE_TX_N1	B6	D2		inv. Transmitter Lane 1
PCIE_TX_P2	B8	F2		Transmitter Lane 2
PCIE_TX_N2	B9	G2		inv. Transmitter Lane 2
PCIE_TX_P3	B11	L2		Transmitter Lane 3
PCIE_TX_N3	B12	L2		inv. Transmitter Lane 3
PCIE_CTRL3	B18	AE22		PCIE-Control
PCIE_CTRL4	B19	AE23		PCIE-Control

Table10 : PCIE Connections

9. SFP interface.

The ADDA_MGT board features three SFP (Small Factor Pluggable) connectors for optical links. The connectors are directly connected to high speed SERDES of Virtex5 (Figure 8). Table 11, 12 and 13 describes signal/pin assignments for SFP connectors.

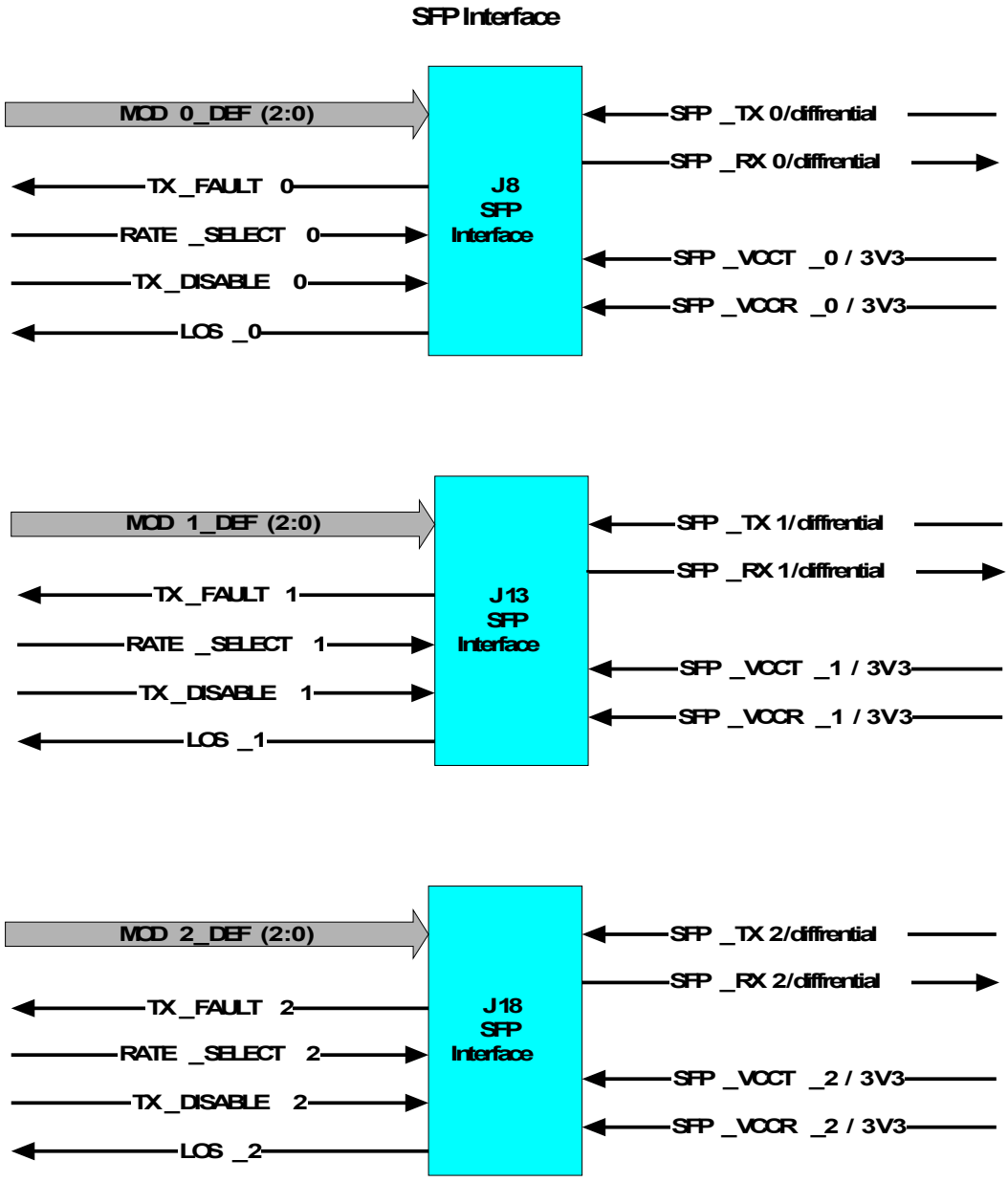

Figure 8: SFP interface.

		SFP0		
	J8	Virtex5		
Signal	Pin Nr.	Pin Nr.	IO-Standard	Function
SFP_TX_P0	18	M2	LVPECL_25	Transmitter0 Data Out
SFP_TX_N0	19	N2	LVPECL_25	Inv. Transmitter0 Data Out
SFP_RX_P0	13	N1	LVPECL_25	Receiver0 Data In
SFP_RX_N0	12	P1	LVPECL_25	Inv. Receiver0 Data In
MOD0_DEF0	6	AH20	LVTTL	Module Definition
MOD0_DEF1	5	AG13	LVTTL	Module Definition
MOD0_DEF2	4	AH12	LVTTL	Module Definition
TX_FAULT0	2	AG22	LVTTL	Transmitter0 Fault Indication
TX_DISABLE0	3	AH22	LVTTL	Transmitter0 Disable
RATE_SELECT0	7	AH19	LVTTL	Rata Rate Select
LOS_0	8	AE13	LVTTL	Loss of Signal

Table11: SFP0 interface.

		SFP1		
	J13	Virtex5		
Signal	Pin Nr.	Pin Nr.	IO-Standard	Function
SFP_TX_P1	18	V2	LVPECL_25	Transmitter1 Data Out
SFP_TX_N1	19	W2	LVPECL_25	Inv. Transmitter1 Data Out
SFP_RX_P1	13	W1	LVPECL_25	Receiver1 Data In
SFP_RX_N1	12	Y1	LVPECL_25	Inv. Receiver1 Data In
MOD1_DEF0	6	AH15	LVTTL	Module Definition
MOD1_DEF1	5	AG20	LVTTL	Module Definition
MOD1_DEF2	4	AG21	LVTTL	Module Definition
TX_FAULT1	2	AH14	LVTTL	Transmitter1 Fault Indication
TX_DISABLE1	3	AH13	LVTTL	Transmitter1 Disable
RATE_SELECT1	7	AG15	LVTTL	Data Rate Select
LOS_1	8	AE12	LVTTL	Loss of Signal

Table12:SFP1 interface.

		SFP2		
	J18	Virtex5		
Signal	Pin Nr.	Pin Nr.	IO-Standard	Function
SFP_TX_P2	18	AD2	LVPECL_25	Transmitter2 Data Out
SFP_TX_N2	19	AE2	LVPECL_25	Inv. Transmitter2 Data Out
SFP_RX_P2	13	AE1	LVPECL_25	Receiver2 Data In
SFP_RX_N2	12	AF1	LVPECL_25	Inv. Receiver2 Data In
MOD2_DEF0	6	AF18	LVTTL	Module Definition
MOD2_DEF1	5	AG16	LVTTL	Module Definition
MOD2_DEF2	4	AH17	LVTTL	Module Definition
TX_FAULT2	2	AG18	LVTTL	Transmitter2 Fault Indication
TX_DISABLE2	3	AF19	LVTTL	Transmitter2 Disable
RATE_SELECT2	7	AE18	LVTTL	Data Rate Select
LOS_2	8	AF23	LVTTL	Loss of Signal

Table13:SFP2 interface.

10. MMCX Rockets interface.

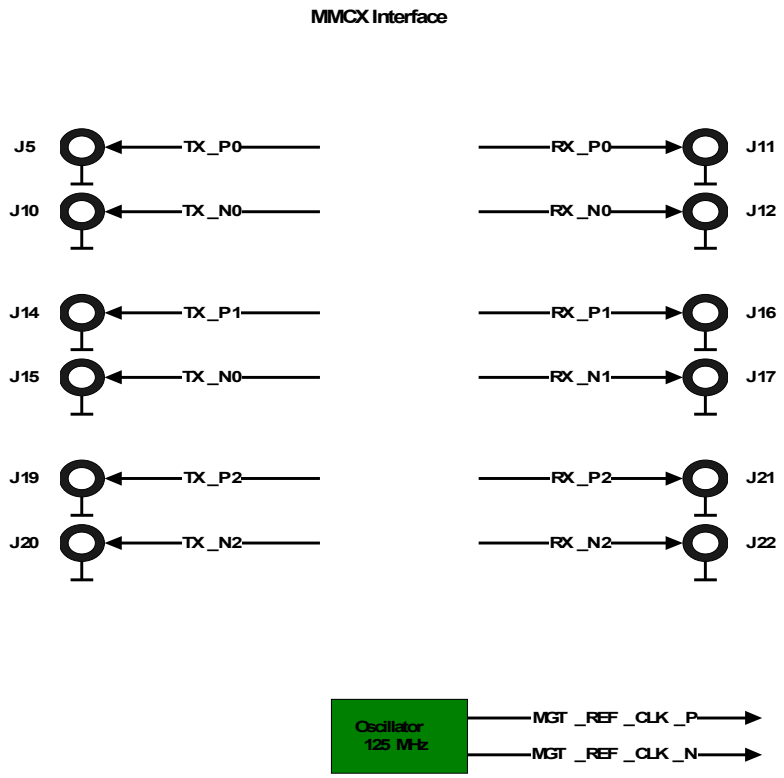

Figure 9: MMCX Rockets.

		MMCX		
		Virtex5		
Signal	Connector	Pin Nr.	IO-Standard	Function
MMCX_TX_P0	J9	U2	LVPECL_25	MMCX-Transmitter0 Out
MMCX_TX_N0	J10	T2	LVPECL_25	inv. MMCX-Transmitter0 Out
MMCX_TX_P1	J14	AC2	LVPECL_25	MMCX-Transmitter1 Out
MMCX_TX_N1	J15	AB2	LVPECL_25	inv. MMCX-Transmitter1 Out
MMCX_TX_P2	J19	AJ2	LVPECL_25	MMCX-Transmitter2 Out
MMCX_TX_N2	J20	AH2	LVPECL_25	inv. MMCX-Transmitter2 Out
MMCX_RX_P0	J11	T1	LVPECL_25	MMCX-Receiver0 Out
MMCX_RX_N0	J12	R1	LVPECL_25	inv. MMCX-Receiver0 Out
MMCX_RX_P1	J16	AB1	LVPECL_25	MMCX-Receiver1 Out
MMCX_RX_N1	J17	AA1	LVPECL_25	inv. MMCX-Receiver1 Out
MMCX_RX_P2	J21	AH1	LVPECL_25	MMCX-Receiver2 Out
MMCX_RX_N2	J22	AG1	LVPECL_25	inv. MMCX-Receiver2 Out

Table14: MMCX interface.

11. Measurement and user connectors.

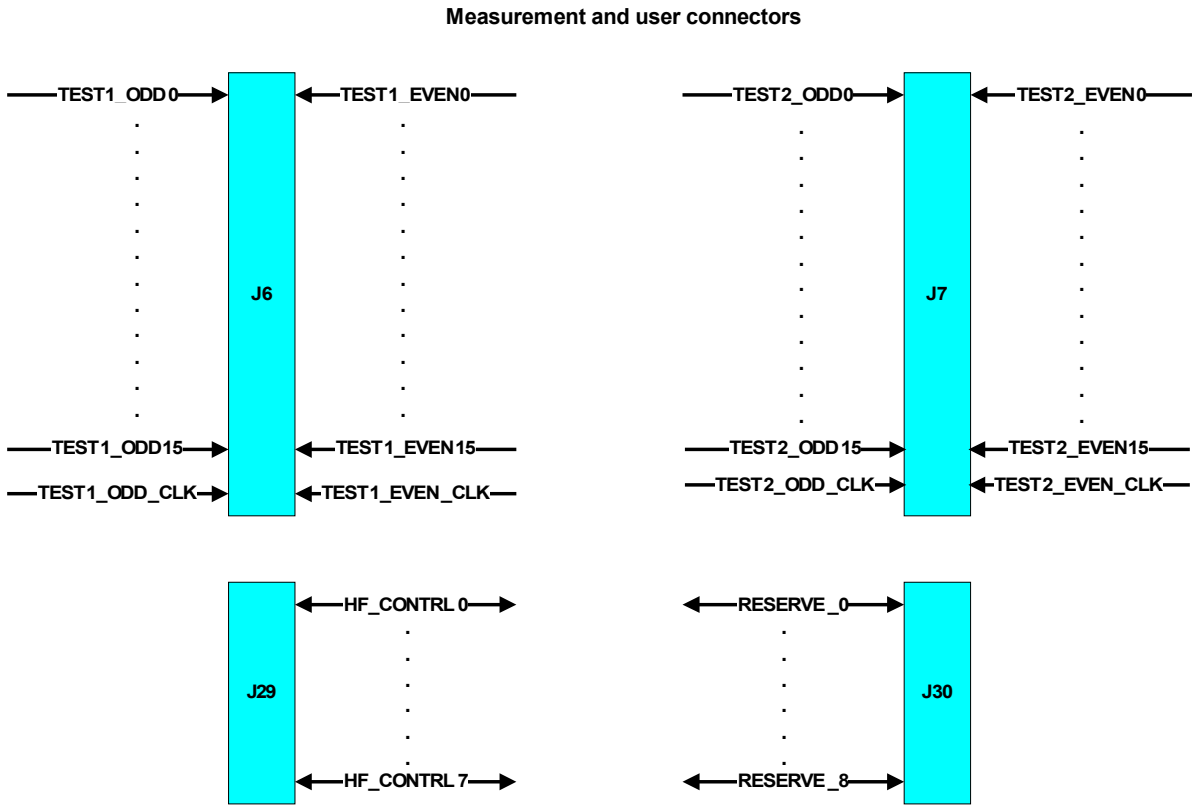

Figure 10: Measurement and user connectors.

TEST CONNECTOR1			
	J6	Virtex5	
Signal	Pin Nr.	Pin Nr.	IO-Standard
TEST1_ODD0	7	W24	LVTTL
TEST1_ODD1	11	V24	LVTTL
TEST1_ODD2	15	Y26	LVTTL
TEST1_ODD3	19	W26	LVTTL
TEST1_ODD4	23	V25	LVTTL
TEST1_ODD5	27	W25	LVTTL
TEST1_ODD6	31	Y27	LVTTL
TEST1_ODD7	35	W27	LVTTL
TEST1_ODD8	39	V30	LVTTL
TEST1_ODD9	43	W30	LVTTL
TEST1_ODD10	47	V28	LVTTL
TEST1_ODD11	51	V27	LVTTL
TEST1_ODD12	55	W31	LVTTL
TEST1_ODD13	59	Y31	LVTTL
TEST1_ODD14	63	W29	LVTTL
TEST1_ODD15	67	V29	LVTTL
TEST1_ODD_CLK	79	Y28	LVTTL
TEST1_EVEN0	8	Y29	LVTTL
TEST1_EVEN1	12	AB31	LVTTL
TEST1_EVEN2	16	AA31	LVTTL
TEST1_EVEN3	20	AB30	LVTTL
TEST1_EVEN4	24	AC30	LVTTL
TEST1_EVEN5	28	AA29	LVTTL
TEST1_EVEN6	32	AA30	LVTTL
TEST1_EVEN7	36	AD31	LVTTL
TEST1_EVEN8	40	AE31	LVTTL
TEST1_EVEN9	44	AD30	LVTTL
TEST1_EVEN10	48	AC29	LVTTL
TEST1_EVEN11	52	AF31	LVTTL
TEST1_EVEN12	56	AG31	LVTTL
TEST1_EVEN13	60	AE29	LVTTL
TEST1_EVEN14	64	AD29	LVTTL
TEST1_EVEN15	68	AJ31	LVTTL
TEST1_EVEN_CLK	80	AK31	LVTTL

Table15

TEST CONNECTOR2			
	J7	Virtex5	
Signal	Pin Nr.	Pin Nr.	IO-Standard
TEST2_ODD0	7	E29	LVTTL
TEST2_ODD1	11	F29	LVTTL
TEST2_ODD2	15	G30	LVTTL
TEST2_ODD3	19	F30	LVTTL
TEST2_ODD4	23	H29	LVTTL
TEST2_ODD5	27	J29	LVTTL
TEST2_ODD6	31	F31	LVTTL
TEST2_ODD7	35	E31	LVTTL
TEST2_ODD8	39	L29	LVTTL
TEST2_ODD9	43	K29	LVTTL
TEST2_ODD10	47	H30	LVTTL
TEST2_ODD11	51	G31	LVTTL
TEST2_ODD12	55	J30	LVTTL
TEST2_ODD13	59	J31	LVTTL
TEST2_ODD14	63	L30	LVTTL
TEST2_ODD15	67	M30	LVTTL
TEST2_ODD_CLK	79	N29	LVTTL
TEST2_EVEN0	8	N30	LVTTL
TEST2_EVEN1	12	R28	LVTTL
TEST2_EVEN2	16	R29	LVTTL
TEST2_EVEN3	20	T31	LVTTL
TEST2_EVEN4	24	R31	LVTTL
TEST2_EVEN5	28	U30	LVTTL
TEST2_EVEN6	32	T30	LVTTL
TEST2_EVEN7	36	T28	LVTTL
TEST2_EVEN8	40	T29	LVTTL
TEST2_EVEN9	44	U27	LVTTL
TEST2_EVEN10	48	U28	LVTTL
TEST2_EVEN11	52	R26	LVTTL
TEST2_EVEN12	56	R27	LVTTL
TEST2_EVEN13	60	U26	LVTTL
TEST2_EVEN14	64	T26	LVTTL
TEST2_EVEN15	68	U25	LVTTL
TEST2_EVEN_CLK	80	T25	LVTTL

Table16

	User Connectors		
	J30	Virtex5	
Signal	Pin.Nr	Pin Nr.	IO-Standard
RESERVE0	1	AH7	LVTTL
RESERVE1	2	AJ7	LVTTL
RESERVE2	3	AJ6	LVTTL
RESERVE3	4	AN32	LVTTL
RESERVE4	5	AP32	LVTTL
RESERVE5	6	AN33	LVTTL
RESERVE6	7	AK6	LVTTL
RESERVE7	8	V10	LVTTL
RESERVE8	9	V9	LVTTL
GND	10		
Signal	J29	Pin Nr.	IO-Standard
RESERVE9	1	K31	LVTTL
RESERVE10	2	AH30	LVTTL
RESERVE11	3	P29	LVTTL
RESERVE12	4	AH29	LVTTL
RESERVE13	5	P31	LVTTL
RESERVE14	6	AG30	LVTTL
RESERVE15	7	M31	LVTTL
RESERVE16	9	AJ30	LVTTL
GND	8, 10		

Table15

12. DC-Specification:

	Min	Typ	Max
Power Supply Voltage Range	+4,5 V	+5 V	+5,5 V
Power Supply Current		2A	