IAF GmbH
Berliner Straße 52j
38104 Braunschweig
Germany

Phone: ++49 531 379 88-0
Fax: ++49 531 379 88-30
e-mail: info@iaf-bs.de
www.iaf-bs.de

Virtex5 SX95 Board (Rev. 1.0)

(Datasheet Web Rev. 1.0 August 2010)

Figure 1: Picture of the Virtex5 SX95 Board

The Board has the following key features:

- Xilinx Virtex 5 SX95 T FPGA (XC5VSX95T)
- Usable as standalone board or as Add-On-Module for IAF FFP Basic+-Board or IAF LTE-S-Board
- Single +5V power supply, with on board power-conversion for all needed voltages
- Clock-generation on board
    - 100MHz for FPGA
    - 125MHz or external differential clock via connectors for GTPs
- 128 Mbyte Flash-Prom on board
- 4M * 18 QDR II RAM on board
- 2 MGT-Lanes on MMCX-connectors for free use
- ASP-Measurment Connector for usage with Agilent-Devices
- JTAG-programming via 14-Pin Connector for Xilinx-Programming-Cable
- 4 free programmable LEDs
- EEPROM for Board Parameter

Block Diagramm:

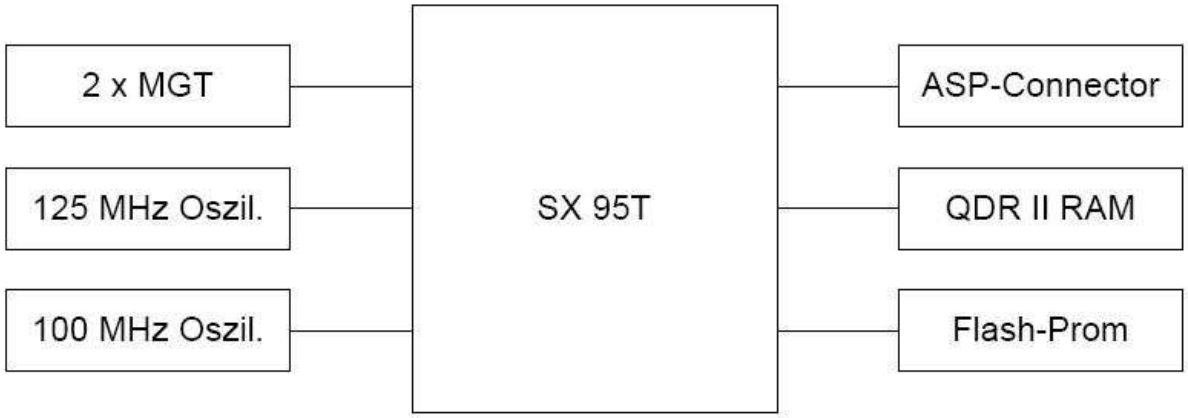

Figure 2: Block Diagram of Virtex5 SX95 Board

Board-Dimensions 60 mm x 94 mm:

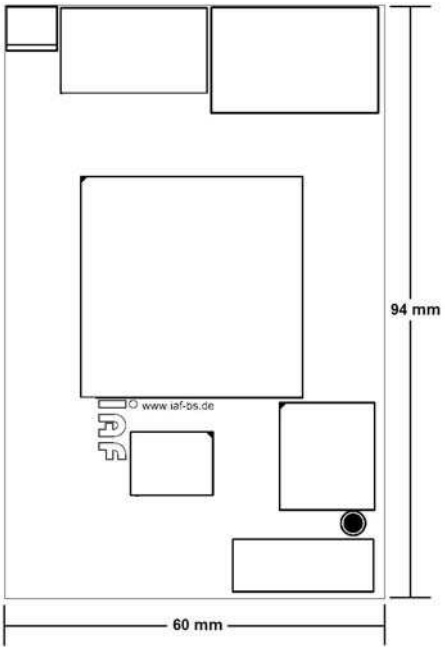

Figure 3: Board-Dimensions of Virtex5 SX95 Board

Layout and components:

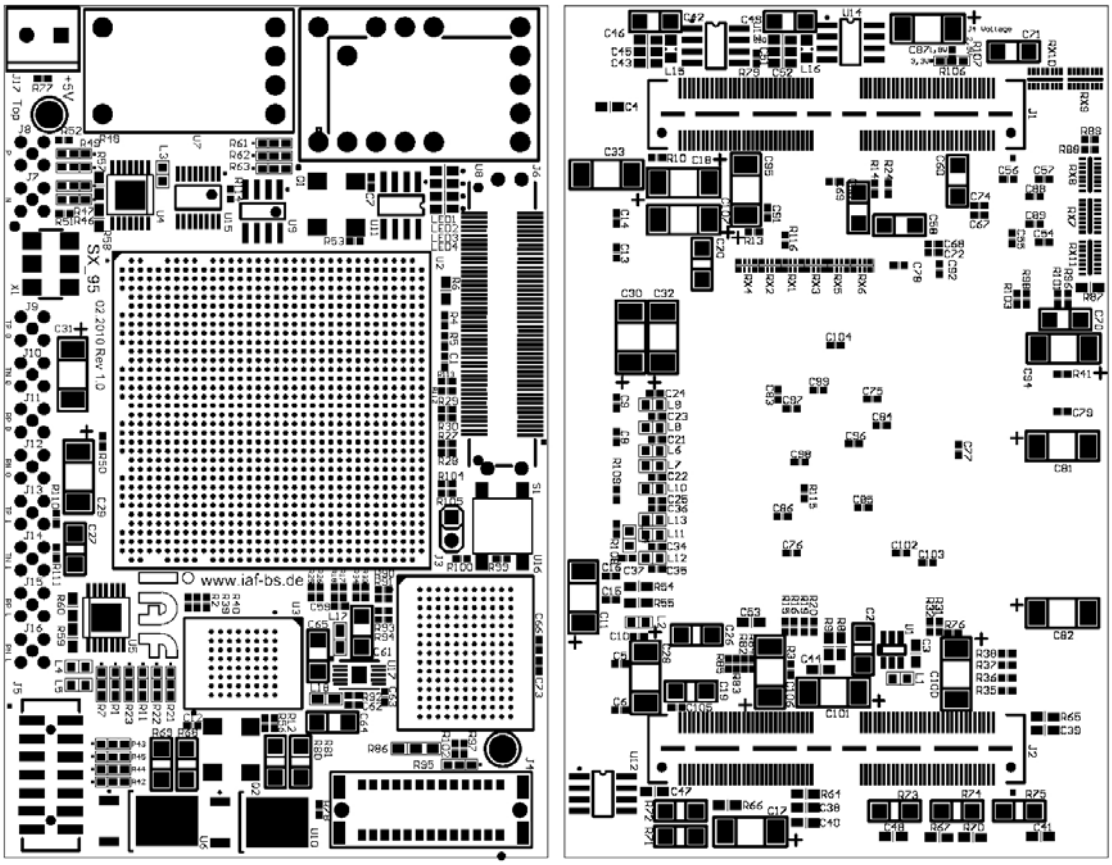

Figure 4: Top- and Bottom-Layout of Virtex5 SX95 Board

J1/J2	Connectors to LTE-S-Board QTH-060 Samtec
J3	2-Pin Connector for external Reset-Button
J4	26-Pin Connector ERNI SMC
J5	14-Pin Connector for JTAG-Programming of Virtex 5 MOLEX 3 321420
J6	AGILENT ASP-Test Connector
J7	alternative positive differential clock input for GTPs
J8	alternative negative differential clock input for GTPs
J9	MGT P0 TX
J10	MGT N0 TX
J11	MGT P0 RX
J12	MGT N0 RX
J13	MGT P1 TX
J14	MGT N1 TX
J15	MGT P1 RX
J16	MGT N1 RX

J17	5V Power Connector
LED_1	green LED, free configurable by FPGA
LED_2	green LED, free configurable by FPGA
LED_3	green LED, free configurable by FPGA
LED_4	green LED, free configurable by FPGA
Q1	50 MHz Oscillator single ended for Flash
Q2	100 MHz Oscillator single ended for Virtex
S1	Reset Button
U1	power supply for system monitor
U2	Virtex-5-SX-95T Xilinx
U3	Flash PROM 128 Mb = 8M * 16XCF128XFTG64C Xilinx
U4	5V-1,2V linear Power Converter for MGTs MAX852X Maxim
U5	5V-1V linear Power Converter for MGTs MAX852X Maxim
U6	Voltage Regulator LD1086 ST Microelectronics 3,3V
U7	5V-1V Power Converter
U8	5V-2,5V Power Converter
U9	EEPROM for Board Parameter
U10	Voltage Regulator LD1086 ST Microelectronics 1,8V
U11-U14	High-Side Current-Sense Amplifier MAX4172ESA Maxim
U15	Analog-to-Digital Converter MAX1039 Maxim
U16	QDR II SRAM 4Mx18 K7R641882M Samsung
U17	Termination Regulator TPS51100 Texas Instruments
X1	125 MHz MGT Clock Oscillator differential

Power supply:

The Virtex5 SX95 Board only needs a single + 5V power supply. The power-conversion for all other needed supplies is integrated on the board.

Figure 5 shows the layout and the pinout of the power-connector J17.

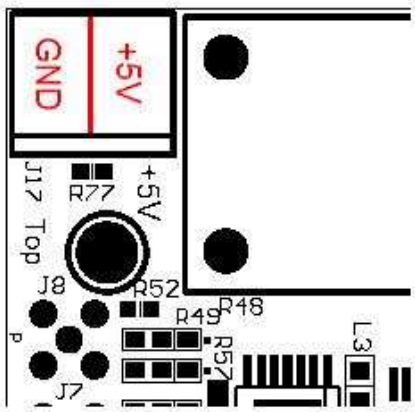

Figure 5: Power-Connector of Virtex5 SX95 Board

Programming of the Virtex5 SX95 FPGA :

To program the FPGA the Xilinx Download Cable can be used. J5 is the 14-Pin connector which makes the needed signals available for the user.

LEDs:

The FPGA-Board has four LEDs, which can be controlled by the FPGA.

Control bus:

A control bus on connector J1 is part of the extension slot connector. It allows the LTE-S-Board to identify the type of extension board by reading an ID-Prom at a fix position.

Via the control-signals Ex1_CNTRL0 - Ex1_CNTRL5 it is possible to program the FPGA directly by the LTE-S-Board.

Clock

On the board three oscillators can be found.

A 100 MHz oscillator for FPGA clock-supply, a 50 MHz oscillator for the Flash-PROM and a differential 125 MHz oscillator for the MGTs.

MGTs

Two MGT-Lanes of the FPGA are plugged to connectors **(**J9 - J16). For the MGT clock supply a differential 125 MHz oscillator is positioned on the module.
Alternatively an external differential clock can be plugged to the FPGA via the connectors J7 and J8.

Flash PROM

The Flash PROM is a XCF128XFTG64C from Xilinx with 128 Mb = 8M * 16.

Not all signals of the Flash are directly connected to the FPGA. Some signals are connected parallel to a connector and for some signals a resistor works like a switch to select which signals are connected to the FPGA.

QDR II SRAM

The QDR II SRAM is a K7R641882M from Samsung with 4Mx18.

All signals are directly connected to the FPGA.