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LTE-S Hardware Platform (Rev. 3.0)

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Combined DSP / FPGA platform for development of next generation radio interfaces like 3G LTE. The combination of high performance FPGA and multicore communications infrastructure DSP offers a high flexibility signal processing performance.

The platform has been designed for implementation of 3G LTE downlink and uplink layer 1 and layer 2 processing. It is well suited for all applications which require high bandwidth real-time processing.

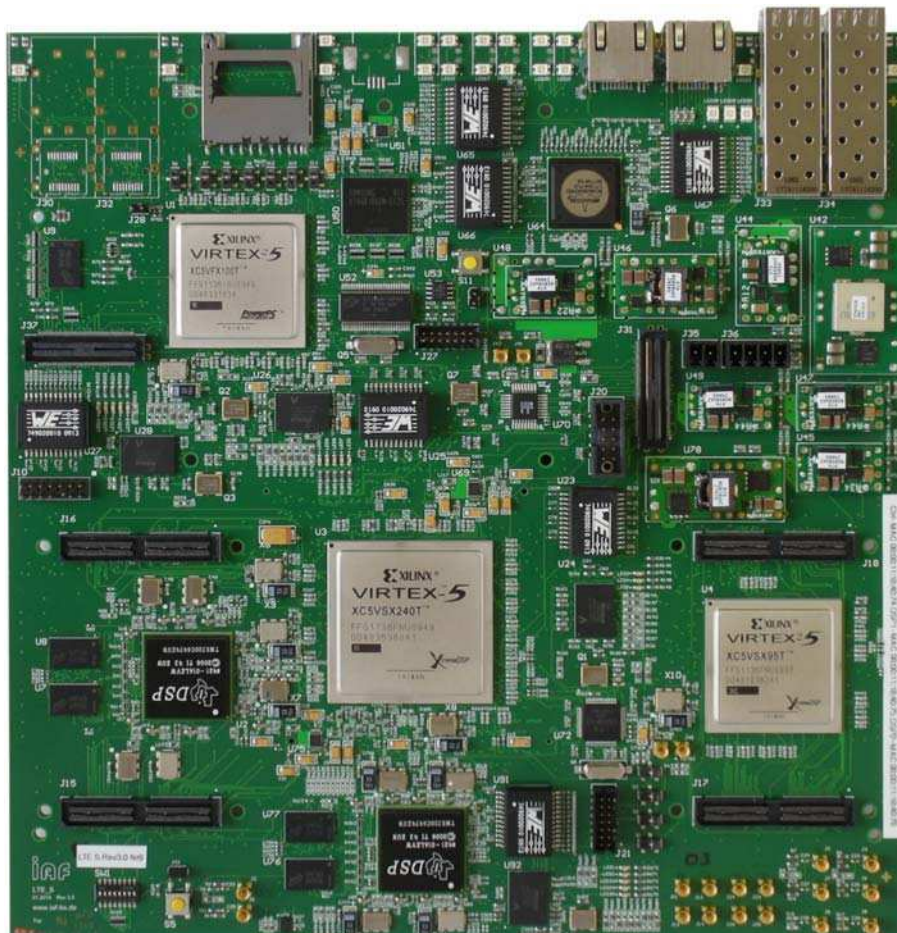


Figure 1: Picture of LTE-S Hardware Platform

Applications:

- Hardware platform for high bandwidth real-time signal processing
- Base station development
- Test terminal development
- 3G LTE physical layer decoding
- 3G LTE MAC layer decoding
- 3G LTE higher layer implementation

The Board has the following key features:

- 2 user-programmable FPGAs (1 XC5VSX240T and 1 XC5VSX95T)
- 2 Faraday DSPs TMS320TCI6488 in Serial RapidIO chain
- CPRI interface for RF frontend connection
- Gigabit Ethernet interface for core network connection
- 1 Gigabit Ethernet interface using Broadcom switch to the 2 FPGAs and 2 DSPs
- 1 direct Gigabit Ethernet interface to XC5VSX240T
- 4 GB DDRII RAM connected to XC5VSX240T in 2 DIMM modules
- 256 MB DDRII RAM for each DSP
- 2 SFP serial gigabit connections to XC5VSX240T for e.g. CPRI
- 2 optional SFP connections to DSP antenna interface for CPRI
- 1 optional USB 2.0
- 2 JTAG chains for FPGA and DSP
- 1 onboard PLL for global clock generation
- 1 additional PLL for CPRI clock regeneration
- 1 MMC card interface for configuration data of FPGA and DSP
- 1 XC5VFX100T as board controller using embedded Linux
- 2 firmware EEPROMs for save update over Ethernet
- several parallel connections between all 3 FPGAs
- 2 bidirectional GTP lanes between all 3 FPGAs
- 2 extension slots for several add-on modules (compatible with **FFP Basic+** format)
- 1 single 5V power supply

Block Diagramm:

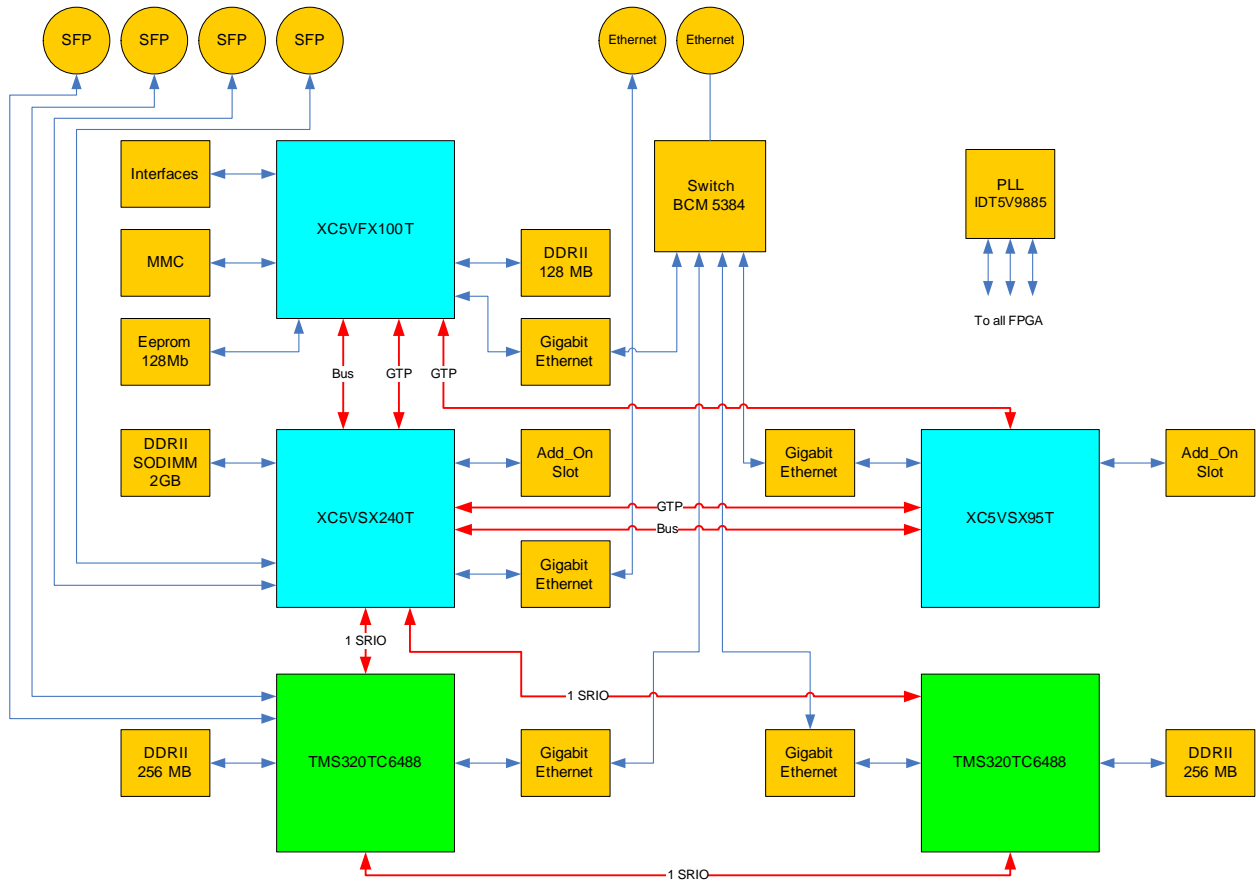


Figure 2: Functional Blocks

Functional Overview:

The board combines the power of fast and flexible FPGA architecture with the ability of multicore communications infrastructure digital signal processing. The Xilinx FPGA XC5VSX240T is connected to two DIMM modules of 2 GByte each. Two SFP type connectors provide a fast interface that is connected to GTP transceivers. It can be configured as CPRI interface for connection of Radio frontend modules. An extension slot offers the ability to add compatible add-on modules with parallel or serial data bus connection to increase the FPGA or DSP resources.

The Xilinx XC5VSX95T FPGA can be used for implementation of additional user logic and is connected to the SX240T by a parallel bus. This chip offers an extension slot too. For more logic resources a further XC5VSX95T add-on module is available.

The two DSP are connected to the XCV5SX240T via a serial RapidIO interface in daisy chain. An additional DSP can be looped into the chain via MMCX connectors. Each DSP has a separate 256 MB DDRII RAM and an Ethernet connection.

A board controller unit using a Xilinx XC5VFX100T FPGA is used to configure the complete board from the MMC card. The firmware for the board controller FPGA is loaded from redundant flash PROMs, which can be updated through the Ethernet port.

An embedded Linux operating system can be run on the FPGA internal Power PC 440 core. The OS can be configured via a separate flash. The communication to external devices can be done via Gigabit Ethernet interface running under the Linux OS.

For external data communications of user FPGA and DSP devices the several onboard Ethernet interfaces are bundled by an Ethernet switch. To have full bandwidth a separate Ethernet connection to the XC5VSX240T is integrated too. Two bidirectional GTP lines between the FPGAs can be used to share fast data between the applications. Several oscillators allow different data rates.

For flexible and configurable onboard clock generation a programmable 3 core PLL device is implemented. For evaluation purposes JTAG interfaces for FPGA and DSP are available.

The power supply is a single 5V input; all other voltages are generated onboard internally.

Interfaces:

- J44, J39 Ethernet connector
- J33, J34 SFP Connector
- J19 MMC card
- J10 JTAG DSP
- J21 JTAG FPGA
- SW1 User DIP switch
- S5 User Reset button
- J15, J16 Extension slot XC5VSX204T
- J17, J18 Extension slot XC5VSX95T
- J35, J36 Power supply
- J2, J5 external GTP clock input XC5VSX240T
- J11, J12, J13; J14, J23, J24, J25 J26 SRIO insert (R692 – R699 readjust)
- J3, J6, J4, J7 2 times LVDS global clock inputs XC5VSX240T
- J8, J9 2 times LVCMOS global clock inputs XC5VSX240T
- J41 global clock PLL output
- J42 global clock PLL reference input

Board-Dimensions – Power Supply:

Width: 234mm, Length: 240mm, Height 25mm / 45mm with / without add-on

Power Supply: 5V - 4A /16 A min / typ, normal operating conditions

Layout and components:

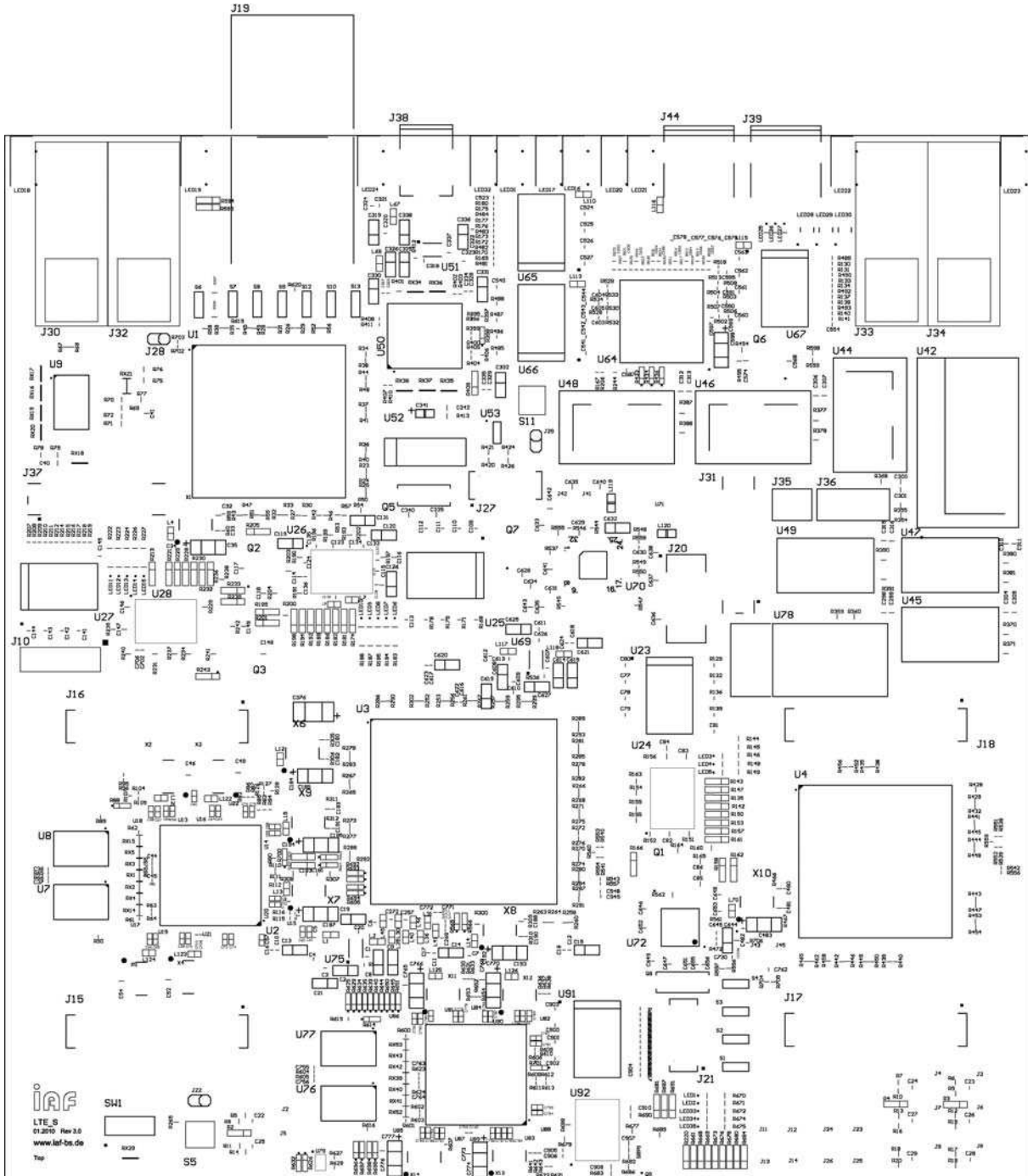


Figure3: Layout Top

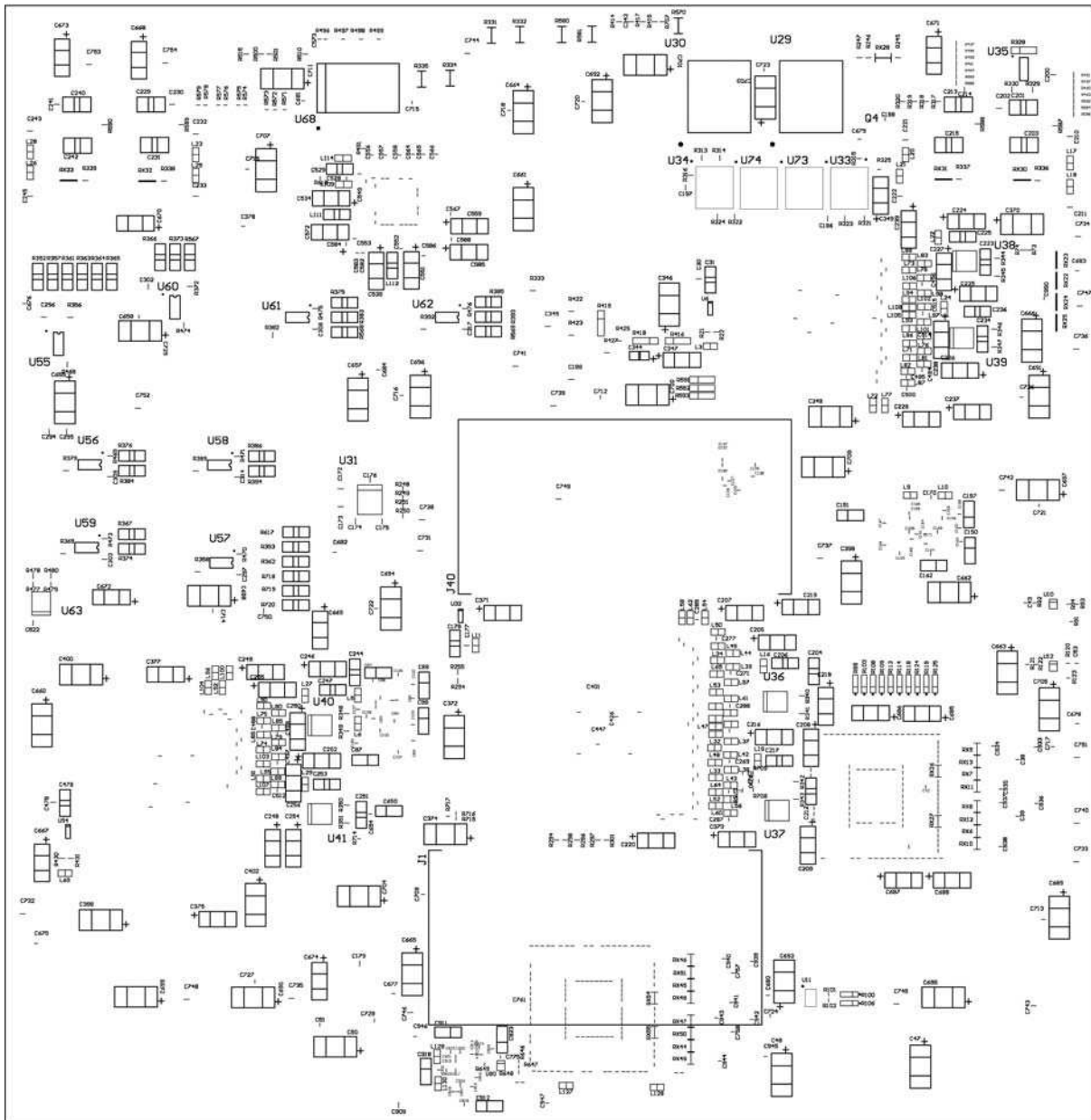


Figure 4: Layout Bottom