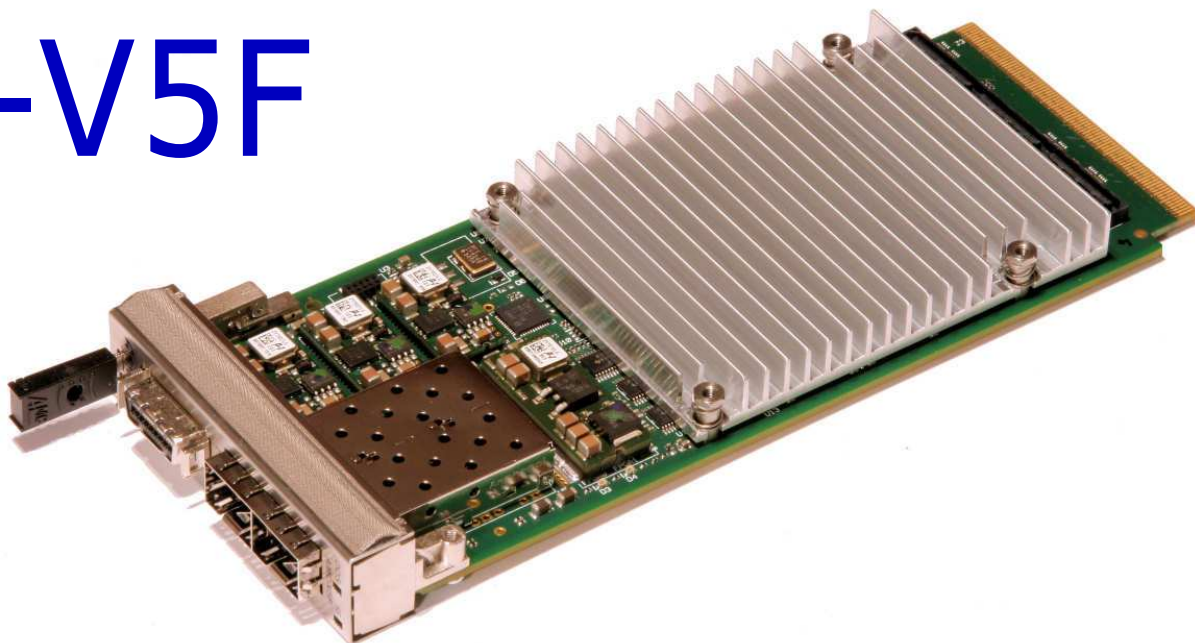# AMC-V5F

DATASHEET

A high performance FPGA based interface and processing card for wireless baseband and other applications

Optical SFP sockets for CPRI RE/REC and OBSAI RP3-01 antenna interfacing. Flexible sync options including a 1 PPS GPS clock

Multiple 10 Gbps Serial RapidIO and Gigabit Ethernet connections for system expansion

KEY FEATURES

⬥ Xilinx Virtex-5 SX95T FPGA, customer programmable (alternatives also possible)

⬥ Dual highly flexible optical front panel interfaces, for wireless antenna or other high speed data links

⬥ Advanced clock recovery and synchronisation options including master and slave modes; AMC, front panel and GPS clocks

⬥ Tundra Tsi578 Serial RapidIO Switch for full SRIO infrastructure including FPGA, AMC backplane and (optional) front panel

⬥ Full Gigabit Ethernet infrastructure

⬥ Single width, mid-size PICMG AMC.0 R2.0 Advanced Mezzanine Card

⬥ Software and firmware library support

⬥ Developed for use in OEM products

RESULTING BENEFITS

+ High performance FPGA resource for wireless baseband or customer applications

+ Industry standard CPRI and OBSAI links to wireless radios, base stations under test, or other optical data links such as SRIO

+ Covers multiple requirements for Base Stations and Test Equipment; GPS clock sync avoids a separate card in the system

+ Dependable low-latency high-bandwidth interconnect, both on and off card, at up to 10Gbps per link

+ Industry standard interconnect

+ Works with Industry standard MicroTCA and AdvancedTCA systems

+ Fast route to application code porting

+ Reduces risk and speeds time to market

The CommAgility AMC-V5F is a single width, mid-size Advanced Mezzanine Card. It is aimed at the latest wireless baseband applications but also very suitable for any high performance FPGA processing application, especially where optical interfacing or SRIO support is required.

A Xilinx Virtex-5 SX95T FPGA provides the main processing. This configures and boots from FLASH on reset, using one of 4 selectable configuration images which are customer programmable and can be updated over Ethernet. The FPGA is fully customer configurable. The FPGA build normally contains a Microblaze processor for basic board configuration and control, and a full example FPGA build and Microblaze Board Support Package is provided.

The dual SFP sockets for optical interfaces to the FPGA are key features of the AMC-V5F. These are typically used for CPRI or OBSAI interfaces, although many other options are possible. Linked to this interface is a highly flexible, low jitter programmable PLL circuit, allowing a wide range of wireless synchronisation options including a low cost 1 PPS GPS clock.

A range of build options are available, and further customisation is possible in volume, to enable the best technical and commercial fit to a customer application to be achieved.

Comm Agility

Comm Agility

HARDWARE SPECIFICATIONS

FPGA: Xilinx Virtex-5™ FPGA. Standard configuration is SX95T-2, options include LX110T, LX155T, FX100T. With:
* 2 independent banks of 128Mbytes x16 DDR2-600 SDRAM
* 128Mbytes of parallel FLASH
* 10Gbps 4x SRIO
* 2 Full-duplex Gigabit Ethernet ports
* 4x RocketIO™ to front panel 10Gbps CX4 connector, option to AMC ports 17-20

Antenna Interface: 2 SFP sockets for optical CPRI RE/REC and OBSAI RP3-01 compliant antenna interface links, connected to FPGA RocketIO. Also usable for other optical links such as SRIO, GigE or Aurora. Data rate up to 4 Gbps per link.

Clock Synchronisation: Low-jitter VCXO based PLL, digitally controlled from the FPGA. Allows clock synchronisation and distribution from an external 30.72 MHz or 1PPS GPS clock via AMC backplane, front panel (option) or SFP SERDES. IEEE1588 is also possible.

Serial RapidIO: 10Gbps 4x infrastructure using Tundra Tsi578™ switch:
* AMC.4 compliant 10Gbps 4x connections to AMC ports 4-7 and 8-11
* Dedicated 10Gbps 4x link to FPGA
* Optional Front Panel 10Gbps 4x SRIO link using CX4 connector

Ethernet: Gigabit Ethernet infrastructure using Broadcom BCM5389™ switch:
* AMC.2 (1000BASE-BX) compliant connections to AMC Ports 0 & 1
* Full-duplex 1Gbps links

IPMI: ATMega128 IPMI controller:
* AMC.0 IPMB_L interface
* FRU EEPROM data
* Power and reset control
* Real-time health monitoring

Form Factor: Advanced Mezzanine Card
* AMC.0 Rev 2.0 compliant
* Mid-size, single-width; also available as full-size on request
* For AdvancedTCA™ and MicroTCA™
* AMC.2 GigE and AMC.4 4x SRIO
* Hot swap support

CONFIGURATION AND DEBUG

* FPGA and MicroBlaze boot from FLASH.
* Choice of 4 boot images, controlled by MMC. Allows 3 user images plus one fall-back in case of boot failure.
* FLASH update utility allows new images to be downloaded over Ethernet.
* On-board debug LEDs for FPGA, power, Ethernet and SFP ports.
* Debug connector and breakout board for Xilinx JTAG and FPGA/MMC serial ports.

ENVIRONMENTAL/EMC/SAFETY

* Operating temperature: 0-40 °C ambient
* Power consumption: up to 28W max, dependent on SFPs used and FPGA load
* Designed for NEBS and ETSI compliance when used in appropriate chassis
* 2004/108/EC and FCC EMC compliant
* 2002/95/EC RoHS, 2002/96/EC WEEE and 2006/95/EC Low Voltage Directive compliant

SOFTWARE SPECIFICATIONS

FPGA: to demonstrate configuration and functionality; Xilinx ISE and EDK project

MicroBlaze Board Support Library (BSL): support for board setup and interfaces, self test and FLASH update

MMC: full management suite based on PigeonPoint BMR software

AdvancedMC™   μTCA™   AdvancedTCA®

RoHS 2002/95/EC

CommAgility Ltd   sales@commagility.com   Tel: +44 1509 228866
Loughborough, UK   www.commagility.com   Fax: +44 8452 991150

PICMG®

Datasheet describes products in development by CommAgility. Information may be subject to change. AMC-V5F P1/0908

TUNDRA™