AMC-2C6616

DATASHEET

A high performance AMC card based on TI's new C6616 DSPs and Xilinx Virtex 6, with high speed, flexible I/O

Ideal for LTE and LTE Advanced test equipment and other applications requiring very high DSP performance

Front panel I/O options: triple SFP+ (to DSP or FPGA) or dual mini-SAS

Synchronisation via front panel or AMC TCLKs; GPS receiver option

KEY FEATURES	RESULTING BENEFITS
• Dual TMS320TCI6616 multi-core DSPs	⇒ The latest high performance TI DSPs
• Xilinx Virtex-6 FPGA, LX240T-2 standard, up to LX550T possible	⇒ Cost effective, high density device; largest FPGA available if required
• Multiple banks of DDR3 SDRAM for both DSPs and FPGA	⇒ Latest external memory technology with multiple high bandwidth buses
• Flash memory	⇒ Stores multiple FPGA images & software
• IDT CPS-1848 Serial RapidIO switch	⇒ SRIO V2.1 at up to 20Gbps per port
• Broadcom BCM5389 Ethernet switch	⇒ Gigabit Ethernet to all main devices
• Separate "glue logic" for board configuration and management	⇒ Allows control, FPGA configuration and FLASH reprogramming over SRIO/SPI
• Three front panel SFP+ optical interfaces configurable as CPRI, OBSAI, GigE, SRIO or other standards	⇒ Flexible high-speed optical links, especially suitable for wireless applications. Options to link to DSP AIF2 or FPGA.
• Dual mini-SAS; to FPGA and SRIO	⇒ Flexible high-speed cabled connectivity
• Timing and synchronisation from front panel or backplane clock I/O, or optional GPS receiver	⇒ No additional timing equipment needed, significantly reducing system complexity; syncs easily to wireless test equipment.
• Single width Full Size PICMG AMC.0 R2.0 Advanced Mezzanine Card	⇒ Works with industry standard MicroTCA chassis; can also run standalone

The CommAgility AMC-2C6616 is a high performance DSP/FPGA based processing card in the extremely compact Advanced Mezzanine Card form factor. It is powered by two of the latest Texas Instruments TMS320TCI6616 DSPs plus a high-density Xilinx Virtex-6 FPGA. It is ideal for LTE and LTE Advanced eNodeB and wireless test, as well as other high performance DSP/FPGA processing applications.

Serial RapidIO at up to 20Gbps per port is supported by an IDT CPS-1848 Gen2 SRIO switch. As standard, the board provides three front panel SFP+ optical interfaces that link directly to the DSP AIF2 for CPRI or OBSAI. Alternative build options are SFP+ interfaces to the FPGA, or dual mini-SAS connectors for up to 40 Gbps of front panel I/O. Timing and synchronisation for wireless applications is achieved via the front panel or backplane clock I/O or an optional built-in GPS receiver, reducing overall system complexity and cost.

CommAgility Ltd
sales@commagility.com
www.commagility.com
Tel: +44 1509 228866

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HARDWARE SPECIFICATIONS

DSP: 2 TMS320TCI6616 DSPs, each with:
- 1 GHz (initial) or 1.2 GHz clock speed
- Up to 1 Gbyte x64 DDR3-1600 SDRAM
- 16 Gbps, 4x SRIO V2.1 link to switch
- 8 Gbps, 2x PCI Express link to FPGA
- Hyperlink50 bus (to other DSP)
- Single Gigabit Ethernet link to switch

FPGA: Xilinx Virtex-6™ FPGA:
- 128 Mbytes x16 DDR3-1066 SDRAM
- 256 Mbytes x32 DDR3-1066 SDRAM
- 128 Mbytes x16 parallel FLASH
- Dual 20Gbps 4x SRIO V2.1 to switch
- Three Gigabit Ethernet links to switch
- 4x GTX to AMC ports 20-17
- Configuration from FLASH or SRIO

Glue: Embedded glue logic for configuration of FPGA, general board control, Flash update. Controlled from SRIO or SPI.

Timing: full timing and sync support:
- Optional on-board GPS receiver
- Front panel clock input or output
- AMC Telecom clock A-D support
- Configurable PLL and jitter cleaner based on TI CDCE62005 device

Front panel I/O:
- Standard: Triple SFP+ to DSP AIF2
- Dual mini-SAS: 4x SRIO, 4x FPGA GTX
- Triple SFP+ at up to 6.25 Gbaud: CPRI, OBSAI, SRIO, Aurora, GigE etc
- SMB for sync clock I/O, optional GPS

Form Factor:
- Single-width, full-size Advanced Mezzanine Card, AMC.0 Rev 2.0 compliant
- IDT CPS-1848™ switch for AMC.4 compliant 20 Gbps x4 connections to AMC ports 4-7 and 8-11
- Broadcom BCM5389 switch for AMC.2 compliant GigE to AMC Ports 0 and 1
- Hot swap support

Debug:
- Breakout board for debug and RS-232
- Separate FPGA JTAG debug connector
- RS-232 headers for each DSP
- Optional MICTOR connector to FPGA

Module Management Controller:
- AMC.0 IPMB_L, FRU EEPROM data
- Power & reset, health monitoring

ENVIRONMENT/EMC/SAFETY

- Operating temp: 0-40°C ambient
- Power consumption: up to 48W max
- Designed for NEBS/ETSI compliance when used in appropriate chassis
- 2004/108/EC and FCC EMC compliant
- 2002/95/EC RoHS, 2002/96/EC WEEE and 2006/95/EC LVD compliant

SOFTWARE

Management: Full embedded suite based on Pigeon Point™ Software.

FPGA: Xilinx ISE and EDK project to demonstrate configuration functionality; MicroBlaze BSL including Flash update.

DSP: Full Board Support Libraries

LTE stacks from Tata Elxsi and others, contact CommAgility for further details

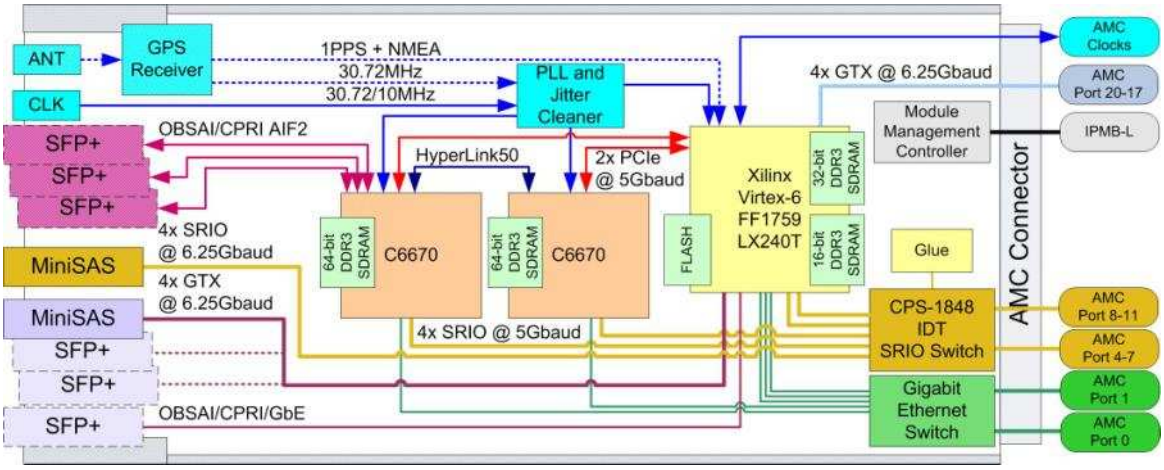
OEM PARTNERSHIP SERVICES:

IN DEVELOPMENT: Support and training; hardware customisation; software and FPGA development.

IN PRODUCTION: lead-time reduction; extended warranty; and repair; quick turn repairs and/or spares stocking.

EXTENDED LIFE obsolescence management; guaranteed lifecycle; Escrow.

LICENSING is offered for high volume projects.



CommAgility Ltd, Loughborough, UK
Tel: +44 1509 228866
World-wide support details:

sales@commagility.com
www.commagility.com
www.commagility.com/contact

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