AMC-D4F1-1200

DATASHEET

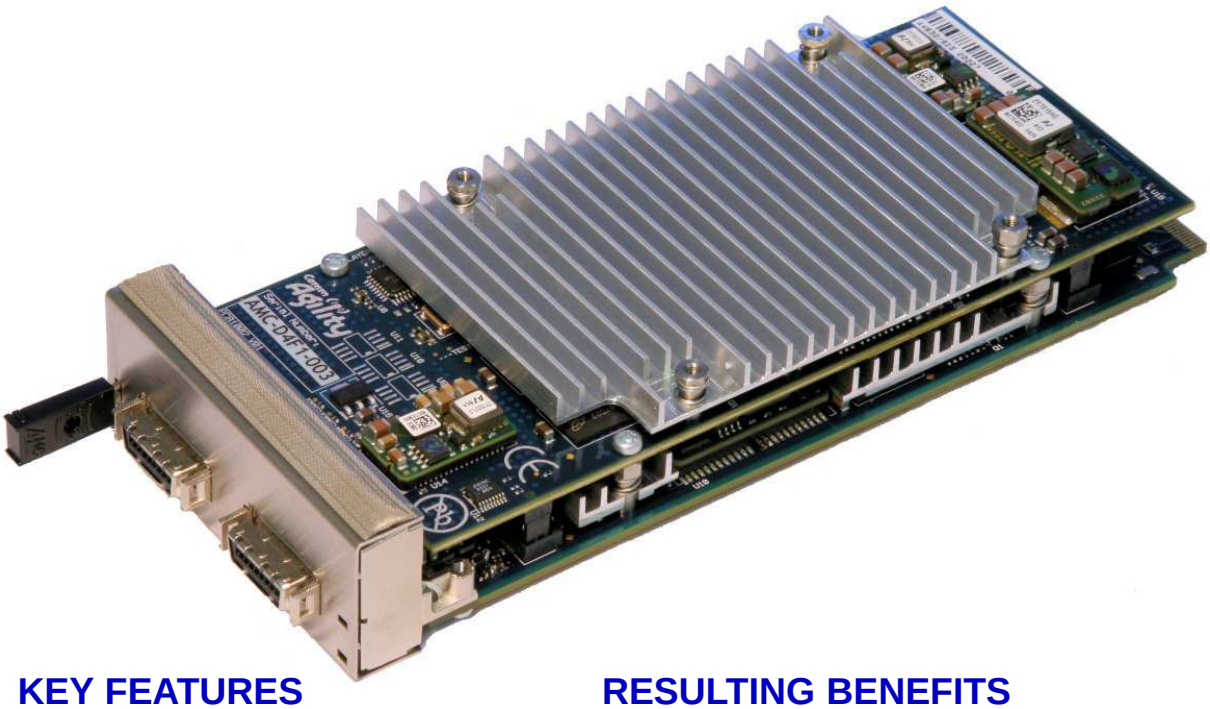
A state of the art signal processing card which combines DSP and FPGA devices on a single width AMC

Suitable for a range of wireless baseband solutions including WiMax and LTE

Flexible processing and interconnect for image and video applications in medical, industrial and military

Densely packed performance to meet signal processing requirements with fewer slots

10 Gbps data paths around the card and externally to chassis and front panel



KEY FEATURES

- 4 x 1.2 GHz TI TMS320C6455 DSPs
- Xilinx Virtex-4 FX series FPGA, customer programmable
- Over 1GB total card memory
- 10 Gbps 4x Serial RapidIO infrastructure
- Full Gigabit Ethernet infrastructure
- Serial RapidIO and programmable front panel I/O
- Single width, full height PICMG AMC.0 R2.0 Advanced Mezzanine Card
- Software and firmware library support
- Developed for use in OEM products
- Fully supported with customisation options and OEM lifecycle services

RESULTING BENEFITS

+ Fastest available DSP resource
+ additional I/O, pre-processing or signal processing resource
+ extensive data storage
+ dependable high-bandwidth interconnect
+ industry standard interconnect
+ fast and flexible links to external data
+ works with Industry standard MicroTCA and AdvancedTCA systems
+ fast route to application code porting
+ reduces integration risk and speeds time to market
+ allows a detailed fit to specific OEM requirements

The CommAgility AMC-D4F1-1200 is a single width, full-height Advanced Mezzanine Card offering unprecedented signal processing performance and bandwidth in a highly compact package, for wireless telecom, medical imaging, and other high performance applications. Using the fastest available DSPs along with a large FPGA enables an application to be balanced and optimised for most effective use of resources and development time.

A full 10 Gbps SRIO infrastructure based on the PICMG AMC.4 standard provides the deterministic bandwidth needed for radio or other raw data transfers on and off card. Separate AMC.2 Gigabit Ethernet is provided for control, management and delivery of baseband or other processed data streams.

Additional high speed user-configurable I/O is provided to the backplane or (optionally) front panel via multiple high-speed serial ports from the FPGA. Should modifications be required to make this product fit your OEM requirements, CommAgility are fully set up to support your needs through customisation of the hardware architecture or providing additional software and firmware.

TI DSP Third Party Network Member

DSP™ TEXAS INSTRUMENTS

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Comm Agility

AMC-D4F1

HARDWARE SPECIFICATIONS

DSPs: 4 x 1.2GHz TMS320C6455 DSPs
- 128 or 256MB DDR2-500 SDRAM each
- Direct FPGA EMIF connections: DSP0 64bit/150MHz; DSP1-3 32bit/120MHz
- Connection to XDS510™ emulator
- SRIO, Ethernet, HPI, McBSP & MMC connections

FPGA: Xilinx Virtex-4 FX100 FPGA:
- Dedicated DSP EMIF slave interfaces
- 18Mbytes x36 250MHz SRAM
- 10Gbps 4x SRIO
- 2 Full-duplex Gigabit Ethernet ports
- 10Gbps Front Panel RocketIO™
- RocketIO™ connections to AMC ports 12-13 and 17-20
- Xilinx parallel cable connection
- Optional Chipscope header

Serial RapidIO: 10Gbps 4x infrastructure using Tundra TSI578
- AMC.4 compliant connections to AMC ports 4-7 and 8-11
- Dedicated 10Gbps 4x links to all DSPs
- Dedicated 10Gbps 4x link to FPGA
- Front Panel 10Gbps 4x Connector

Ethernet: Gigabit Ethernet infrastructure using Broadcom BCM5389:
- AMC.2 (1000BASE-BX) compliant connections to AMC Ports 0 & 1
- Full-duplex 1Gbps links
- 9300 byte Jumbo Packet support
- FPGA & AMC Fabric port pairs capable of bandwidth aggregation

IPMI: Atmega128 IPMI controller:
- AMC.0 IPMB_L interface
- FRU EEPROM data
- Power and reset control
- Real-time health monitoring

Form Factor: Advanced Mezzanine Card
- AMC.0 Rev 2.0 compliant
- Full-height, single-width
- Usable in both AdvancedTCA™ and
- MicroTCA™ systems.
- AMC.2 Gigabit Ethernet
- AMC.4 4x Serial RapidIO
- Hot swap support

CONFIGURATION AND DEBUG

- DSP boot: EEPROM, Ethernet or SRIO
- FPGA loaded from DSP0 via SelectMap
- On-board debug LEDs for DSPs, FPGA, power and Ethernet ports
- Debug connector and breakout board for XDS-510, Xilinx platform cable, DSP and MMC serial ports

ENVIRONMENTAL/EMC/SAFETY

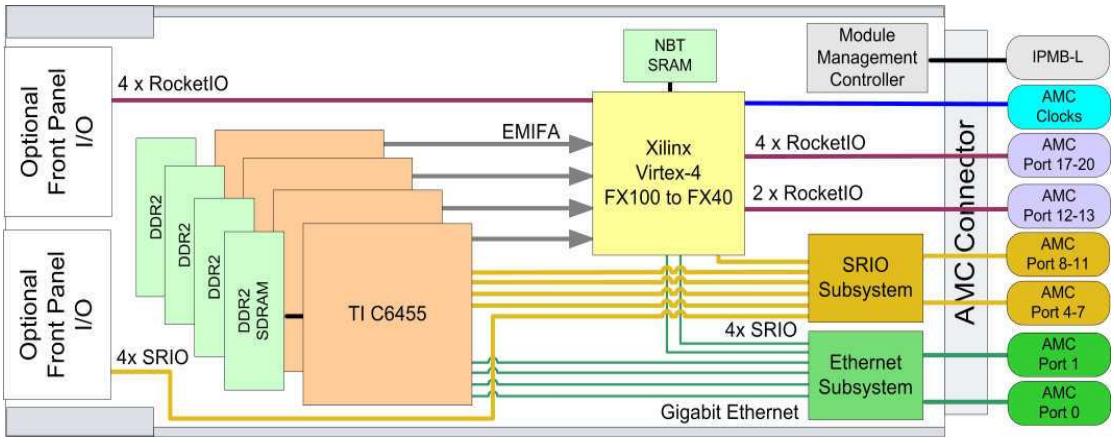
- Operating temperature: 0-40 °C ambient
- Power consumption: up to 45W, dependent on software and FPGA load
- Designed for NEBS and ETSI compliance when used in appropriate chassis
- 2004/108/EC and FCC EMC compliant
- 2002/95/EC RoHS compliant
- 2002/96/EC WEEE compliant
- 2006/95/EC Low Voltage Directive compliant

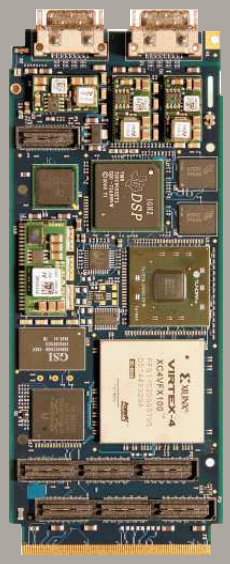
SOFTWARE SPECIFICATIONS

DSP library: support for controlling board functions, interfaces and self test. TCP/IP stack also available for DSPs

FPGA: to demonstrate configuration and functionality; Xilinx ISE project

MMC: full management suite based on PigeonPoint BMR software





OEM PARTNERSHIP SERVICES:

IN DEVELOPMENT
support and training; hardware customisation; software and FPGA development.

IN MANUFACTURE
leadtime reduction through stocking components or products; extended warranty and repair; quick turn repairs and/or spares stocking. Licensing of designs considered for high volumes.

DURING LIFECYCLE
obsolescence management; guaranteed lifecycle; design information held in Escrow.

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