

# AMC-V7-2C6678

## DATASHEET

A high performance AMC card based on a Xilinx Virtex-7 and TI's TMS320C6678 DSPs, with high speed, flexible I/O

16 DSP cores with shared memory, ideal for a range of high performance DSP applications

Front panel I/O: SFP+ to FPGA and mini-SAS to SRIO. Front panel or AMC clock sync

Flexible, high bandwidth off-board communications via Gen2 Serial RapidIO



### KEY FEATURES

- Xilinx Virtex-7 FPGA, XC7VX415T-2
- Dual TMS320C6678 octal-core DSPs
- Multiple banks of DDR3 SDRAM for both DSPs and FPGA
- Flash memory
- IDT CPS-1848 Serial RapidIO switch
- On-board Ethernet switch
- Separate "glue logic" for board configuration and management
- Front panel SFP+ optical interface to the FPGA
- Mini-SAS to SRIO switch
- Timing and synchronisation from front panel or backplane clock I/O
- Single width Full Size PICMG AMC.0 R2.0 Advanced Mezzanine Card

### RESULTING BENEFITS

- ⇒ Cost effective, high density device
- ⇒ The latest high performance TI DSPs
- ⇒ Latest external memory technology with multiple high bandwidth buses
- ⇒ Stores multiple FPGA images & software
- ⇒ SRIO V2.1 at up to 25 Gbaud per port
- ⇒ Gigabit Ethernet to all main devices
- ⇒ Allows control, FPGA configuration and FLASH reprogramming over SRIO/SPI
- ⇒ Flexible high-speed optical link, suitable for a range of applications
- ⇒ Flexible high-speed cabled connectivity
- ⇒ Syncs easily to other equipment
- ⇒ Works with industry standard MicroTCA chassis; can also run standalone

The CommAgility AMC-V7-2C6678 is a high performance DSP/FPGA based processing card in the extremely compact Advanced Mezzanine Card form factor. It is powered by two of the latest Texas Instruments TMS320C6678 DSPs plus a high-density Xilinx Virtex-7 FPGA. It is ideal for a range of high performance DSP/FPGA processing applications including telecoms and image processing.

Serial RapidIO at up to 25 Gbaud per port is supported by an IDT CPS-1848 Gen2 SRIO switch. As standard, the board provides a single front panel SFP+ optical interface that links directly to the FPGA, plus a single mini-SAS connector linked to the SRIO switch. Should applications require timing and synchronisation, this is achieved via the front panel or backplane clock I/O.



CommAgility Ltd  
sales@commagility.com  
www.commagility.com  
Tel: +44 1509 228866

Comm (( ))  
**Agility**

