HARDWARE THEORY OF OPERATION

for the XMOS/Attero Tech Ethernet AVB Evaluation Platform

OBJECTIVE

The objective of this document is to explain the operation of the XMOS/Attero Tech Ethernet AVB Evaluation Platform. Refer to the AVB Evaluation Platform schematics and Quick Start Guide while reading this document.

APPLICATION NOTE

THEORY OF OPERATION

The AVB Eval Platform supports up to four stereo I^2S digital audio inputs and up to 4 stereo I^2S digital audio outputs. It has a 24-bit stereo ADC, U4, on board that can be connected in SDATA_IN0 by installing a shunt on the "channel 1 & 2 input source selection header", J12. Removing this shunt allows the expansion header, J7, to drive SDATA_IN0. Only one device can utilize SDATA_IN0 at a time. The AVB Eval Platform also has a 24-bit stereo DAC, U5, on board that is permanently connected to SDATA_OUT0. SDATA_OUT0 is always present on the expansion header.

Both the ADC and DAC operate as I^2S slaves and they receive their word clock and bit clock directly from the XS1-L2 processor, U1. The master clocks are generated by an external fractional-n clock multiplier PLL, U6. Configuration of this PLL is provided by the XS1-L2 via I^2C. A reference clock is also provided by the XS1-L2.

Analog audio input to the on-board ADC is provided by either a 3.5mm TRS jack, J3, or 2 RCA jacks, J4. The "input jack selection header", J11, determines which input jack is connected to the ADC. With shunts installed across pin pairs 1 – 3 and 2 – 4, the 3.5mm TRS jack is connected to the ADC. With shunts installed across pin pairs 3 – 5 and 4 – 6, the two RCA jacks are connected to the ADC. Only one jack should be connected at a time.

Analog audio output from the on-board DAC is provided by either a 3.5 mm TRS jack, J5, or 2 RCA jacks, J2. Both are permanently connected to the DAC. The analog output can be muted by Q1 by asserting \MUTE at any time on the XS1-L2.

On the analog audio input and output jacks, the tip of the 3.5 mm TRS jack is the first channel

(left), the ring is the second (right), and the sleeve is analog ground. Furthermore, the white (bottom) RCA jack is the first channel (left), the red (top) jack is the second (right), and the both shields are analog ground.

Network connectivity for the AVB Eval Platform is provided to the XS1-L2 by the LAN8710A MAC/PHY, U3, via MII. The Ethernet jack, J6, provides a 10/100 BASE-T interface to the network.

The AVB Eval Platform provides one remote button, S3, and one remote LED, LED5, which are user configurable. It also provides a "select listener stream" push-button, S1, and "select stereo channel pair" push-button, S2, to route the desired I^2S stereo pair to the on-board DAC. The current stereo pair is indicated by LED1, LED2, LED3, and LED4. LED1 indicates channels 1 and 2 are selected, LED2 – 3 and 4, LED3 – 5 and 6, and LED5 – 7 and 8. These push-buttons and LEDs are directly controlled by the XS1-L2.

The AVB Eval Platform is powered by an external regulated +5 VDC power adapter connected to the 2.1 mm barrel jack (J1). The required on-board voltages are regulated by U15, U16, and U17. U15 is a switching regulator that regulates the +5 VDC input down to +3.3 V for XS1-L2 I/O voltage and peripheral supply voltages. U16 is a switching regulator that regulates the +5 VDC input down to +1 V for the XS1-L2 processor core voltage. U17 is a low-drop out linear voltage regulator that regulates the +5 VDC input down to a low-noise +3.3 V for ADC/DAC analog voltage.

The voltage supervisor U12 monitors the +3.3 V supply and U13 monitors the +1 V supply. These supervisors are cascaded in such a way that the +3.3 V supply must be within regulation before the +1 V regulator is enabled and \RESET is only asserted after all supplies are within regulation. This ensures proper voltage sequencing and reset timing to the XS1-L2 and peripherals power-up. The reset button, S4, provides a manual hardware board reset.

The XSYS header, J8, provides a programming and debugging interface to the XS1-L2. The expansion header provides access to all I2S digital audio input and output pairs, master clock, word clock, bit clock, and one spare 8-bit GPIO bank (or two spare 4-bit GPIO bank) of the XS1-L2. The expansion header also provides signal return grounds and +3.3 V. The load on this +3.3 V pin must not exceed the total 1.5 A maximum of U15.

ABOUT ATTERO TECH

Attero Tech is a leading provider of networked audio interfaces. These interfaces make it easy and cost effective to integrate a wide variety of audio components such as consumer electronics, microphones, paging speakers, computers, and recording devices into a networked audio system.

Attero Tech is headquartered in Fort Wayne, Indiana. For more information on Attero Tech's full line of products and services, please visit www.atterotech.com.