Nutaq
VHS-ADC

cPCI advanced
development plaform
PRODUCT SHEET

RoHS compliant

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Nutaq **VHS-ADC**

- **Onboard, 8-channel, 105 MSPS, 14-bit ADCs on 6U cPCI (PXI compatible)**
- **Mezzanine expansion site to support more channels or memory**
- **Outstanding clock synchronization**
- **Onboard, high processing speed LX/SX Virtex-4 FPGA**
- **Sustained 8 Gbps raw data RX/TX RapidCHANNEL ports (one each)**
- **Recording software tools**
- **Support for model-based design flow**

The VHS-ADC is a high-speed, multichannel acquisition platform. It is equipped with eight phase-synchronous ADCs capable of a maximum rate of 105 MHz and a high-capacity Virtex-4 FPGA for high-speed processing. It also comes with SDRAM for data storage and an expansion connector to add eight input channels, eight output channels, or several gigabytes of DDR2 SDRAM for simultaneous full-speed recording. This makes the VHS-ADC perfect for multichannel intermediate-frequency processing (AC-coupled option) or baseband processing (DC-coupled option), and other applications outlined below.

When combined to other DSP–FPGA processing platforms such as the SignalMaster Quad or the SignalMaster Dual, the VHS-ADC becomes a complete and very-high-performance IF/baseband solution. The VHS-ADC can also be combined with the VHS-DAC to offer an end-toend chain for high-speed processing on up to 16 channels (or more if you add more platforms in a common cPCI chassis).

STELLAR PROCESSING POWER

The 256 GMACS of the Virtex-4 FPGA allows fulfilling the highest processing needs. The Virtex-4 family provides some of the most advanced logic, highest performance, highestbdensity, and greatest memory capacity of other FPGA families.

Integration to System Generator for DSP

The VHS-ADC is fully integrated to System Generator for DSP, which allows using high-level abstractions that can be compiled automatically into the FPGA, without loss of performance over designs implemented with VHDL.

MULTIPURPOSE PLATFORM

Use the VHS-ADC in development cycles for:

- Data storage, which allows you to use actual multichannel signals in algorithm simulation or create actual multichannel signals from simulation files.
- FPGA development (hardware-in-the-loop co-simulation or real-time implementation).

REDUCE THE RISK OF FACING INTERCONNECTION PROBLEMS

Using the only FPGA-based platform with eight onboard inputs helps avoid interconnection problems. The number of inputs can be expanded to 16 by adding an ADC module. The 8 Gbps, full-duplex RapidCHANNEL ports allow adding processing platforms such as the SignalMaster Quad to a system or adding an FPDP-I/II long-term hard disk drive storage systems capable of sustained recording at up to 200 MBps (which makes recording large bandwidth baseband signals possible).

BETTER ACCURACY

The VHS-ADC has outstanding clock synchronization—very-low-skew interchannel clock routing through all the ADC, optimized for tight synchronous acquisition applications.

The VHS-ADC is also shielded for an excellent between-channel and external noise insulation (up to 102 dB interchannel crosstalk insulation).

STAND-ALONE CAPABILITIES

The VHS-ADC is equipped with an onboard flash memory for the FPGA and an I2C/JTAG external port, making it possible to use the VHS-ADC without a cPCI CPU.

CUSTOMIZABLE FOR OEM APPLICATIONS

Lower the cost of the VHS-ADC by requesting downsized versions of the development platform, yielding more economical production units.

APPLICATIONS

The following are some of the applications where the VHS-ADC truly shines.

- Advanced base stations
- Smart antennas, multichannel IF systems, beamformers
- Wireless applications (routers, OFDM antenna diversity, Wi-Fi, WiMAX)
- MIMO space-time coding
- Software-defined radio (SDR)
- Geolocation (based on TDOA, DOA, and ADOA)
- High-speed test and measurement systems

FEATURES

The VHS-ADC offers the following features:

- Virtex-4 FPGA
  - 256 GMACS, 152,000 logic cells
  - 500 MHz performance
- Multichannel 105-MSPS ADC technology, supplied with AC-coupled or DC-coupled analog inputs (coupling option must be • defined upon purchase), making it possible to reach high SNR baseband or IF signals
- Powerful LVDS serial and parallel interface
  - **Serial digital intermediate frequency (DIF) interface**—Synchronous LVDS ports (two LVDS pairs RX/TX) on the RJ45 front panel, 105 MBps, full-duplex, based on serdes technology. The LVDS clock is linked to the acquisition frequency
  - **RapidCHANNEL interfaces (TX ×1, RX ×1)**—LVDS ports (eight LVDS data pairs and others for synchronization and control at each port) on two Samtec Q-Pair micro coaxial connectors (1 RX, 1 TX), 8 Gbps, full-duplex, based on the Virtex-4 on-chip serializer. The bandwidth is fixed and data is transferred through FIFO (refer to RapidCHANNEL specifications for details)
- The front panel data port (FPDP-I/II) allows data to be transferred at high speeds between FPDP-I/II-compliant hardware and can be configured as input or output through software
- Data recording and playback on the onboard 128 MB SDRAM or with the 2 GB memory module
- Stand-alone configuration through the onboard flash memory
- Language-based (C and VHDL) board software development kit
- Windows-based utility for parameter control
- Very-low-skew interchannel clock routing through all the ADCs
- Unlimited multiplatform cPCI configuration. Phase synchronization is achieved by providing the same external clock to all the platforms
- Independent, software-programmable gain amplifier on each acquisition channel (optional)
- Ease of development with the model-based design kit (optional) for MATLAB and Simulink (optional)

SOFTWARE DEVELOPMENT TOOLS

The VHS-ADC also comes with the following software development tools:

VHS-ADC board software development kit

The VHS-ADC board software development kit (BSDK) allows targeting the VHS-ADC's onboard FPGA through ISE Foundation projects and comes with FPGA core documentation. Further, the BSDK includes a host API and programs that allow communicating with the VHS-ADC's FPGA. Finally, the BSDK includes a complete set of hardware functional examples that demonstrate how to use the VHS-ADC's onboard I/Os and interfaces.

VHS-ADC model-based design kit (optional)

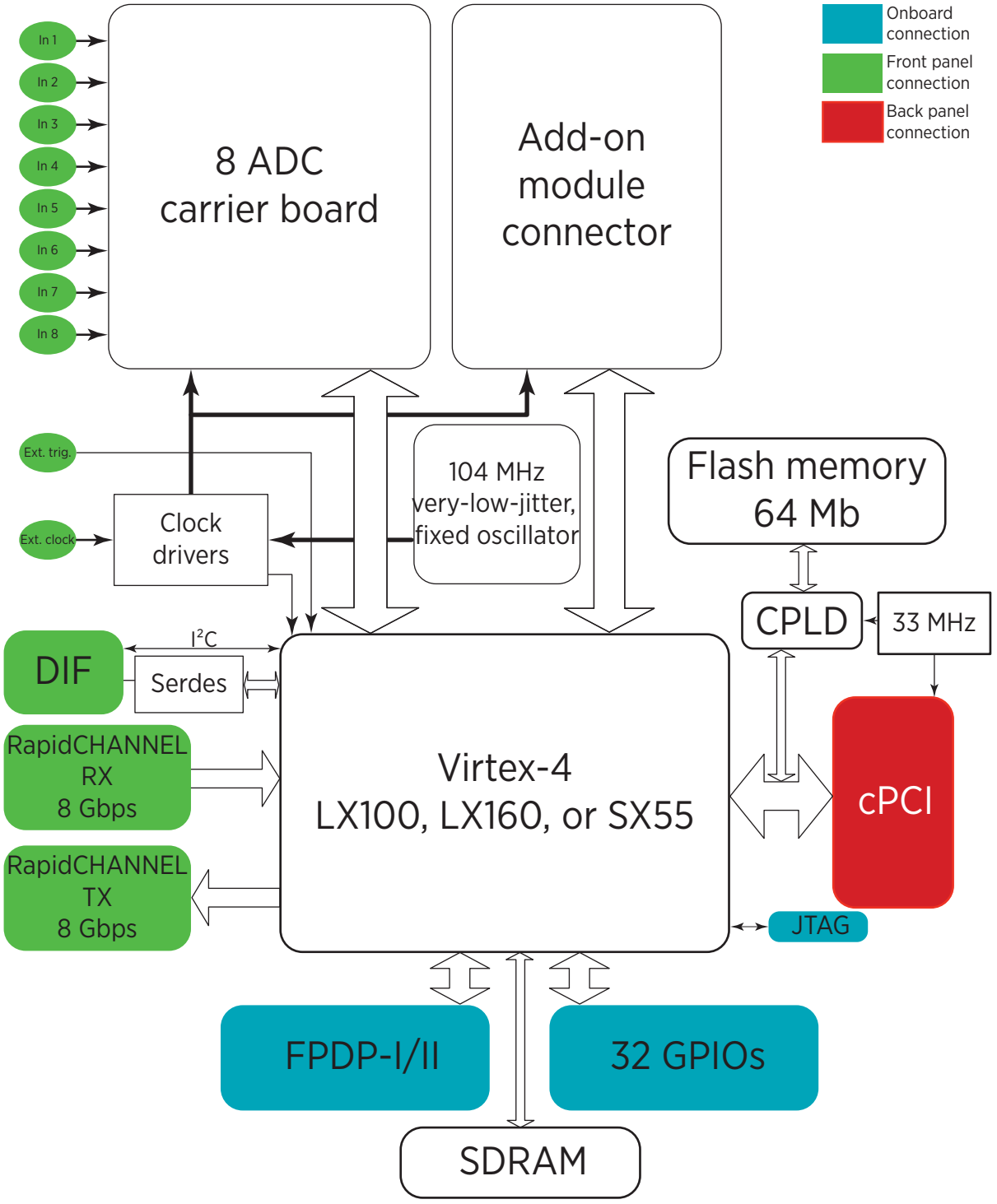
The optional VHS-ADC model-based design kit (MBDK) allows generating code for the VHS-ADC's FPGA from MATLAB and Simulink through System Generator for DSP. Modifying model parameters on the fly and performing FPGA hardware-in-the-loop co-simulations are also a breeze with Simulink. The MBDK also comes with a complete set of hardware functional examples that demonstrate how to use the VHS-ADC's onboard I/Os and interfaces in a model-based design environment.

Specifications

ANALOG-TO-DIGITAL CONVERTERS	• Analog Devices AD6645 (×8) • Can be upgraded to 16 channels by adding an optional add-on module • Guaranteed maximum sampling rate of 105MSPS (resolution: 14 bits)	
ANALOG INPUT	**Default**	50-Ω MMCX connectors
	Optional	• AC coupled without programmable gain • 0.4 MHz to 200 MHz analog input bandwidth (–3 dB) • 6-dBm full-scale input • 77.59 dBc SFDR at 70 MHz F_{in} (bandwidth = 50 MHz) • Interchannel crosstalk insulation: –102 dB at 70 MHz F_{in}
		• AC coupled with programmable gain • 0.4 MHz to 200 MHz analog input bandwidth (–3 dB) • –18 dBm to 4 dBm full-scale input • 75.78 dBc SFDR at 70 MHz F_{in} (bandwidth = 50 MHz) • Interchannel crosstalk insulation: –87 dB at 70 MHz F_{in} (minimum to maxmum gain)
		• DC coupled without programmable gain • DC to 50 MHz analog input bandwidth (–3 dB) • 11 dBm full-scale input • 92.34 dBc SFDR at 1 MHz F_{in} (bandwidth = 2 MHz) • 68.49 dBc SFDR at 30 MHz F_{in} (bandwidth = 50 MHz) • Interchannel crosstalk insulation: –89 dB at 30 MHz F_{in}
SAMPLING CLOCKS	Software-selectable onboard or external clock Factory-fixed oscillator, 104 MHz very-low-jitter clock (0.5 ps typical) External 50-Ω clock source (TTL, LVTTL, CMOS, LVCMOS) used for very-low-jitter and user-defined frequencies	
CONTROL AND PROCESSING FPGA	• Processing Virtex-4 FPGA (for signal decimation and/or filtering) • FPGA packages: XC4VSX55, XC4VLX100, or XC4VLX160 • 128 MB SDRAM	
OFF-BOARD COMMUNICATION CHANNELS	• Two RapidCHANNEL ports (TX ×1, RX ×1), yielding 8 Gbps, full-duplex • Transfers at 400 MBps through the external FPDP-I /II (software-selectable as input or output) • LVDS hardware serdes input/output DIF connection (105 MBps) on RJ45. 16-bit parallel data routed to the FPGA (serdes), 52.5 MHz maximum clock • 32-bit, PCI, external port with 33 MHz control interface • 32-bit, user-defined, external Virtex-4 single-ended GPIO-32 header • I^2C interface for stand-alone control (flash memory programming, parameter control)	
OPTIONAL ADD-ON HARDWARE MODULES SOLD SEPARETELY. CONTACT NUTAQ FOR DETAILS.	**ADC module**	• Eight ADC inputs, each capable of a maximum 105 MSPS (14 bits) • Same analog input options as the VHS-ADC
	DAC module	• Eight DAC outputs, each capable of a maximum 480 MSPS (14-bit interpolating DAC) • Same analog output options as the VHS-ADC
	Memory module	Module adding 2 GB of DDR2 SDRAM to the VHS-ADC, yielding a solution with eight full-speed simultaneous channels for recording/playback.

Nutaq **VHS-ADC**

Block diagram



With over 25 years of experience delivering advanced digital signal processing solutions to companies worldwide, Nutaq serves customers across the Americas, Asia, and Europe. Nutaq offers a full range of DSP–FPGA development platforms, as well as product development services. Nutaq works in partnership with such industry leaders as Texas Instruments, The MathWorks, and Xilinx to deliver unsurpassed quality and support to its large OEM customer base, which includes many prestigious names of the consumer electronics, telecommunications, aerospace, and defense fields. In a world where digital signal processing technology is vital to network and wireless communications, audio and video processing, as well as electronic systems in all fields of technology, Nutaq is an ideal partner.

Nutaq products are constantly being improved; therefore, Nutaq reserves itself the right to modify the information herein at any time and without notice.

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