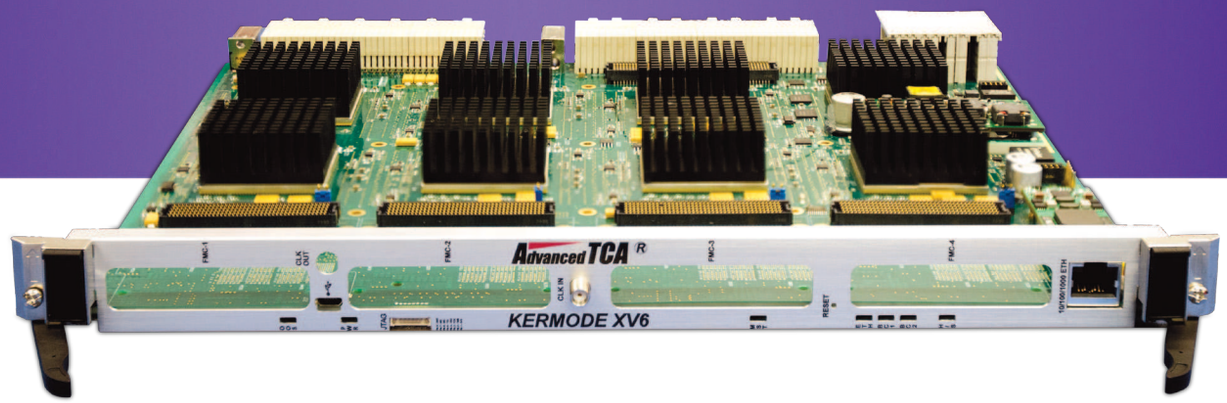
Nutaq
KERMODE XV6

AdvancedTCA FPGA Compute Blade

PRODUCT SHEET



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Nutaq **Kermode XV6**

- **8 Virtex-6 SX475T FPGAs**
- **4 Mezzanine Sites (FMC)**
- **Over 8 TeraMACs/s**
- **AdvancedTCA**

The Nutaq RD Kermode XV6 is the most powerful AdvancedTCA compute blade ever built. It has been specifically designed to tackle the most demanding signal processing applications that exist.

Processing power

The Kermode XV6 packs eight Xilinx Virtex-6 SX475T FPGAs, delivering an outstanding 8.8 TeraMACs solely from their DSP48E1 dedicated multiply-accumulate engines. Each FPGA interfaces with two DDR-3 SDRAM SODIMM modules, capable of supporting up to 4 GBytes, for an aggregate memory capacity of 64 GBytes. This memory may be used to store intermediate results of memory-intensive algorithms such as multi-dimensional correlation or tomography, or to record full-rate digitized signals for post-processing and analysis purposes.

The blade connects with Zone 2 backplane and Zone 3 (custom backplane or RTM) at rates exceeding 500 Gbps, making for highly-efficient clusters, with up to 128 FPGAs in a single chassis.

Expansion

The Kermode XV6 has four mezzanine sites onto which standard VITA-57 high-pin-count FPGA Mezzanine Card (FMC) modules may be connected. These expansion sites may host A/D & D/A converters to directly incorporate mixed signal capability, or add front-panel optical links for up to 160 Gbps data exchange. Please consult the list of FMC modules offered by Nutaq RD.

Applications

- Radioastronomy
- Adaptive Optics
- Radar
- Beamforming
- Tomography
- FPGA Farming
- Instrumentation

Data Links

Distributed computing involves moving massive amounts of information effectively. The Kermode XV6 was architected to maximize data throughput. The FPGAs are organized in two rows, and are symmetrically interconnected to optimize the flow of data between front panel expansions, the FPGAs themselves, and the backplane. The front row of FPGAs (F1-F4) interfaces directly with the FMC expansion sites. Processed data streams may be forwarded to the backplane with the same throughput capability, routed to other cards, or looped back with a custom backplane to reach the rear row of FPGAs (R1-R4). The rear FPGAs connect to the Zone 3 backplane with bidirectional links in excess of 100 Gbps each, and have direct transmit access to front FPGAs with such rates. All FPGAs within a row may exchange lower rate data with direct links.

Development Environment

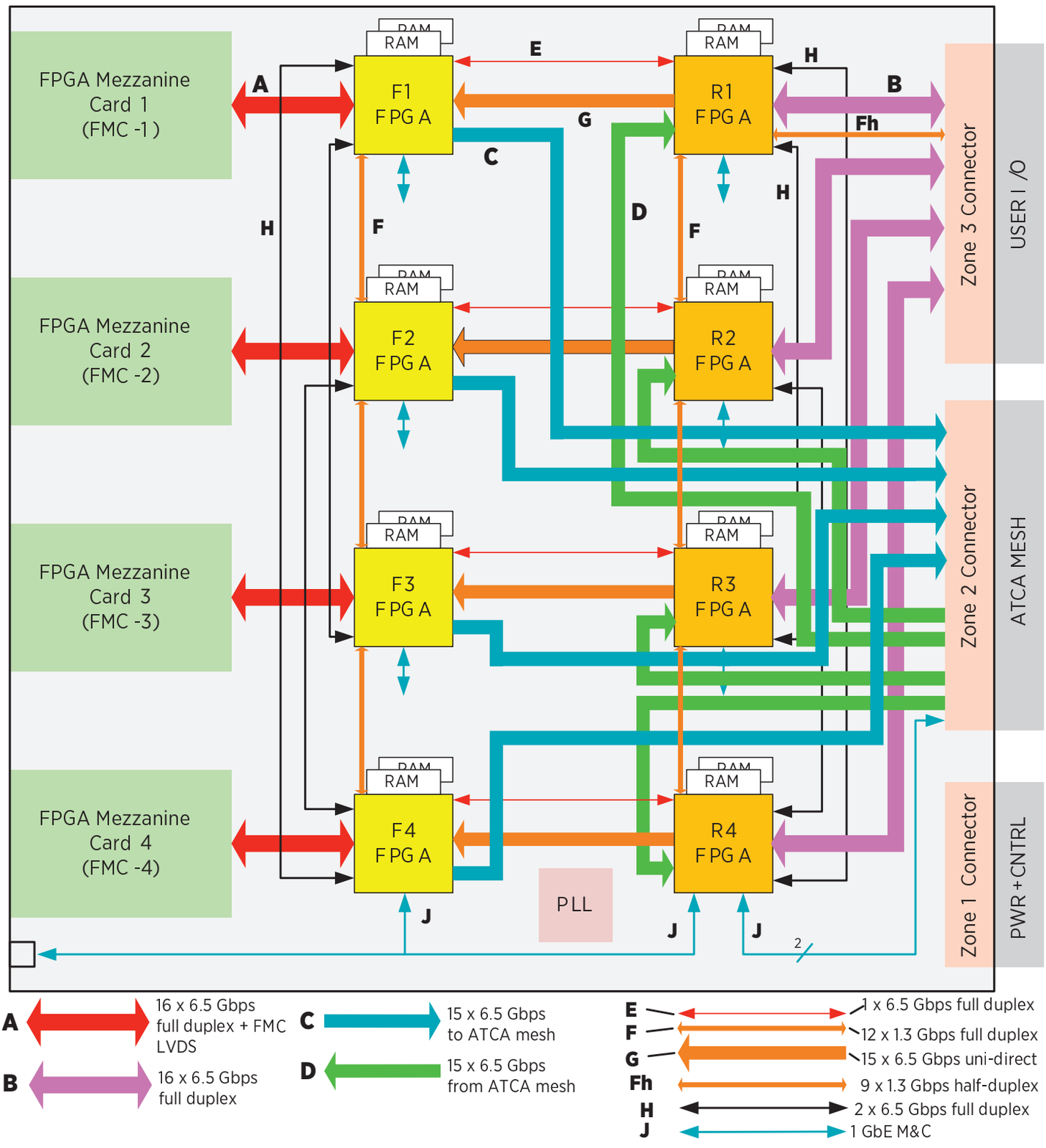
The Kermode XV6 comes with Nutaq's world-renowned Board Software Development Kit (BSDK), a comprehensive set of tools aimed at accelerating the developer's prototyping cycle. This environment includes an embedded Linux Micro-kernel which provides a user-friendly programming, control, and management interface from a host using Gigabit Ethernet. It also includes functionalities such as data stream record/playback, memory read/write, real-time data exchange with host through GbE, co-simulation from Matlab, and much more.

Intelligent Platform Management

The Intelligent Platform Management (IPM) module provides valuable information on the operation of the blade. It monitors parameters such as supplied voltages, board temperatures, and power, but also reports events such as reset, failures, etc. The PICMG-compliant IPM Controller of the Kermode XV6 ensures proper communication with the ATCA shelf manger .

Supported FMC Modules

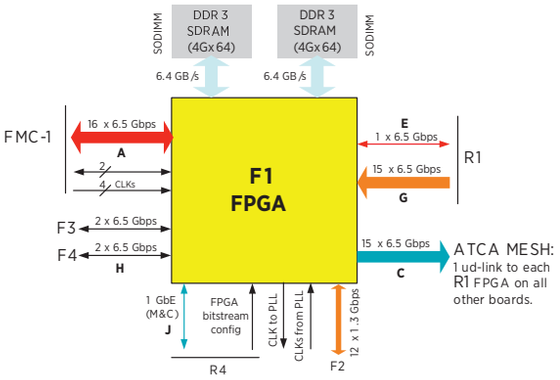
PART	DESCRIPTION
ADC550	2-ch 12-bit 550 MSPS ADC
DAC1200	4-ch 16-bit 1200 MSPS DAC
ADAC250	2-ch 14-bit 250 MSPS ADC; 2-ch 16-bit 1 GSPS DAC
MI125	16/32-ch 14-bit 125 MSPS ADC
MI250	8-ch 14-bit, 250 MSPS ADC
ADC5000	1 / 2 / 4-ch 10-bit 5 / 2.5 / 1.25 GSPS ADC
2x 10-GbE	2x 10-GbE SFP+
4x 10-GbE	4x 10-GbE
QSFP/SFP+	1x QSFP, 2x SFP+
Radio 420x	Tunable UHF wireless transceiver

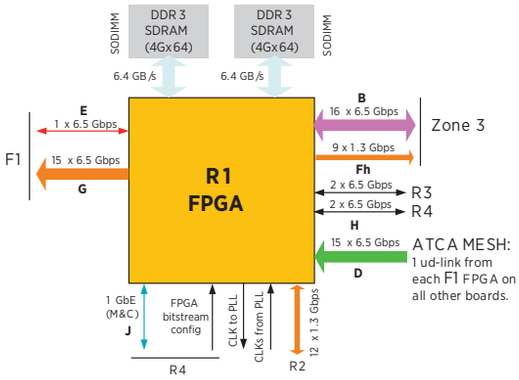

FPGA Mezzanine Card 1 (FMC -1)
FPGA Mezzanine Card 2 (FMC -2)
FPGA Mezzanine Card 3 (FMC -3)
FPGA Mezzanine Card 4 (FMC -4)
RAM
F1 FPGA
F2 FPGA
F3 FPGA
F4 FPGA
R1 FPGA
R2 FPGA
R3 FPGA
R4 FPGA
PLL
A
B
C
D
E
F
G
H
Fh
J
2
Zone 3 Connector
Zone 2 Connector
Zone 1 Connector
USER I /O
ATCA MESH
PWR +CNTRL
A 16 x 6.5 Gbps full duplex + FMC LVDS
B 16 x 6.5 Gbps full duplex
C 15 x 6.5 Gbps to ATCA mesh
D 15 x 6.5 Gbps from ATCA mesh
E 1 x 6.5 Gbps full duplex
F 12 x 1.3 Gbps full duplex
G 15 x 6.5 Gbps uni-direct
Fh 9 x 1.3 Gbps half-duplex
H 2 x 6.5 Gbps full duplex
J 1 GbE M&C

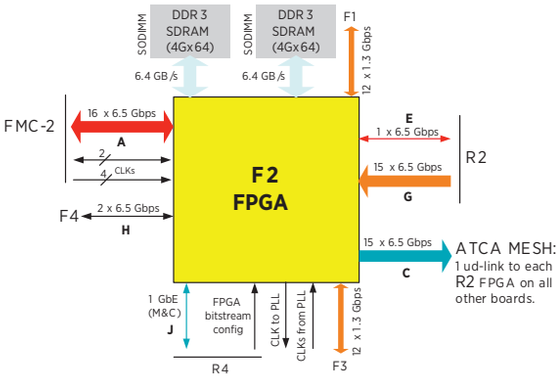
Embedded Processors at a Glance

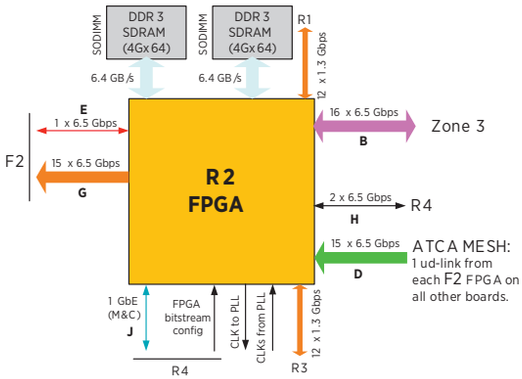
Virtex-6 SX475T

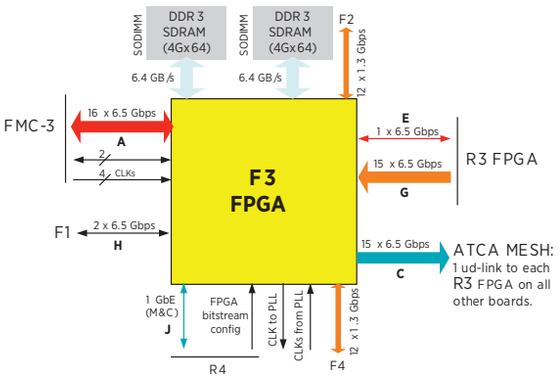
- 74,400 CLB slices
  - Real 6-input look-up table (LUT) technology
  - Dual LUT5 (5-input LUT) option
  - SRL32/dual SRL16 with registered outputs option
- 38,304 Kbits BRAM
- 2,016 DSP48E1, 600 MHz
  - 25 x 18 bits multiplier/accumulator
- 36 GTX transceivers: 150 Mb/s to 6.5 Gb/s
- 2 Integrated interface blocks for PCI Express® designs
- 4 Integrated 10/100/1000 Mb/s Ethernet MAC block
- 18 Powerful mixed-mode clock managers (MMCM) blocks provide zero-delay buffering, frequency synthesis, clock-phase shifting, input-jitter filtering, and phase-matched clock division

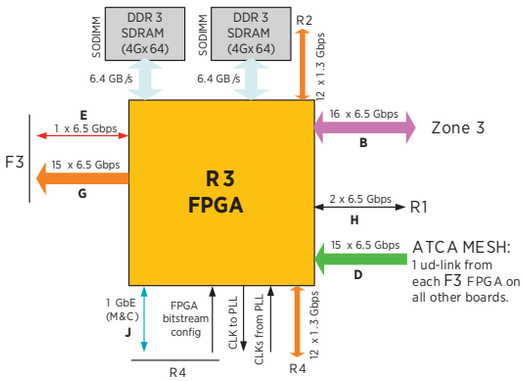

SODIMM
DDR 3 SDRAM (4Gx64)
DDR 3 SDRAM (4Gx64)
SODIMM
6.4 GB/s
6.4 GB/s
FMC-1
16 x 6.5 Gbps
A
2
4 CLKs
F3
2 x 6.5 Gbps
F4
2 x 6.5 Gbps
H
F1 FPGA
E
1 x 6.5 Gbps
15 x 6.5 Gbps
G
R1
15 x 6.5 Gbps
C
ATCA MESH:
1 ud-link to each R1 FPGA on all other boards.
1 GbE (M&C)
J
FPGA bitstream config
CLK to PLL
CLKs from PLL
12 x 1.3 Gbps
R4
F2

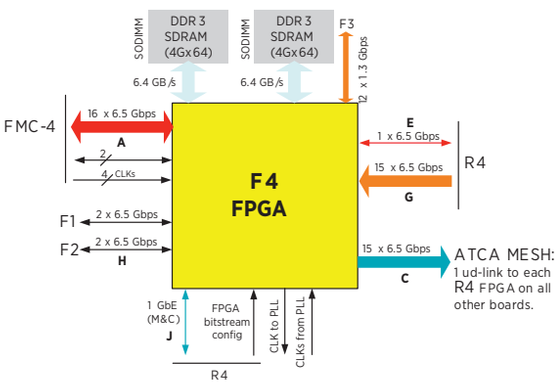

SODIMM
DDR 3 SDRAM (4Gx64)
DDR 3 SDRAM (4Gx64)
SODIMM
6.4 GB/s
6.4 GB/s
F1
E
1 x 6.5 Gbps
15 x 6.5 Gbps
G
R1 FPGA
B
16 x 6.5 Gbps
Zone 3
9 x 1.3 Gbps
Fh
2 x 6.5 Gbps
R3
2 x 6.5 Gbps
R4
H
15 x 6.5 Gbps
D
ATCA MESH:
1 ud-link from each F1 FPGA on all other boards.
1 GbE (M&C)
J
FPGA bitstream config
CLK to PLL
CLKs from PLL
12 x 1.3 Gbps
R4
R2

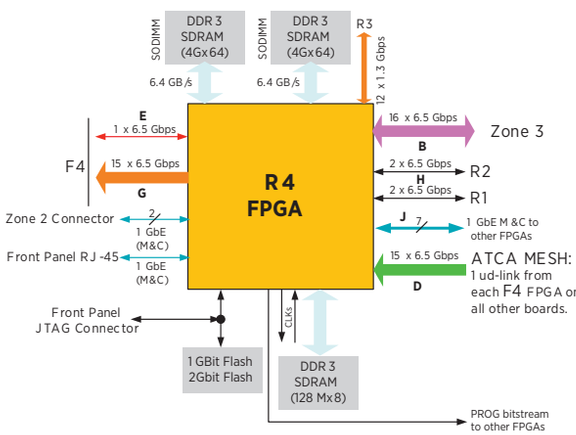

SODIMM
DDR 3 SDRAM (4Gx64)
DDR 3 SDRAM (4Gx64)
SODIMM
F1
12 x 1.3 Gbps
6.4 GB/s
6.4 GB/s
FMC-2
16 x 6.5 Gbps
A
2
4 CLKs
F4
2 x 6.5 Gbps
H
F2 FPGA
E
1 x 6.5 Gbps
15 x 6.5 Gbps
G
R2
15 x 6.5 Gbps
C
ATCA MESH:
1 ud-link to each R2 FPGA on all other boards.
1 GbE (M&C)
J
FPGA bitstream config
CLK to PLL
CLKs from PLL
12 x 1.3 Gbps
R4
F3


SODIMM
DDR 3 SDRAM (4Gx64)
DDR 3 SDRAM (4Gx64)
SODIMM
R1
12 x 1.3 Gbps
6.4 GB/s
6.4 GB/s
F2
E
1 x 6.5 Gbps
15 x 6.5 Gbps
G
R2 FPGA
16 x 6.5 Gbps
B
Zone 3
2 x 6.5 Gbps
R4
H
15 x 6.5 Gbps
D
ATCA MESH:
1 ud-link from each F2 FPGA on all other boards.
1 GbE (M&C)
J
FPGA bitstream config
CLK to PLL
CLKs from PLL
12 x 1.3 Gbps
R4
R3


SODIMM
DDR 3 SDRAM (4Gx64)
DDR 3 SDRAM (4Gx64)
SODIMM
F2
12 x 1.3 Gbps
6.4 GB/s
6.4 GB/s
FMC-3
16 x 6.5 Gbps
A
2
4 CLKs
F1
2 x 6.5 Gbps
H
F3 FPGA
E
1 x 6.5 Gbps
15 x 6.5 Gbps
G
R3 FPGA
15 x 6.5 Gbps
C
ATCA MESH:
1 ud-link to each R3 FPGA on all other boards.
1 GbE (M&C)
J
FPGA bitstream config
CLK to PLL
CLKs from PLL
12 x 1.3 Gbps
R4
F4


SODIMM
DDR 3 SDRAM (4Gx64)
DDR 3 SDRAM (4Gx64)
SODIMM
R2
12 x 1.3 Gbps
6.4 GB/s
6.4 GB/s
F3
E
1 x 6.5 Gbps
15 x 6.5 Gbps
G
R3 FPGA
16 x 6.5 Gbps
B
Zone 3
2 x 6.5 Gbps
R1
H
15 x 6.5 Gbps
D
ATCA MESH:
1 ud-link from each F3 FPGA on all other boards.
1 GbE (M&C)
J
FPGA bitstream config
CLK to PLL
CLKs from PLL
12 x 1.3 Gbps
R4
R4


SODIMM
DDR 3 SDRAM (4Gx64)
DDR 3 SDRAM (4Gx64)
SODIMM
F3
12 x 1.3 Gbps
6.4 GB/s
6.4 GB/s
FMC-4
16 x 6.5 Gbps
A
2
4 CLKs
F1
2 x 6.5 Gbps
F2
2 x 6.5 Gbps
H
F4 FPGA
E
1 x 6.5 Gbps
15 x 6.5 Gbps
G
R4
15 x 6.5 Gbps
C
ATCA MESH:
1 ud-link to each R4 FPGA on all other boards.
1 GbE (M&C)
J
FPGA bitstream config
CLK to PLL
CLKs from PLL
R4


SODIMM
DDR 3 SDRAM (4Gx64)
DDR 3 SDRAM (4Gx64)
SODIMM
R3
12 x 1.3 Gbps
6.4 GB/s
6.4 GB/s
F4
E
1 x 6.5 Gbps
15 x 6.5 Gbps
G
R4 FPGA
16 x 6.5 Gbps
B
Zone 3
2 x 6.5 Gbps
R2
H
2 x 6.5 Gbps
R1
Zone 2 Connector
2
1 GbE (M&C)
Front Panel RJ-45
1 GbE (M&C)
J
7
1 GbE M &C to other FPGAs
15 x 6.5 Gbps
D
ATCA MESH:
1 ud-link from each F4 FPGA on all other boards.
Front Panel JTAG Connector
CLKs
1 GBit Flash 2Gbit Flash
DDR 3 SDRAM (128 Mx8)
PROG bitstream to other FPGAs

Specifications

Processors

- FPGA
- 8 Xilinx Virtex-6 SX475T
- 16 DDR-3 SDRAM SODIMM modules up to 16 GB each
  - (Xilinx MIG currently supports up to 4 GB)

Backplane Interfaces

- Zone 2:
  - 60x 6.5 Gbps (F1-F4 to Zone 2)
  - 60x 6.5 Gbps (Zone 2 to R1-R4)
  - 2x GbE (base channels)
- Zone 3:
  - 64x 6.5 Gbps (full duplex)
  - 9x 1.3 Gbps (half duplex)

Front-panel Interfaces

- (4) FMC bays
- (1) GbE
- (1) Reference input / sampling clock (SMA)
- (3) LEDs (Hotswap, Out of Service, OK)

Mezzanine sites

- (4) VITA 57 FMC High-pin count connectors

Electrical

- Power consumption:
  - 300 W
  - 50 W available to supply an RTM
- Input voltage:
  - -48 VDC

Mechanical

- Form factor:
  - AdvancedTCA
- Dimensions:
  - 8U x 280 mm x 30.48 mm

Environmental

- Temperature (operating):
  - 0˚C to +45˚C
- Temperature (storage):
  - -40˚C to +70˚C
- Humidity (operating):
  - 5% to 95% non-condensing
- Humidity (storage):
  - 95% non-condensing
- Altitude (operating):
  - 0 to 10,000 ft
- Altitude (storage):
  - 0 to 16,400 ft

Nutaq products are constantly being improved; therefore, Nutaq reserves the right to modify the information herein at any time and without prior notice. The FMC logo is a trademark of VITA.

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