Nutaq
WD8G/WD20G

RF Wideband 8/20 GHz Digitizer

PRODUCT SHEET

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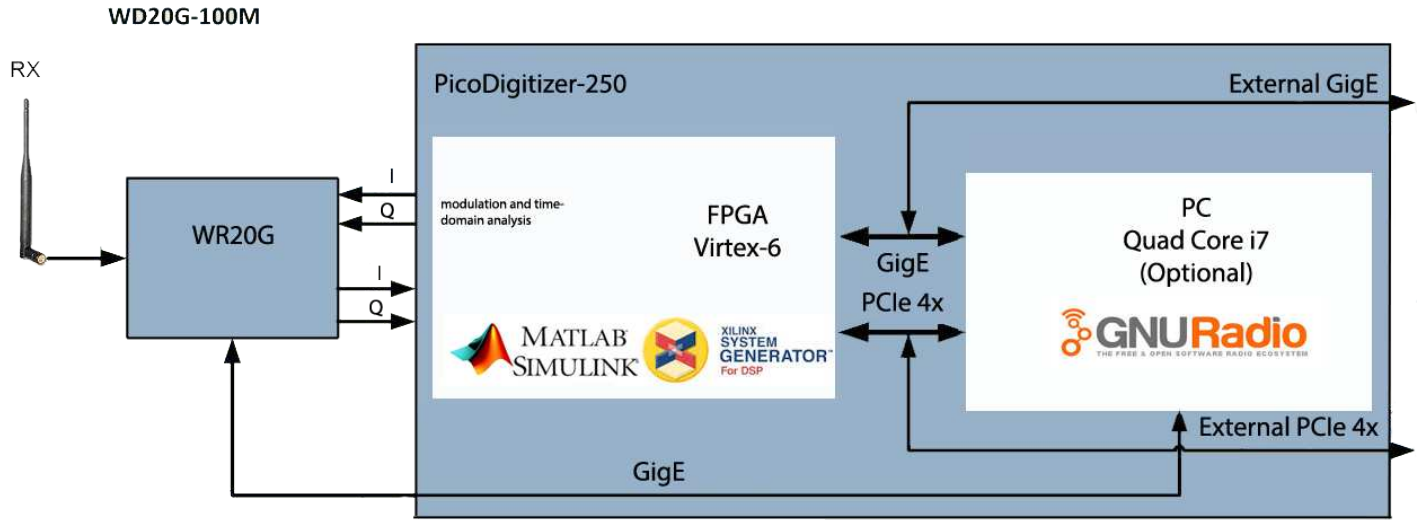
Nutaq **WD8G/WD20G**

The WD8G/WD20G is an FPGA-based, 8 or 20 GHz RF wideband digitizer. A table-top solution, the WD8G/WD20G incorporates Nutaq's WR8G/20G RF front-end and the PicoDigitizer 250 Series FPGA-based I/Q digitizer.

The WR8G/20G is a highly tunable receiver that can capture an entire 100 MHz wide band anywhere within a frequency range of 100 kHz to 20 GHz.

The PicoDigitizer 250 Series is a high-speed, FPGA-based 250 MHz wideband I/Q processor. The PicoDigitizer incorporates an I/Q processor node that includes a dual 250 MSPS 14-bit A/D converter and a dual 1 GSPS 16-bit D/A channel (for modulation and time-domain analysis) on a large Virtex-6 FPGA. An optional embedded Intel Quad-core i7 processor is available for standalone applications.



WD8G/20G Key Features

WR8G/20G:

- 100 kHz to 20 GHz tuning range
- Up to 100 MHz wide instantaneous captured signal bandwidth
- 10 MHz In/Out for multi-channel synchronization
- Analog I/Q inputs for modulation and time-domain analysis
- Analog I/Q outputs for real-time digitization
- Time triggering, PPS and other GPIO access for external peripheral control
- GigE control interface

PicoDigitizer 250:

- Wideband I/Q processor node, enabling the processing of up to 250 MHz baseband bandwidth
- A dual 250 MSPS 14 bits A/D and dual 1000 MSPS 16 bit D/A
- A large Virtex-6 (LX240T, LX550T, SX315T or SX475T)
- Optional Intel Quad-core i7 (embedded version)
- GigE and PCIe 4x interfaces

Configurations

	WD8G	WD8G (embedded)	WD20G	WD20G (embedded)
RF Tuning Range	100 kHz - 8 GHz	100 kHz - 8 GHz	100 kHz - 20 GHz	100 kHz - 20 GHz
Maximum BW	100 MHz	100 MHz	100 MHz	100 MHz
Max. Dynamic Range	100 dB	100 dB	100 dB	100 dB
A/D Converters	2	2	2	2
Maximum Input Sampling Frequency	250 MSPS	250 MSPS	250 MSPS	250 MSPS
Input Resolution	14 bits	14 bits	14 bits	14 bits
D/A Converters	2	2	2	2
Maximum Output Sampling Frequency	1000 MSPS	1000 MSPS	1000 MSPS	1000 MSPS
Output Resolution	16 bits	16 bits	16 bits	16 bits
FPGA*	1x Virtex-6*	1x Virtex-6*	1x Virtex-6*	1x Virtex-6*
Remote Host Interface	1x GigE 1x PCIe-4x	1x GigE Dual PCIe 4x (between embedded i7 and Virtex-6) Or Single PCIe 4x (between embedded i7 and Virtex-6) + Single PCIe 4x external	1x GigE 1x PCIe-4x	1x GigE Dual PCIe 4x (between Embedded i7 and Virtex-6) Or Single PCIe 4x (between embedded i7 and Virtex-6) + Single PCIe 4x external
Embedded CPU	None	Intel Quad-core i7-2715QE	None	Intel Quad-core i7-2715QE
Embedded Storage**	N.A.	64 GB SSD +2x SATA** interface	N.A.	64 GB SSD +2x SATA** interface

* Available Virtex-6 options: LX240T, LX550T, SX315T or SX475T
** 1X SATA connection Rear PicoDigitizer panel, 1X SATA for internal 1.8-inch SSD drive

Model-Based Design Flow

Rapid System-Level FPGA Development in MATLAB and Xilinx System Generator for DSP

Built on top of Nutaq's Board Software Development Kit (BSDK), the Model-Based Design Kit (MBDK) enables the rapid design, simulation, testing, and deployment of applications from the Simulink graphical environment without the need for hand-coding in either VHDL or C.

Some of the benefits presented by Nutaq's model-based design approach include:

- A significant reduction in the time spent on low value-added tasks such as programming I/O interfaces, adjusting FPGA constraints, debugging drivers etc.
- Providing host co-simulation tools which enables:
    - o I/O integration within simulations
    - o Step-by-step FPGA fabric design migration
    - o Easy FPGA-to-host interaction
    - o Data logging
- Tools such as record/playback, host I/O control, and data streaming libraries.

FPGA Recording/Playback Core

The FPGA SDRAM recording/playback module enables the storage and playback of very high speed multi-channel bursts of data in the FPGA-attached SDRAM. The data can then be transferred to a host device for storage and/or real-time analysis or loaded into memory for looped playback transmission over the high-speed D/A converters.

The FPGA record/playback IP core comes with standard trigger mechanisms (single shot, normal and continuous). The trigger sources can come from the host processor, a user-defined FPGA signal, or from the external WD8G/WD20G analog trigger front-panel input.

The FPGA recording/playback core is flexible, enabling the user to define the number of channels to record/playback, as well as the acquisition rate so that the available recording memory bandwidth is used efficiently. Note that FPGA pre/post-processing on the channels can be performed before recording or after playback, in order to potentially reduce recording/playback bandwidth needs.

- DDR3 FPGA memory size = 4 GB
- Maximum data throughput = 5.7 GBps

Application Example:

FPGA-based filtering on two channels sampled at 125 MSPS on the FPGA (decimation by 16), then record for both channels. Each channel can be recorded for 128 seconds.

Applications

- Passive RADAR
- MIMO RADAR
- Distributed RADAR
- Signal intelligence and electronic warfare (SIGINT/EW)
- Satellite communication (SATCOM)
- Beam forming or direction finding
- Wireless spectrum analysis
- Spectrum monitoring
- Channel sounding

RTDEx (Real Time Data Exchange)

Nutaq's RTDEx IP core provides users with a framework to exchange data with a host device through either the GigE or PCIe links, yielding the highest bandwidth and lowest possible latency.

Built to complement our "snapshot" FPGA recording/playback capabilities, the RTDEx IP core provides a continuous data flow (also supports burst mode) from the acquisition/transmission to/from the host computer, for further real-time computing or real-time PC recording/playback.

HOST - FPGA Streaming	GigE	PCIe 4x (Gen 1)
Data BW	1 Gbps	10 Gbps
Data Throughput	900 Mbps	6.4 Gbps
Roundtrip Latency (4kB, send & receive)	1 msec	200-300 µsec

Specifications

WR8 / 20G

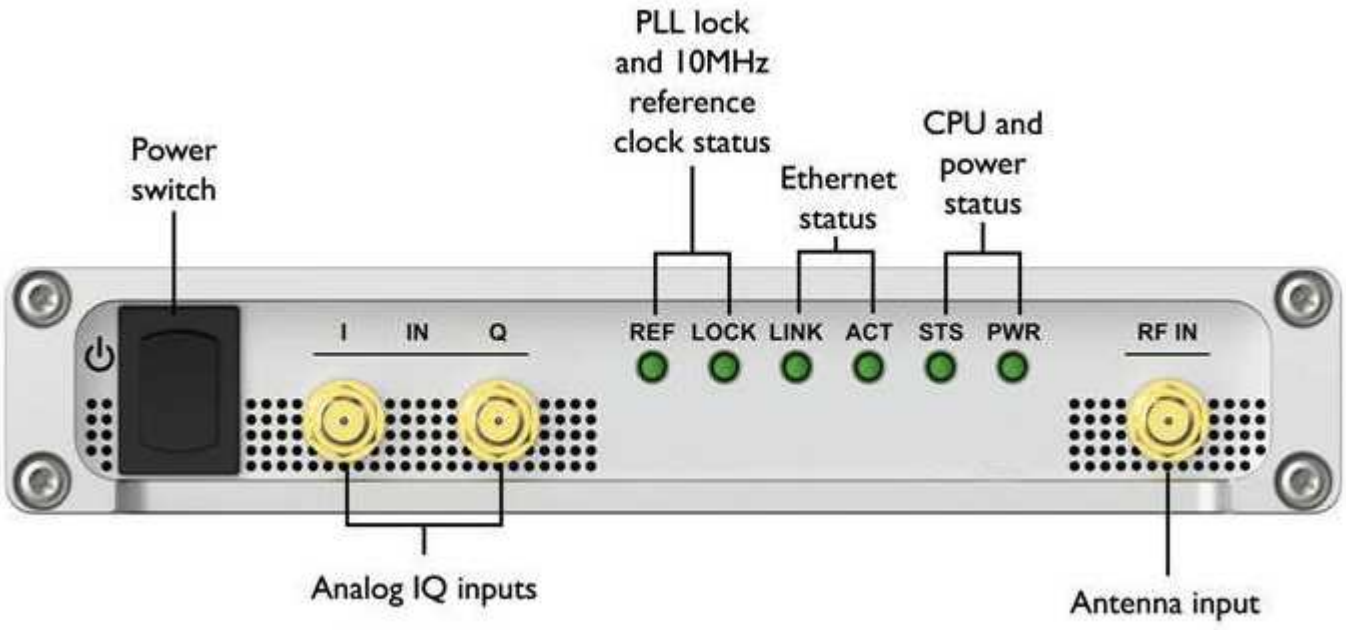
Frequency Range	100 kHz to 8/20 GHz
Max. Instantaneous Bandwidth	10 MHz; 100 MHz
Max. Dynamic Range	100 dB
Noise Figure	< 15 dB
Absolute Max RF Input Power (Attenuater OFF)	-10 dBm
Absolute Max RF Input Power (Attenuater ON)	+10 dBm
Max. RF Gain	20 dB
Max. IF Gain	20 dB
Gain Control	30 dB; 0.5 dB steps
RF PLL Phase Noise (2 GHz)	-100 dBc @ 100 kHz offset
Spectrum Scan Rate	200 GHz/s @ 122 kHz RBW
RF PLL Lock Time	< 100 µs

PicoDigitizer 250

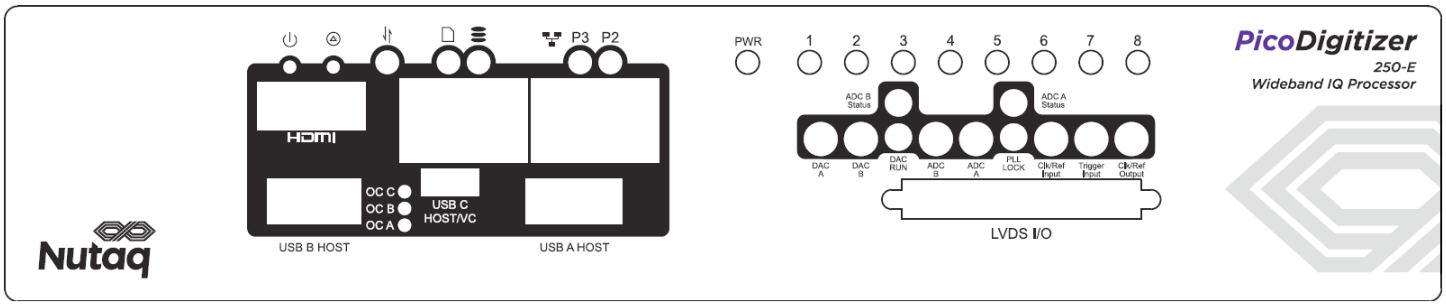
FPGA	
	Supports LX240T, LX550T, SX315T and SX475T FPGA devices
	Supports up to 2 PCIe (4X) interfaces; Supports GigE interface
	4 GB SODIMM DDR3
	18 MB QDR2 SRAM
	64 MB NOR Flash
	128 MB DDR3 SRAM dedicated for Nutaq's Central Communication Engine (CCE) application and the MicroBlaze's Embedded Linux OS
	Remote host throughput: approx. 900 Mbps (GigE), approx. 6.4 Gbps (PCIe)
Embedded CPU Section	
	Intel Quad-core i7 Gen2 CPU, 2.1 GHz processor
	8 GB DDR3 SDRAM
	64 GB SSD
	GigE & Dual PCIe 4x support
	SATA –II/III support
	Embedded throughput (FPGA-CPU): 1x PCIe 4x (approx. 6.4 Gbps)
A/D Sampler Coupling	
	AC coupled
	Single-ended
A/D Sampler Characteristics	
	14 bit
	250 MSPS maximum
	2 channels
A/D Performance	
	Input external CLK or external reference
	Output CLK or reference
	Analog input bandwidth : 470 MHz (-3dB)
	SNR (dB): 70.5 (@ 30 MHz) , 70 (@ 70 MHz), 65 (@ 150 MHz)
	SFDR (dBc): 75 (@ 30 MHz) , 85 (@ 70 MHz), 74 (@ 150 MHz)
	THD (dBc): 74 (@ 30 MHz) , 84 (@ 70 MHz), 74 (@ 150 MHz)
D/A Sampler Coupling	
	A/C coupled
	Single-ended
D/A Sampler Characteristics	
	16 bit
	1000 MSPS maximum
	2 channels
D/A Performance	
	Analog output bandwidth : 500 MHz (1GSPS DAC)
	Phase noise (1MHz; dBc/Hz): 125 (@ 30 MHz) , 122 (@ 70 MHz), 121 (@ 150 MHz)
	2nd harmonic (dBc): 63 (@ 30 MHz) , 57 (@ 70 MHz), 54 (@ 150 MHz)
	3rd harmonic (dBc): 69 (@ 30 MHz) , 61 (@ 70 MHz), 52 (@ 150 MHz)
Sampling Clock	
	Equipped with an onboard, low-jitter reference clock and synchronization PLL (AD9511)
	Input PPS signal for GPS disciplining of on-board reference clock

Front Panel Connectors

WR8 / 20G



PicoDigitizer 250



Analog Inputs, CLK & Triggers (All digitizer models)

Each I/Q Processor Node

- 2x A/D channel MMCX inputs
- 2x D/A channel MMCX outputs
- 1x external trigger/PPS input
- 1x external sampling or reference CLK input
- 1x sampling or reference CLK output

Digital Inputs & Outputs (All digitizer models)

- 1x VHDCI connector

VHDCI Connector Signal Map

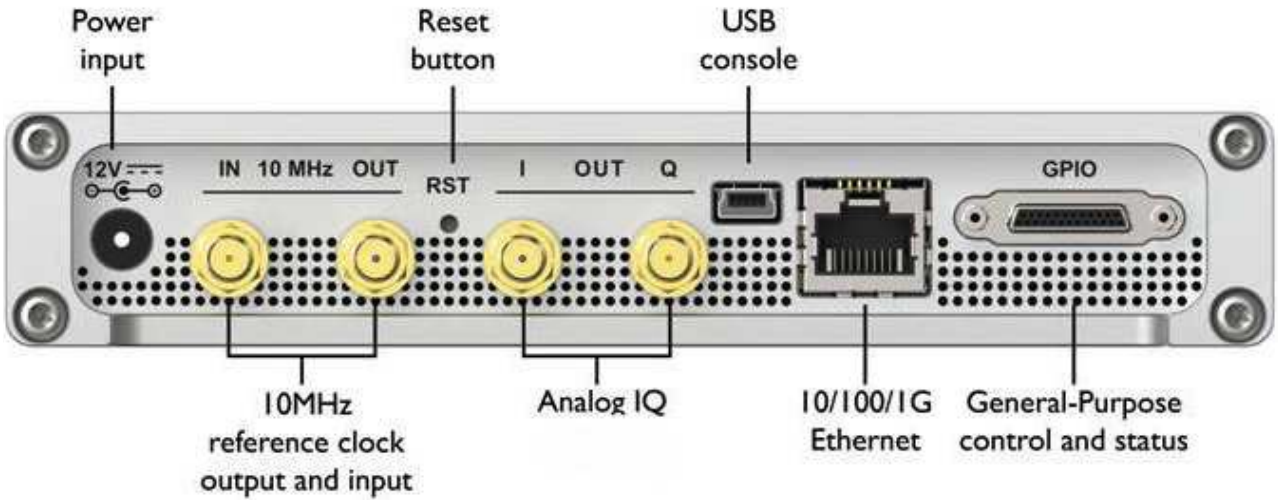
- 14x user LVDS I/O data
- 1x LVDS clock

Additional Front Panel Connectors (Embedded models only)

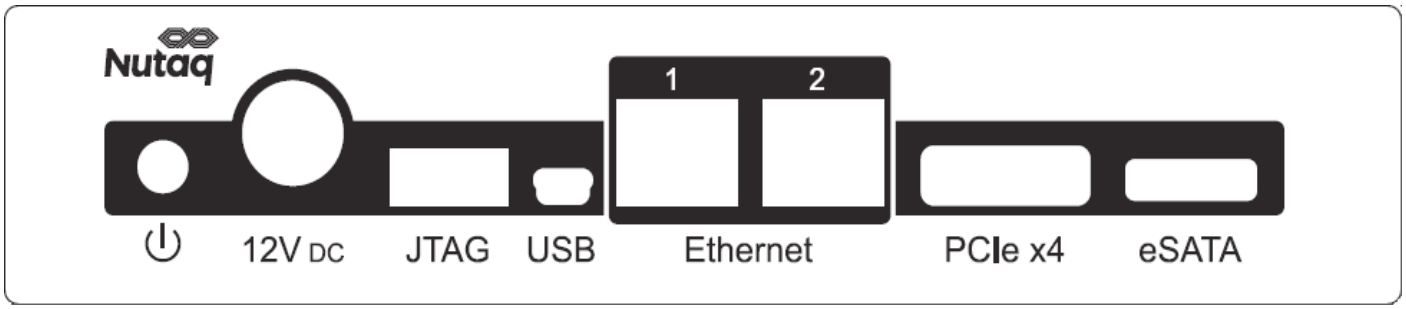
- 1x HDMI
- 2x GigE
- 1x Mini-USB
- 1x COM
- 1x USB 2.0

Rear Panel Connectors

WR8 / 20G



PicoDigitizer 250



- 2x GigE ports
- 1x USB UART FPGA console port
- 1x external universal power supply
- 1x SATA (Embedded models only)
- 1x PCIe 4x cable interface connector

Ordering Information

WD8 / 20G-A-B-C-D-E

8/20G	8 G = 8 GHz version	20 G = 20 GHz version
A (Embedded CPU Option)	0 = No Embedded CPU	1 = 4C i7 Embedded CPU
B (FPGA Option)	0 = LX240T	1 = LX550T
	2 = SX315T	3= SX475T
C (Additional Embedded Storage)	0 = None	1 = 200 GB SSD [for Embedded CPU option only] (172 MBytes/s)
D (External PCIe)	0 = No external PCIe (For embedded CPU option only : dual PCIe 4x between V6 and embedded 4Ci7)	1 = PCIe 4x external link to FPGA
E (Model-Based Design Software License)	0 = No software license	1 = 1x MBDK workstation license