INNOVATIVE DISPLAY TECHNOLOGIES
17171 MURPHY AVENUE
IRVINE, CALIFORNIA 92614-5915
P: 949-417-8070/F: 949-417-8075

E-mail: info@shellyinc.com
Website: www.shellyinc.com

Specification

Part Number : SOG24006437-BTN-ELLW

Customer :

Note : Recommended use BOOSTER: 4x

APPROVED BY: (FOR CUSTOMER USE ONLY)	PCB VERSION: DATE:

SOLD BY	APPROVED BY	CHECKED BY	ISSUE DATE

MODLE NO :
DOC. FIRST ISSUE

RECORDS OF REVISION

VERSION	DATE	REVISED PAGE NO.	**SUMMARY**
0	2007.12.14		First issue
A	2008.04.15	6	Modify I_{DD}
B	2008.11.19	52	Modify Backlight information

Contents

1. Module Classification Information

SOG24006437- BTN - ELLW
① ②　③　④　⑤ ⑥ ⑦　⑧

① Brand：Shelly Associates Inc.

② Display Type：SOG→ COG Type

③ Display Font：240 x 64 dots

④ Model serials no. A

⑤ Backlight Type：　LW→ LED, White

⑥ LCD Mode：　EL→ FSTN Negative

⑦ LCD Polarize Type/ Temperature range/ View direction　E→ Transmissive, W. T, 6:00

⑧ Special Code　#:Fit in with the ROHS Directions and regulations

2. Precautions in use of LCD Modules

(1)Avoid applying excessive shocks to the module or making any alterations or modifications to it.
(2)Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.
(3)Don't disassemble the LCM.
(4)Don't operate it above the absolute maximum rating.
(5)Don't drop, bend or twist LCM.
(6)Soldering: only to the I/O terminals.
(7)Storage: please storage in anti-static electricity container and clean environment.
(8) The factory has the right to change the passive components
(9) The factory has the right to change the PCB Rev.

3.General Specification

Item	Dimension	Unit
Number of Characters	240 x 64 dots	-
Module dimension	142.5x 51.7 x 14.9(MAX)	mm
View area	130.2 x 37.6	mm
Active area	127.065 x 33.841	mm
Dot size	0.5 x 0.5	mm
Dot pitch	0.53 x 0.53	mm
LCD type	FSTN Negative, Transmissive (In LCD production, It will occur slightly color difference. We can only guarantee the same color in the same batch.)	
Duty	1/64	
View direction	6 o'clock	
Backlight Type	LED White	

4.Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_{OP}	-20	-	+70	℃
Storage Temperature	T_{ST}	-30	-	+80	℃
Input Voltage	V_I	V_{SS}	-	V_{DD}	V
Supply Voltage For Logic	V_{DD}-V_{SS}	-0.3	3.3	5.0	V
Supply Voltage For LCD	V_{DD}-V_O	-0.3	*	18	V

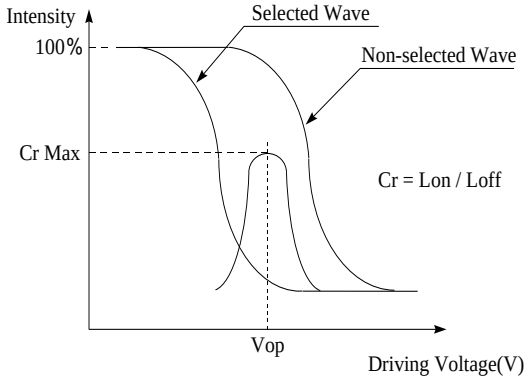
5.Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	V_{DD}-V_{SS}	-	3.0	3.3	3.6	V
Supply Voltage For LCD	V_{DD}-V_0	Ta=-20℃ Ta=25℃ Ta=70℃	- 9.3 -	- 10.0 -	- 10.7 -	V V V
Input High Volt.	V_{IH}	-	0.8 V_{DD}	-	V_{DD}	V
Input Low Volt.	V_{IL}	-	Vss	-	0.2 V_{DD}	V
Output High Volt.	V_{OH}	-	0.8 V_{DD}	-	V_{DD}	V
Output Low Volt.	V_{OL}	-	Vss	-	0.2V_{DD}	V
Supply Current(No include LED Backlight)	I_{DD}	V_{DD}=3.3V	-	1.5	2.5	mA

6.Optical Characteristics

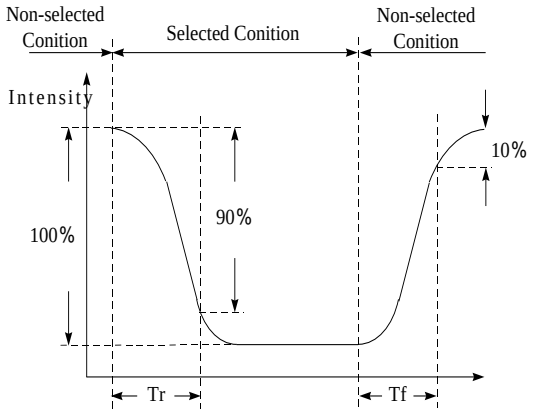
Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V)θ	CR≧ 2	30	-	60	deg
	(H)φ	CR≧ 2	-45	-	45	deg
Contrast Ratio	CR	-	-	5	-	-
Response Time	T rise	-	-	200	300	ms
	T fall	-	-	200	300	ms

Definition of Operation Voltage (Vop)



[positive type]

Definition of Response Time (Tr , Tf)



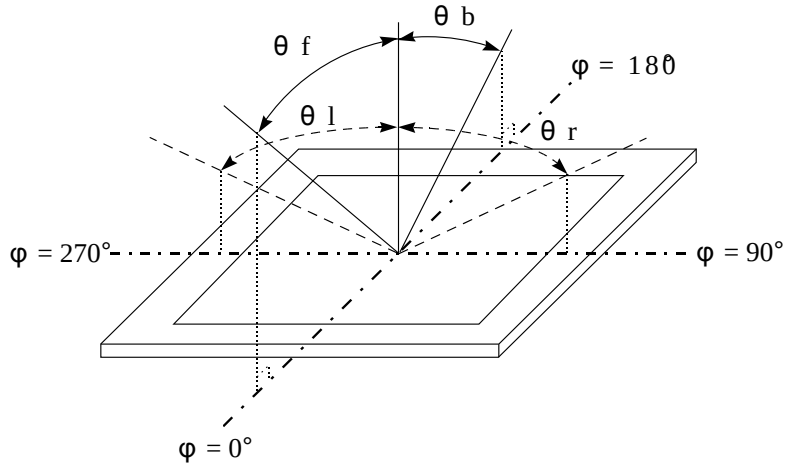
[positive type]

Conditions :

Operating Voltage : Vop Viewing Angle(θ , φ) : 0° , 0°

Frame Frequency : 64 HZ Driving Waveform : 1/N duty , 1/a bias

Definition of viewing angle(CR≧ 2)



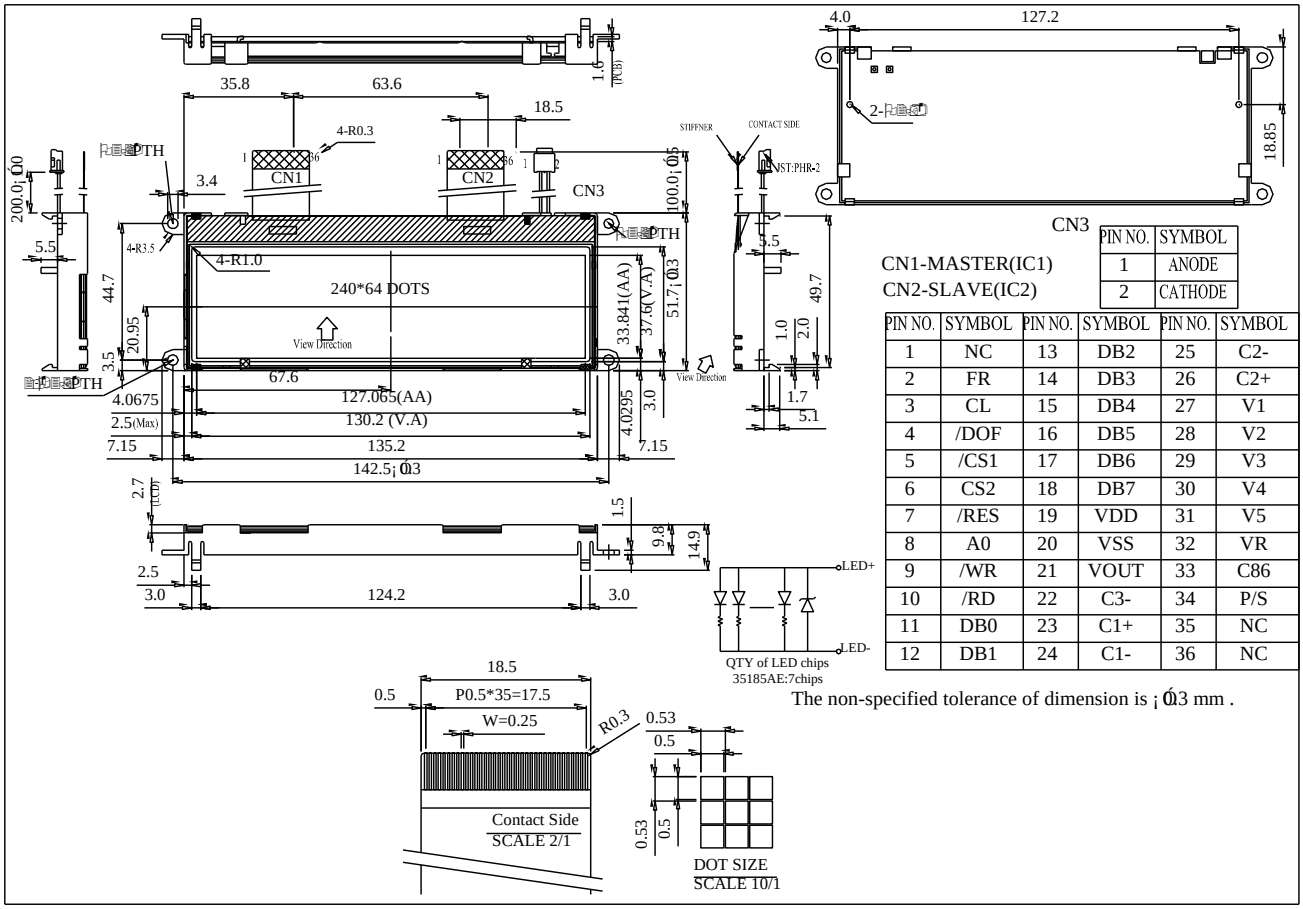
7.Interface Pin Function

Pin No.	Symbol	Level	Description
1	NC		No connection
2	FR	O	This is the liquid crystal alternating current signal terminal.
3	CL	I/O	This is the display clock input terminal The following is true depending on the M/S and CLS status. M/S: "H" → CLS: "H" → CL: Output; CLS: "L" → CL: Input M/S: "L" → CLS: "H" → CL: Input; CLS: "L" → CL: Input
4	/DOF	O	This is the LCD blanking control terminal.
5	/CS1	H/L	This is the chip select signal. When /CS1 = "L" and CS2 = "H," then the chip select becomes active, and data/command I/O is enabled.
6	CS2	H/L	
7	/RES	I	When /RES is set to "L," the settings are initialized. The reset operation is performed by the /RES signal level.
8	A0	H/L	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = "H": Indicates that D0 to D7 are display data. A0 = "L": Indicates that D0 to D7 are control data.
9	/WR	H/L	• When connected to an 8080 MPU, this is active LOW. (R/W) This terminal connects to the 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. • When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When R/W = "H": Read. When R/W = "L": Write.

<table>
<tr><td>10</td><td>/RD</td><td>I</td><td>• When connected to an 8080 MPU, this is active LOW.
(E) This pin is connected to the /RD signal of the 8080 MPU, and the ST7565S series data bus is in an output status when this signal is “L”.
• When connected to a 6800 Series MPU, this is active HIGH.
This is the 6800 Series MPU enable clock input terminal.</td></tr>
<tr><td>11</td><td>DB0</td><td>H/L</td><td>Data bus line</td></tr>
<tr><td>12</td><td>DB1</td><td>H/L</td><td>Data bus line</td></tr>
<tr><td>13</td><td>DB2</td><td>H/L</td><td>Data bus line</td></tr>
<tr><td>14</td><td>DB3</td><td>H/L</td><td>Data bus line</td></tr>
<tr><td>15</td><td>DB4</td><td>H/L</td><td>Data bus line</td></tr>
<tr><td>16</td><td>DB5</td><td>H/L</td><td>Data bus line</td></tr>
<tr><td>17</td><td>DB6</td><td>H/L</td><td>Data bus line</td></tr>
<tr><td>18</td><td>DB7</td><td>H/L</td><td>Data bus line</td></tr>
<tr><td>19</td><td>V_{DD}</td><td>3.3V</td><td>Supply Voltage for logic</td></tr>
<tr><td>20</td><td>V_{SS}</td><td>0V</td><td>Ground</td></tr>
<tr><td>21</td><td>Vout</td><td></td><td>Operating voltage for LCD</td></tr>
<tr><td>22</td><td>C3-</td><td></td><td></td></tr>
<tr><td>23</td><td>C1+</td><td></td><td></td></tr>
<tr><td>24</td><td>C1-</td><td></td><td></td></tr>
<tr><td>25</td><td>C2-</td><td></td><td></td></tr>
<tr><td>26</td><td>C2+</td><td></td><td></td></tr>
<tr><td>27</td><td>V1</td><td></td><td rowspan="5">This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on VDD, and must maintain the relative magnitudes shown below.
VDD (= V0) ≧V1 ≧V2 ≧V3 ≧V4 ≧V5
When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.
<table><tr><td></td><td>1/65 DUTY</td><td>1/49 DUTY</td><td>1/33 DUTY</td><td>1/55 DUTY</td><td>1/53 DUTY</td></tr><tr><td>V1</td><td>1/9*V5,1/7*V5</td><td>1/8*V5,1/6*V5</td><td>1/6*V5,1/5*V5</td><td>1/8*V5,1/6*V5</td><td>1/8*V5,1/6*V5</td></tr><tr><td>V2</td><td>2/9*V5,2/7*V5</td><td>2/8*V5,2/6*V5</td><td>2/6*V5,2/5*V5</td><td>2/8*V5,2/6*V5</td><td>2/8*V5,2/6*V5</td></tr><tr><td>V3</td><td>7/9*V5,5/7*V5</td><td>6/8*V5,4/6*V5</td><td>4/6*V5,3/5*V5</td><td>6/8*V5,4/6*V5</td><td>6/8*V5,4/6*V5</td></tr><tr><td>V4</td><td>8/9*V5,6/7*V5</td><td>7/8*V5,5/6*V5</td><td>5/6*V5,4/5*V5</td><td>7/8*V5,5/6*V5</td><td>7/8*V5,5/6*V5</td></tr></table></td></tr>
<tr><td>28</td><td>V2</td><td></td></tr>
<tr><td>29</td><td>V3</td><td></td></tr>
<tr><td>30</td><td>V4</td><td></td></tr>
<tr><td>31</td><td>V5</td><td></td></tr>
<tr><td>32</td><td>VR</td><td></td><td>Output voltage regulator terminal. Provides the voltage between VDD and
V5 through a resistive voltage divider.
IRS = “L” : the V5 voltage regulator internal resistors are not used .
IRS = “H” : the V5 voltage regulator internal resistors are used</td></tr>
</table>

<table>
<tr><td>33</td><td>C86</td><td></td><td>This is the MPU interface switch terminal.
C86 = “H”: 6800 Series MPU interface.
C86 = “L”: 8080 MPU interface.</td></tr>
<tr><td>34</td><td>P/S</td><td></td><td>This is the parallel data input/serial data input switch terminal.
P/S = “H”: Parallel data input.
P/S = “L”: Serial data input.
The following applies depending on the P/S status:
<table>
<tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr>
<tr><td>“H”</td><td>A0</td><td>D0 to D7</td><td>/RD, /WR</td><td>X</td></tr>
<tr><td>“L”</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr>
</table>
When P/S = “L”, D0 to D5 fixed “H”.
/RD (E) and /WR (R/W) are fixed to either “H” or “L”.
With serial data input, It is impossible read data from RAM .</td></tr>
<tr><td>35</td><td>NC</td><td></td><td>No connection</td></tr>
<tr><td>36</td><td>NC</td><td></td><td>No connection</td></tr>
</table>

8.Contour Drawing &Block Diagram



CN1-MASTER(IC1)
CN2-SLAVE(IC2)

CN3

PIN NO.	SYMBOL
1	ANODE
2	CATHODE

PIN NO.	SYMBOL	PIN NO.	SYMBOL	PIN NO.	SYMBOL
1	NC	13	DB2	25	C2-
2	FR	14	DB3	26	C2+
3	CL	15	DB4	27	V1
4	/DOF	16	DB5	28	V2
5	/CS1	17	DB6	29	V3
6	CS2	18	DB7	30	V4
7	/RES	19	VDD	31	V5
8	A0	20	VSS	32	VR
9	/WR	21	VOUT	33	C86
10	/RD	22	C3-	34	P/S
11	DB0	23	C1+	35	NC
12	DB1	24	C1-	36	NC

The non-specified tolerance of dimension is ¡ 0.3 mm .

9.Function Description

The MPU Interface

Selecting the Interface Type

With the ST7565S chips, data transfers are done through an 8-bit parallel data bus (D7 to D0) or through a serial data input (SI). Through selecting the P/ S terminal polarity to the "H" or "L" it is possible to select either parallel data input or serial data input as shown in Table 1.

Table 1

P/S	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D5~D0
H: Parallel Input	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D5~D0
L: Serial Input	/CS1	CS2	A0	—	—	—	SI	SCL	(HZ)

"—" indicates fixed to either "H" or to "L"

The Parallel Interface

When the parallel interface has been selected (P/S ="H"), then it is possible to connect directly to either an 8080-system MPU or a 6800 Series MPU (shown in Table 2) by selecting the C86 terminal to either "H" or to "L".

Table 2

C86 (P/S=H)	/CS1	CS2	A0	E(/RD)	R/W(/WR)	D7~D0
H: 6800 Series	/CS1	CS2	A0	E	R/W	D7~D0
L: 8080 Series	/CS1	CS2	A0	/RD	/WR	D7~D0

Moreover, data bus signals are recognized by a combination of A0, /RD (E), /WR (R/W) signals, as shown in Table 3.

Table 3

Shared	6800 Series	8080 Series		Function
A0	R/W	/RD	/WR	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	1	0	1	Status read
0	0	1	0	Write control data (command)

The Serial Interface

When the serial interface has been selected (P/S = "L") then when the chip is in active state (/CS1 = "L" and CS2 = "H") the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the eighth serial clock for the processing.

The A0 input is used to determine whether or the serial data input is display data or command data; when

A0 = “H”, the data is display data, and when A0 = “L” then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active. Figure 1 is a serial interface signal chart.

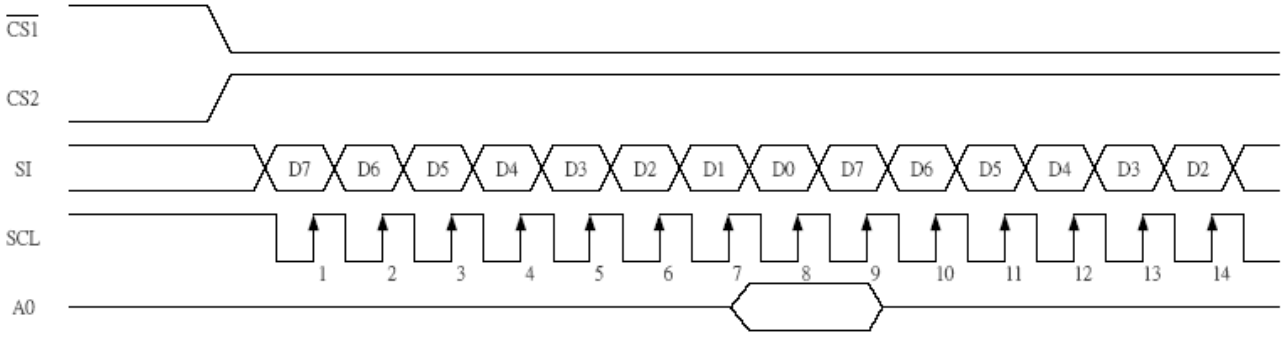


Figure 1

* When the chip is not active, the shift registers and the counter are reset to their initial states.
* Reading is not possible while in serial interface mode.
* Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

The Chip Select

The ST7565S have two chip select terminals: /CS1 and CS2.

The MPU interface or the serial interface is enabled only when /CS1 = “L” and CS2 = “H”.

When the chip select is inactive, D0 to D7 enter a high impedance state, and the A0, /RD, and /WR inputs are inactive. When the serial interface is selected, the shift register and the counter are reset.

The Accessing the Display Data RAM and the Internal Registers

Data transfer at a higher speed is ensured since the MPU is required to satisfy the cycle time (tCYC) requirement alone in accessing the ST7565S. Wait time may not be considered.

And, in the ST7565S, each time data is sent from the MPU, a type of pipeline process between LSIs is performed through the bus holder attached to the internal data bus.

Internal data bus.

For example, when the MPU writes data to the display data RAM, once the data is stored in the bus holder, then it is written to the display data RAM before the next data write cycle. Moreover, when the MPU reads the display data RAM, the first data read cycle (dummy) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle.

There is a certain restriction in the read sequence of the display data RAM. Please be advised that data of the specified address is not generated by the read instruction issued immediately after the address setup. This data is generated in data read of the second time. Thus, a dummy read is required whenever the address setup or write cycle operation is conducted.

This relationship is shown in Figure 2.

The Busy Flag

When the busy flag is “1” it indicates that the ST7565S is running internal processes, and at this time no command aside from a status read will be received. The busy flag is outputted to D7 pin with the read instruction. If the cycle time (tCYC) is maintained, it is not necessary to check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.

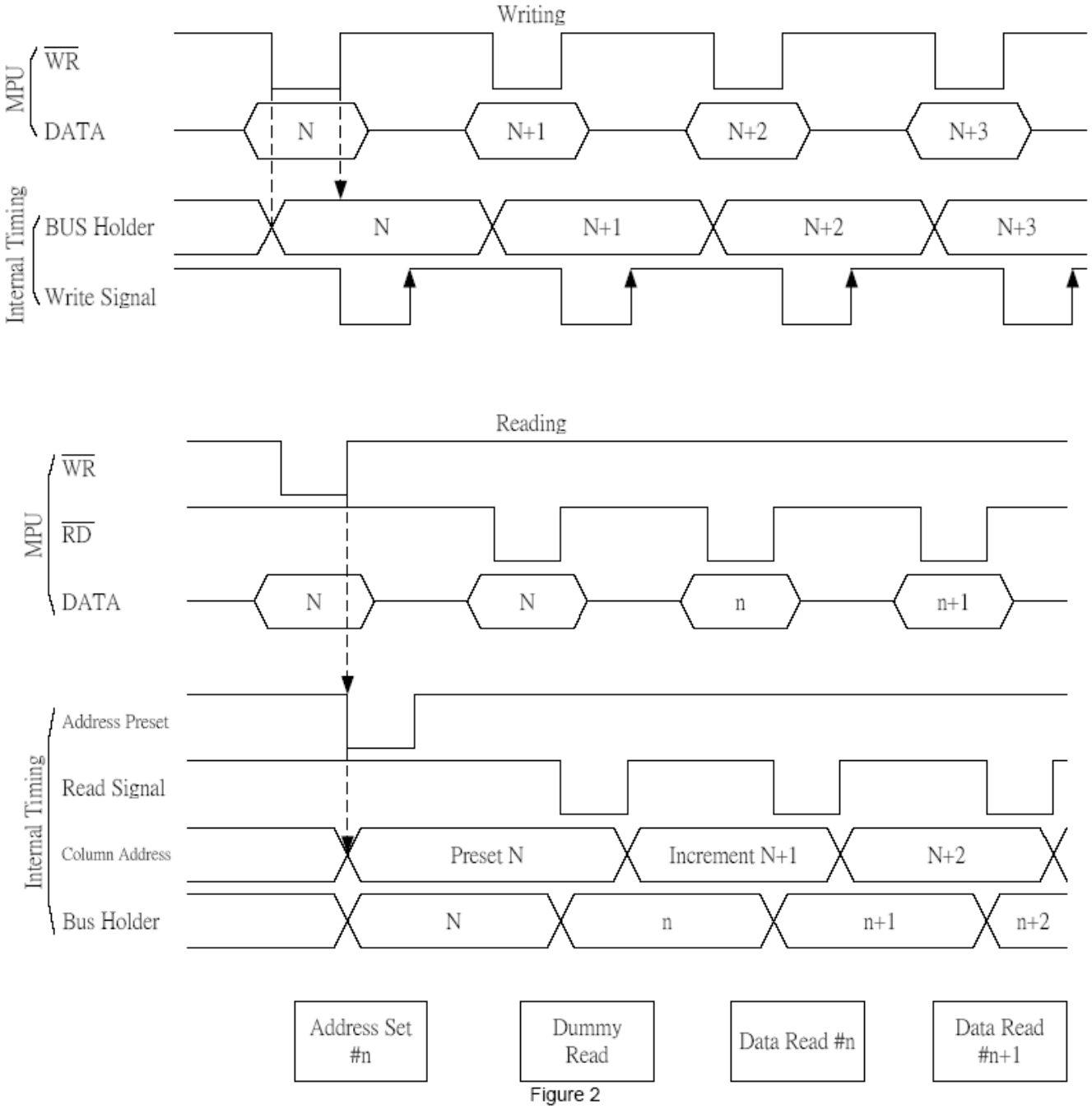


Figure 2

Display Data RAM

The display data RAM stores the dot data for the LCD. It has a 65 (8 page x 8 bit +1) x 132 bit structure. As is shown in Figure 3, the D7 to D0 display data from the MPU corresponds to the LCD display common direction; there are few constraints at the time of display data transfer when multiple ST7565S are used, thus and display structures can be created easily and with a high degree of freedom. Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).

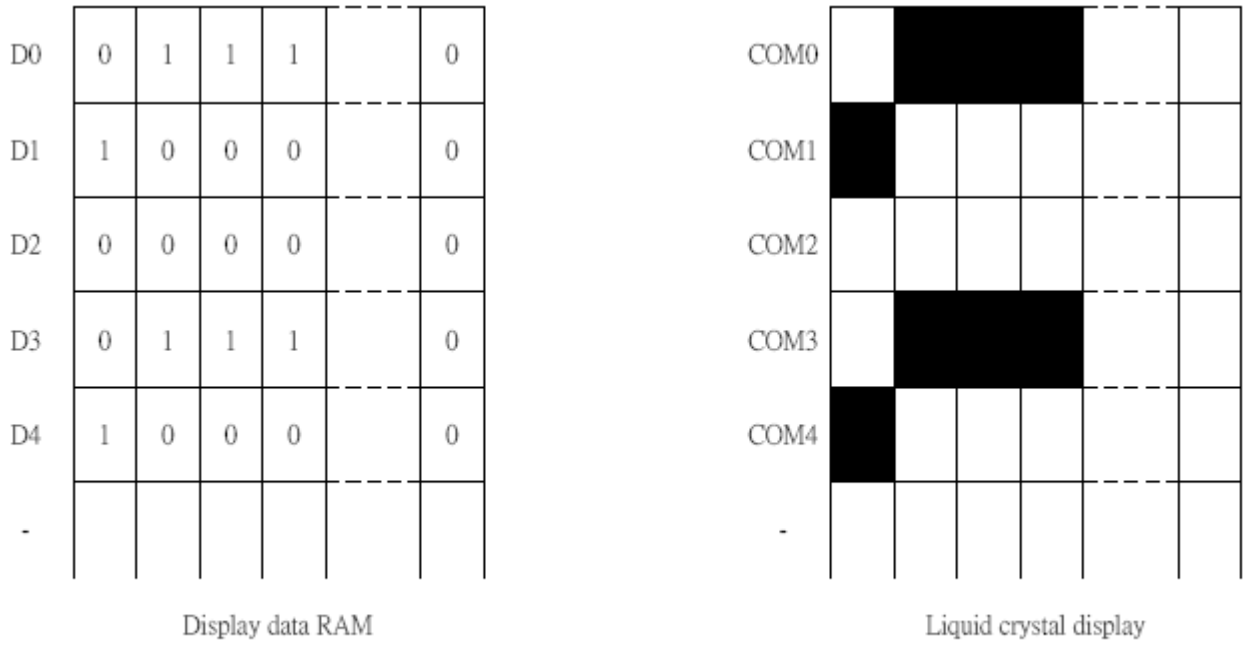


Figure 3

The Page Address Circuit

Page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.

Page address 8 (D3, D2, D1, D0 = 1, 0, 0, 0) is a special RAM for icons, and only display data D0 is used. (see Figure 4)

The Column Addresses

The display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously. Moreover, the incrementing of column addresses stops with 83H. Because the column address is independent of the page address, when moving, for example, from page 0 column 83H to page 1 column 00H, it is necessary to respective both the page address and the column address. Furthermore, as is shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized. As is shown in Figure 4,

Table 4

SEG Output ADC	SEG0		SEG 131
(D0) "0"	0 (H)	→ Column Address →	83 (H)
(D0) "1"	83 (H)	← Column Address ←	0 (H)

The Line Address Circuit

The line address circuit, as shown in Table 4, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COM63 output for ST7565S , the detail is shown page.11 The display area is a 65 line area for the ST7565S.

If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. can be performed.

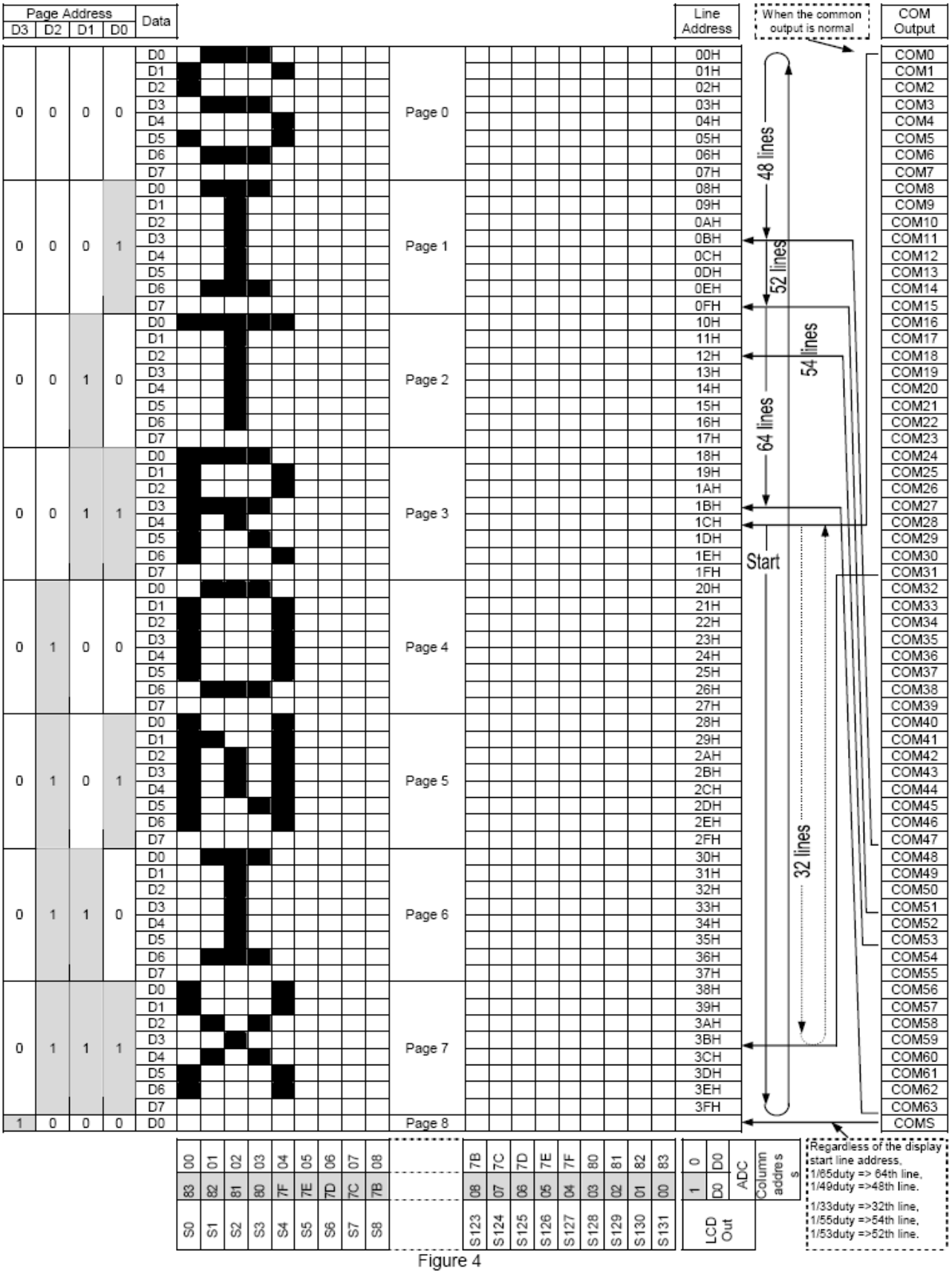


Figure 4

The Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM.

Because the display normal/reverse status, display ON/OFF status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the display data RAM itself.

The Oscillator Circuit

This is a CR-type oscillator that produces the display clock.

The oscillator circuit is only enabled when M/S= “H” and CLS = “H”.

When CLS = “L” the oscillation stops, and the external clock is input through the CL terminal.

Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal.

Reading to the display data liquid crystal driver circuits is completely independent of accesses to the display data RAM by the MPU. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, there is absolutely no adverse effect (such as flickering) on the display.

Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive wave form using a 2 frame alternating current drive method, as is shown in Figure 5, for the liquid crystal drive circuit.

Two-frame alternating current drive waveform

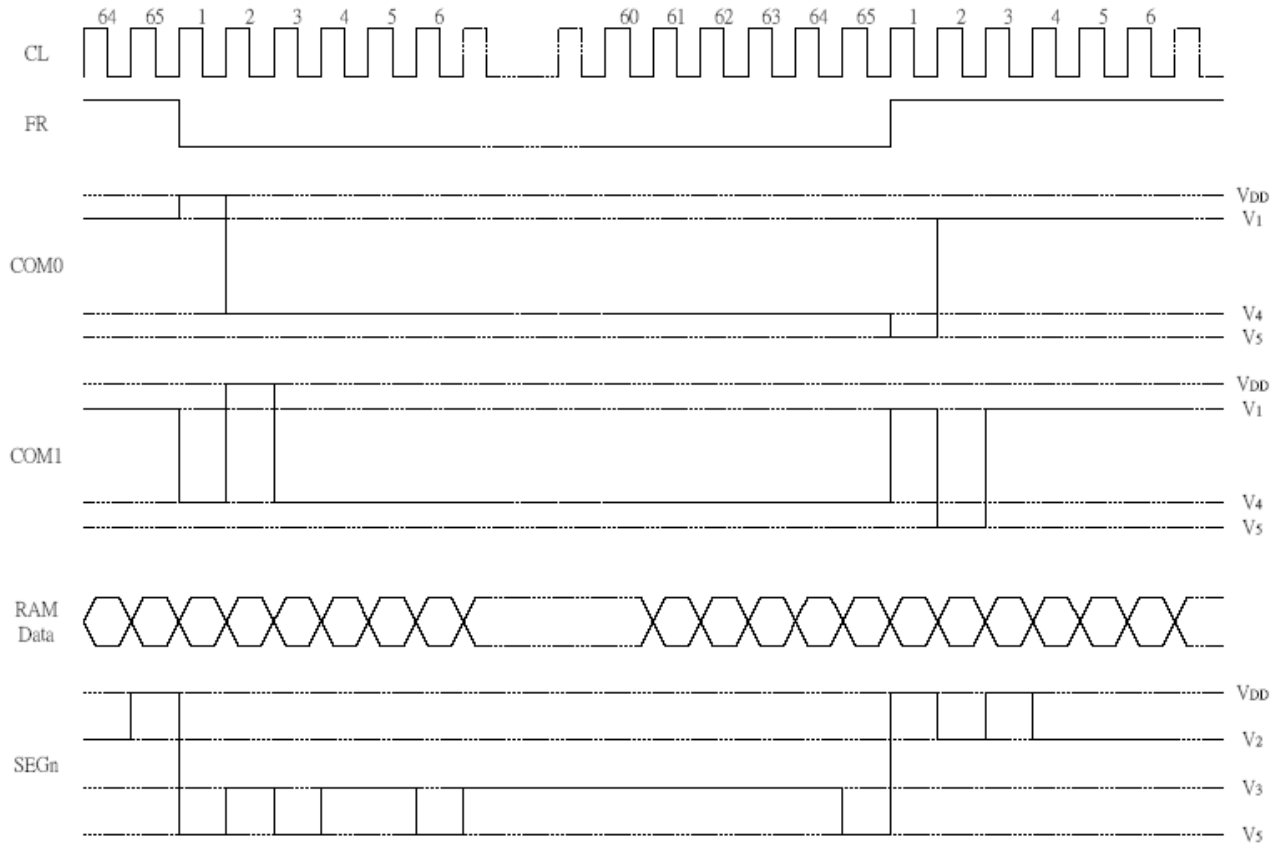


Figure 5

The Common Output Status Select Circuit

In the ST7565S chips, the COM output scan direction can be selected by the common output status select command. (See Table 6.) Consequently, the constraints in IC layout at the time of LCD module assembly can be minimized.

Table 6

Status	COM Scan Direction				
	1/65 DUTY	1/49 DUTY	1/33 DUTY	1/55 DUTY	1/53 DUTY
Normal	COM0 → COM63	COM0 → COM47	COM0 → COM31	COM0 → COM53	COM0 → COM51
Reverse	COM63 → COM0	COM47 → COM0	COM31 → COM0	COM53 → COM0	COM51 → COM0

Duty	Com dir	Common output pins							
		com[0:15]	com[16:23]	com[24:26]	com[27:36]	com[37:39]	com[40:47]	com[48:63]	coms
1/65	0	com[0:63]							coms
	1	com[63:0]							coms
1/49	0	com[0:23]		reserve			com[24:47]		coms
	1	com[47:24]		reserve			com[23:0]		coms
1/33	0	com[0:15]	reserve					com[16:31]	coms
	1	com[31:16]	reserve					com[15:0]	coms
1/55	0	com[0:26]			reserve	com[27:53]			coms
	1	com[53:27]			reserve	com[26:0]			coms
1/53	0	com[0:25]			reserve	com[26:51]			coms
	1	com[51:26]			reserve	com[25:0]			coms

The LCD Driver Circuits

These are a 187-channel that generates four voltage levels for driving the LCD. The combination of the display data, the COM scan signal, and the FR signal produces the liquid crystal drive voltage output. Figure 6 shows examples of the SEG and COM output wave form.

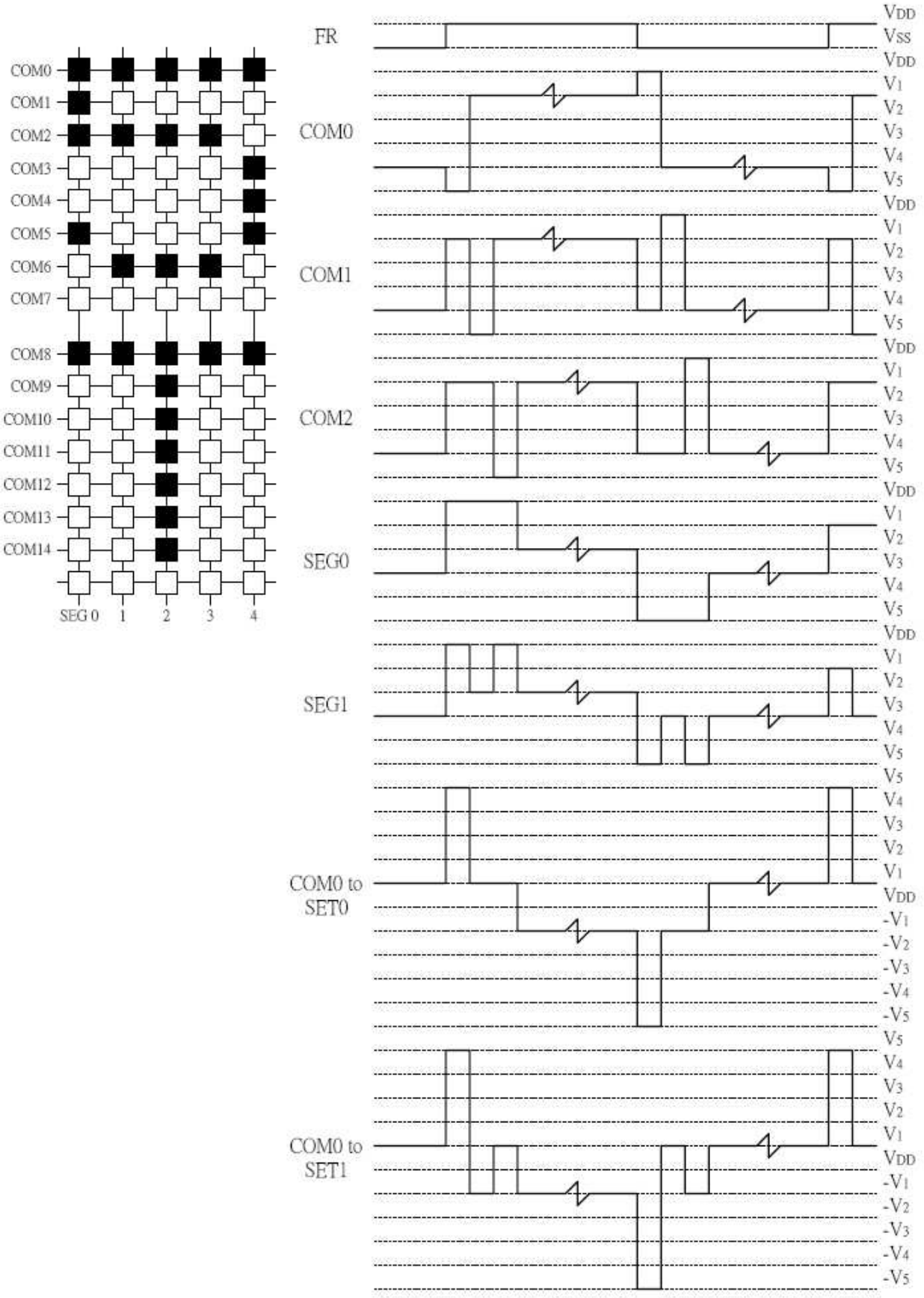

COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
SEG 0
1
2
3
4
FR
COM0
COM1
COM2
SEG0
SEG1
COM0 to SET0
COM0 to SET1
VDD
VSS
V1
V2
V3
V4
V5
-V1
-V2
-V3
-V4
-V5

Figure 6

The Power Supply Circuits

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the LCD drivers. They are Booster circuits, voltage regulator circuits, and voltage follower circuits. They are only enabled in master operation.

The power supply circuits can turn the Booster circuits, the voltage regulator circuits, and the voltage follower circuits ON or OFF independently through the use of the Power Control Set command. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel. Table 7 shows the Power Control Set Command 3-bit data control function, and Table 8 shows reference combinations.

Table 7

bit	function	Status "1"	Status "0"
D2	Booster circuit control bit	ON	OFF
D1	Voltage regulator circuit control bit (V/R circuit)	ON	OFF
D0	Voltage follower circuit control bit (V/F circuit)	ON	OFF

The Control Details of Each Bit of the Power Control Set Command

Table 8

Use Settings	D2	D1	D0	Voltage booster	Voltage regulator	Voltage follower	External voltage input	Step-up voltage
Only the internal power supply is used	1	1	1	ON	ON	ON	V_{SS2}	Used
Only the voltage regulator circuit and the voltage follower circuit are used	0	1	1	OFF	ON	ON	V_{OUT}, V_{SS2}	Open
Only the V/F circuit is used	0	0	1	OFF	OFF	ON	V5, V_{SS2}	Open
Only the external power supply is used	0	0	0	OFF	OFF	OFF	V_1 to V_5	Open

Reference Combinations

* The "step-up system terminals" refer CAP1+, CAP1–, CAP2+, CAP2–, and CAP3–.

* While other combinations, not shown above, are also possible, these combinations are not recommended because they have no practical use.

The Step-up Voltage Circuits

Using the step-up voltage circuits equipped within the ST7565S chips it is possible to product a 2X,3X,4X,5X or 6X step-up of the VDD – VSS2 voltage levels.

6X step-up: Connect capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2–, between CAP1+ and CAP3–, between CAP2+ and CAP4–,between CAP1+ and CAP5–, and between VSS2 and VOUT, to produce a voltage level in the negative direction at the VOUT terminal that is 6 times the voltage level between VDD and VSS2.

5X step-up: Connect capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2–, between CAP1+ and CAP3–, between CAP2+ and CAP4–, and between VSS2 and VOUT, to produce a voltage level in the negative direction at the VOUT terminal that is 5 times the voltage level between VDD and VSS2.

4X step-up: Connect capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2–, between CAP1+ and CAP3–, and between VSS2 and VOUT, to produce a voltage level in the negative direction at the VOUT terminal that is 4 times the voltage level between VDD and VSS2.

3X step-up: Connect capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2– and between VSS2 and VOUT, and short between CAP3– and VOUT to produce voltages level in the negative direction at the VOUT terminal that is 3 times the voltage difference between VDD and VSS2.

2X step-up: Connect capacitor C1 between CAP1+ and CAP1–, and between VSS2 and VOUT, leave CAP2+ open, and short between CAP2–, CAP3– and VOUT to produce a voltage in the negative direction at the VOUT terminal that Is twice the voltage between VDD and VSS2.

The step-up voltage relationships are shown in Figure 7.

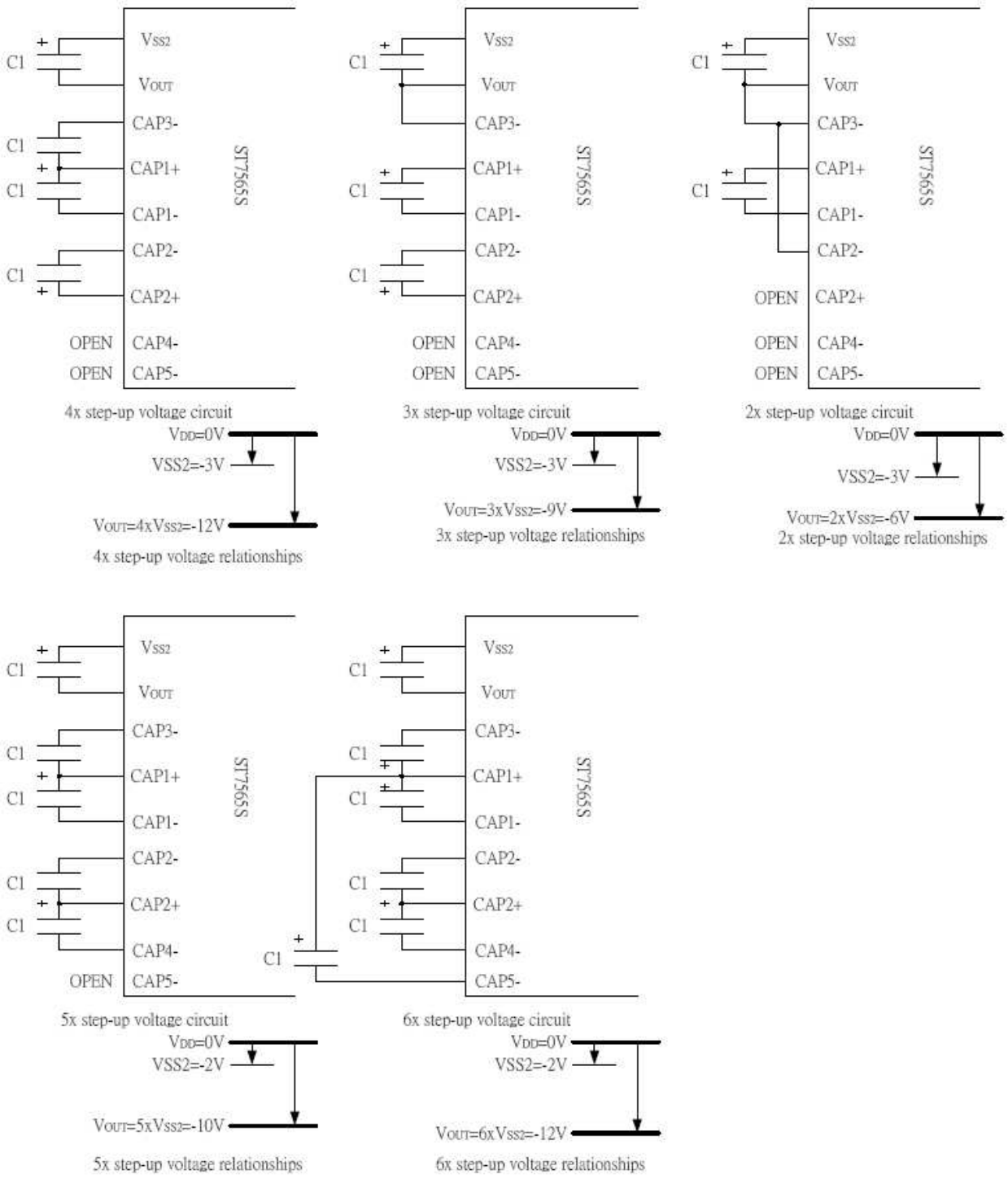


Figure 7

* The VSS2 voltage range must be set so that the VOUT terminal voltage does not exceed the absolute maximum rated value.

The Voltage Regulator Circuit

The step-up voltage generated at VOUT outputs the LCD driver voltage V5 through the voltage regulator circuit. Because the ST7565S chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V5 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components.
(VREG thermal gradients approximate -0.05%/°C)

(A) When the V5 Voltage Regulator Internal Resistors Are Used

Through the use of the V5 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V5 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V5 voltage can be calculated using equation A-1 over the range where | V5 | < | VOUT |.

$$V_5 = \left(1 + \frac{Rb}{Ra}\right) \bullet V_{EV}$$

$$= \left(1 + \frac{Rb}{Ra}\right) \bullet \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}\right]$$

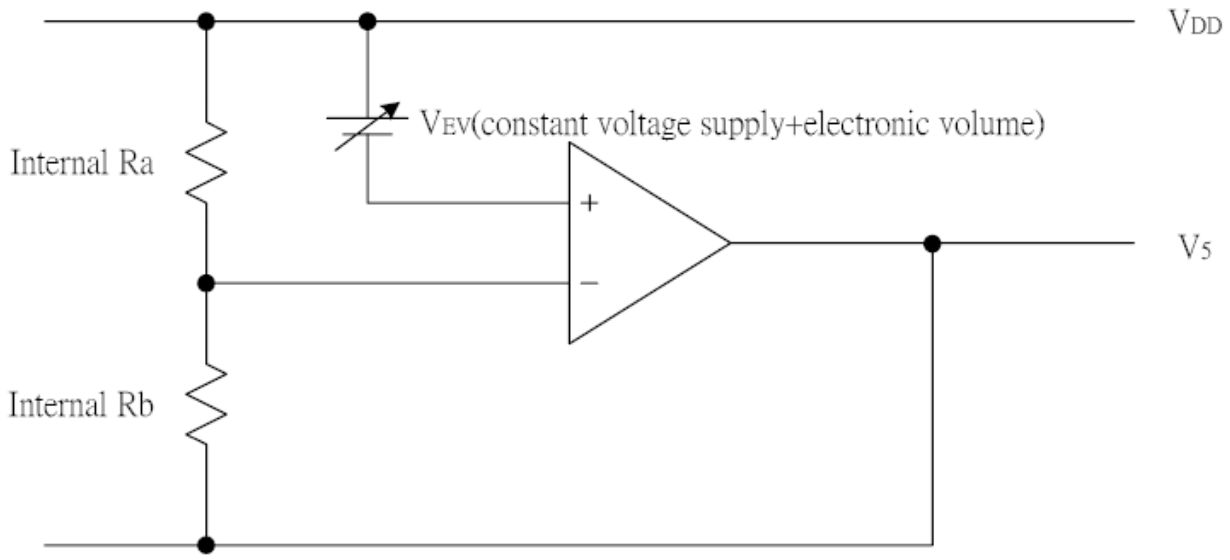


Figure 8

VREG is the IC-internal fixed voltage supply, and its voltage at Ta = 25°C is as shown in Table 9.

Table 9

Part no.	Equipment Type	Thermal Gradient	VREG
ST7565S	Internal Power Supply	–0.05 %/°C	–2.1V

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume registers. Table 10 shows the value for α depending on the electronic volume

register settings. Rb/Ra is the V5 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V5 voltage regulator internal resistor ratio set command. The (1 + Rb/Ra) ratio assumes the values shown in Table 11 depending on the 3-bit data settings in the V5 voltage regulator internal resistor ratio register.

Table 10

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
			⋮			⋮
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

V5 voltage regulator internal resistance ratio register value and (1 + Rb/Ra) ratio (Reference value)

Table 11

Register			ST7565S
D2	D1	D0	(1) –0.05 %/°C
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0
1	0	1	5.5
1	1	0	6.0
1	1	1	6.5

Figures 9, 10 show V5 voltage measured by values of the internal resistance ratio resistor for V5 voltage adjustment and electric volume resister for each temperature grade model.

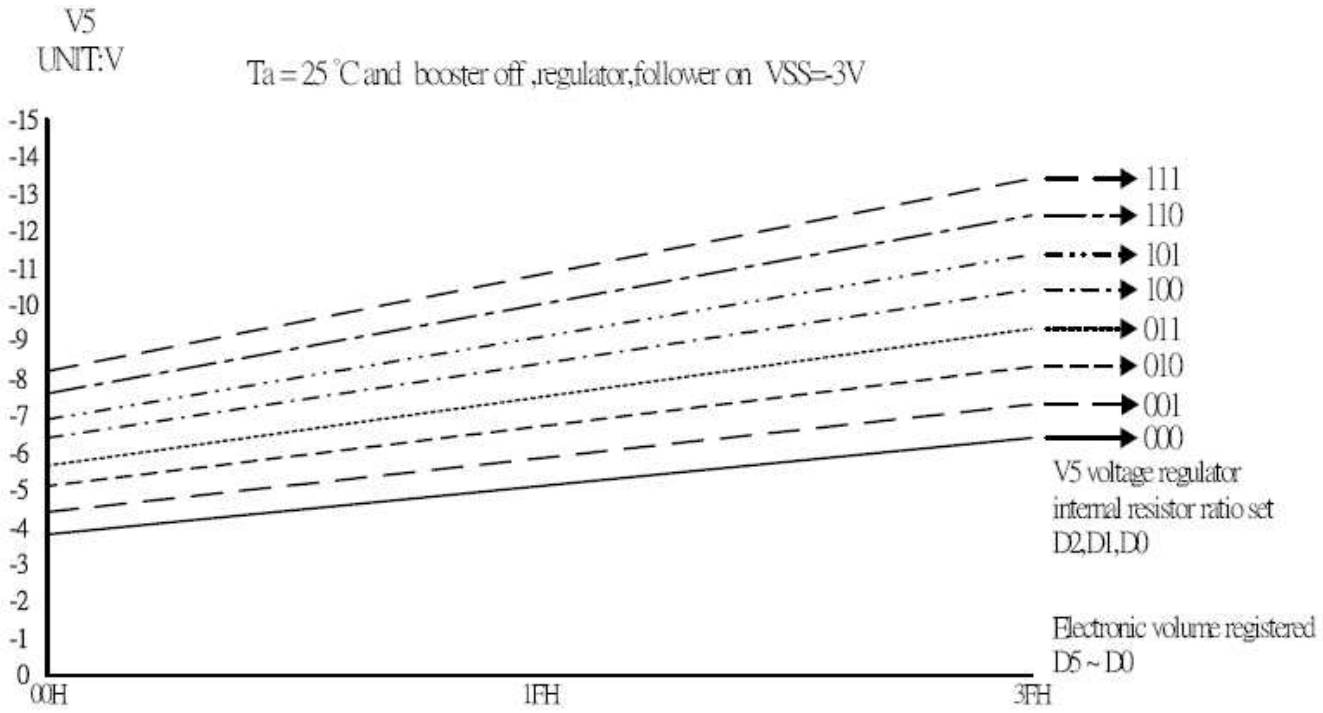


Figure 9 : (1) For ST7565S the Thermal Gradient = -0.05%/°C

The V5 voltage as a function of the V5 voltage regulator internal resistor ratio register and the electronic volume register.

Setup example: When selecting Ta = 25°C and V5 = –7V for an ST7565S on which Temperature gradient = –0.05%/°C.

Using Figure 9 and the equation A-1, the following setup is enabled.

At this time, the variable range and the notch width of the V5 voltage is, as shown Table 13, as dependent on the electronic volume.

Table 12

Contents	Register					
	D5	D4	D3	D2	D1	D0
For V5 voltage regulator	—	—	—	0	1	0
Electronic Volume	1	0	0	1	0	1

Table 13

V5	Min	Typ	Max	Units
Variable Range	–8.4 (63 levels)	–7.0 (central value)	–5.1 (0 level)	[V]
Notch width		51		[mV]

(B) When an External Resistance is Used (The V5 Voltage Regulator Internal Resistors Are Not Used) (1)

The liquid crystal power supply voltage V5 can also be set without using the V5 voltage regulator internal resistors (IRS terminal = "L") by adding resistors Ra' and Rb' between VDD and VR, and between VR and V5, respectively. When this is done, the use of the electronic volume function makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal power supply voltage

V5 through commands.

In the range where | V5 | < | VOUT |, the V5 voltage can be calculated using equation B-1 based on the external resistances Ra' and Rb'.

$$V_5 = \left(1 + \frac{Rb'}{Ra'}\right) \bullet V_{EV}$$

$$= \left(1 + \frac{Rb'}{Ra'}\right) \bullet \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}\right]$$

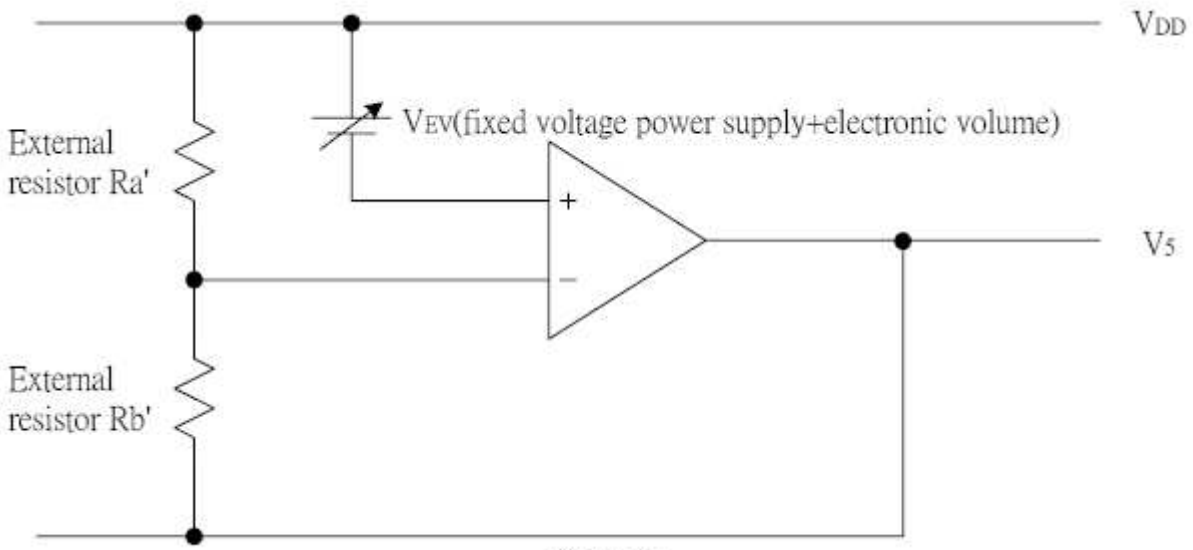


Figure 11

Setup example: When selecting Ta = 25°C and V5 = –7 V for ST7565S the temperature gradient = –0.05%/°C.

When the central value of the electron volume register is (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0), then α = 31 and VREG = –2.1V so, according to equation B-1,

$$V_5 = \left(1 + \frac{Rb'}{Ra'}\right) \bullet \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}$$

$$-7V = \left(1 + \frac{Rb'}{Ra'}\right) \bullet \left(1 - \frac{31}{162}\right) \bullet (-2.1)$$

Moreover, when the value of the current running through Ra' and Rb' is set to 5 uA,

$$Ra' + Rb' = 1.4M\Omega \qquad \text{(Equation B-3)}$$

Consequently, by equations B-2 and B-3, At this time, the V5 voltage variable range and notch width, based on the electron volume function, is as given in Table 14.

Table 14

V5	Min	Typ	Max	Units
Variable Range	–8.6 (63 levels)	–7.0 (central value)	–5.3 (0 level)	[V]
Notch width		52		[mV]

(C) When External Resistors are Used (The V5 Voltage Regulator Internal Resistors Are Not Used)

(2) When the external resistor described above are used, adding a variable resistor as well makes it possible to perform fine adjustments on Ra' and Rb', to set the liquid crystal drive voltage V5. In this case, the use of the electronic volume function makes it possible to control the liquid crystal power supply voltage V5 by commands to adjust the liquid crystal display brightness.

In the range where | V5 | < | VOUT | the V5 voltage can be calculated by equation C-1 below based on the R1 and R2 (variable resistor) and R3 settings, where R2 can be subjected to fine adjustments (Δ R2).

$$V_5 = \left(1 + \frac{R3+R2-\Delta R2}{R1+\Delta R2}\right) \bullet V_{EV}$$

$$= \left(1 + \frac{R3+R2-\Delta R2}{R1+\Delta R2}\right) \bullet \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}\right]$$

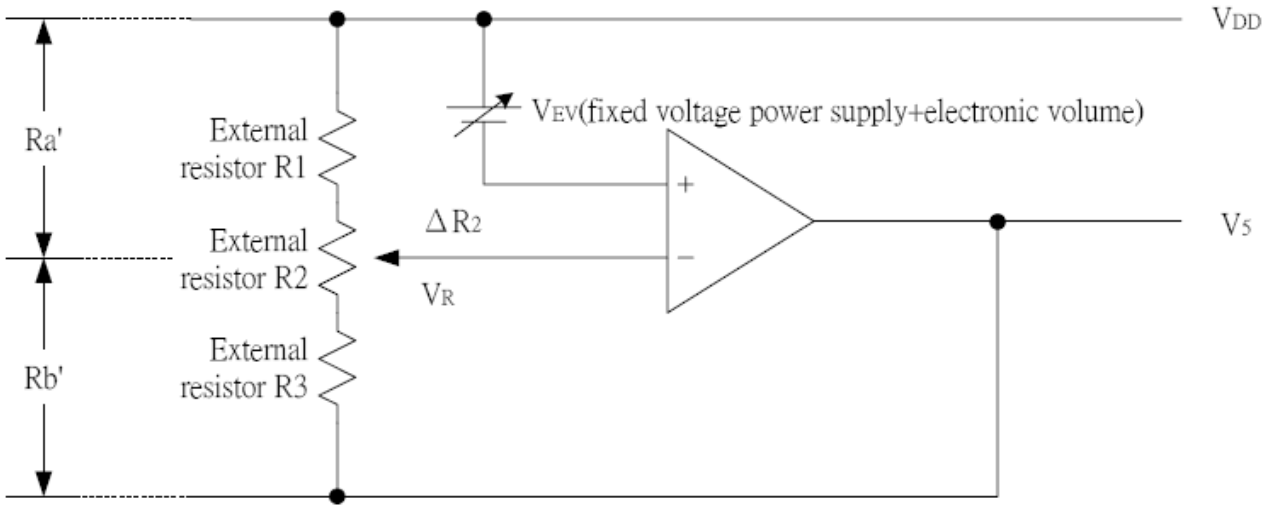


Figure 12

Setup example: When selecting Ta = 25°C and V5 = –5 to –9V (using R2) for an ST7565S the temperature gradient = –0.05%/°C.

When the central value for the electronic volume register is set at (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0), then α = 31 and VREG = –2.1 V so, according to equation C-1, when Δ R2 = 0 Ω, in order to make V5 = –9 V,

$$-9V = \left(1 + \frac{R3+R2}{R1}\right) \bullet \left(1 - \frac{31}{162}\right) \bullet (-2.1)$$

When ΔR2 = R2, in order to make V = –5 V,

$$-5V = \left(1 + \frac{R3}{R1+R2}\right) \bullet \left(1 - \frac{31}{162}\right) \bullet (-2.1)$$

When the current flowing VDD and V5 is set to 5 uA,

$$R_1 + R_2 + R_3 = 1.4M\Omega \qquad \text{(Equation C-4)}$$

With this, according to equation C-2, C-3 and C-4, R1 = 264kΩ, R2 = 211kΩ, R3 = 925kΩ

The V5 voltage variable range and notch width based on the electron volume function is as shown in

Table 15.

Table 15

V_5	Min	Typ	Max	Units
Variable Range	–8.7 (63 levels)	–7.0 (central value)	–5.3 (0 level)	[V]
Notch width		53		[mV]

* When the V5 voltage regulator internal resistors or the electronic volume function is used, it is necessary to at least set the voltage regulator circuit and the voltage follower circuit to an operating mode using the power control set commands.
Moreover, it is necessary to provide a voltage from VOUT when the Booster circuit is OFF.
* The VR terminal is enabled only when the V5 voltage regulator internal resistors are not used (i.e. the IRS terminal = "L").
When the V5 voltage regulator internal resistors are used (i.e. when the IRS terminal = "H"), then the VR terminal is left open.
* Because the input impedance of the VR terminal is high, it is necessary to take into consideration short leads, shield cables, etc. to handle noise.

The LCD Voltage Generator Circuit

The V5 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V1, V2, V3, and V4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V1, V2, V3 and V4 to the liquid crystal drive circuit.

High Power Mode

The power supply circuit equipped in the ST7565S chips has very low power consumption (normal mode: HPM = "H").
However, for LCDs or panels with large loads, this low-power power supply may cause display quality to degrade. When this occurs, setting the HPM terminal to "L" (high power mode) can improve the quality of the display. We recommend that the display be checked on actual equipment to determine whether or not to use this mode. Moreover, if the improvement to the display is inadequate even after high power mode has been set, then it is necessary to add a liquid crystal drive power supply externally.

The Internal Power Supply Shutdown Command Sequence

The sequence shown in Figure 13 is recommended for shutting down the internal power supply, first placing the power supply in power saver mode and then turning the power supply OFF.

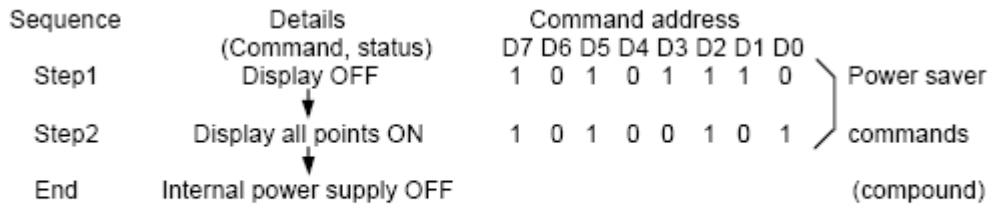


Figure 13

The temperature grade of the Internal Power Supply for ST7565S (-0.05%/°C) :

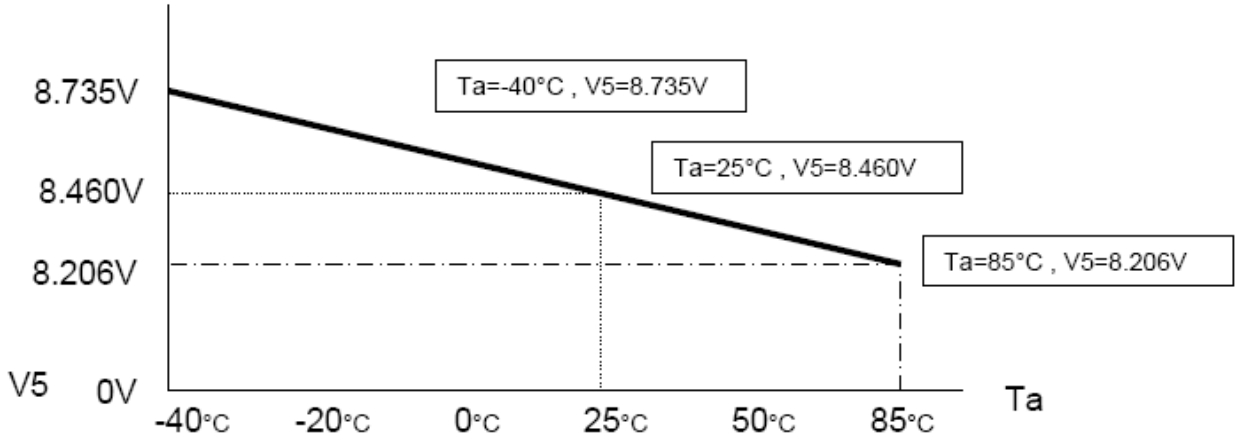


Figure 14

Reference Circuit Examples

Figure 15 shows reference circuit examples.

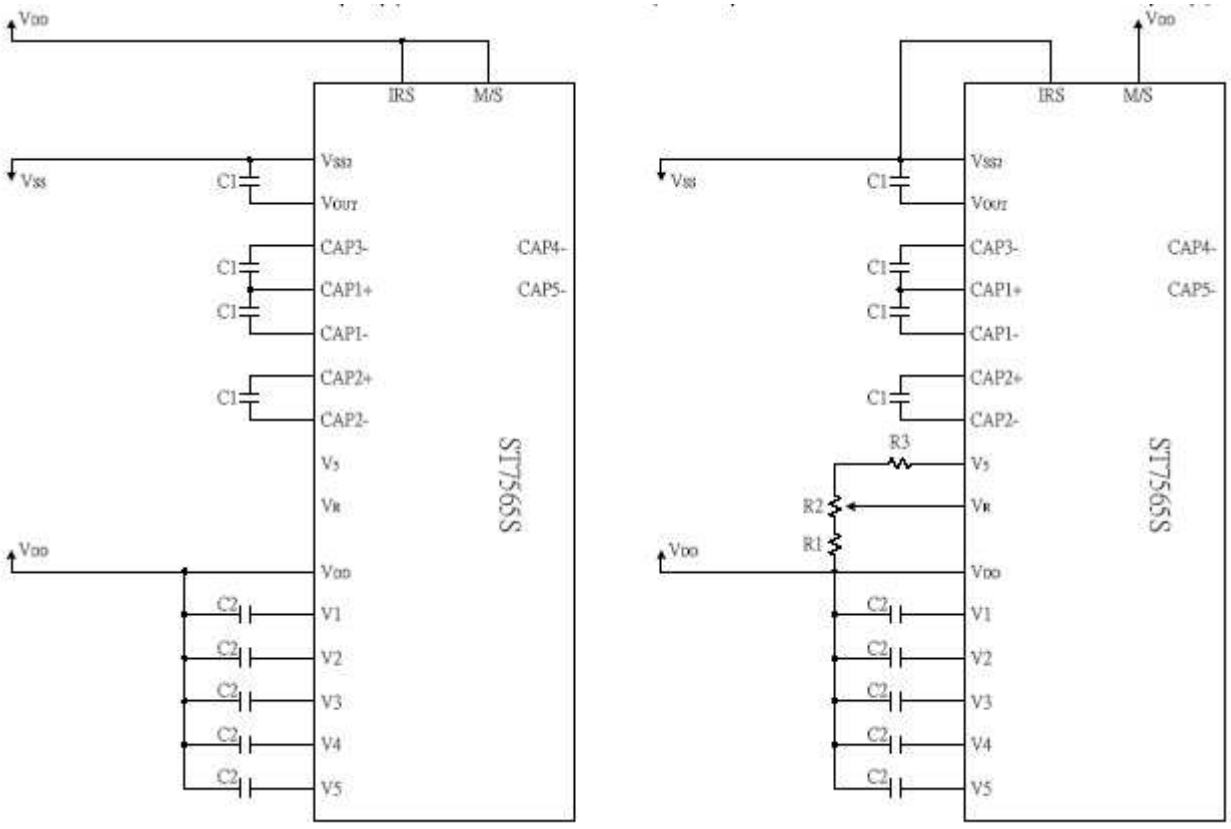
1. When used all of the step-up circuit, voltage regulating circuit and V/F circuit

(1) When the voltage regulator internal resistor is used.

(Example where VSS2 = VSS, with 4x step-up)

(2) When the voltage regulator internal resistor is not used.

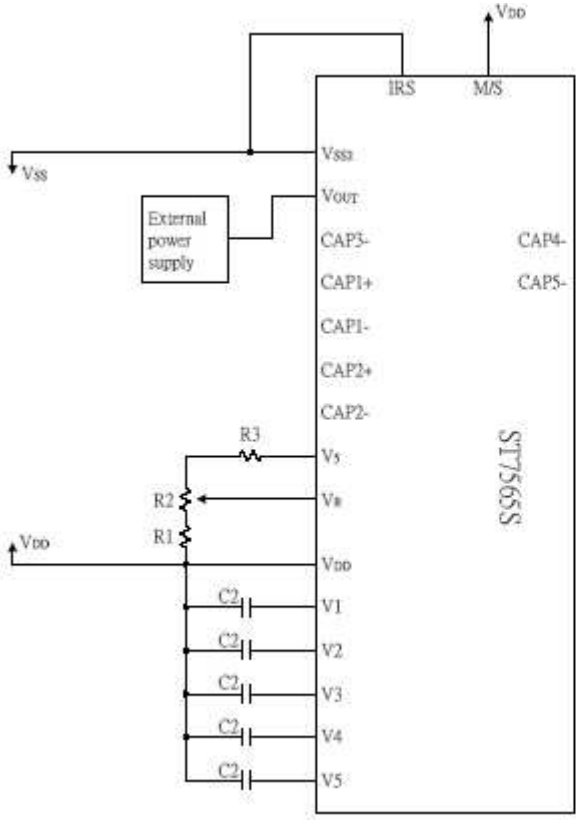
(Example where VSS2 = VSS, with 4x step-up)

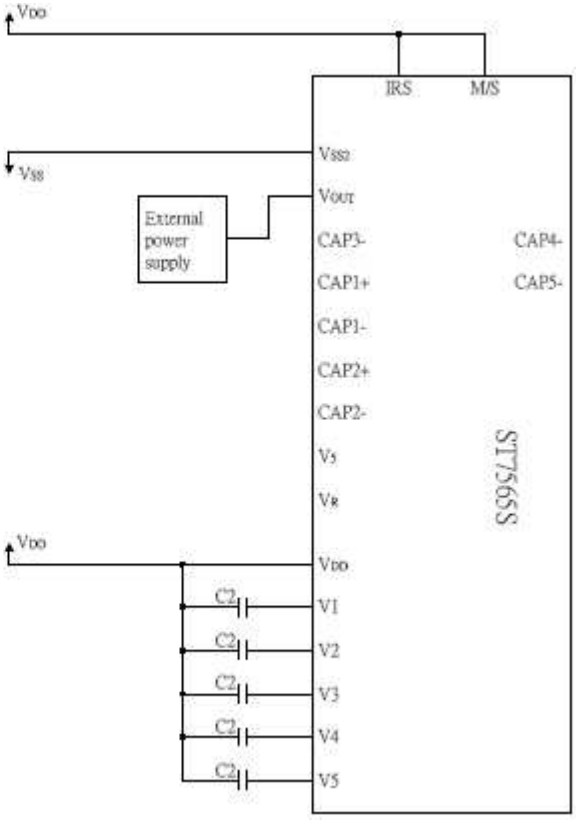


2. When the voltage regulator circuit and V/F circuit alone are used

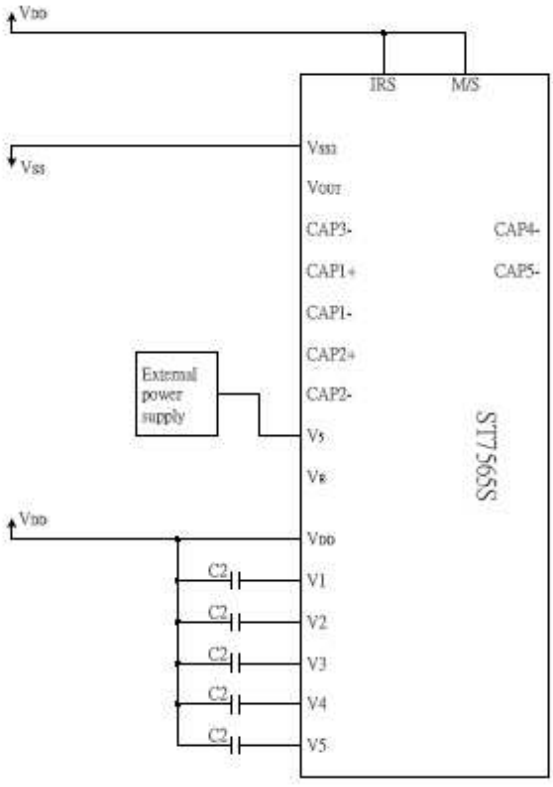
(1) When the V5 voltage regulator internal resistor is not used.

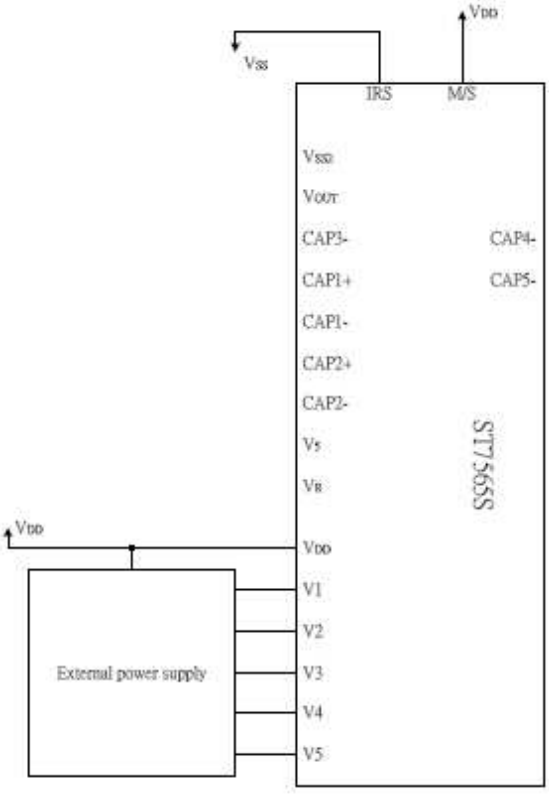
(2) When the V5 voltage regulator internal resistor is used.





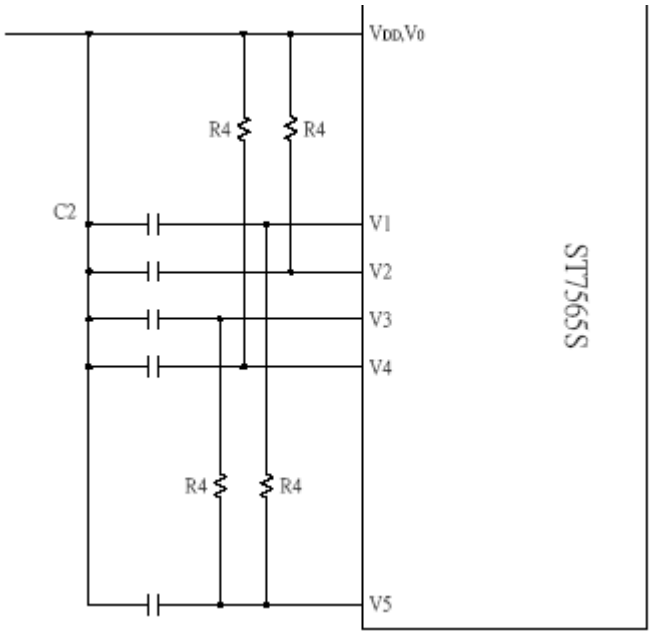
3. When the V/F circuit alone is used 4. When the built-in power is not used





5. When the built-in power circuit is used to drive a liquid crystal panel heavily loaded with AC or DC, it is recommended to connect an external resistor to stabilize potentials of V1, V2, V3 and V4 which are output from the built-in voltage follower.

Examples of shared reference settings When V5 can vary between –8 and 12 V



Item	Set value	units
c1	1.0 to 4.7	uF
c2	0.1 to 4.7	uF

C1 and C2 are determined by the size of the LCD being driven

Reference set value R4: 100KΩ ~ 1MΩ It is recommended to set an optimum resistance value R4 taking the liquid crystal display and the drive waveform.

Figure 15

* 1. Because the VR terminal input impedance is high, use short leads and shielded lines.

* 2. C1 and C2 are determined by the size of the LCD being driven. Select a value that will stabilize the liquid crystal drive voltage.

Example of the Process by which to Determine the Settings:

• Turn the voltage regulator circuit and voltage follower circuit ON and supply a voltage to VOUT from the outside.

• Determine C2 by displaying an LCD pattern with a heavy load (such as horizontal stripes) and selecting a C2 that stabilizes the liquid crystal drive voltages (V1 to V5). Note that all C2 capacitors must have the same capacitance value.

• Next turn all the power supplies ON and determine C1.

The Reset Circuit

When the /RES input comes to the “L” level, these LS Is return to the default state. Their default states are as follows:

1. Display OFF
2. Normal display
3. ADC select: Normal (ADC command D0 = “L”)
4. Power control register: (D2, D1, D0) = (0, 0, 0)
5. Serial interface internal register data clear
6. LCD power supply bias rate:

1/65 DUTY = 1/9 bias
1/49,1/55,1/53 DUTY = 1/8 bias
1/33 DUTY = 1/6 bias
7. All-indicator lamps-on OFF (All-indicator lamps ON/OFF command D0 = “L”)
8. Power saving clear
9. V5 voltage regulator internal resistors Ra and Rb separation
10. Output conditions of SEG and COM terminals SEG=VDD , COM=VDD
11. Read modify write OFF
12. Static indicator OFF Static indicator register : (D1, D2) = (0, 0)
13. Display start line set to first line
14. Column address set to Address 0
15. Page address set to Page 0
16. Common output status normal
17. V5 voltage regulator internal resistor ratio set mode clear
18. Electronic volume register set mode clear Electronic volume register :
(D5, D4, D3, D2, D1, D0) = (1, 0. 0, 0, 0,0)
19. Test mode clear
On the other hand, when the reset command is used, the above default settings from 11 to 19 are only executed.
When the power is turned on, the IC internal state becomes unstable, and it is necessary to initialize it using the /RES terminal. After the initialization, each input terminal should be controlled normally. Moreover, when the control signal from the MPU is in the high impedance, an over current may flow to the IC. After applying a current, it is necessary to take proper measures to prevent the input terminal from getting into the high impedance state.
If the internal liquid crystal power supply circuit is not used on ST7565S,it is necessary that /RES is “H” when the external liquid crystal power supply is turned on. This IC has the function to discharge V5 when /RES is “L,” and the external power supply short-circuits to VDD when /RES is “L.”
While /RES is “L,” the oscillator and the display timing generator stop, and the CL, FR, FRS and /DOF terminals are fixed to “H.” The terminals D0 to D7 are not affected. The VDD level is output from the SEG and COM output terminals.
This means that an internal resistor is connected between VDD and V5.
When the internal liquid crystal power supply circuit is not used on other models of ST7565S series, it is necessary that /RES is “L” when the external liquid crystal power supply is turned on.
While /RES is “L,” the oscillator works but the display timing generator stops, and the CL, FR, FRS and /DOF terminals are fixed to “H.” The terminals D0 to D7 are not affected.

COMMANDS

The ST7565S identify the data bus signals by a combination of A0, /RD (E), /WR(R/W) signals. Command interpretation and execution does not depend on the external clock, but rather is performed through internal timing only, and thus the processing is fast enough that normally a busy check is not required.

In the 8080 MPU interface, commands are launched by inputting a low pulse to the RD terminal for reading, and inputting a low pulse to the /WR terminal for writing. In the 6800 Series MPU interface, the interface is placed in a read mode when an "H" signal is input to the R/W terminal and placed in a write mode when a "L" signal is input to the R/W terminal and then the command is launched by inputting a high pulse to the E terminal. Consequently, the 6800 Series MPU interface is different than the 80x86 Series MPU interface in that in the explanation of commands and the display commands the status read and display data read /RD (E) becomes "1(H)". In the explanations below the commands are explained using the 8080 Series MPU interface as the example.

When the serial interface is selected, the data is input in sequence starting with D7.

<Explanation of Commands>

Display ON/OFF

This command turns the display ON and OFF.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

When the display OFF command is executed when in the display all points ON mode, power saver mode is entered. See the section on the power saver for details.

Display Start Line Set

This command is used to specify the display start line address of the display data RAM shown in Figure 4. For further details see the explanation of this function in "The Line Address Circuit".

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	0	0	1	0	2
							↓				↓
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

Page Address Set

This command specifies the page address corresponding to the low address when the MPU accesses the display data RAM (see Figure 4). Specifying the page address and column address enables to access a desired bit of the display data RAM.

Changing the page address does not accompany a change in the status display.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
							↓				↓
							0	1	1	1	7
							1	0	0	0	8

Column Address Set

This command specifies the column address of the display data RAM shown in Figure 4. The column address is split into two sections (the higher 4 bits and the lower 4 bits) when it is set (fundamentally, set continuously). Each time the display data RAM is accessed, the column address automatically increments (+1), making it possible for the MPU to continuously read from/write to the display data. The column address increment is topped at 83H. This does not change the page address continuously. See the function explanation in "The Column Address Circuit," for details.

	A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0	Column address
High bits →	0	1	0	0	0	0	1	A7	A6	A5	A4	0	0	0	0	0	0	0	0	0
Low bits →							0	A3	A2	A1	A0	0	0	0	0	0	0	0	1	1
												0	0	0	0	0	0	1	0	2
																↓				↓
												1	0	0	0	0	0	1	0	130
												1	0	0	0	0	0	1	1	131

Status Read

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	BUSY = 1: it indicates that either processing is occurring internally or a reset condition is in process. BUSY = 0: A new command can be accepted . if the cycle time can be satisfied, there is no need to check for BUSY conditions.
ADC	This shows the relationship between the column address and the segment driver. 0: Normal (column address n ↔ SEG n) 1: Reverse (column address 131-n ↔ SEG n) (The ADC command switches the polarity.)
ON/OFF	ON/OFF: indicates the display ON/OFF state. 0: Display ON 1: Display OFF (This display ON/OFF command switches the polarity.)
RESET	This indicates that the chip is in the process of initialization either because of a /RES signal or because of a reset command. 0: Operating state 1: Reset in progress

Display Data Write

This command writes 8-bit data to the specified display data RAM address. Since the column address is automatically incremented by "1" after the write, the MPU can write the display data.

A0	E /RD	R/W /WR	D7 D6 D5 D4 D3 D2 D1 D0
1	1	0	Write data

Display Data Read

This command reads 8-bit data from the specified display data RAM address. Since the column address is automatically incremented by "1" after the read, the CPU can continuously read multiple-word data. One dummy read is required immediately after the column address has been set. See the function explanation in "Display Data RAM" for the explanation of accessing the internal registers. When the serial interface is used, reading of the display data becomes unavailable.

A0	E /RD	R/W /WR	D7 D6 D5 D4 D3 D2 D1 D0
1	0	1	Read data

ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence between the display RAM data column address and the segment driver output.

Thus, sequence of the segment driver output pins may be reversed by the command. See the column address circuit (page 1–20) for the detail. Increment of the column address (by "1") accompanying the reading or writing the display data is done according to the column address indicated in Figure 4.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

Display Normal/Reverse

This command can reverse the lit and unlit display without overwriting the contents of the display data RAM. When this is done the display data RAM contents are maintained.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM Data "H" LCD ON voltage (normal)
										1	RAM Data "L" LCD ON voltage (reverse)

Display All Points ON/OFF

This command makes it possible to force all display points ON regardless of the content of the display data RAM. The contents of the display data RAM are maintained when this is done. This command takes priority over the display normal/reverse command.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display mode
										1	Display all points ON

When the display is in an OFF mode, executing the display all points ON command will place the display in power save mode. For details, see the Power Save section.

LCD Bias Set

This command selects the voltage bias ratio required for the liquid crystal display.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Select Status				
											1/65duty	1/49duty	1/33duty	1/55duty	1/53duty
0	1	0	1	0	1	0	0	0	1	0	1/9 bias	1/8 bias	1/6 bias	1/8 bias	1/8 bias
										1	1/7 bias	1/6 bias	1/5 bias	1/6 bias	1/6 bias

Read/Modify/Write

This command is used paired with the “END” command. Once this command has been input, the display data read command does not change the column address, but only the display data write command increments (+1) the column address. This mode is maintained until the END command is input. When the END command is input, the column address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

* Even in read/modify/write mode, other commands aside from display data read/write commands can also be used.

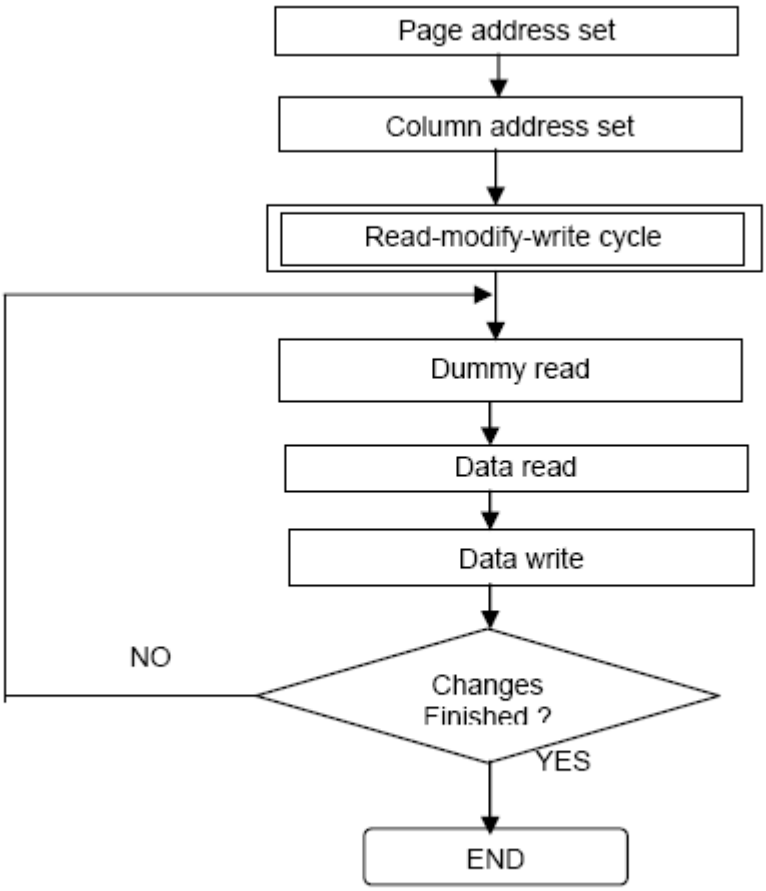


Figure 24 Command Sequence For read modify write

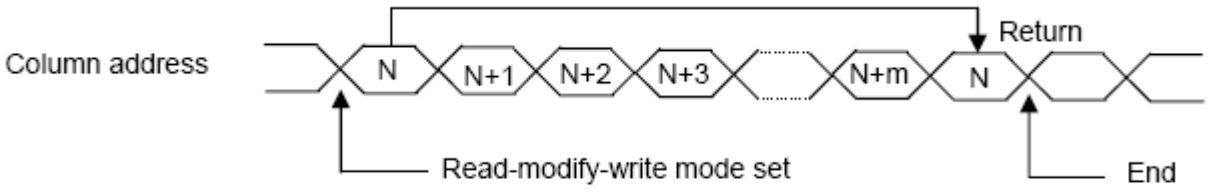


Figure 25

End

This command releases the read/modify/write mode, and returns the column address to the address it was at when the mode was entered.

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

Reset

This command initializes the display start line, the column address, the page address, the common output mode, the V5 voltage regulator internal resistor ratio, the electronic volume, and the static indicator are reset, and the read/modify/write mode and test mode are released. There is no impact on the display data RAM. See the function explanation in “Reset” for details.

The reset operation is performed after the reset command is entered.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The initialization when the power supply is applied must be done through applying a reset signal to the /RES terminal. The reset command must not be used instead.

Common Output Mode Select

This command can select the scan direction of the COM output terminal. For details, see the function explanation in “Common Output Mode Select Circuit.”

E R/W A0 /RD /WR	D7 D6 D5 D4 D3 D2 D1 D0	Selected Mode					
			1/65duty	1/49duty	1/33duty	1/55duty	1/53duty
0 1 0	1 1 0 0 0 * * *	Normal	COM0→COM63	COM0→COM47	COM0→COM31	COM0→COM53	COM0→COM51
	1	Reverse	COM63→COM0	COM47→COM0	COM31→COM0	COM53→COM0	COM51→COM0

* Disabled bit

Power Controller Set

This command sets the power supply circuit functions. See the function explanation in “The Power Supply Circuit,” for details

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	0	0	1	0	1	0			Booster circuit: OFF
								1			Booster circuit: ON
									0		Voltage regulator circuit: OFF
									1		Voltage regulator circuit: ON
										0	Voltage follower circuit: OFF
										1	Voltage follower circuit: ON

V5 Voltage Regulator Internal Resistor Ratio Set

This command sets the V5 voltage regulator internal resistor ratio. For details, see the function explanation is “The Voltage Regulator circuit " and table 11 .

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									↓		↓
								1	1	1	
								1	1	1	Large

The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the LCD drive voltage V5 through the output from the voltage regulator circuits of the internal liquid crystal power supply. This command is a two byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

The Electronic Volume Mode Set

When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal drive voltage V5 assumes one of the 64 voltage levels.

When this command is input, the electronic volume mode is released after the electronic volume register has been set.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	| V_5 |
0	1	0	*	*	0	0	0	0	0	1	Small
			*	*	0	0	0	0	1	0	
			*	*	0	0	0	0	1	1	
							↓				↓
			*	*	1	1	1	1	1	0	
			*	*	1	1	1	1	1	1	Large

* Inactive bit (set “0”)

When the electronic volume function is not used, set this to (1, 0, 0, 0, 0, 0)

The Electronic Volume Register Set Sequence

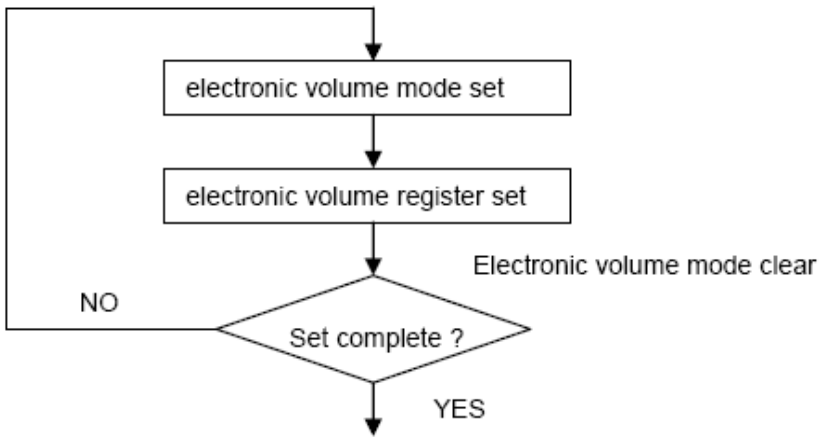


Figure 26

Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands.

This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes.

The static indicator ON command is a double byte command paired with the static indicator register set command, and thus one must execute one after the other. (The static indicator OFF command is a single byte command.)

Static Indicator ON/OFF

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used.

This mode is cleared when data is set in the register by the static indicator register set command.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Static Indicator
0	1	0	1	0	1	0	1	1	0	0	OFF
										1	ON

Static Indicator Register Set

This command sets two bits of data into the static indicator register, and is used to set the static indicator into a blinking mode.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Indicator Display State
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON (blinking at approximately one second intervals)
									1	0	ON (blinking at approximately 0.5 second intervals)
									1	1	ON (constantly on)

* Disabled bit (set “0”)

Static Indicator Register Set Sequence

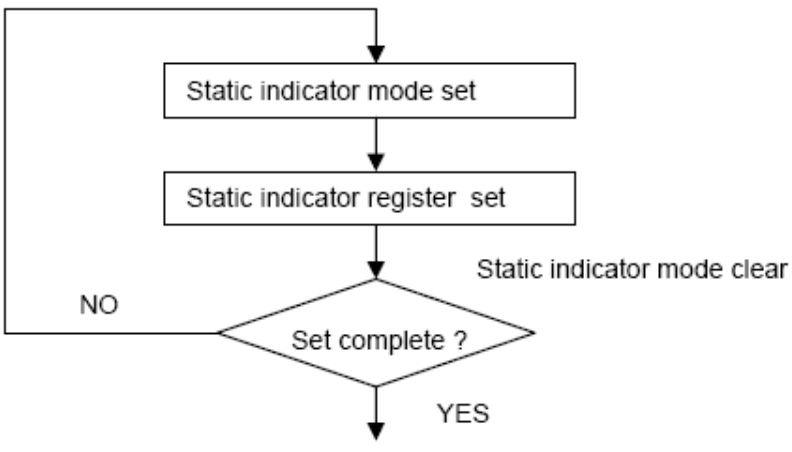


Figure 27

Power Save (Compound Command)

When the display all points ON is performed while the display is in the OFF mode, the power saver mode is entered, thus greatly reducing power consumption.

The power saver mode has two different modes: the sleep mode and the standby mode. When the static indicator is OFF, it is the sleep mode that is entered. When the static indicator is ON, it is the standby mode that is entered.

In the sleep mode and in the standby mode, the display data is saved as is the operating mode that was in effect before the power saver mode was initiated, and the MPU is still able to access the display data RAM.

Refer to figure 28 for power save off sequence.

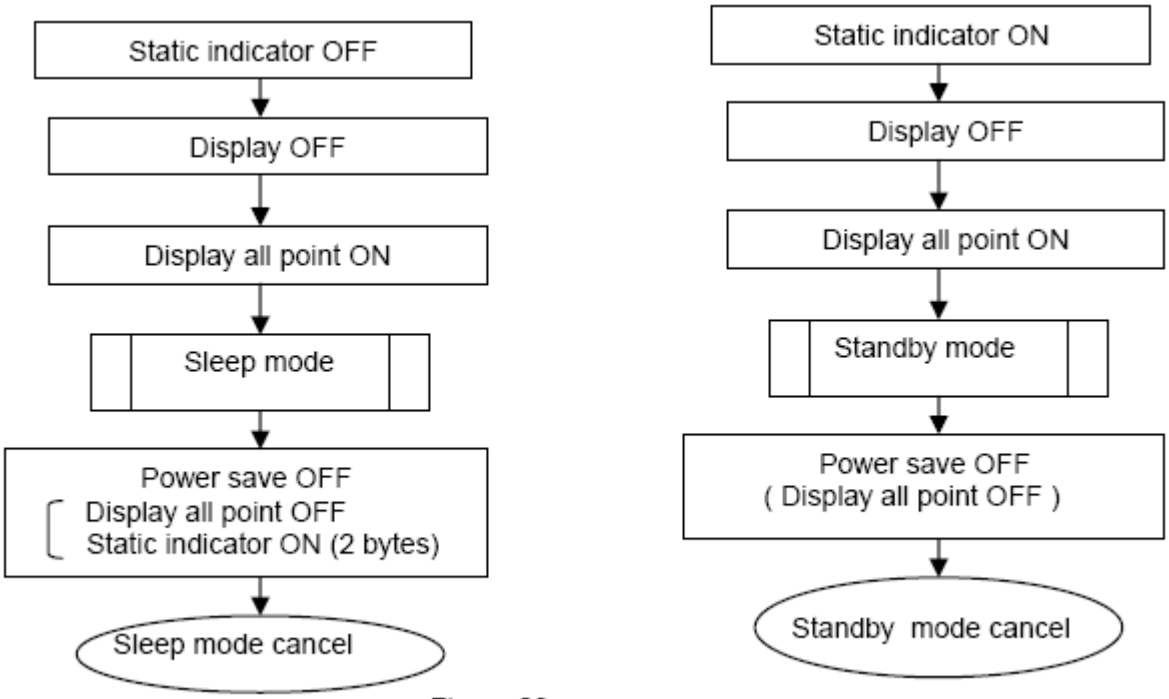


Figure 28

Sleep Mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:

1. The oscillator circuit and the LCD power supply circuit are halted.
2. All liquid crystal drive circuits are halted, and the segment in common drive outputs output a VDD level.

Standby Mode

The duty LCD display system operations are halted and only the static drive system for the indicator continues to operate, providing the minimum required consumption current for the static drive. The internal modes are in the following states during standby mode.

1 The LCD power supply circuits are halted. The oscillator circuit continues to operate.

2 The duty drive system liquid crystal drive circuits are halted and the segment and common driver outputs output a VDD level.

The static drive system does not operate.
When a reset command is performed while in standby mode, the system enters sleep mode.
* When an external power supply is used, it is recommended that the functions of the external power supply circuit be stopped when the power saver mode is started. For example, when the various levels of liquid crystal drive voltage are provided by external resistive voltage dividers, it is recommended that a circuit be added in order to cut the electrical current flowing through the resistive voltage divider circuit when the power saver mode is in effect. The ST7565S series chips have a liquid crystal display blanking control terminal /DOF. This terminal enters an "L" state when the power saver mode is launched. Using the output of /DOF, it is possible to stop the function of an external power supply circuit.
* When the master is turned on, the oscillator circuit is operable immediately after the powering on.

The Booster Ratio (Double Byte Command)

This command makes it possible to select step-up ratio. It is used when the power control set have turn on the internal booster circuit. This command is a two byte command used as a pair with the booster ratio select mode set command and the booster ratio register set command, and both commands must be issued one after the other.

Booster Ratio Select Mode Set

When this command is input, the Booster ratio register set command becomes enabled. Once the booster ratio select mode has been set, no other command except for the booster ratio register command can be used. Once the booster ratio register set command has been used to set data into the register, then the booster ratio select mode is released.

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	0	0	0

Booster Ratio Register Set

By using this command to set two bits of data to the booster ratio register, it can be select what kind of the booster ratio can be used.
When this command is input, the booster ratio select mode is released after the booster ratio register has been set.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Booster ratio select
0	1	0	*	*	*	*	*	*	0	0	2x,3x,4x
			*	*	*	*	*	*	0	1	5x
			*	*	*	*	*	*	1	1	6x

* Inactive bit (set "0")
When the booster ratio select function is not used, set this to (0, 0) 2x,3x,4x step-up mode

The booster ratio Register Set Sequence

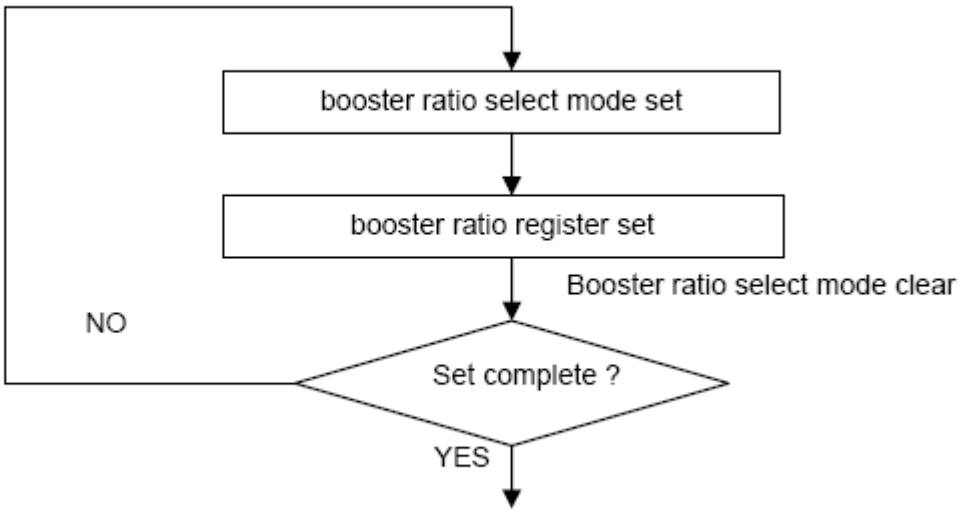


Figure 29

NOP

Non-OPeration Command

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

Test

This is a command for IC chip testing. Please do not use it. If the test command is used by accident, it can be cleared by applying a “L” signal to the /RES input by the reset command or by using an NOP.

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	1	*	*

* Inactive bit

Note: The ST7565S maintain their operating modes until something happens to change them. Consequently, excessive external noise, etc., can change the internal modes of the ST7565S . Thus in the packaging and system design it is necessary to suppress the noise or take measure to prevent the noise from influencing the chip. Moreover, it is recommended that the operating modes be refreshed periodically to prevent the effects of unanticipated noise.

Table 16: Table of ST7565S Commands (Note) *: disabled data

Command	Command Code										Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit Column address set lower bit	0 0	1 1	0 0	0 0	0 0	0 0	1 0	Most significant column address Least significant column address				Sets the most significant 4 bits of the display RAM column address. Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM
(7) Display data read	1	0	1	Read data								Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565S)
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17) Vs voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set Electronic volume register set	0	1	0	1 0	0 0	0 Electronic volume value	0	0	0	0	1	Set the Vs output voltage electronic volume register
(19) Static indicator ON/OFF Static indicator register set	0	1	0	1 0	0 0	1 0	0 0	1 0	1 0	0 0	0 1 Mode	0: OFF, 1: ON Set the flashing mode
(20) Booster ratio set	0	1	0	1 0	1 0	1 0	1 0	1 0	0 0	0 step-up value	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
(21) Power saver												Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation

(23) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

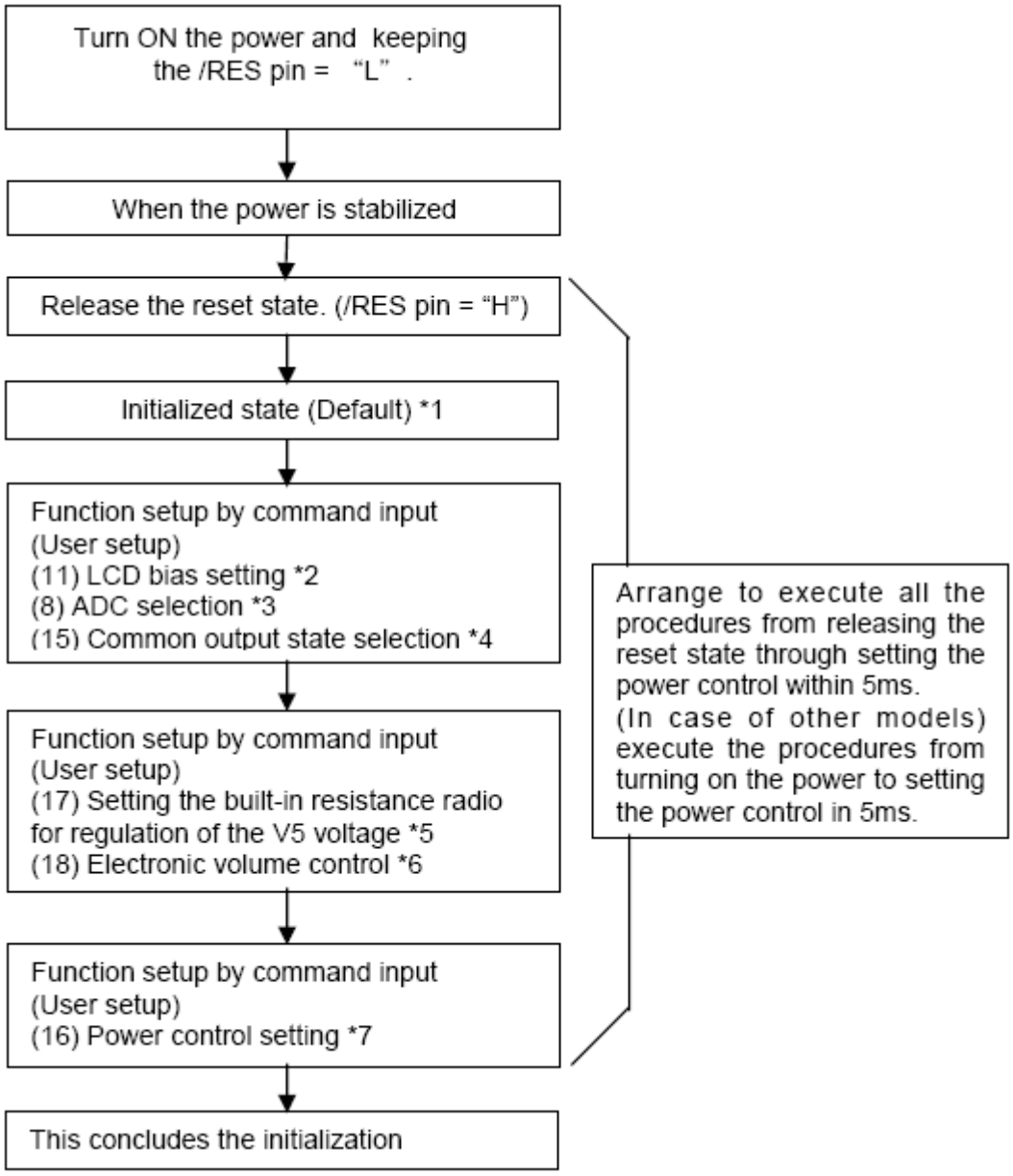
COMMAND DESCRIPTION

Instruction Setup: Reference

(1) Initialization

Note: With this IC, when the power is applied, LCD driving non-selective potentials V2 and V3 (SEG pin) and V1 and V4 (COM pin) are output through the LCD driving output pins SEG and COM. When electric charge is remaining in the smoothing capacitor connecting between the LCD driving voltage output pins (V1 ~ V5) and the VDD pin, the picture on the display may become totally dark instantaneously when the power is turned on. To avoid occurrence of such a failure, we recommend the following flow when turning on the power.

1. When the built-in power is being used immediately after turning on the power:



* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Notes: Refer to respective sections or paragraphs listed below.

*1: Description of functions; Resetting circuit

*2: Command description; LCD bias setting

*3: Command description; ADC selection

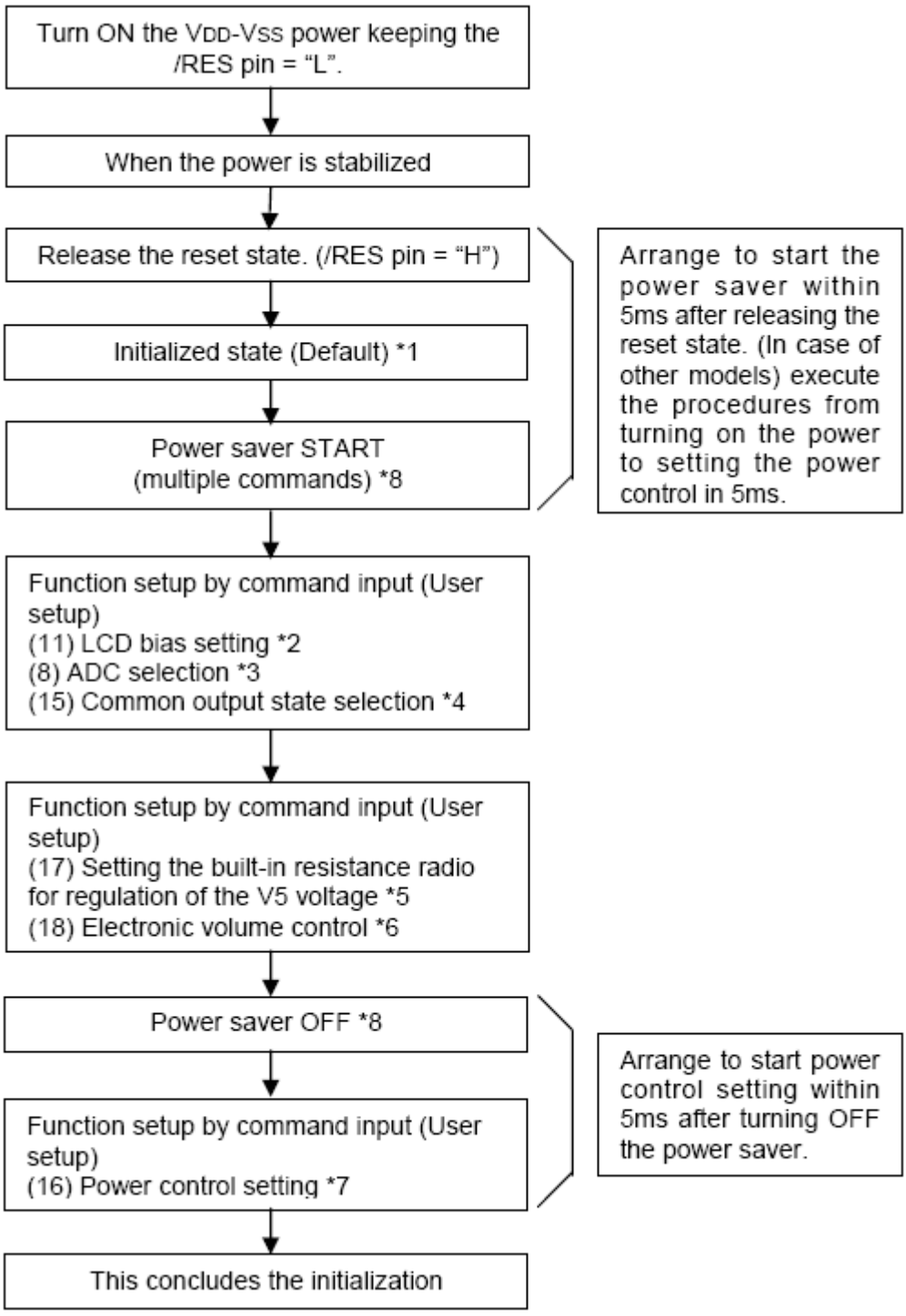
*4: Command description; Common output state selection

*5: Description of functions; Power circuit & Command description; Setting the built-in resistance radio for regulation of the V5 voltage

*6: Description of functions; Power circuit & Command description; Electronic volume control

*7: Description of functions; Power circuit & Command description; Power control setting

2. When the built-in power is not being used immediately after turning on the power:



* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Notes: Refer to respective sections or paragraphs listed below.

*1: Description of functions; Resetting circuit

*2: Command description; LCD bias setting

*3: Command description; ADC selection

*4: Command description; Common output state selection

*5: Description of functions; Power circuit & Command description; Setting the built-in resistance radio for regulation of the V5 voltage

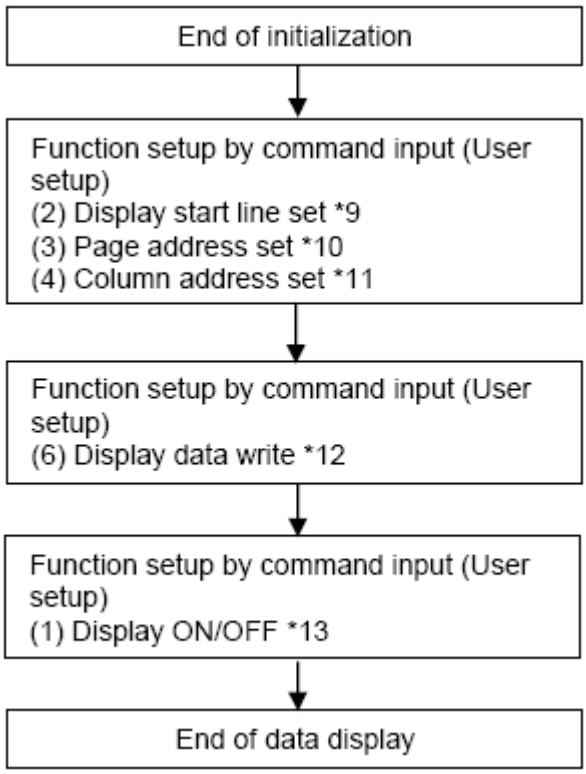
*6: Description of functions; Power circuit & Command description; Electronic volume control

*7: Description of functions; Power circuit & Command description; Power control setting

*8: The power saver ON state can either be in sleep state or stand-by state.

Command description; Power saver START (multiple commands)

(2) Data Display



Notes: Reference items

*9: Command Description; Display start line set

*10: Command Description; Page address set

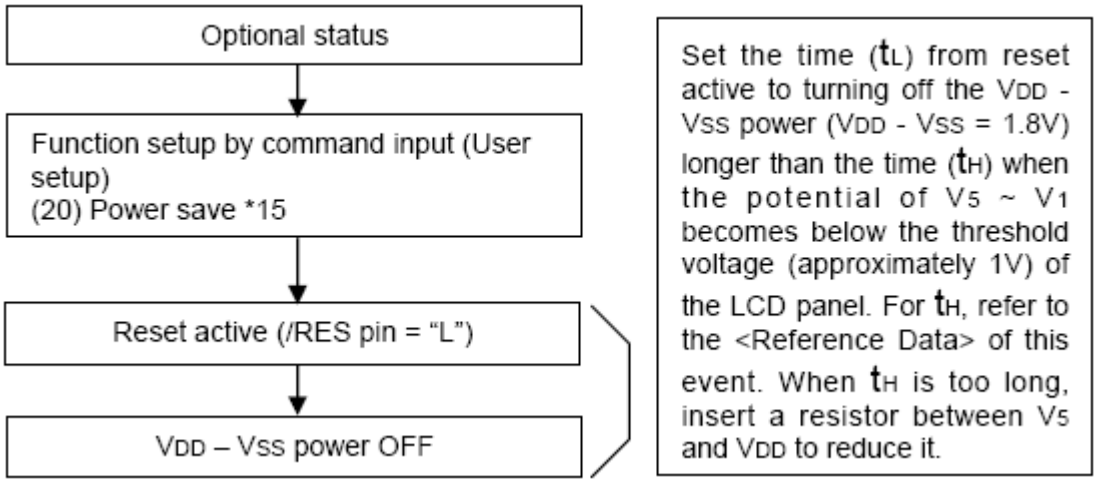
*11: Command Description; Column address set

*12: Command Description; Display data write

*13: Command Description; Display ON/OFF

Avoid displaying all the data at the data display start (when the display is ON) in white.

(3) Power OFF *14



Notes: Reference items

*14: The logic circuit of this IC's power supply VDD - VSS controls the driver of the LCD power supply VDD - V5. So, if the power supply VDD - VSS is cut off when the LCD power supply VDD - V5 has still any residual voltage, the driver (COM. SEG) may output any uncontrolled voltage. When turning off

the power, observe the following basic procedures:

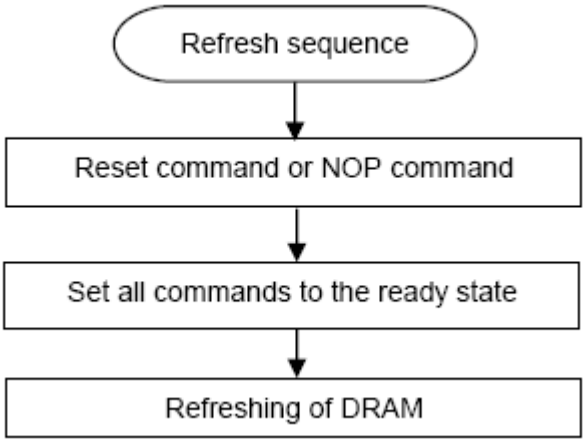
• After turning off the internal power supply, make sure that the potential V5 ~ V1 has become below the threshold voltage of the LCD panel, and then turn off this IC’s power supply (VDD - VSS). 6. Description of Function, 6.7 Power Circuit

*15: After inputting the power save command, be sure to reset the function using the /RES terminal until the power supply VDD - VSS is turned off. 7. Command Description (20) Power Save

*16: After inputting the power save command, do not reset the function using the /RES terminal until the power supply VDD - VSS is turned off. 7. Command Description (20) Power Save

Refresh

It is recommended to turn on the refresh sequence regularly at a specified interval.



Precautions on Turning off the power

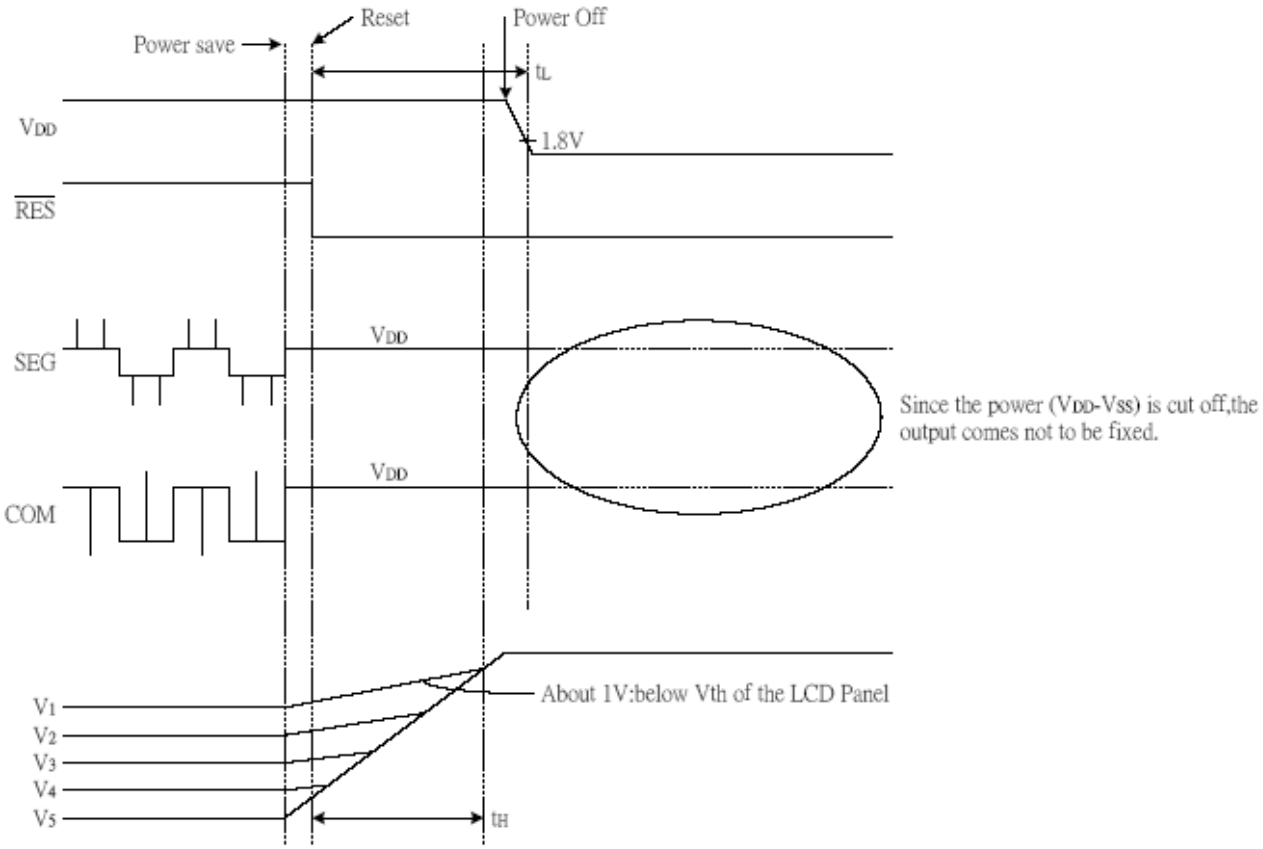
<Turning the power (VDD - VSS) off>

1) Power Save (The LCD powers (VDD - V5) are off.) → Reset input → Power (VDD - VSS) OFF

• Observe tL > tH.

• When tL < tH, an irregular display may occur.

Set tL on the MPU according to the software. tH is determined according to the external capacity C2 (smoothing capacity of V5 ~ V1) and the driver’s discharging capacity.



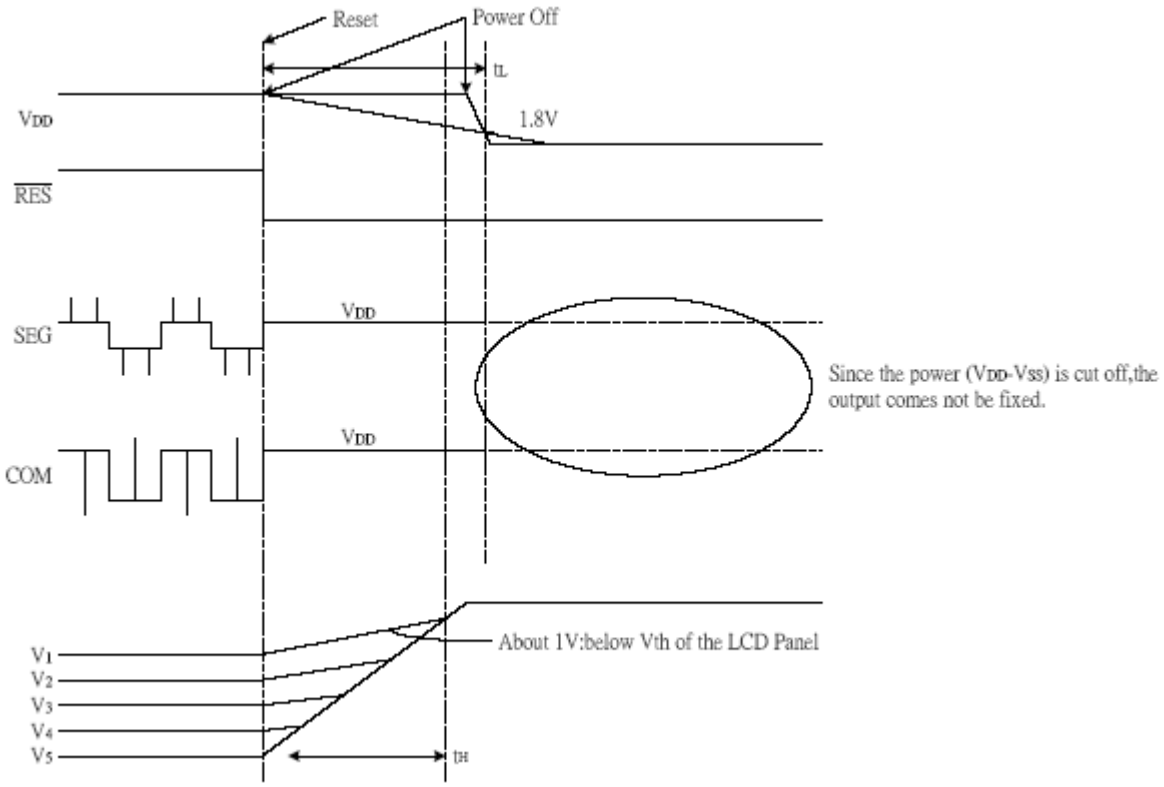
<Turning the power (VDD - VSS) off : When command control is not possible.>

2) Reset (The LCD powers (VDD - VSS) are off.) → Power (VDD - VSS) OFF

• Observe tL > tH.

• When tL < tH, an irregular display may occur.

For tL, make the power (VDD - VSS) falling characteristics longer or consider any other method. tH is determined according to the external capacity C2 (smoothing capacity of V5 to V1) and the driver's discharging capacity.



<Reference Data>

V5 voltage falling (discharge) time (tH) after the process of operation → power save → reset.

V5 voltage falling (discharge) time (tH) after the process of operation → reset.

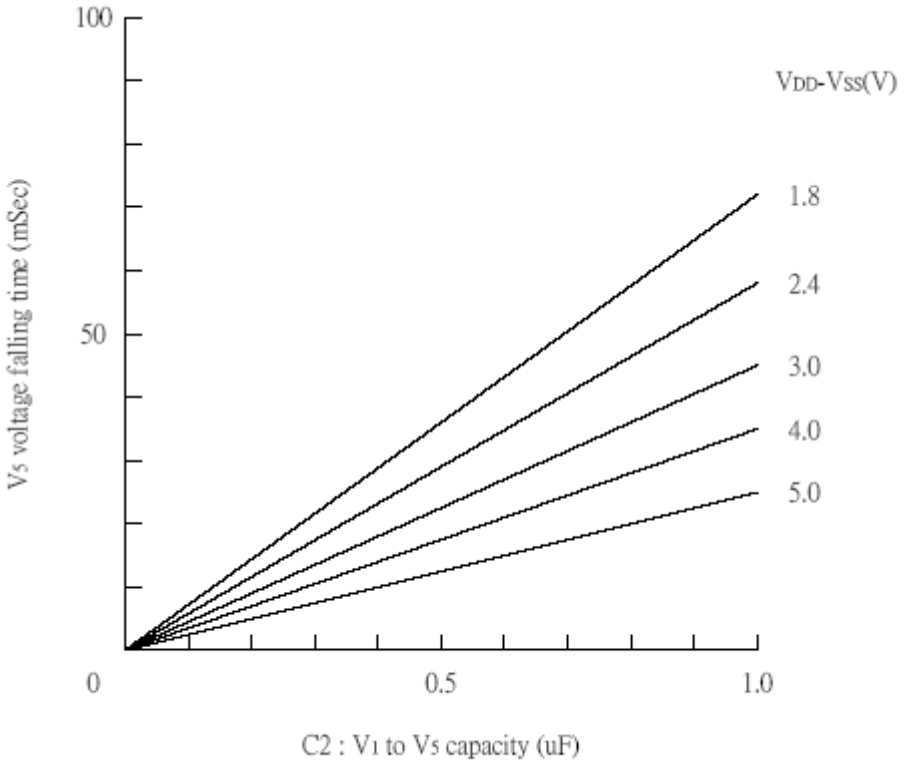


Figure 31

10.Reliability

Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Note**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	____
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60 ℃,90%RH max For 96hrs under no-load condition excluding the polarizer, Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation -20℃ 25℃ 70℃ 3 1 cycle	-20℃/70℃ 10 cycles	____
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V,RS=1.5kΩ CS=100pF 1 time	____

C**ontent of Reliability Test (wide temperature, -20℃~70℃)**

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal

Temperature and humidity after remove from the test chamber.

Note3: Vibration test will be conducted to the product itself without putting it in a container.

11.Backlight Information

Specification

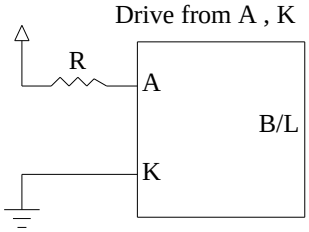
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
Supply Current	ILED	80	101	150	mA	V=*V
Supply Voltage	V	3.4	3.5	3.6	V	
Reverse Voltage	VR	-	-	5	V	-
Luminous Intensity	IV	800	1000	-	CD/M^2	ILED=101mA
Wave Length	X	0.27	0.30	0.33		ILED=101mA
	Y	0.26	0.29	0.32		
LED Life Time	-	-	50K	-	Hr.	ILED=101mA 25℃,50-60%RH, Note 1
Color	White					

Note: The LED of B/L is drive by current only；driving voltage is only for reference

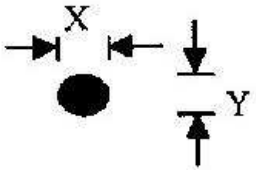
To make driving current in safety area (waste current between minimum and maximum).

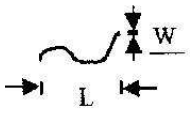
Note1 :50K hours is only an estimate for reference.

LED B\L Drive Method
Drive from A , K



12. Inspection specification

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>01</td><td>Electrical Testing</td><td>1.1 Missing vertical, horizontal segment, segment contrast defect.
1.2 Missing character , dot or icon.
1.3 Display malfunction.
1.4 No function or no display.
1.5 Current consumption exceeds product specifications.
1.6 LCD viewing angle defect.
1.7 Mixed product types.
1.8 Contrast defect.</td><td>0.65</td></tr>
<tr><td>02</td><td>Black or white spots on LCD (display only)</td><td>2.1 White and black spots on display ≦ 0.25mm, no more than three white or black spots present.
2.2 Densely spaced: No more than two spots or lines within 3mm</td><td>2.5</td></tr>
<tr><td>03</td><td>LCD black spots, white spots, contamination (non-display)</td><td>3.1 Round type : As following drawing
Φ =(x + y) / 2
 

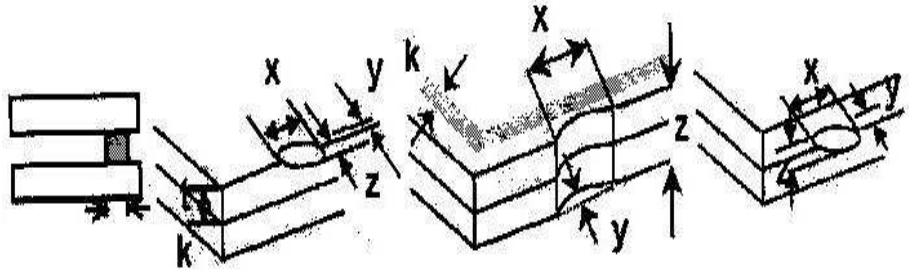
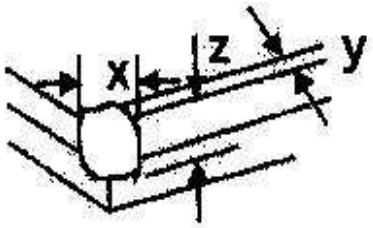
<table>
<tr><th>SIZE</th><th>Acceptable Q TY</th></tr>
<tr><td>Φ ≦ 0.10</td><td>Accept no dense</td></tr>
<tr><td>0.10 < Φ ≦ 0.20</td><td>2</td></tr>
<tr><td>0.20 < Φ ≦ 0.25</td><td>1</td></tr>
<tr><td>0.25 < Φ</td><td>0</td></tr>
</table>
3.2 Line type : (As following drawing)
 

<table>
<tr><th>Length</th><th>Width</th><th>Acceptable Q TY</th></tr>
<tr><td>---</td><td>W≦ 0.02</td><td>Accept no dense</td></tr>
<tr><td>L≦ 3.0</td><td>0.02 < W≦ 0.03</td><td rowspan="2">2</td></tr>
<tr><td>L≦ 2.5</td><td>0.03 < W≦ 0.05</td></tr>
<tr><td>---</td><td>0.05 < W</td><td>As round type</td></tr>
</table></td><td>2.5

2.5</td></tr>
</table>

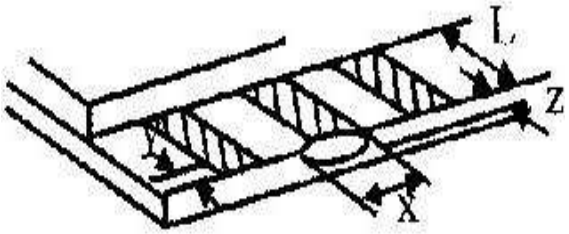
<table>
<tr>
<td>04</td>
<td>Polarizer bubbles</td>
<td>If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction.
<table>
<tr><td>Size Φ</td><td>Acceptable Q TY</td></tr>
<tr><td>Φ ≦ 0.20</td><td>Accept no dense</td></tr>
<tr><td>0.20 < Φ ≦ 0.50</td><td>3</td></tr>
<tr><td>0.50 < Φ ≦ 1.00</td><td>2</td></tr>
<tr><td>1.00 < Φ</td><td>0</td></tr>
<tr><td>Total Q TY</td><td>3</td></tr>
</table>
</td>
<td>2.5</td>
</tr>
</table>

NO	Item	Criterion	AQL
05	Scratches	Follow NO.3 LCD black spots, white spots, contamination	

06	Chipped glass	Symbols Define: x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: LCD side length L: Electrode pad length: 6.1 General glass chip : 6.1.1 Chip on panel surface and crack between panels:  **z: Chip thickness / y: Chip width / x: Chip length** Z≦ 1/2t — Not over viewing area — x≦ 1/8a 1/2t < z≦ 2t — Not exceed 1/3k — x≦ 1/8a ⊙ If there are 2 or more chips, x is total length of each chip. 6.1.2 Corner crack:  **z: Chip thickness / y: Chip width / x: Chip length** Z≦ 1/2t — Not over viewing area — x≦ 1/8a 1/2t < z≦ 2t — Not exceed 1/3k — x≦ 1/8a ⊙ If there are 2 or more chips, x is the total length of each chip.	2.5

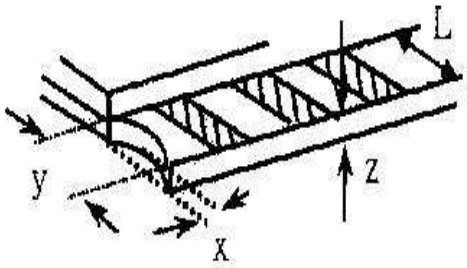
NO	Item	Criterion	AQL

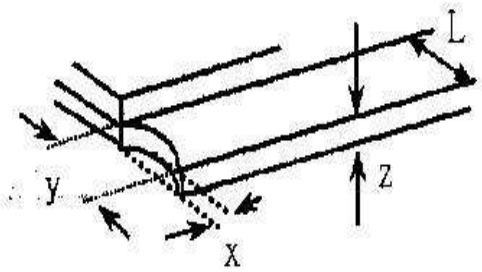
06	Glass crack	Symbols : x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: LCD side length L: Electrode pad length 6.2 Protrusion over terminal : 6.2.1 Chip on electrode pad :	2.5



y: Chip width	x: Chip length	z: Chip thickness
y≦ 0.5mm	x≦ 1/8a	0 < z ≦ t

6.2.2 Non-conductive portion:



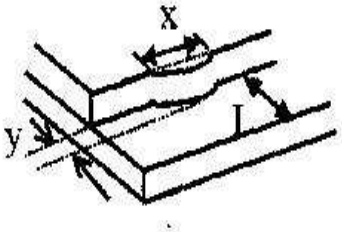


y: Chip width	x: Chip length	z: Chip thickness
y≦ L	x≦ 1/8a	0 < z ≦ t

⊙ If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.

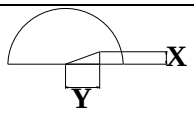
⊙ If the product will be heat sealed by the customer, the alignment mark not be damaged.

6.2.3 Substrate protuberance and internal crack.



y: width	x: length
y≦ 1/3L	x ≦ a

NO	Item	Criterion	AQL
07	Cracked glass	The LCD with extensive crack is not acceptable.	2.5
08	Backlight elements	8.1 Illumination source flickers when lit. 8.2 Spots or scratched that appear when lit must be judged. Using LCD spot, lines and contamination standards. 8.3 Backlight doesn’ t light or color wrong.	0.65 2.5 0.65
09	Bezel	9.1 Bezel may not have rust, be deformed or have fingerprints, stains or other contamination. 9.2 Bezel must comply with job specifications.	2.5 0.65
10	PCB、COB	10.1 COB seal may not have pinholes larger than 0.2mm or contamination. 10.2 COB seal surface may not have pinholes through to the IC. 10.3 The height of the COB should not exceed the height indicated in the assembly diagram. 10.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places. 10.5 No oxidation or contamination PCB terminals. 10.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts. 10.7 The jumper on the PCB should conform to the product characteristic chart. 10.8 If solder gets on bezel tab pads, LED pad, zebra pad or screw hold pad, make sure it is smoothed down. 10.9 The Scraping testing standard for Copper Coating of PCB	2.5 2.5 0.65 2.5 2.5 0.65 0.65 2.5 2.5

		 **X * Y<=2mm^2**	
11	Soldering	11.1 No un-melted solder paste may be present on the PCB. 11.2 No cold solder joints, missing solder connections, oxidation or icicle. 11.3 No residue or solder balls on PCB. 11.4 No short circuits in components on PCB.	2.5 2.5 2.5 0.65

NO	Item	Criterion	AQL
12	General appearance	12.1 No oxidation, contamination, curves or, bends on interface Pin (OLB) of TCP. 12.2 No cracks on interface pin (OLB) of TCP. 12.3 No contamination, solder residue or solder balls on product. 12.4 The IC on the TCP may not be damaged, circuits. 12.5 The uppermost edge of the protective strip on the interface pin must be present or look as if it cause the interface pin to sever. 12.6 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color. 12.7 Sealant on top of the ITO circuit has not hardened. 12.8 Pin type must match type in specification sheet. 12.9 LCD pin loose or missing pins. 12.10 Product packaging must the same as specified on packaging specification sheet. 12.11 Product dimension and structure must conform to product specification sheet.	2.5 0.65 2.5 2.5 2.5 2.5 2.5 0.65 0.65 0.65 0.65

13. Material List of Components for RoHs

1. The factory hereby declares that all of or part of products (with the mark "#"in code), including, but not limited to, the LCM, accessories or packages, manufactured and/or delivered to your company (including your subsidiaries and affiliated company) directly or indirectly by our company (including our subsidiaries or affiliated companies) do not intentionally contain any of the substances listed in all applicable EU directives and regulations, including the following substances.

Exhibit A：The Harmful Material List

.

Material	(Cd)	(Pb)	(Hg)	(Cr6+)	PBBs	PBDEs
Limited Value	100 ppm	1000 ppm	1000 ppm	1000 ppm	1000 ppm	1000 ppm
Above limited value is set up according to RoHS.						

2.Process for RoHS requirement：

(1) Use the Sn/Ag/Cu soldering surface；the surface of Pb-free solder is rougher than we used before.

(2) Heat-resistance temp.：

Reflow：250℃,30 seconds Max.；

Connector soldering wave or hand soldering：320℃, 10 seconds max.

(3) Temp. curve of reflow, max. Temp.：235±5℃；

Recommended customer's soldering temp. of connector：280℃, 3 seconds.

SOG24006437-BTN-ELLW

Sales signature：_____

Customer Signature：_____ **Date： / /**