



INNOVATIVE DISPLAY TECHNOLOGIES

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Specification

Part Number : SCA05735-BFN-LNC

Customer : _____

APPROVED BY: (FOR CUSTOMER USE ONLY)	PCB VERSION:	DATE:
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SOLD BY	APPROVED BY	CHECKED BY	ISSUE DATE

MODLE NO :

DOC. FIRST ISSUE

RECORDS OF REVISION

VERSION	DATE	REVISED PAGE NO.	SUMMARY
0	2009/5/14		First issue
A	2009/8/12	20	Modify LED Life Time

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4. Absolute Maximum Ratings
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1.Module Classification Information

SCA 0 5 7 35 – B F N – L N C

① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪

- ① Brand : Shelly Associates Inc.
- ② Display Type : SCA → TFT Type
- ③ Display Size : 5.7” TFT
- ④ Model serials no.
- ⑤ Backlight Type : L→ LED, White

- ⑥ LCD Polarize F→ Transmissive,
Type/ Temperature B → W. T, 6:00
range/ View
direction
- ⑦ C: TFT+FR+CONTROL BOARD

- ⑧ Solution: C:320240
D: Digital
- ⑨ Version

- ⑩
- ⑪ Special Code #:Fit in with ROHS directive regulations

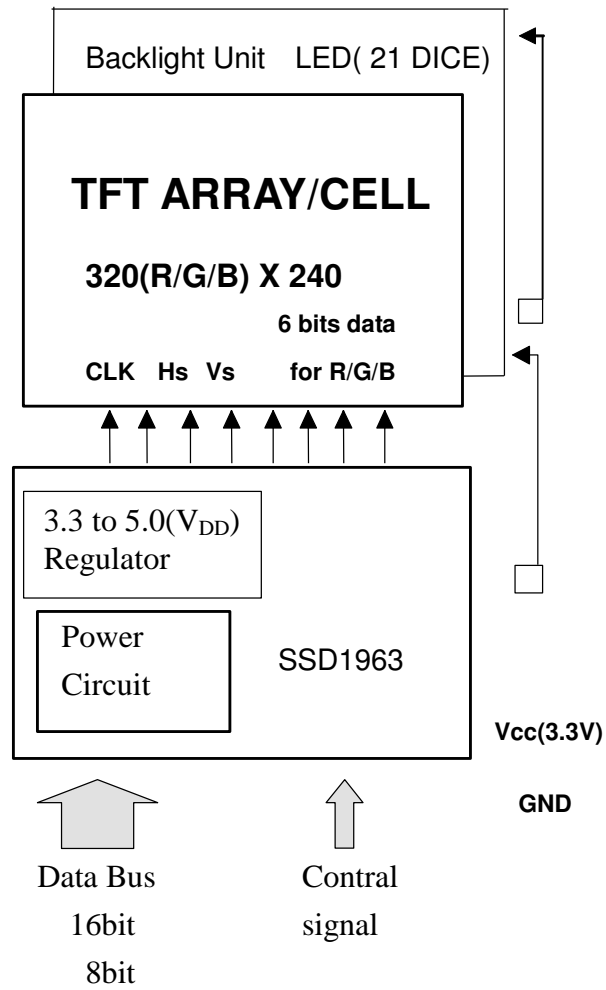
This product is composed of a TFT LCD panel, driver ICs, FPC, Control Board and a backlight unit. The following table described the features of SCA05735-BFN-LNC.

Item	Dimension	Unit
Dot Matrix	320 x RGBx240(TFT)	dots
Module dimension	141.12x 101.55 x 5.8 (max)	mm
View area	126.0x 89.1	mm
Dot pitch	0.12 x 0.36	mm
Driving IC package	COG	
LCD type	TFT, Negative, Transmissive	
View direction	6 o'clock	
Backlight Type	LED, Normally White	
Controller IC	SSD1963	

*Expose the IC number blaze (Luminosity over than 1 cd) when using the LCM may cause IC operating failure.

*Color tone slight changed by temperature and driving voltage.

2. Block Diagram



3. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	VCC	-	3.0	3.3	3.6	V
Input High Volt.	V _{IH}	-	0.8VDD IO	-	VDDIO + 0.5	V
Input Low Volt.	V _{IL}	-	-	-	0.2VDDIO	V
LCD Driving Supply Voltage	V _{GH} *1	Ta=25°C		15		V *3
	V _{GL} *2			-10		V
	Vcom		-	3.7	-	
Supply Current	I _{VDD}	V _{DD} =3.3V	-	121	-	mA

Notes:

*1) VGH is TFT Gate on operating Voltage.

*2) VGL is TFT Gate off operating Voltage, VGL signal must be fluctuates with same phase as Vcom when Storage on Gate structure.

*3) Vcom must be adjusted to optimize display quality_Crosstalk, Contrast Ratio and etc.

4. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T _{OP}	-20	-	+70	°C
Storage Temperature	T _{ST}	-30	-	+80	°C
Power Supply Voltage	V _{GH}	-0.3	-	18	V
	V _{GL}	-15	-	0.3	V
	VCC	-0.3	-	6.0	V

5.Interface Pin Function

5-1 Pins Connection To Control Board

P/N	Symbol	8 B IT Function
1	GND	Ground
2	VCC	Power supply for Logic
3	NC	No connection
4	RS	
5	WR	8080 family MPU interface : Write signal
6	RD	8080 family MPU interface: Read signal
7	DB0	Data bus
8	DB1	
9	DB2	
10	DB3	
11	DB4	
12	DB5	
13	DB6	
14	DB7	
15	CS	Chip select
16	RST	RESET
17	NC	No connection
18	RL	Scan direction
19	UD	Scan direction
20	NC	No connection

6. DC CHARACTERISTICS

Conditions:

Voltage referenced to VSS

VDDD, VDDPLL = 1.2V

VDDIO, VDDLCD = 3.3V

TA = 25°C

DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
PSTY	Quiescent Power			300		uW
IIZ	Input leakage current		-1		1	uA
IOZ	Output leakage current		-1		1	uA
VOH	Output high voltage		0.8VDDIO			V
VOL	Output low voltage				0.2VDDIO	V
VIH	Input high voltage		0.8VDDIO		VDDIO + 0.5	V
VIL	Input low voltage				0.2VDDIO	V

7. AC Characteristics

Conditions:

Voltage referenced to V_{SS}

V_{DD}, V_{DDPLL} = 1.2V

V_{DDIO}, V_{DDLCD} = 3.3V

T_A = 25°C

C_L = 50pF (Bus/CPU Interface)

C_L = 0pF (LCD Panel Interface)

7.1 Clock Timing

Clock Input Requirements for CLK (PLL-bypass)

Symbol	Parameter	Min	Max	Units
FCLK	Input Clock Frequency (CLK)		120	MHz
TCLK	Input Clock period (CLK)	1/fCLK		ns

Clock Input Requirements for CLK (Using PLL)

Symbol	Parameter	Min	Max	Units
FCLK	Input Clock Frequency (CLK)	2.5	50	MHz
TCLK	Input Clock period (CLK)	1/fCLK		ns

Clock Input Requirements for crystal oscillator XTAL (Using PLL)

Symbol	Parameter	Min	Max	Units
FXTAL	Input Clock Frequency	2.5	10	MHz
TXTAL	Input Clock period	1/fXTAL		ns

7.2 MCU Interface Timing

7.2.1 6800 Mode

Table 7-4: 6800 Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit
tcyc	Reference Clock Cycle Time	9	-	-	ns
tPWCSL	Pulse width CS# or E low	1	-	-	tCYC
tPWCSH	Pulse width CS# or E high	1	-	-	tCYC
tFDRD	First Data Read Delay	5	-	-	tCYC
tAS	Address Setup Time	1	-	-	ns
tAH	Address Hold Time	1	-	-	ns
tDSW	Data Setup Time	4	-	-	ns
tDHW	Data Hold Time	1	-	-	ns
tDSR	Data Access Time	-	-	5	ns
tDHR	Output Hold time	1	-	-	ns

Figure 7-1: 6800 Mode Timing Diagram (Use CS# as Clock)

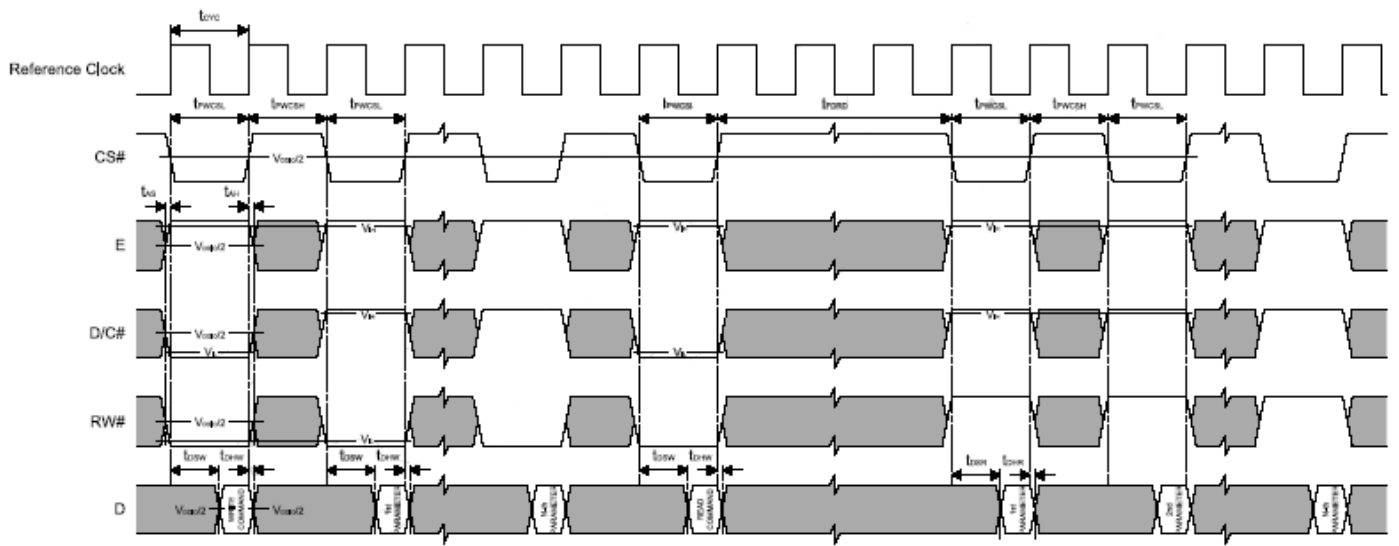
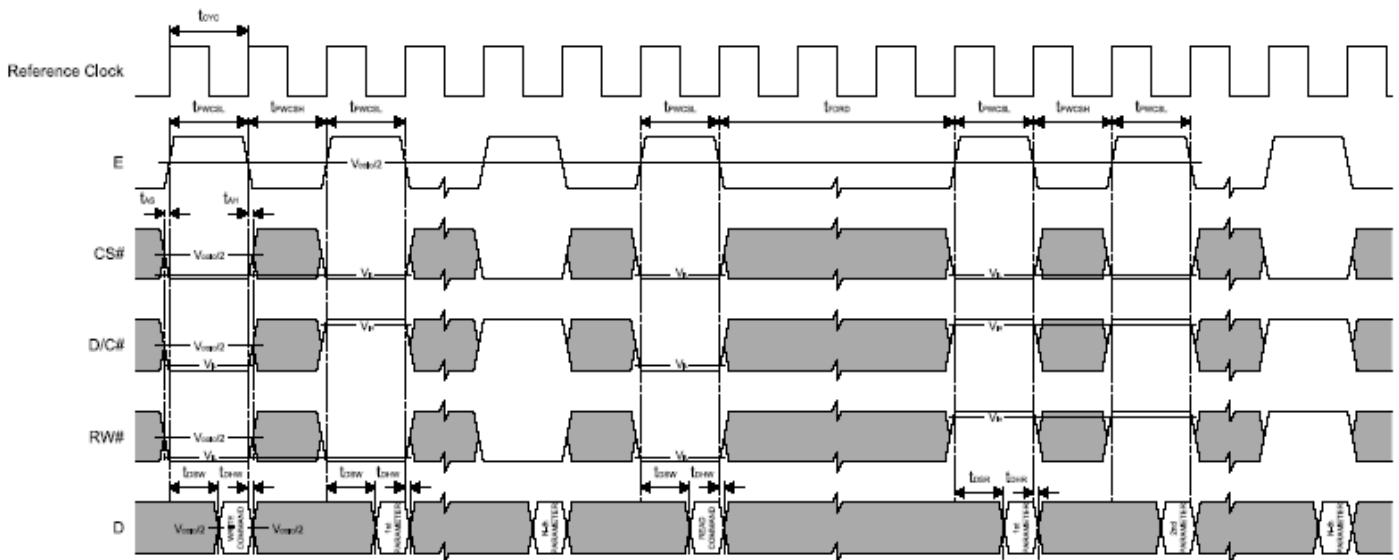


Figure 7-2: 6800 Mode Timing Diagram (Use E as Clock)

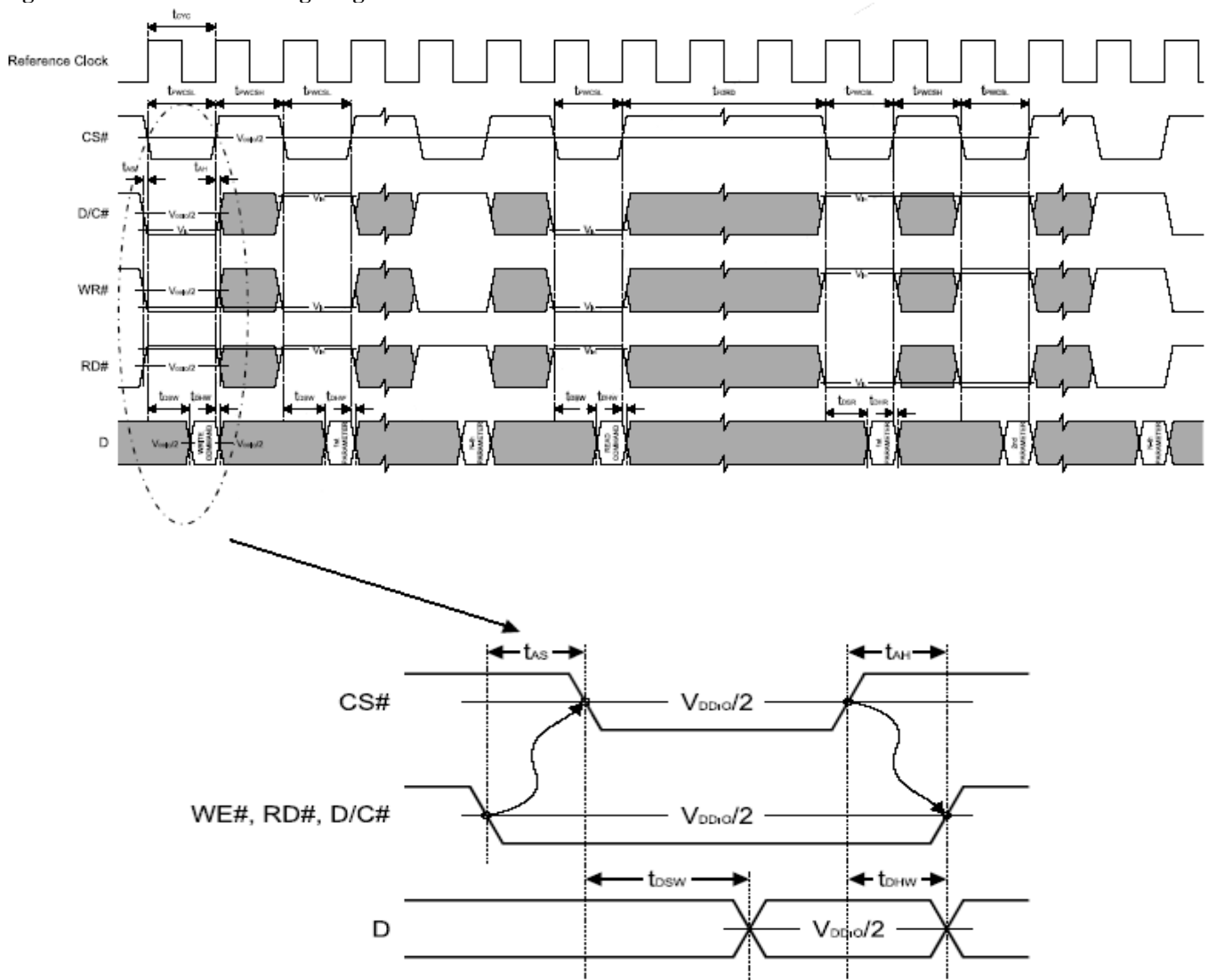


7.2.2 8080 Mode Write Cycle

Table 7-5: 8080 Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit
t _{cy}	Reference Clock Cycle Time	9	-	-	ns
t _{PWCSL}	Pulse width CS# low	1	-	-	t _{CYC}
t _{PWCSH}	Pulse width CS# high	1	-	-	t _{CYC}
t _{FDRD}	First Read Data Delay	5	-	-	t _{CYC}
t _{AS}	Address Setup Time	1	-	-	ns
t _{AH}	Address Hold Time	1	-	-	ns
t _{DSW}	Data Setup Time	4	-	-	ns
t _{DHW}	Data Hold Time	1	-	-	ns
t _{DSR}	Data Access Time	-	-	5	ns
t _{DHR}	Output Hold time	1	-	-	ns

Figure 7-3: 8080 Mode Timing Diagram



8. Data transfer order Setting

Pixel Data Format

Both 6800 and 8080 support 8-bit, 9-bit, 16-bit, 18-bit and 24-bit data bus. Depending on the width of the data bus, the display data are packed into the data bus in different ways.

Pixel Data Format :

Interface	Cycle	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]		
24 bits	1 st	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0		
18 bits	1 st							R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0		
16 bits (565 format)	1 st									R5	R4	R3	R2	R1	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1		
16 bits	1 st									R5	R4	R3	R2	R1	R0	X	X	G5	G4	G3	G2	G1	G0	X	X		
	2 nd									B5	B4	B3	B2	B1	B0	X	X	R5	R4	R3	R2	R1	R0	X	X		
	3 rd									G5	G4	G3	G2	G1	G0	X	X	B5	B4	B3	B2	B1	B0	X	X		
9 bits	1 st																	R5	R4	R3	R2	R1	R0	G5	G4	G3	
	2 nd																	G2	G1	G0	B5	B4	B3	B2	B1	B0	
8 bits	1 st																			R5	R4	R3	R2	R1	R0	X	X
	2 nd																			G5	G4	G3	G2	G1	G0	X	X
	3 rd																			B5	B4	B3	B2	B1	B0	X	X

X: Don't Care

9 Register Depiction

Please consult the spec of SSD1963

10. OPTICAL CHARACTERISTIC

Ta=25±2°C, ILED=20mA

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Tr	$\theta = 0^\circ, \Phi = 0^\circ$	-	10		ms	Note 3,5
	Tf		-	15		ms	
Contrast ratio	CR	At optimized viewing angle	300	400	-	-	Note 4,5
Color Chromaticity	White	Wx	$\theta = 0^\circ, \Phi = 0^\circ$	(0.26)	(0.31)	(0.36)	Note 2,6,7
		Wy		(0.28)	(0.33)	(0.38)	
	Red	Rx	$\theta = 0^\circ, \Phi = 0^\circ$				
		Ry					
	Green	Gx	$\theta = 0^\circ, \Phi = 0^\circ$				
		Gy					
Blue	Bx	$\theta = 0^\circ, \Phi = 0^\circ$					
	By						
Viewing angle	Hor.	Θ_R	CR ≥ 10	(50)	(60)	Deg.	Note 1
		Θ_L		(50)	(60)		
	Ver.	Φ_T		(40)	(50)		
		Φ_B		(45)	(55)		
Brightness	-	-	200	250	-	cd/m ²	Center of display

Ta=25±2°C, IL=20mA

Note 1: Definition of viewing angle range

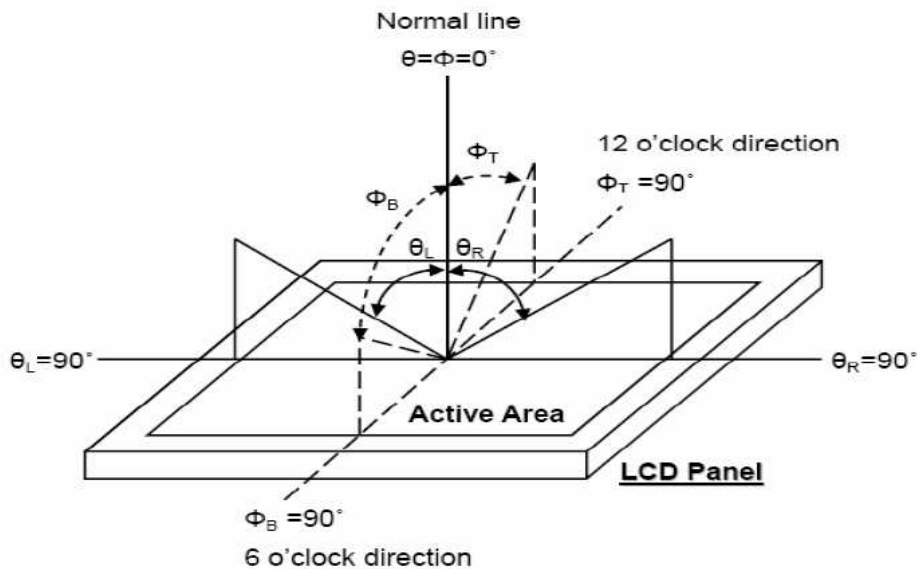


Fig. 8-1 Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

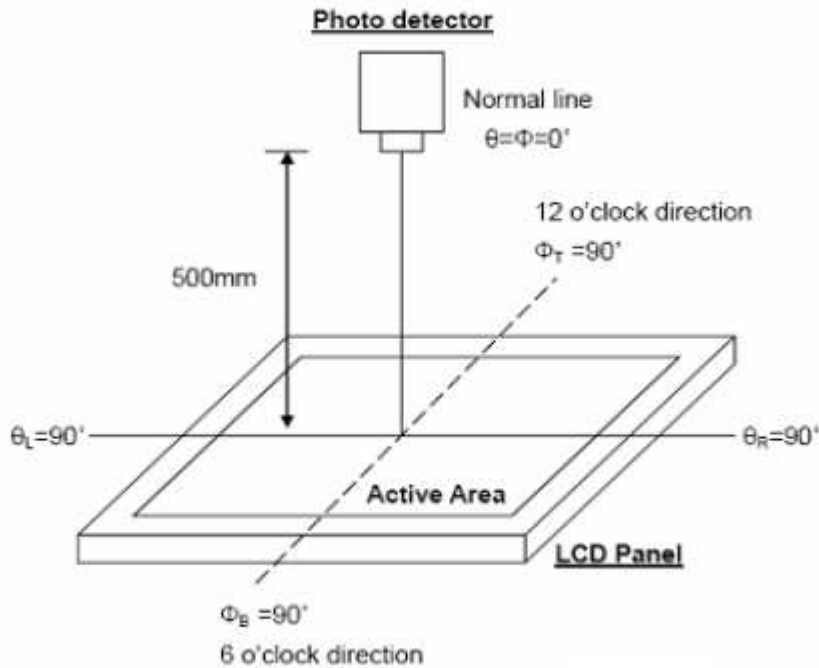


Fig. 8-2 Optical measurement system setup

Note 3: Definition of Response time:

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time, T_r , is the time between photo detector output intensity changed from 90% to 10% . And fall time, T_f , is the time between photo detector output intensity changed from 10% to 90% .

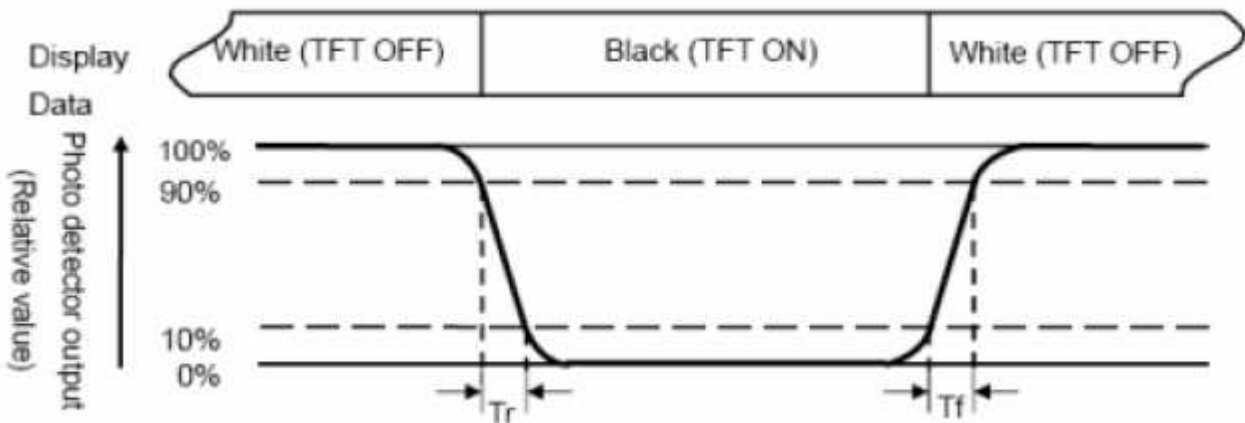


Fig. 3-3 Definition of response time

Note 4: Definition of contrast ratio:

The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: White $V_i = V_{i50} \pm 1.5V$

Black $V_i = V_{i50} \pm 2.0V$

“±” means that the analog input signal swings in phase with VCOM signal.

“±” means that the analog input signal swings out of phase with VCOM signal.

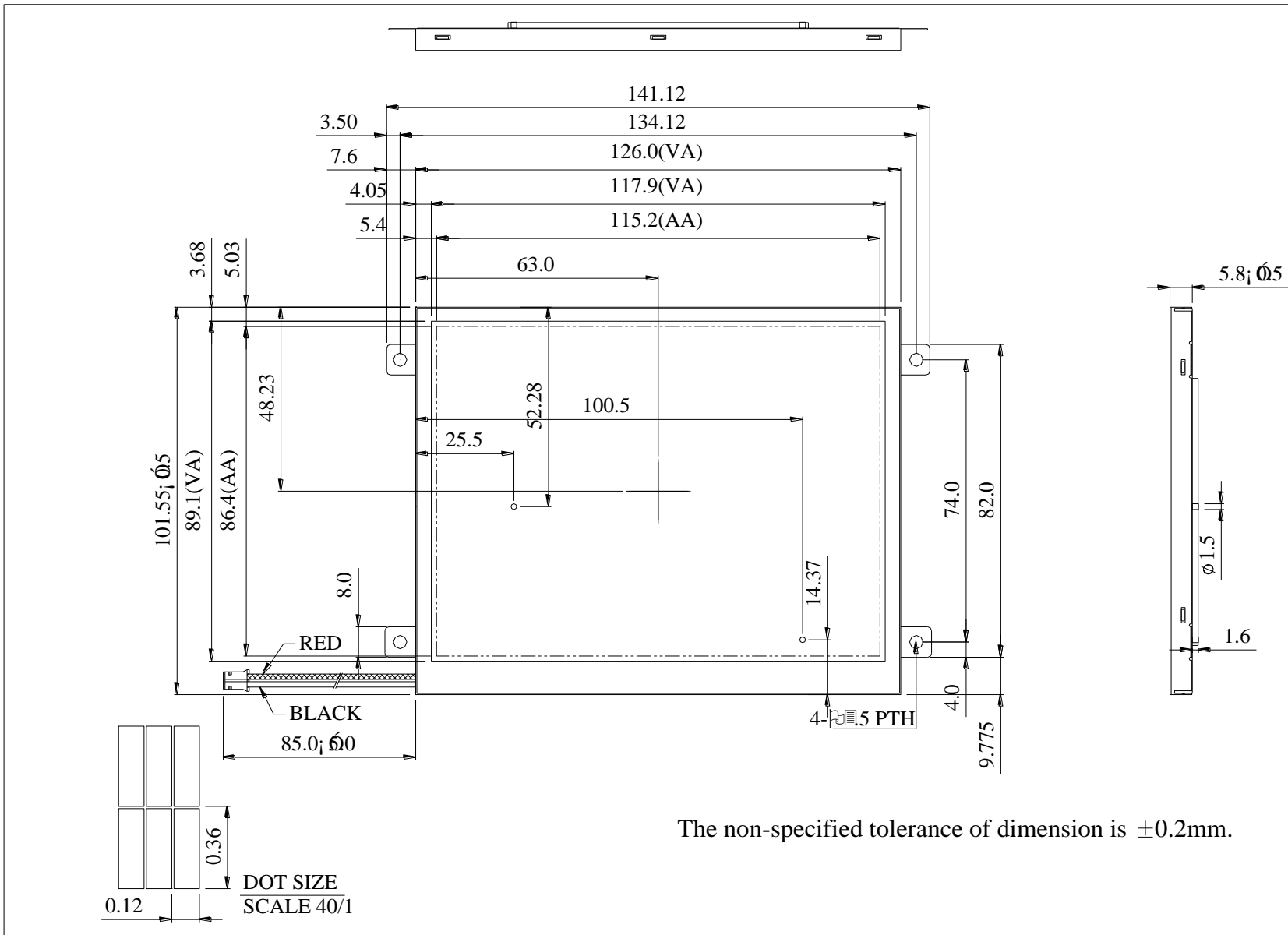
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 6: Definition of color chromaticity (CIE 1931)
Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

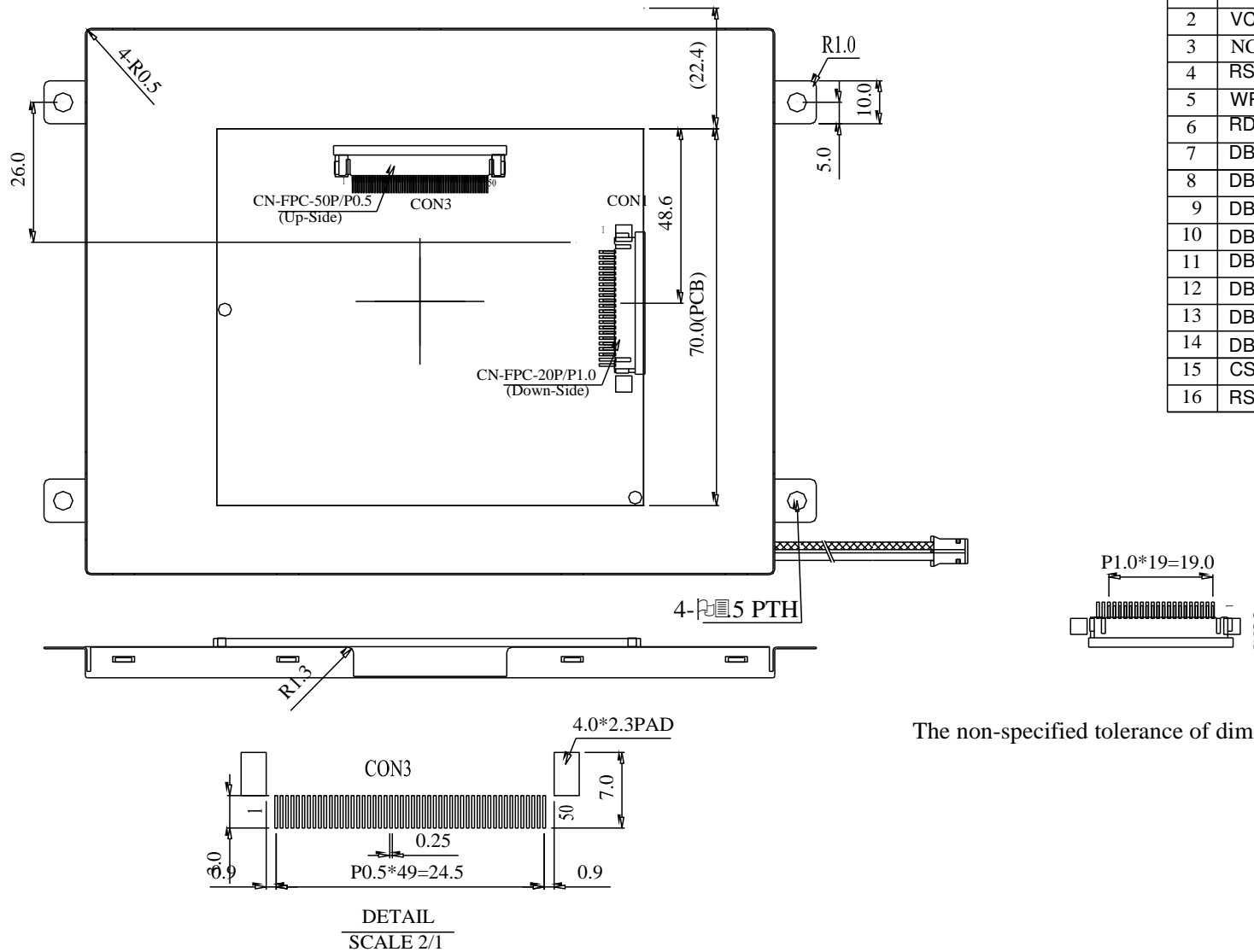
$$\text{Note 8 : Uniformity (U)} = \frac{\text{Brightness (min)}}{\text{Brightness (max)}} \times 100\%$$

11. Contour Drawing



8bit mode

PIN NO.	SYMBOL	PIN NO.	SYMBOL
1	GND	17	NC
2	VCC	18	RL
3	NC	19	UD
4	RS	20	NC
5	WR		
6	RD		
7	DB0		
8	DB1		
9	DB2		
10	DB3		
11	DB4		
12	DB5		
13	DB6		
14	DB7		
15	CS		
16	RST		

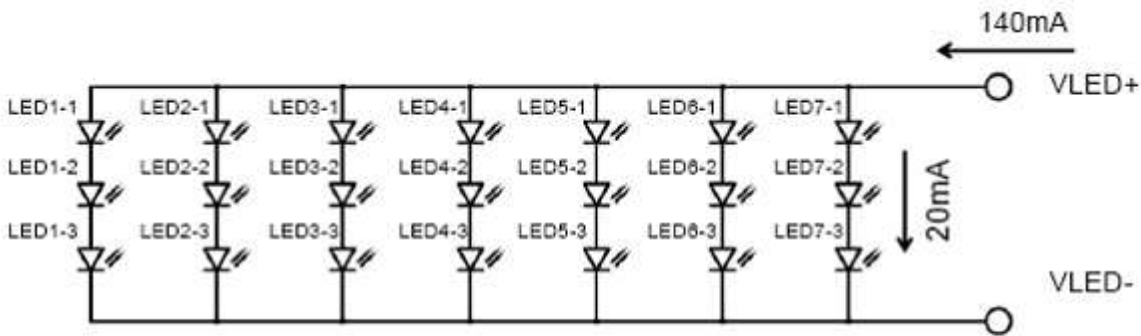


The non-specified tolerance of dimension is $\pm 0.2\text{mm}$.

12. LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Current	I_{LED}	----	140	210	mA	Note1
LED voltage	V_{LED}	9.0	10.2	10.5	V	
LED life Time	-	----	50K	----	-	Note 2,3,5
Luminous Intensity	IV	----	300	----	CD/M ²	Note 4

Note 1: There are 7 Groups LED shown as below, =9.9 V(Min)



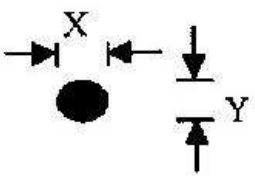
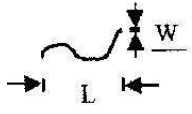
Note 2 : $T_a = 25^{\circ}\text{C}$,

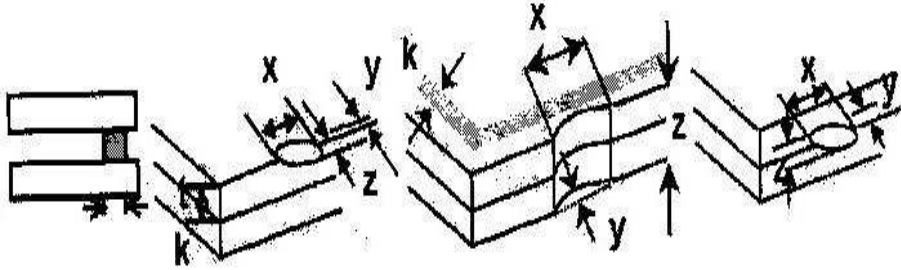
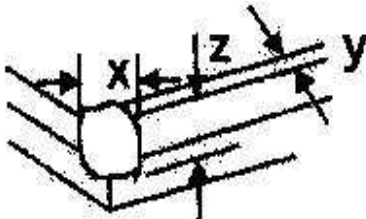
Note 3 : Brightness to be decreased to 50% of the initial value.

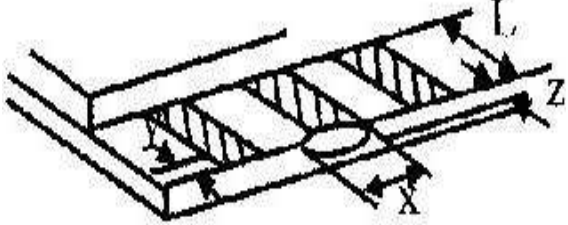
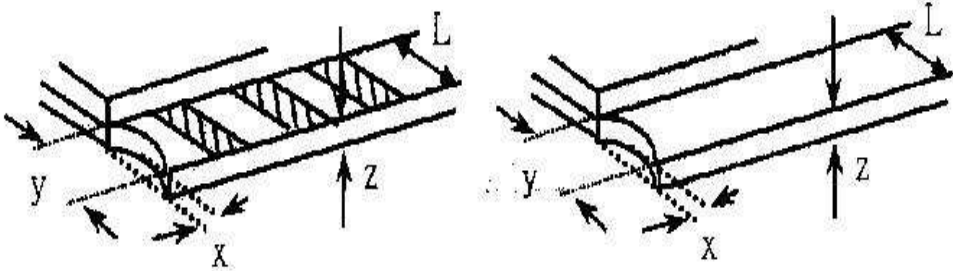
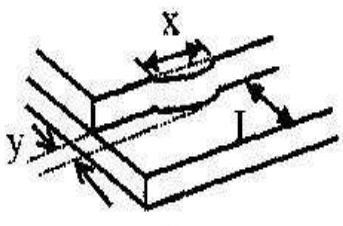
Note 4: The luminous is measured through LCD panel.

Note5:50K hours is only an estimate for reference.

13. Inspection specification

NO	Item	Criterion	AQL													
01	Electrical Testing	1.1 Missing vertical, horizontal segment, segment contrast defect. 1.2 Missing character , dot or icon. 1.3 Display malfunction. 1.4 No function or no display. 1.5 Current consumption exceeds product specifications. 1.6 LCD viewing angle defect. 1.7 Mixed product types. 1.8 Contrast defect.	0.65													
02	Black or white spots on LCD (display only)	2.1 White and black spots on display $\leq 0.25\text{mm}$, no more than three white or black spots present. 2.2 Densely spaced: No more than two spots or lines within 3mm	2.5													
03	LCD black spots, white spots, contamination (non-display)	3.1 Round type : As following drawing $\Phi = (x + y) / 2$  <table border="1" data-bbox="869 884 1348 1400"> <thead> <tr> <th>SIZE</th> <th>Acceptable QTY</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.10$</td> <td>Accept no dense</td> </tr> <tr> <td>$0.10 < \Phi \leq 0.20$</td> <td>2</td> </tr> <tr> <td>$0.20 < \Phi \leq 0.25$</td> <td>1</td> </tr> <tr> <td>$0.25 < \Phi$</td> <td>0</td> </tr> </tbody> </table>	SIZE	Acceptable QTY	$\Phi \leq 0.10$	Accept no dense	$0.10 < \Phi \leq 0.20$	2	$0.20 < \Phi \leq 0.25$	1	$0.25 < \Phi$	0	2.5			
		SIZE	Acceptable QTY													
$\Phi \leq 0.10$	Accept no dense															
$0.10 < \Phi \leq 0.20$	2															
$0.20 < \Phi \leq 0.25$	1															
$0.25 < \Phi$	0															
3.2 Line type : (As following drawing)  <table border="1" data-bbox="710 1433 1348 1702"> <thead> <tr> <th>Length</th> <th>Width</th> <th>Acceptable QTY</th> </tr> </thead> <tbody> <tr> <td>---</td> <td>$W \leq 0.02$</td> <td>Accept no dense</td> </tr> <tr> <td>$L \leq 3.0$</td> <td>$0.02 < W \leq 0.03$</td> <td rowspan="2">2</td> </tr> <tr> <td>$L \leq 2.5$</td> <td>$0.03 < W \leq 0.05$</td> </tr> <tr> <td>---</td> <td>$0.05 < W$</td> <td>As round type</td> </tr> </tbody> </table>	Length	Width	Acceptable QTY	---	$W \leq 0.02$	Accept no dense	$L \leq 3.0$	$0.02 < W \leq 0.03$	2	$L \leq 2.5$	$0.03 < W \leq 0.05$	---	$0.05 < W$	As round type		
Length	Width	Acceptable QTY														
---	$W \leq 0.02$	Accept no dense														
$L \leq 3.0$	$0.02 < W \leq 0.03$	2														
$L \leq 2.5$	$0.03 < W \leq 0.05$															
---	$0.05 < W$	As round type														
04	Polarizer bubbles	If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction.	<table border="1" data-bbox="837 1736 1348 2060"> <thead> <tr> <th>Size Φ</th> <th>Acceptable QTY</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.20$</td> <td>Accept no dense</td> </tr> <tr> <td>$0.20 < \Phi \leq 0.50$</td> <td>3</td> </tr> <tr> <td>$0.50 < \Phi \leq 1.00$</td> <td>2</td> </tr> <tr> <td>$1.00 < \Phi$</td> <td>0</td> </tr> <tr> <td>Total QTY</td> <td>3</td> </tr> </tbody> </table>	Size Φ	Acceptable QTY	$\Phi \leq 0.20$	Accept no dense	$0.20 < \Phi \leq 0.50$	3	$0.50 < \Phi \leq 1.00$	2	$1.00 < \Phi$	0	Total QTY	3	2.5
Size Φ	Acceptable QTY															
$\Phi \leq 0.20$	Accept no dense															
$0.20 < \Phi \leq 0.50$	3															
$0.50 < \Phi \leq 1.00$	2															
$1.00 < \Phi$	0															
Total QTY	3															

NO	Item	Criterion	AQL																		
05	Scratches	Follow NO.3 LCD black spots, white spots, contamination																			
06	Chipped glass	<p>Symbols Define: x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: LCD side length L: Electrode pad length:</p> <p>6.1 General glass chip : 6.1.1 Chip on panel surface and crack between panels:</p>  <table border="1" data-bbox="443 831 1353 1055"> <thead> <tr> <th>z: Chip thickness</th> <th>y: Chip width</th> <th>x: Chip length</th> </tr> </thead> <tbody> <tr> <td>$Z \leq 1/2t$</td> <td>Not over viewing area</td> <td>$x \leq 1/8a$</td> </tr> <tr> <td>$1/2t < z \leq 2t$</td> <td>Not exceed 1/3k</td> <td>$x \leq 1/8a$</td> </tr> </tbody> </table> <p>⊙ If there are 2 or more chips, x is total length of each chip.</p> <p>6.1.2 Corner crack:</p>  <table border="1" data-bbox="443 1507 1353 1731"> <thead> <tr> <th>z: Chip thickness</th> <th>y: Chip width</th> <th>x: Chip length</th> </tr> </thead> <tbody> <tr> <td>$Z \leq 1/2t$</td> <td>Not over viewing area</td> <td>$x \leq 1/8a$</td> </tr> <tr> <td>$1/2t < z \leq 2t$</td> <td>Not exceed 1/3k</td> <td>$x \leq 1/8a$</td> </tr> </tbody> </table> <p>⊙ If there are 2 or more chips, x is the total length of each chip.</p>	z: Chip thickness	y: Chip width	x: Chip length	$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$	$1/2t < z \leq 2t$	Not exceed 1/3k	$x \leq 1/8a$	z: Chip thickness	y: Chip width	x: Chip length	$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$	$1/2t < z \leq 2t$	Not exceed 1/3k	$x \leq 1/8a$	2.5
z: Chip thickness	y: Chip width	x: Chip length																			
$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$																			
$1/2t < z \leq 2t$	Not exceed 1/3k	$x \leq 1/8a$																			
z: Chip thickness	y: Chip width	x: Chip length																			
$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$																			
$1/2t < z \leq 2t$	Not exceed 1/3k	$x \leq 1/8a$																			

NO	Item	Criterion	AQL								
06	Glass crack	<p>Symbols :</p> <p>x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: LCD side length L: Electrode pad length</p> <p>6.2 Protrusion over terminal :</p> <p>6.2.1 Chip on electrode pad :</p> 	2.5								
		<table border="1"> <tr> <td data-bbox="352 705 655 763">y: Chip width</td> <td data-bbox="655 705 959 763">x: Chip length</td> <td data-bbox="959 705 1262 763">z: Chip thickness</td> </tr> <tr> <td data-bbox="352 763 655 824">$y \leq 0.5\text{mm}$</td> <td data-bbox="655 763 959 824">$x \leq 1/8a$</td> <td data-bbox="959 763 1262 824">$0 < z \leq t$</td> </tr> </table>		y: Chip width	x: Chip length	z: Chip thickness	$y \leq 0.5\text{mm}$	$x \leq 1/8a$	$0 < z \leq t$		
		y: Chip width		x: Chip length	z: Chip thickness						
		$y \leq 0.5\text{mm}$		$x \leq 1/8a$	$0 < z \leq t$						
<p>6.2.2 Non-conductive portion:</p> 											
<table border="1"> <tr> <td data-bbox="427 1167 715 1279">y: Chip width</td> <td data-bbox="715 1167 1002 1279">x: Chip length</td> <td data-bbox="1002 1167 1262 1279">z: Chip thickness</td> </tr> <tr> <td data-bbox="427 1279 715 1339">$y \leq L$</td> <td data-bbox="715 1279 1002 1339">$x \leq 1/8a$</td> <td data-bbox="1002 1279 1262 1339">$0 < z \leq t$</td> </tr> </table> <p>⊙ If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.</p> <p>⊙ If the product will be heat sealed by the customer, the alignment mark not be damaged.</p> <p>6.2.3 Substrate protuberance and internal crack.</p>  <table border="1"> <tr> <td data-bbox="762 1686 1018 1744">y: width</td> <td data-bbox="1018 1686 1268 1744">x: length</td> </tr> <tr> <td data-bbox="762 1744 1018 1803">$y \leq 1/3L$</td> <td data-bbox="1018 1744 1268 1803">$x \leq a$</td> </tr> </table>	y: Chip width	x: Chip length	z: Chip thickness	$y \leq L$	$x \leq 1/8a$	$0 < z \leq t$	y: width	x: length	$y \leq 1/3L$	$x \leq a$	
y: Chip width	x: Chip length	z: Chip thickness									
$y \leq L$	$x \leq 1/8a$	$0 < z \leq t$									
y: width	x: length										
$y \leq 1/3L$	$x \leq a$										

NO	Item	Criterion	AQL
07	Cracked glass	The LCD with extensive crack is not acceptable.	2.5
08	Backlight elements	8.1 Illumination source flickers when lit. 8.2 Spots or scratched that appear when lit must be judged. Using LCD spot, lines and contamination standards. 8.3 Backlight doesn't light or color wrong.	0.65 2.5 0.65
09	Bezel	9.1 Bezel may not have rust, be deformed or have fingerprints, stains or other contamination. 9.2 Bezel must comply with job specifications.	2.5 0.65
10	PCB, COB	10.1 COB seal may not have pinholes larger than 0.2mm or contamination. 10.2 COB seal surface may not have pinholes through to the IC. 10.3 The height of the COB should not exceed the height indicated in the assembly diagram. 10.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places. 10.5 No oxidation or contamination PCB terminals. 10.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts. 10.7 The jumper on the PCB should conform to the product characteristic chart. 10.8 If solder gets on bezel tab pads, LED pad, zebra pad or screw hold pad, make sure it is smoothed down.	2.5 2.5 0.65 2.5 2.5 0.65 2.5
11	Soldering	11.1 No un-melted solder paste may be present on the PCB. 11.2 No cold solder joints, missing solder connections, oxidation or icicle. 11.3 No residue or solder balls on PCB. 11.4 No short circuits in components on PCB.	2.5 2.5 2.5 0.65

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NO	Item	Criterion	AQL
12	General appearance	12.1 No oxidation, contamination, curves or, bends on interface Pin (OLB) of TCP.	2.5
		12.2 No cracks on interface pin (OLB) of TCP.	0.65
		12.3 No contamination, solder residue or solder balls on product.	2.5
		12.4 The IC on the TCP may not be damaged, circuits.	2.5
		12.5 The uppermost edge of the protective strip on the interface pin must be present or look as if it cause the interface pin to sever.	2.5
		12.6 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color.	0.65
		12.7 Sealant on top of the ITO circuit has not hardened.	0.65
		12.8 Pin type must match type in specification sheet.	0.65
		12.9 LCD pin loose or missing pins.	0.65
		12.10 Product packaging must the same as specified on packaging specification sheet.	0.65
		12.11 Product dimension and structure must conform to product specification sheet.	0.65



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IRVINE, CALIFORNIA 92614-5915

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SCA05735-BFN-LNC

Sales signature : _____

Customer Signature : _____

Date : / / _____