



Features

- Built-in PHY supporting SGMII Interface
- Built-in high performance MCU supporting easier configuration
- Dual data-rate of 100BASE-FX/1000BASE-LX operation
- 1310nm FP laser and PIN photo-detector
- Up to 2km transmission with MMF at 125Mbps
- Up to 550m transmission with MMF at 1.25Gbps
- Standard serial ID information Compatible with SFP MSA
- SFP MSA package with duplex LC connector
- With Spring-Latch for high density application
- +3.3V single power supply
- Operating case temperature: -40 to +85°C
 Commercial temperature: -5 to +70°C

Regulatory Compliance

Table 1 - Regulatory Compliance

Feature	Standard	Performance	
Electrostatic Discharge	MIL-STD-883E	Class 1	
(ESD) to the Electrical Pins	Method 3015.7	Class I	
Electrostatic Discharge (ESD) to the	IEC 61000-4-2	Compliant with standards	
Duplex LC Receptacle	120 01000-4-2	Compilant with standards	
Electromagnetic	FCC Part 15 Class B	Compliant with standards	
Interference (EMI)	T CC F art 13 Class B	Compliant with standards	
Lagor Evo Safoty	FDA 21CFR 1040.10 and 1040.11	Compliant with Class I laser	
Laser Eye Safety	EN (IEC) 60825-1,2	product.	
RoHS	2011/65/EU	Compliant with RoHS	

Absolute Maximum Ratings

Table 2 - Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Storage Temperature	Ts	-40	-	+85	°C	
Supply Voltage	V _{CC}	-0.5	-	+3.6	V	
Operating Relative Humidity	RH	5	-	+95	%	



Recommended Operating Conditions

Table 3 – Recommended Operating Conditions

Parameter		Symbol	Min.	Typical	Max.	Unit	Notes	
Operating Case	C-temp	T _C	-5	-	+70	°C		
Temperature	I-temp	ı C	-40		+85	°C		
Power Supply Vol	Power Supply Voltage		3.13	3.3	3.47	V		
Power Supply Cur	rent	I _{CC}	-	-	350	mA	1	
Power Dissipation		P _D	-	-	1.5	W		
Date Rate	1000BASE-LX			1250		Mbps		
	100BASE-FX			125		ivibps		

Note 1: The max power supply current after module work stable.

Optical Characteristics

Table 4 – Optical Characteristics

Transmitter										
Parar	neter	Symbol	Min.	Typical	Max.	Unit	Notes			
Centre Waveleng	ıth	λ _C	1260	1310	1360	nm				
Average Output	1000BASE-LX	P _{0ut}	-11.5		-3	dBm	1			
Power	100BASE-FX	P _{0ut}	-20		-14	UDIII	1			
P _{0ut} @TX Disable	Asserted	P _{0ut}			-45	dBm	1			
Spectral Width	1000BASE-LX	_			4	nm				
(RMS)	100BASE-FX	σ			7.7	11111				
Extinction Ratio		EX	9			dB				
Rise/Fall Time	1000BASE-LX	+ /+			0.26	no	2			
(20%~80%)	100BASE-FX	t _r /t _f			3	ns	2			
Total Jitterat	1000BASE-LX	J_{T}			0.481		3			
TP2	100BASE-FX	JŢ			0.4	UI	3			
Deterministic	1000BASE-LX	- J _D			0.250	Oi	3			
Jitter at TP2	100BASE-FX	JD			0.305		3			
Output Optical E	ye	Compatible	with IEEE 80	2.3ah-2004			4			
			Receiver							
Centre Waveleng	Centre Wavelength		1260	1310	1570	nm				
Receiver	1000BASE-LX				-22	dBm	5			
Sensitivity	100BASE-FX				-28	ubili	6			
Receiver	1000BASE-LX		-3			dBm	5			



Overload	100BASE-FX		-8			6
Return Loss			12		dB	
LOS De-Assert	1000BASE-LX	LOS _D		-23	dBm	
LOS De-Assert	100BASE-FX	LOSD		-23	иын	
LOS Assert	1000BASE-LX	108	-45		dBm	
LOS Assert	100BASE-FX	LOS _A	-45		UDIII	
LOS Hysteresis			0.5	4.5	dB	
Total Jitter at	SGMII	1		0.749	UI	3
TP4	SGIVIII	J_T		0.748	Oi	3
Deterministic	SGMII	I_		0.462	UI	
Jitter at TP4	JOINIII	J_{D}		0.402	OI	

Notes:

- 1. The optical power is launched into 62.5/125um SMF.
- 2. Unfiltered, measured with 8B/10B code for 1.25Gbps and 4B/5B code for 125Mbps
- 3. Meet the specified maximum output jitter requirements if the specified maximum input jitter is present.
- 4. Measured with 8B/10B code for 1.25Gbps and 4B/5B code for 125Mbps.
- 5. Measured with 8B/10B code for 1.25Gbps, worst-case extinction ratio, and BER ≤1 × 10⁻¹².
- 6. Measured with 4B/5B code for 125Mbps, worst-case extinction ratio, and BER \leq 1 × 10⁻¹².

Electrical Characteristics

Table 5 – Electrical Characteristics

Transmitter										
Para	meter	Symbol	Min.	Typical	Max.	Unit	Notes			
Data Input Sv (SGMII Series in	wing Differential terface)	V_{IN}	200		2100	mV	1			
Input Differential	Impedance	Z _{IN}	80	100	120	Ω				
TX Disable	Disable		2.0		Vcc	V				
	Enable		Vee		Vee+0.8					
TX Fault	Fault		2.0		Vcc	V				
.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	Normal		Vee		Vee+0.5	•				
			Receiver							
·	Data Output Swing Differential (SGMII Series Interface)		370		2000	mV	1			
LOS	High		2.0		Vcc+0.3	V				
	Low		Vee		Vee+0.5					

Notes:

1. PECL logic, internally AC coupled.



Recommended Host Board Power Supply Circuit

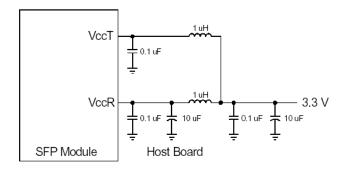


Figure 1, Recommended Host Board Power Supply Circuit

Recommended Interface Circuit

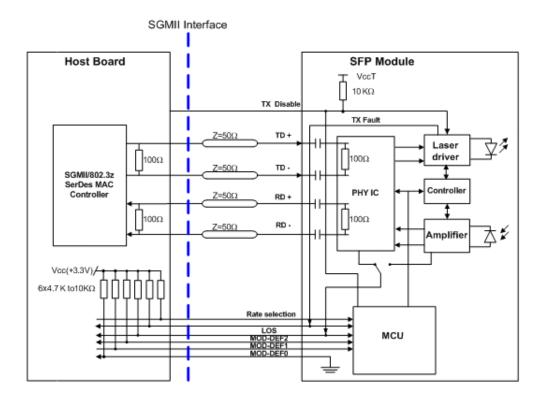


Figure 2, Recommended Interface Circuit



Pin Definitions

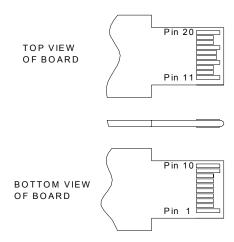


Figure 3, Pin View

Table 6-Pin Function Definitions

Pin No.	Name	Function	Plug Seq.	Notes
1	VeeT	Transmitter Ground	1	
2	TX Fault	Transmitter Fault Indication	3	Note 1
3	TX Disable	Transmitter Disable	3	Note 2
4	MOD-DEF2	Module Definition 2	3	Note 3
5	MOD-DEF1	Module Definition 1	3	Note 3
6	MOD-DEF0	Module Definition 0	3	Note 3
7	Rate Select	Not Use	3	
8	LOS	Loss of Signal	3	Note 4
9	VeeR	Receiver Ground	1	
10	VeeR	Receiver Ground	1	
11	VeeR	Receiver Ground	1	
12	RD-	Inv. Received Data Out	3	Note 5
13	RD+	Received Data Out	3	Note 5
14	VeeR	Receiver Ground	1	
15	VccR	Receiver Power	2	
16	VccT	Transmitter Power	2	
17	VeeT	Transmitter Ground	1	
18	TD+	Transmit Data In	3	Note 6
19	TD-	Inv. Transmit Data In	3	Note 6
20	VeeT	Transmitter Ground	1	

Notes:

- 1. TX Fault is an open collector output, which should be pulled up with a $4.7k\sim10k\Omega$ resistor on the host board to a voltage between 2.0V and Vcc+0.3V. Logic 0 indicates normal operation; logic 1 indicates a laser fault of some kind. In the low state, the output will be pulled to less than 0.8V.
- 2. TX Disable is an input that is used to shut down the transmitter optical output. It is pulled up within the



module with a $4.7k\sim10k\Omega$ resistor. Its states are: Low (0~0.8V): Transmitter on

(>0.8V, <2.0V): Undefined

High (2.0~3.465V): Transmitter Disabled Open: Transmitter Disabled

3. MOD-DEF 0,1,2 are the module definition pins. They should be pulled up with a $4.7k\sim10k\Omega$ resistor on the host board. The pull-up voltage shall be VccT or VccR.

MOD-DEF 0 is grounded by the module to indicate that the module is present

MOD-DEF 1 is the clock line of two wire serial interface for serial ID

MOD-DEF 2 is the data line of two wire serial interface for serial ID

- 4. LOS is an open collector output, which should be pulled up with a 4.7k~10kΩ resistor on the host board to a voltage between 2.0V and Vcc+0.3V. Logic 0 indicates normal operation; logic 1 indicates loss of signa or link down with partner I. In the low state, the output will be pulled to less than 0.8V.
- 5. These are the differential receiver output. They are internally AC-coupled 100Ω differential lines which should be terminated with 100Ω (differential) at host with SGMII interface.
- 6. These are the differential transmitter inputs. They are AC-coupled, differential lines with 100Ω differential termination inside the module.

EEPROM Information

The SFP MSA defines a 256-byte memory map in EEPROM describing the transceiver's capabilities, standard interfaces, manufacturer, and other information, which is accessible over a 2 wire serial interface at the 8-bit address 1010000X (A0h). The memory contents refer to Table 7.

Table 7 – EEPROM Serial ID Memory Contents (A0h)

Addr.	Field Size (Bytes)	Name of Field	Hex	Description			
0	1	Identifier	03	SFP			
1	1	Ext. Identifier	04	MOD4			
2	1	Connector	07	LC			
3—10	8	Transceiver	00 00 00 22 00 00 00 00				
11	1	Encoding	01	8B10B			
12	1	BR, nominal	0D	1.25Gb/s			
13	1	Reserved	00				
14	1	Length (9um)-km	00				
15	1	Length (9um)m	00				
16	1	Length (50um)	37	550m			
17	1	Length (62.5um)	37	550m			
18	1	Length (copper)	00				
19	1	Reserved	00				
20—35	16	Vendor name	53 4F 55 52 43 45 50 48 4F 54 4F 4E 49 43 53 20	"SOURCEPHOTONICS "(ASC II)			



36	1	Reserved	00	
37—39	3	Vendor OUI	00 1F 22	
40—55	16	Vendor PN	53 50 47 44 52 46 58 xx	"CDCDDEVyDEC" (ACCII)
40—55	10	vendor Pin	44 46 43 20 20 20 20 20	"SPGDRFXxDFC" (ASC [])
56—59	4	Vendor rev	31 30 20 20	ASC II ("31 30 20 20" means 1.0 revision)
60-61	2	Wavelength	05 1E	1310nm
62	1	Reserved	00	
63	1	CC BASE	xx	Check sum of bytes 0 - 62
64—65	2	Options	00 1A	LOS, TX_FAULT and TX_DISABLE
66	1	BR, max	00	
67	1	BR, min	00	
68—83	16	Vendor SN	xx xx xx xx xx xx xx xx	ASC II .
00—03	10		xx xx xx xx xx xx xx xx	AGO II .
84—91	8	Vendor date code	xx xx xx xx xx xx xx xx	Year (2 bytes), Month (2 bytes), Day (2 bytes)
92	1	Diagnostic type	68	Diagnostics(Int.Cal)
				Diagnostics(Optional Alarm/warning flags,
93	1	Enhanced option		Soft TX_FAULT and Soft TX_LOS
			В0	monitoring)
94	1	SFF-8472	02	Diagnostics(SFF-8472 Rev 9.4)
95	1	CC_EXT	xx	Check sum of bytes 64 - 94
96-255	160	Vendor specific		

Note: The "xx" byte should be filled in according to practical case. For more information, please refer to the related document of SFF-8472 Rev 9.5.

Recommended Software configuration

How to configure auto-negotiation, loopback, work speed

The module can support auto-negotiation, loopback configuration.

Please refer the following steps to configure:

Step 1: Access the module at 0xA2 via two-wire serial interface.

Step 2: Configure 0x6Dh/6Eh (Byte 109~110) as below table. Addr.109 default is "1Fh". Addr.110 default is "00h".

Addr. 109	Function	"1"	"0"	Default Value
				(BIN)
bit7	FEFI Status	FEFI condition detected	FEFI condition not	' 0'
			detected	
bit6	Fiber	Disable	Enable	·O'
	Auto-Negotiation			
Bit5	MAC	Disable	Enable	'0'
	Auto-Negotiation			
bit4	FEFI function	Disable	Enable	'1'



bit3	CRC checker	Disable/Reset	Enable	'1'
bit2	Fiber loop back	Disable	Enable	'1'
bit1	MAC loop back	Disable	Enable	'1'
bit0	Reserved	Reserved	Reserved	'1'

Addr. 110	Function	"1"	"0"	Default Value
				(BIN)
bit7	TX Disable State	TX-Disable	TX-Enable	'0'
bit6	TX-Disable	TX-Disable	TX-Enable	'0'
Bit5~Bit4	Reserved	Reserved	Reserved	' 0'
Bit3	Work speed mode	1000Base	100Base	'0'
Bit2	TX fault output	TX fault indication	No fault	'0'
	status			
Bit1	LOS pin output	LOS asserted	LOS de-asserted	'0'
	status	(Link down)	(Link up)	
Bit0	Data Ready status	Not ready	Ready	'0'

Monitoring Specification

The digital diagnostic monitoring interface also defines another 256-byte memory map in EEPROM, which makes use of the 8 bit address 1010001X (A2h). Please see Figure 4. For detail EEPROM information, please refer to the related document of SFF-8472 Rev 9.5. The monitoring specification of this product is described in Table 8.

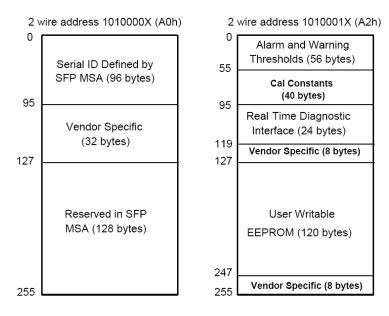


Figure 4, EEPROM Memory Map Specific Data Field Descriptions



Table 8- Monitoring Specification

Parameter		Range	Accuracy	Calibration
Temperature	I-temp	-40 to 95°C	±3°C	Internal
remperature	C-temp	-10 to 80°C	±3°C	Internal
Volt	age	2.97 to 3.63V	±3%	Internal
Bias Current		3 to 80mA	±10%	Internal
TX Power(10	000Base-LX)	-11.5 to -3 dBm	±3dB	Internal
TX Power(1	00Base-FX)	-20 to -14 dBm	±3dB	Internal
RX Power(10	000Base-LX)	-26 to -3 dBm	±3dB	Internal
RX Power(1	00Base-FX)	-32 to -8 dBm	±3dB	Internal

Mechanical Diagram

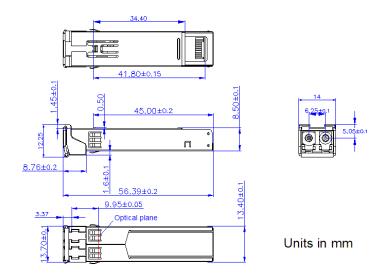


Figure 4, Mechanical Diagram of SFP

Order Information

Table 9 - Order Information

Part No.	Media	Data Rate(Mbps)	Transmission Distance	Temperature
SPG-DR-FX-IDFC	MMF	125/1250	2km/550m	-40~+85°C
SPG-DR-FX-CDFC	MMF	125/1250	2km/550m	-5~+70°C

Warnings

Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD).



A static free environment is highly recommended. Follow guidelines according to proper ESD procedures. **Laser Safety:** Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.

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