



Features

- Compliant with CSFP MSA 2.0 (Option 2)
 - Burst receive GPON OLT transceiver
 - Small Form Factor Pluggable, Duplex LC Connector
 - "Fast Signal Detect" feature reduces ranging overhead
 - Simplified OLT "reset" timing
 - 1490 nm DFB Tx with isolator
 - 1310 nm APD Rx
 - 2488 Mbps downstream Tx/1244 Mbps upstream Rx
 - Single 3.3 V supply
 - ITU-T G.984.2 compliant
 - 20 km reach; 28 dB link budget
- Operating case temperature: -5~70°C
- RoHS compliant (lead exemption)

General Parameters

Parameter	Minimum	Typical	Maximum	Unit/Conditions
Operating Voltage, Vcc	3.135	3.3	3.465	V
Total Current, Icc	-	-	800	mA
Case Operating Temperature	-5	-	70	°C
Storage Temperature	-40	-	85	°C

Parameter	Minimum	Typical	Maximum	Unit/Conditions
Back Reflection at 1490 nm	-	-	-20	dB
Back Reflection at 1310 nm	-	-	-20	dB
1490 nm to 1310 nm Crosstalk	-	-	-45	dB

Functional Characteristics

The following tables list the performance specifications for the various functional blocks of the integrated optical transceiver module.

Parameter	Minimum	Typical	Maximum	Unit	Notes
Average Optical Output Power, P_O	1.5	-	5	dBm	
Output Power at Transmit Off	-	-	-40	dBm	
Extinction Ratio	8.2	-	-	dB	PRBS 2 ²³ -1, NRZ, 50% duty cycle
Transmitter Output Eye	G.984.2 Figure 2				
Optical Rise and Fall Time	-	-	160	ps	20% to 80%
Center Wavelength, λ	1480	1490	1500	nm	
-20 dB Spectral Width	-	-	1	nm	
Side Mode Suppression Ratio (SMSR)	30	-	-	dB	
Bit Rate	-	2488	-	Mbps	
Tolerance to TX Back Reflection ^a	-15	-	-	dB	

a) 1 dB degradation of Rx sensitivity

Parameter	Minimum	Typical	Maximum	Unit	Notes
Input Differential Impedance	80	100	120	Ω	
Single Ended Data Input Swing	-	750	-	mV	
Tx Disable (LVTTL)	2	-	V _{cc}	V	
Tx Enable (LVTTL)	0	-	0.8	V	
TX_Fail_High	2.4	-	V _{cc}	V	
TX_Fail_Normal	0	-	0.4	V	

Parameter	Minimum	Typical	Maximum	Unit	Notes
Operational Wavelength Range	1260	1310	1360	nm	
Data Rate (burst mode)	-	1244	-	Mbps	
Receiver Burst-Mode Sensitivity	-	-	-28	dBm	At 10 ⁻¹⁰ BER, PRBS 2 ²³ -1
Receiver Overload	-8	-	-	dBm	
Burst Detect Assert	-	-	-28	dBm	
Receiver Burst Mode Dynamic Range	15	-	-	dB	Input power difference between two subsequent high and low burst data
Damage Threshold for Receiver	+3	-	-	dBm	
Maximum Reflectance of Receiver	-	-	-20	dB	

Table 6 – Receiver Specifications (Electrical)

Parameter	Minimum	Typical	Maximum	Unit	Notes
PECL Single Ended Data Output Swing (LVPECL)	-	750	-	mV	
Data Output Rise Time	-	-	300	ps	20% to 80%
Data Output Fall Time	-	-	300	ps	20% to 80%
Signal Detect Output HIGH	2.4	-	V _{cc}	V	
Signal Detect Output LOW ^a	0	-	0.4	V	
Signal Detect Assert Time	-	-	100	ns	
Signal Detect De-Assert Time	-	-	12.8	ns	

a) Signal Detect assert low when module receive “reset” signal, assert high when incoming burst is detected and latch to high state until next “Reset” signal.

Table 7 – Digital RSSI Timing Specification

Parameter	Minimum	Typical	Maximum	Unit	Notes
RSSI Trigger Delay ^a	25	-	-	ns	
RSSI Sampling Time ^a	300	-	-	ns	
Internal I ² C Delay ^a	-	-	500	us	
Receiver Power DDM (RSSI) Error ^b	-	-	+/- 3	dB	

a) RSSI_ACQ input signal rising edge will trigger RSSI sampling, and falling edge will trigger internal digital RSSI information written to I2C. It is recommended that host shall not trigger RSSI_ACQ input again until RSSI data is valid in I2C from previous RSSI trigger.

b) RSSI DDM working range is between -8 to -28 dBm. RSSI DDM accuracy is better than +/- 3dB for input power levels between -10 to -28 dBm under over temp, the accuracy reduces to +/- 2 dB for input power level larger between -8 to 10dBm under room temp.

Timing Diagram

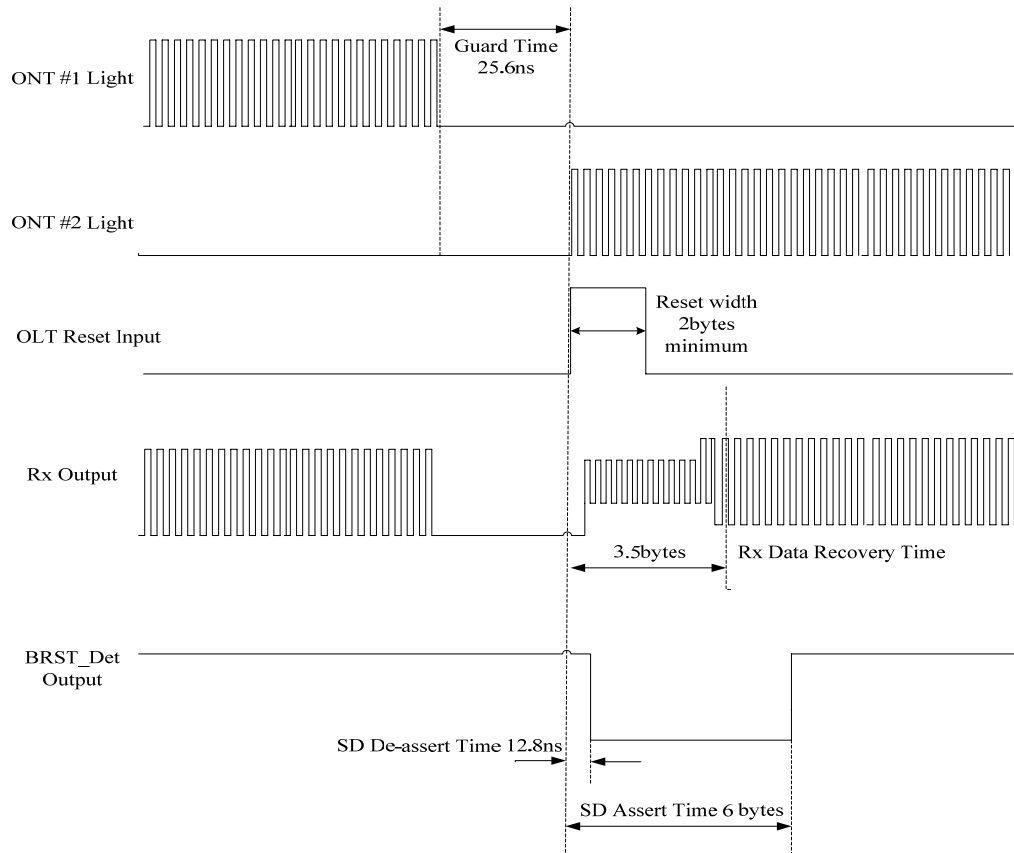


Figure 1. Timing Diagram

Digital RSSI Acquire/Hold Timing Specification

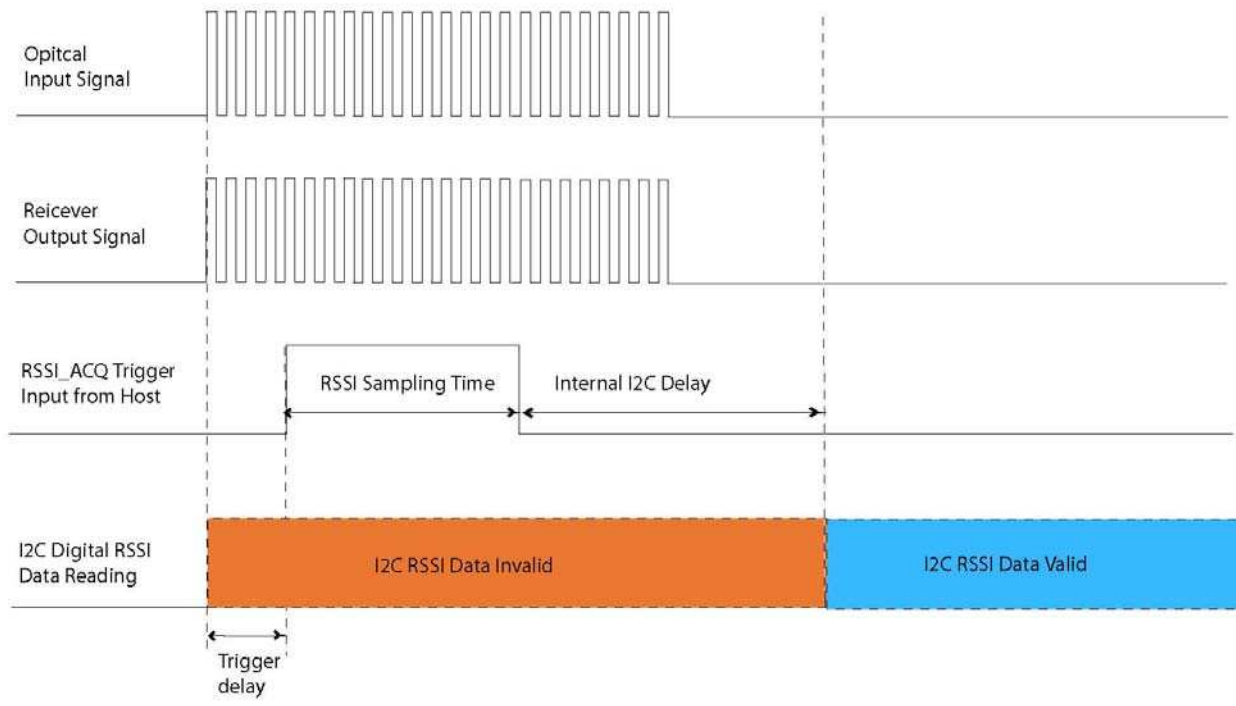


Figure 2. Digital RSSI Timing.

Pin Definitions

Refer to Table-8 for a description of the function of each I/O pin.

Pin Number	Label	Definition
1	Veet	Tx Ground
2	RX_SD2	Receiver Data Output of Ch2
3	Reset2	Reset of Ch2
4	SDA	2-Wire Serial Data I/O Pin. Transfers serial data to and from device
5	SCL	2-Wire Serial Clock Input. Clocks data into and out of the device.
6	RSSI_Trig2	RSSI Trigger Ch2
7	Reset1	Reset of Ch1
8	RX_SD1	Receiver Data Output of Ch1
9	RSSI_Trig1	RSSI_Trigger Ch1
10	TXD2+	Transmit Data Input of Ch2
11	TXD2-	Invert Transmit Data Input of Ch2
12	RXD1-	Inverted Receiver Data Output of Ch1
13	RXD1+	Receiver Data Output Ch1
14	RXD2-	Inverted Receiver Data Output of Ch2
15	Vcc_Rx	Rx Vcc
16	Vcc_Tx	Tx Vcc
17	RXD2+	Receiver Data Output Ch2
18	TXD1+	Transmit Data Input of Ch1
19	TX1D-	Invert Transmit Data Input of Ch1
20	Veet	Tx Ground

EEPROM Information

Table 9 – EEPROM Content (A0h/B0h)

I2C A0h/B0h Address					
DEC Addr.	HEX Addr.	Field Size (bytes)	Name	Default Value	Description
0	00	1	Identifier	03h	SFP transceiver
1	01	1	Extended Identifier	04h	mod4
2	02	1	Connector	07h	LC
3	03	8	Transceiver	11 13 00 00 00 00 00 08h	BASE-PX
11	0B	1	Encoding	03h	NRZ
12	0C	1	Nominal Bit Rate in 100 MBps	19h	2488.32Mbps
13	0D	1	Reserved	00h	Reserved
14	0E	1	Length (9μ, km) in km	14h	20km
15	0F	1	Length (9μ, m) in 100 m	C8h	20km
16	10	1	Length (50μ) in 10 m	00h	Not Supported
17	11	1	Length (62.5μ) in 10 m	00h	Not Supported
18	12	1	Length (Copper) in m	00h	Not Supported
19	13	1	Reserved	00h	Reserved
20	14	16	Vendor Name (ASCII)	"SOURCE PHOTONICS"	Vendor Name (ASCII)
36	24	1	Reserved	00h	Reserved
37	25	3	Vender IEEE Company ID	00 1F 22h	vendor IEEE ID
40	28	16	Vendor Part Number (ASCII)	"SPLC-43-48H-HP-CDE"	Vendor Part Number (ASCII)
56	38	4	Vendor Rev (ASCII)	30 31 20 20	Revision
60	3C	2	Laser Wavelength in nm	05 D2h	1490nm Tx Wavelength
62	3E	1	Reserved	00h	Reserved
63	3F	1	Check Code for Base ID Fields	xxh	Checksum from byte 0-62
64	40	2	Options	00 1Ch	SD, TX_Fault, TX_DIS
66	42	1	Upper Bit Rate Margin in %	00h	BR, Max not specified
67	43	1	Lower Bit Rate Margin in %	00h	BR, Min not specified
68	44	16	Vendor Serial Number (ASCII)	"xxxxxxxxxxxxxxxx"	16 byte Serial number field (ASCII)

84	54	8	Date Code	xx xx xx xx xx xx 20 20h	Year(2 bytes) month(2 bytes) day(2 bytes)
92	5C	1	Diagnostic Monitoring Type	58	External Calibration, Average Power Measurement
93	5D	1	Enhanced Options	E0h	Optical Alarm/warning implemented Soft TX_DIS, TX_FAULT implemented
94	5E	1	SFF-8472 Compliance	02h	Compliance to SFF-8472
95	5F	1	Check Code for Extended ID Fields	xxh	Checksum from byte 64-69
96	60	30	Vendor Specific		
126	7E	2	Vendor Specific		
128	80	128	Reserved		

Note: The "xx" byte should be filled in according to practical case. For more information, please refer to the related document of SFF-8472 Rev 9.5.

Table 10 – EEPROM Content (A2h/B2h)

I2C A2h/B2h Address

DEC Addr.	HEX Addr.	Field Size (bytes)	Name	Default Value	Description
0	00	2	Temp High Alarm	50 00h	80°C
2	02	2	Temp Low Alarm	F3 00h	-13°C
4	04	2	Temp High Warning	4B 00h	75°C
6	06	2	Temp Low Warning	F8 00h	-8°C
8	08	2	Voltage High Alarm	8C A0h	3.6V
10	0A	2	Voltage Low Alarm	75 30h	3V
12	0C	2	Voltage High Warning	88 B8h	3.5V
14	0E	2	Voltage Low Warning	79 18h	3.1V
16	10	2	Bias High Alarm	B9 8Ch	95mA
18	12	2	Bias Low Alarm	03 E8h	2mA
20	14	2	Bias High Warning	A6 04h	85mA
22	16	2	Bias Low Warning	09 C4h	5mA
24	18	2	TX Power High Alarm	8A 99h	5.5dBm
26	1A	2	TX Power Low Alarm	2B D4h	0.5dBm
28	1C	2	TX Power High Warning	7B 86h	5dBm
30	1E	2	TX Power Low Warning	31 2Dh	1dBm

32	20	2	RX Power High Alarm	1F 2Dh	-7dBm
34	22	2	RX Power Low Alarm	00 28h	-30 dBm
36	24	2	RX Power High Warning	18 C3h	-8 dBm
38	26	2	RX Power Low Warning	00 32h	-29 dBm
40	28	16	Reserved	00....000h	Reserved
56	38	4	RX_PWR(4) Calibration	00 00 00 00h	4th order RSSI calibration coefficient
60	3C	4	RX_PWR(3) Calibration	00 00 00 00h	3rd order RSSI calibration coefficient
64	40	4	RX_PWR(2) Calibration	00 00 00 00h	2nd order RSSI calibration coefficient
68	44	4	RX_PWR(1) Calibration	3E 80 00 00h	1st order RSSI calibration coefficient
72	48	4	RX_PWR(0) Calibration	00 00 00 00h	0th order RSSI calibration coefficient
76	4C	2	TX_I(Slope) Calibration	01 00h	Slope for Bias calibration
78	4E	2	TX_I(Offset) Calibration	00 00h	Offset for Bias calibration
80	50	2	TX_PWR(Slope) Calibration	01 00h	Slope for TX Power calibration
82	52	2	TX_PWR(Offset) Calibration	00 00h	Offset for TX Power calibration
84	54	2	T(Slope) Calibration	01 00h	Slope for Temperature calibration
86	56	2	T(Offset) Calibration	00 00h	Offset for Temperature calibration, in units of 256ths C
88	58	2	V(Slope) Calibration	01 00h	Slope for VCC calibration
90	5A	2	V(Offset) Calibration	00 00h	Offset for VCC calibration
92	5C	3	Reserved	00h	reserved
95	5F	1	Checksum	xxh	Checksum
96	60	2	Transceiver Temperature	xx xxh	Temperature in C/256
98	62	2	Supply Voltage	xx xxh	Vcc
100	64	2	TX Bias Current	xx xxh	BIASMON
102	66	2	TX Optical Output Power	xx xxh	Back facet monitor
104	68	2	RX Optical Input Power	xx xxh	RSSI
106	6A	2	Reserved	0000h	Reserved
108	6C	2	Reserved	0000h	Reserved
110	6E.7	1bit	TX_DIS State	x	Digital state of the TX Disable Input Pin.
	6E.6	1bit	Soft TX Disable	x	Read/write bit that allows software disable of laser.
	6E.5	1bit	Reserved.	0	Reserved.
	6E.4	1bit	Rate Select State	0	NOT SUPPORTED.
	6E.3	1bit	Rate Select	0	NOT SUPPORTED.
	6E.2	1bit	TX_FAULT	x	Digital state of the TX Fault Output Pin.

	6E.1	1bit	LOS	0	Digital state of the LOS Output Pin. NOT SUPPORTED
	6E.0	1bit	Data_ready_bar	x	Indicates transceiver has achieved power up and data is ready.
111	6F.7	1bit	Reserved	0	Reserved
	6F.6	1bit	Reserved	0	Reserved
	6F.5	1bit	Reserved	0	Reserved
	6F.4	1bit	Reserved	0	Reserved
	6F.3	1bit	Reserved	0	Reserved
	6F.2	1bit	INTERRUPT_NOT	x	Interrupt state (active low)
	6F.1	1bit	MODE_EN	0	TX FAULT pin enable
	6F.0	1bit	APD_SHUTDOWN	x	APD shut-down latch. Write 0 to clear condition
112	70.7	1bit	Temperature too high alarm	x	Temperature too high alarm
	70.6	1bit	Temperature too low alarm	x	Temperature too low alarm
	70.5	1bit	VCC too high alarm	x	VCC too high alarm
	70.4	1bit	VCC too low alarm	x	VCC too low alarm
	70.3	1bit	BIASMON too high alarm	x	BIASMON too high alarm
	70.2	1bit	BIASMON too low alarm	x	BIASMON too low alarm
	70.1	1bit	BFMON too high alarm	x	BFMON too high alarm
	70	1bit	BFMON too low alarm	x	BFMON too low alarm
113	71.7	1bit	RSSI too high alarm	x	RSSI too high alarm
	71.6	1bit	RSSI too low alarm	x	RSSI too low alarm
	71.5	1bit	Reserved interrupt status bit	x	Reserved interrupt status bit
	71.4	1bit	Reserved interrupt status bit	x	Reserved interrupt status bit
	71.3	1bit	Reserved interrupt status bit	x	Reserved interrupt status bit
	71.2	1bit	Reserved interrupt status bit	x	Reserved interrupt status bit
	71.1	1bit	Reserved interrupt status bit	x	TX Fail went HIGH
	71	1bit	Reserved interrupt status bit	x	APD Shutdown event detected
114	72	1	Reserved	00h	Interrupt Mask for ISRC0

115	73	1	Reserved	00h	Interrupt Mask for ISRC1
116	74.7	1bit	Temperature too high warning	x	Temperature too high warning
	74.6	1bit	Temperature too low warning	x	Temperature too low warning
	74.5	1bit	VCC too high warning	x	VCC too high warning
	74.4	1bit	VCC too low warning	x	VCC too low warning
	74.3	1bit	BIASMON too high warning	x	BIASMON too high warning
	74.2	1bit	BIASMON too low warning	x	BIASMON too low warning
	74.1	1bit	BFMON too high warning	x	BFMON too high warning
	74	1bit	BFMON too low warning	x	BFMON too low warning
117	75.7	1bit	RX Power High Warning	x	RSSI too high warning
	75.6	1bit	RX Power Low Warning	x	RSSI too low warning
	75.5	1bit	Reserved	0	Reserved
	75.4	1bit	Reserved	0	Reserved
	75.3	1bit	Reserved	0	Reserved
	75.2	1bit	Reserved	0	Reserved
	75.1	1bit	Reserved	0	Reserved
	75	1bit	Reserved	0	Reserved
118	76	1	Reserved	00h	Interrupt Mask for ISRC2
119	77	1	Reserved	00h	Interrupt Mask for ISRC3
120	78	8	Vendor Specific	00 00 00 00 00 00 00 00h	Vendor Specific

Table 11 – Digital Diagnostic Specification (A2h for channel 1, B2h for channel 2)

Data Address	Parameter	Range	Accuracy
96-97	Temperature	0 to +70°C	±3°C
98-99	Vcc Voltage	+3.0V to +3.6V	±3%
100-101	Bias Current	0 to 100mA	±10%
102-103	TX Power	0 to 6dBm	±2dB
104-105	RX Power	-28 to -8dBm	±3dB

Mechanical Diagram

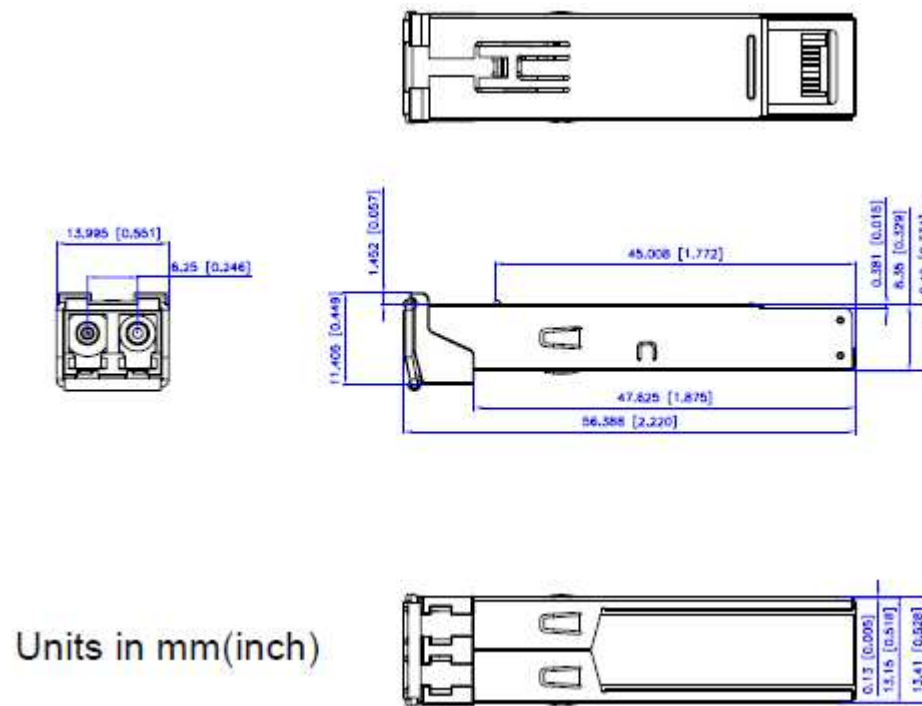


Figure 3. Mechanical Diagram.

Table 12 - Device Handling/ESD Protection

The devices are static sensitive and may easily be damaged if care is not taken during handling. The following handling practices are recommended.

1	Devices should be handled on benches with conductive and grounding surfaces.
2	All personnel, test equipment and tools shall be grounded.
3	Do not handle the devices by their leads.
4	Store devices in protective foam or carriers.
5	Avoid the use of non-conductive plastics, rubber, or silk in the area where the devices are handled
6	All modules shall be packaged in materials that are anti-static to protect against adverse electrical environments.
7	Avoid applications of any voltage higher than maximum rated voltages to this part. For proper operation, any VIN or VOUT should be constrained to the range $GND \leq (VIN \text{ or } VOUT) \leq VCC$. Unused inputs must always be tied to an appropriate logic voltage (e.g. either GND or VCC). Unused outputs must be left open.

Warnings

Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Laser Safety: Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.

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