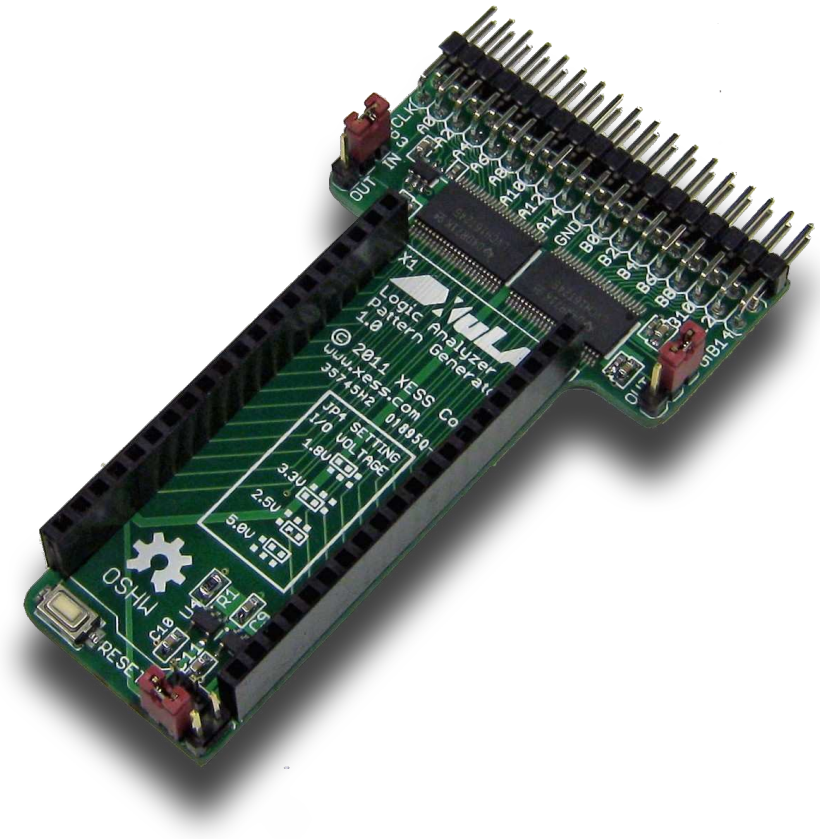
XESS Corporation

Logic Pod Manual

How to install and use your new Logic Pod Module



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Logic Pod Manual
MAN??? (V0.1) October 24, 2013

The following table shows the revision history for this document.

Date	Version	Revision
10/24/2013	0.1	Preliminary release for Logic Pod module V1.0.

Table of Contents

C.1 Preliminaries

Here's some helpful information before getting started.

Getting Help!

Here are some places to get help if you encounter problems:

- If you can't get the Logic Pod module to work, send an e-mail message describing your problem to help@xess.com or submit a problem report at http://www.xess.com/help.php.
- Our web site also has
  - answers to frequently-asked-questions,
  - example designs, application notes and tutorials,
  - a forum where you can post questions.

Take Notice!

It's pretty hard to get in trouble with this module. Just don't insert the XuLA or XuLA2 board backwards; the USB connector should be facing away from the Logic Pod I/O header.

Packing List

Here is what you should have received in your package:

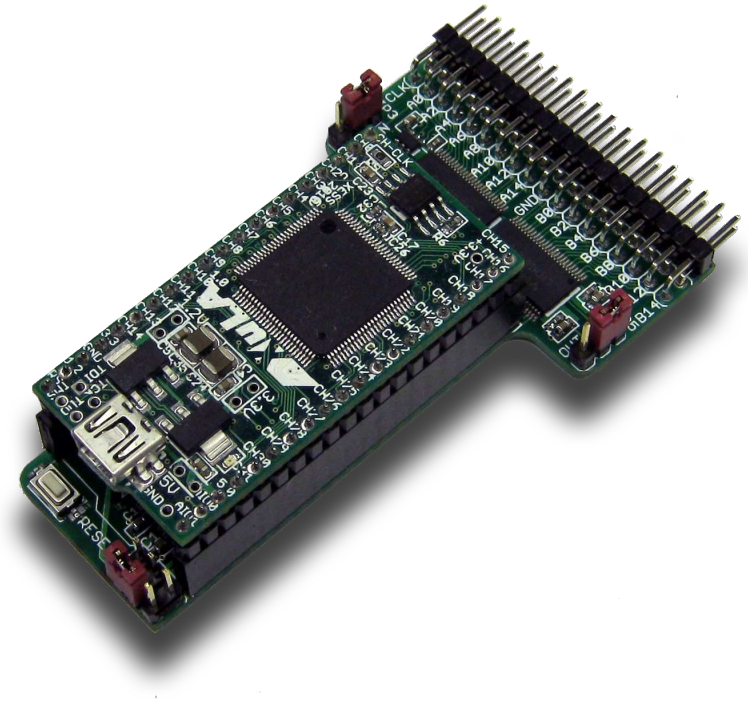
- a Logic Pod module.

C.2 Setup

The Logic Pod module provides an eight-position DIP switch that connects to an eight-bit PMOD or a Wing socket on your StickIt! board.

Inserting Your XuLA/XuLA2 into Your Logic Pod Module

To use the Logic Pod module, insert a XuLA or XuLA2 board as shown below. (**To insure a stable connection, only use headers on the XuLA/XuLA2 with 0.025" square pins.**)

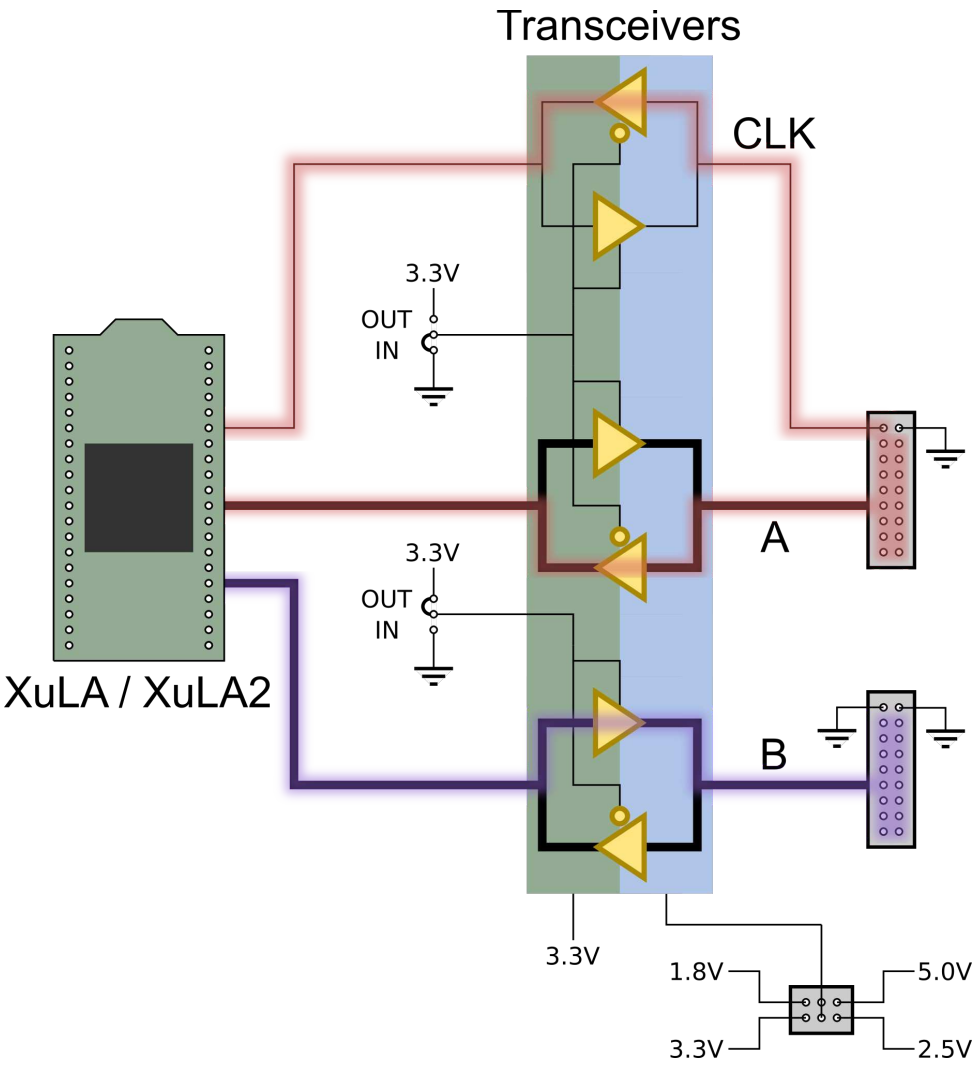


Setting the Jumpers

Jumper	Function
JP3	Setting this jumper to the OUT position lets the FPGA drive signals onto the 16-bit A and CLK header pins. Setting it to IN lets the FPGA receive signals driven through the A and CLK header pins by an external source.
JP5	Setting this jumper to the OUT position lets the FPGA drive signals onto the 16-bit B header pins. Setting it to IN lets the FPGA receive signals driven through the B header pins by an external source.
JP4	This jumper configures the voltage translators between the XuLA I/O pins and the CLK, A and B pins. The voltage can be set to 1.8V, 2.5V, 3.3V or 5.0V. The voltage setting only affects the logic levels on the CLK, A and B pins; because of the voltage translators, the XuLA board will always receive 3.3V logic signals.

C.3 Operation

This chapter describes the operation of the Logic Pod module using a simplified schematic. You can find a complete schematic at the end of this manual.



The Logic Pod module uses transceivers to translate between the 3.3V I/O of the XuLA board and one of four possible I/O voltages for the external system (1.8V, 2.5V, 3.3V, 5.0V). There are two banks of transceivers: one bank that handles the 16-bit A port and the CLK, and a second bank that handles the 16-bit B port. Each bank can be independently set by a jumper to input signals from the external system to the XuLA board or output signals from the XuLA board to the external system. This allows the Logic Pod to be used as a 32-bit logic analyzer plus clock, a 32-bit pattern generator plus clock, or a combination 16-bit logic analyzer / 16-bit pattern generator plus clock.

C.4 Using the Module

To use the Logic Pod module, you will need to do the following:

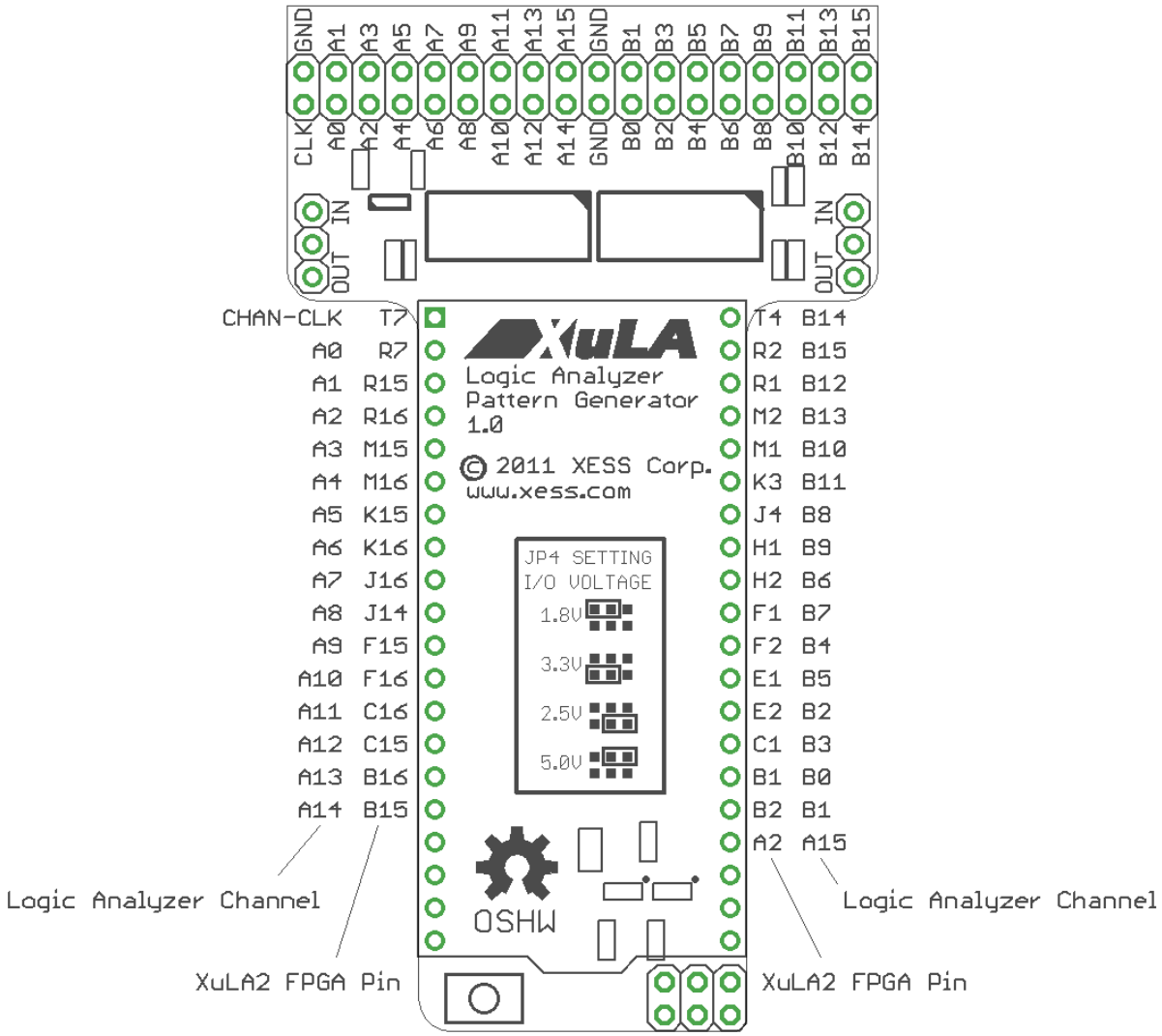
- Create a Xilinx ISE FPGA project and allocate up to 33 I/O ports to connect to the signals from the module.
- Attach the module to either a XuLA or XuLA2 board.
- Determine the FPGA pins that connect to each I/O pin of the module.
- Make a UCF file associating each FPGA pin with an I/O pin of the module.
- Include the UCF file in your ISE project.

That's a lot of work. I know that, otherwise I would have done it already. But I have done a simple project that tests the connectivity of the A and B ports. Just go to https://github.com/xesscorp/XuLA-Logic-Analyzer. There, you will find a subdirectory with a Xilinx ISE project that includes:

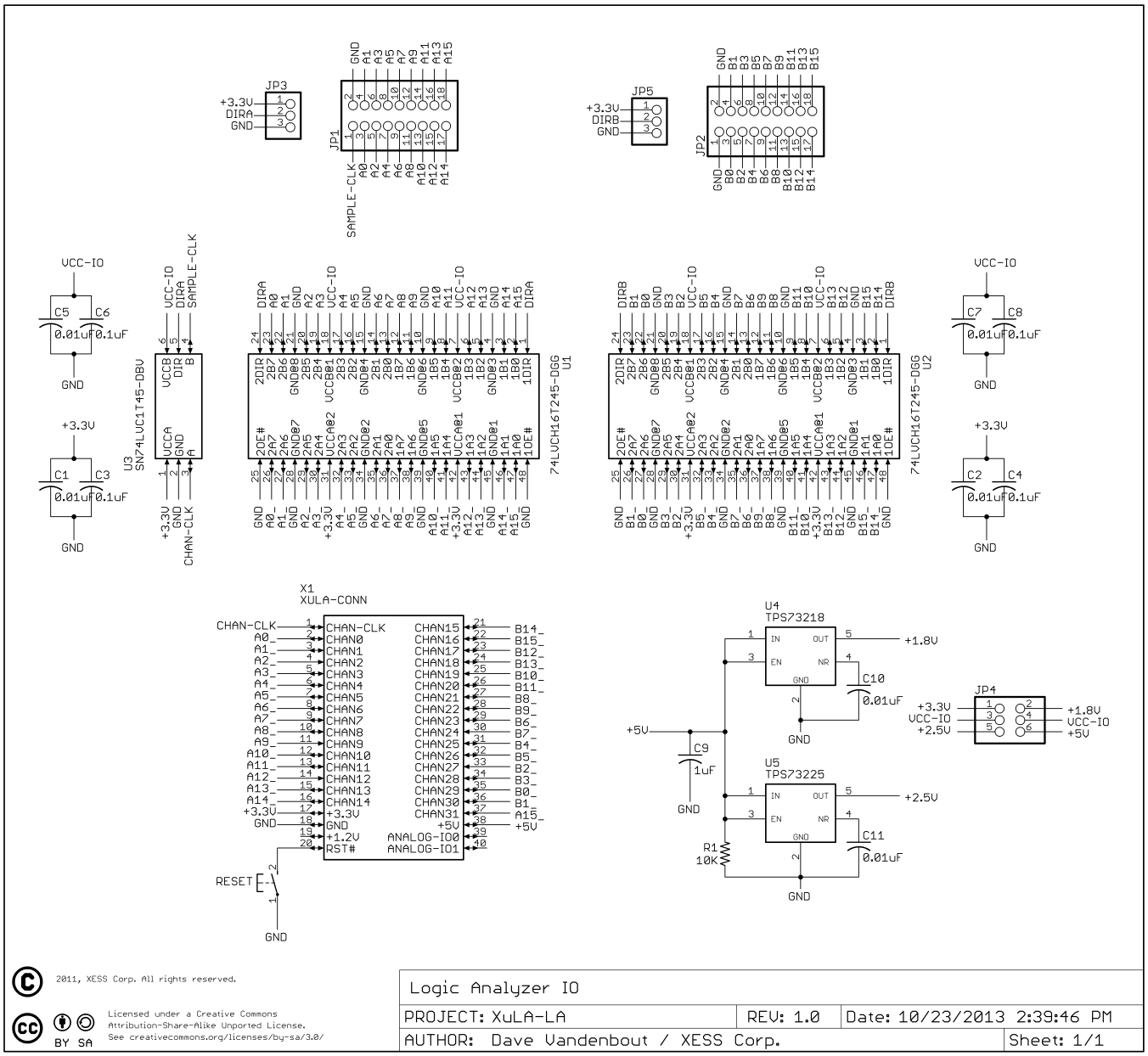
- a test design that uses the HostIoToDut module to drive the A port with a 16-bit value received from the PC over the USB link while also reading the 16-bit value on the B port,
- a UCF file containing the XuLA2 FPGA pin assignments for the Logic Pod module I/O,
- and a Python file that sets the A port to a random 16-bit value and then reads and compares the value on the B port.

A.1 I/O Locations

The connections from the XuLA2 to the Logic Pod module are shown below.



A.2 Schematic



Logic Analyzer IO		
PROJECT: XuLA-LA	REV: 1.0	Date: 10/23/2013 2:39:46 PM
AUTHOR: Dave Vandenbout / XESS Corp.		Sheet: 1/1