



# **fit-PC3 / fit-PC3i**

---

## Hardware Specification

## Legal Notice

© 2013 CompuLab Ltd.

All Rights Reserved. No part of this document may be photocopied, reproduced, stored in a retrieval system, or transmitted, in any form or by any means whether, electronic, mechanical, or otherwise without the prior written permission of CompuLab Ltd.

No warranty of accuracy is given concerning the contents of the information contained in this publication. To the extent permitted by law no liability (including liability to any person by reason of negligence) will be accepted by CompuLab Ltd., its subsidiaries or employees for any direct or indirect loss or damage caused by omissions from or inaccuracies in this document.

CompuLab Ltd. reserves the right to change details in this publication without notice.

Product and company names herein may be the trademarks of their respective owners.

CompuLab Ltd.  
17 HaYetsira St., Yokneam Elite 20692,  
P.O.B 687  
ISRAEL  
Tel: +972-4-8290100  
<http://www.compulab.co.il>  
<http://fit-pc.com/web/>  
Fax: +972-4-8325251

## Revision History

| Revision | Engineer     | Revision Changes       |
|----------|--------------|------------------------|
| 1.0      | Maxim Birger | Initial public release |
|          |              |                        |
|          |              |                        |
|          |              |                        |
|          |              |                        |

## Table of Contents

|  |    |
|--|----|
| Legal Notice.....                                  | 2  |
| Revision History .....                             | 3  |
| <b>1 Introduction</b> .....                        | 9  |
| 1.1 About This Document .....                      | 9  |
| 1.2 Reference .....                                | 9  |
| 1.3 Terms and Acronyms .....                       | 10 |
| <b>2 System Overview</b> .....                     | 11 |
| 2.1 Highlights .....                               | 11 |
| 2.2 Specifications .....                           | 11 |
| 2.3 System Block Diagram.....                      | 14 |
| 2.4 Models and Platform SKUs .....                 | 15 |
| <b>3 Platform</b> .....                            | 16 |
| 3.1 Processor.....                                 | 16 |
| 3.1.1 Processor Features.....                      | 16 |
| 3.2 Graphics Processor.....                        | 17 |
| 3.2.1 Graphics Features .....                      | 17 |
| 3.2.2 Display Interface .....                      | 17 |
| 3.2.3 APU PCI Express* Controller .....            | 18 |
| 3.3 Chipset .....                                  | 19 |
| 3.3.1 Unified Media Interface (UMI).....           | 20 |
| 3.3.2 FCH PCI Express* Controller.....             | 20 |
| 3.3.3 PCI Host Bus Controller .....                | 20 |
| 3.3.4 Serial ATA (SATA) Controller .....           | 20 |
| 3.3.4.1 AHCI.....                                  | 21 |
| 3.3.5 Low Pin Count (LPC) Bridge.....              | 22 |
| 3.3.6 Universal Serial Bus (USB) Controllers ..... | 24 |
| 3.3.7 RTC .....                                    | 25 |
| 3.3.8 GPIO .....                                   | 25 |
| 3.3.9 System Management Bus (SMBus) .....          | 25 |
| 3.3.10 High Definition Audio Controller.....       | 26 |
| 3.3.11 Integrated Clock Controller.....            | 26 |

|          |  |           |
|----------|--|-----------|
| 3.4      | System Memory .....                          | 27        |
| 3.4.1    | Processor Integrated Memory Controller ..... | 27        |
| 3.4.2    | System Supported Memory .....                | 28        |
| 3.4.3    | System Memory Timing Support .....           | 29        |
| 3.4.4    | System Memory Organization Modes .....       | 29        |
| 3.4.5    | Rules for Populating Memory Slots .....      | 29        |
| 3.5      | Storage .....                                | 30        |
| 3.5.1    | Certified storage devices.....               | 31        |
| 3.5.1.1  | HDD examples.....                            | 31        |
| 3.5.1.2  | mSATA SSD examples.....                      | 35        |
| <b>4</b> | <b>Peripherals.....</b>                      | <b>37</b> |
| 4.1      | USB3.0 Host Controller .....                 | 37        |
| 4.2      | Network .....                                | 38        |
| 4.2.1    | Realtek RTL8111F GbE Controller .....        | 38        |
| 4.2.1.1  | Realtek RTL8111F Features.....               | 38        |
| 4.2.1.2  | LAN Ports LEDs notifications .....           | 39        |
| 4.3      | Wireless Networks .....                      | 39        |
| 4.4      | Wireless Module Features .....               | 39        |
| 4.4.1    | WLAN .....                                   | 41        |
| 4.4.2    | Bluetooth .....                              | 41        |
| 4.4.3    | Security .....                               | 41        |
| 4.5      | Audio .....                                  | 42        |
| 4.5.1    | Audio Codec General Description .....        | 42        |
| 4.5.2    | Audio Codec Features .....                   | 42        |
| 4.6      | Super-I/O Controller .....                   | 45        |
| <b>5</b> | <b>Interfaces .....</b>                      | <b>46</b> |
| 5.1      | PCI Express* .....                           | 46        |
| 5.1.1    | PCI Express* Architecture .....              | 46        |
| 5.1.2    | PCI Express* Specifications .....            | 46        |
| 5.1.3    | Mini PCI Express* Edge Connector .....       | 47        |
| 5.2      | Unified Media Interface (UMI).....           | 48        |
| 5.2.1    | UMI Specifications .....                     | 48        |

|           |   |           |
|-----------|---|-----------|
| 5.3       | Digital Display Interface .....                   | 48        |
| 5.3.1     | High Definition Multimedia Interface (HDMI) ..... | 48        |
| 5.3.1.1   | HDMI Connector .....                              | 49        |
| 5.3.2     | Digital Video Interface (DVI) .....               | 50        |
| 5.3.3     | Display Port Interface (DP) .....                 | 50        |
| 5.3.3.1   | DisplayPort Connector .....                       | 52        |
| 5.4       | Analog Display Interface .....                    | 55        |
| 5.4.1     | VGA DB15 Connector .....                          | 55        |
| 5.5       | RS232 Serial Interface .....                      | 56        |
| <b>6</b>  | <b>Miscellaneous Features.....</b>                | <b>57</b> |
| 6.1       | Mini PCI Express/mSATA sharing .....              | 57        |
| 6.2       | FACE Module Interface .....                       | 58        |
| 6.2.1     | Extension Connectors .....                        | 59        |
| 6.2.2     | Connectors Pinout.....                            | 60        |
| 6.3       | Custom Design GPIOs.....                          | 63        |
| 6.4       | Misc Use Connector .....                          | 64        |
| <b>7</b>  | <b>Advanced Technologies.....</b>                 | <b>65</b> |
| 7.1       | AMD Virtualization Technology .....               | 65        |
| <b>8</b>  | <b>Power Management.....</b>                      | <b>66</b> |
| 8.1       | Power Manager.....                                | 66        |
| <b>9</b>  | <b>Electrical Characteristics .....</b>           | <b>67</b> |
| 9.1       | Absolute Maximum Ratings .....                    | 67        |
| 9.2       | Recommended Operating Conditions.....             | 67        |
| 9.3       | DC Electrical Characteristics.....                | 67        |
| 9.4       | Power Supply .....                                | 67        |
| <b>10</b> | <b>Mechanical Characteristics .....</b>           | <b>68</b> |
| 10.1      | Mechanical Drawings .....                         | 68        |
| 10.1.1    | Fit-PC3 Pro.....                                  | 68        |
| 10.1.2    | Fit-PC3 LP .....                                  | 71        |
| 10.1.3    | Fit-PC3i .....                                    | 74        |
| 10.1.4    | Single Board Computer .....                       | 75        |
| 10.1.4.1  | With FACE Module .....                            | 75        |

|          |                           |    |
|----------|---------------------------|----|
| 10.1.4.2 | Without FACE Module ..... | 75 |
| 10.2     | Environmental.....        | 76 |
| 11       | Resources.....            | 77 |

## Table of Figures

|   |    |
|---|----|
| Figure 1 – fit-PC3 Top Level Block Diagram .....                            | 14 |
| Figure 2 – fit-PC3i Top Level Block Diagram .....                           | 15 |
| Figure 3 – Block Diagram for the SATA Module .....                          | 21 |
| Figure 4 – Typical LPC Bus System .....                                     | 22 |
| Figure 5 – Block Diagram of LPC Module.....                                 | 23 |
| Figure 6 – USB Controllers Block Diagram .....                              | 24 |
| Figure 7 – RTC Block Diagram .....  | 25 |
| Figure 8 – System Clock Generation .....                                    | 26 |
| Figure 9 – Memory Interface .....   | 27 |
| Figure 10 – SATA Interface .....  | 30 |
| Figure 11 – Wireless Module Q802XRN5B Block Diagram.....                    | 40 |
| Figure 12 – Audio Codec Functional Block Diagram.....                       | 44 |
| Figure 13 – SMSC SIO1007 Super-I/O Controller functional block diagram..... | 45 |
| Figure 14 – HDMI Link Diagram .....   | 49 |
| Figure 15 – DP Link Diagram .....   | 51 |
| Figure 16 – COM1 Serial Port Pinout .....                                   | 56 |
| Figure 17 – fit-PC3/3i PC Mini PCIe/mSATA scheme.....                       | 57 |
| Figure 18 – FACE Module concept .....                                       | 58 |
| Figure 19 – fit-PC3 Pro Isometric Front.....                                | 68 |
| Figure 20 – fit-PC3 Pro Isometric Back.....                                 | 68 |
| Figure 21 – fit-PC3 Pro Front Panel.....                                    | 69 |
| Figure 22 – fit-PC3 Pro Back Panel .....                                    | 69 |
| Figure 23 – fit-PC3 Pro Top.....  | 70 |
| Figure 24 – fit-PC3 Pro Bottom .....  | 70 |
| Figure 25 – fit-PC3 LP Isometric Front .....                                | 71 |
| Figure 26 – fit-PC3 LP Isometric Back.....                                  | 71 |
| Figure 27 – fit-PC3 LP Front Panel.....                                     | 72 |
| Figure 28 – fit-PC3 LP Back Panel.....                                      | 72 |
| Figure 29 – fit-PC3 LP Top .....  | 73 |
| Figure 30 – fit-PC3 LP Bottom .....   | 73 |
| Figure 31 – fit-PC3i Pro Back Panel .....                                   | 74 |
| Figure 32 – SBC-FITPC3 Mechanical Drawing with FACE Module .....            | 75 |
| Figure 33 – SBC-FITPC3 Mechanical Drawing without FACE Module .....         | 75 |

## Table of Tables

|  |    |
|--|----|
| Table 1 – Reference Documents .....                                | 9  |
| Table 2 – Terms and Acronyms .....                                 | 10 |
| Table 3 – Platform Specifications .....                            | 11 |
| Table 4 – Display and Graphics Specifications .....                | 12 |
| Table 5 – Audio Specifications .....                               | 12 |
| Table 6 – Networking Specifications.....                           | 12 |
| Table 7 – Connectivity Specifications .....                        | 13 |
| Table 8 – Mechanical and Environmental Specifications.....         | 13 |
| Table 9 – Models and Platform SKUs.....                            | 15 |
| Table 10 – Supported Memory Technologies.....                      | 28 |
| Table 11 – Supported Max Memory Size per SO-DIMM .....             | 29 |
| Table 12 – DDR3 System Memory Timing Support .....                 | 29 |
| Table 13 – WD Scorpio Blue HDD series .....                        | 31 |
| Table 14 – WD Scorpio Blue HDD series (cont.) .....                | 32 |
| Table 15 – Hitachi CinemaStar C5K750 HDD models .....              | 33 |
| Table 16 – Seagate Momentus HDD series.....                        | 34 |
| Table 17 – Micron mSATA NAND Flash SSD .....                       | 35 |
| Table 18 – ACPI CMS2G-M SSD .....                                  | 36 |
| Table 19 – LAN ports LEDs status notification.....                 | 39 |
| Table 20 – WLAN Channel Assignment.....                            | 41 |
| Table 21 – BT Channel Assignment.....                              | 41 |
| Table 22 – mini PCI Express edge connector pinout .....            | 47 |
| Table 23 – Downstream Port HDMI Connector Pinout.....              | 49 |
| Table 24 – Downstream Port HDMI Connector Signal Description ..... | 50 |
| Table 25 – Downstream Port DP Connector Pinout.....                | 52 |
| Table 26 – Upstream Port DP Connector Pinout .....                 | 53 |
| Table 27 – Display Port Cable.....                                 | 54 |
| Table 28 – VGA DB15 Connector.....                                 | 55 |
| Table 29 – B2B receptacle connector HOST side .....                | 59 |
| Table 30 – B2B plug connector FACE Module side .....               | 59 |
| Table 31 – EXT1 connector HOST side pinout .....                   | 60 |
| Table 32 – EXT2 connector HOST side pinout .....                   | 61 |
| Table 33 – Custom Design GPIO table .....                          | 63 |
| Table 34 – Misc Use Connector.....                                 | 64 |
| Table 35 – Absolute Maximum Ratings .....                          | 67 |
| Table 36 – Recommended Operating Condition .....                   | 67 |
| Table 37 – DC Electrical Characteristics .....                     | 67 |
| Table 38 – Operating Temperature Grades .....                      | 76 |

## 1 Introduction

---

### 1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate CompuLab's fit-PC3 and fit-PC3i computers.

### 1.2 Reference

For additional information not covered in this manual, please refer to the documents listed in **Table 1**.

**Table 1 – Reference Documents**

| Document                      | Location  |
|-------------------------------|---|
| FACE Module HW Specifications | <a href="http://fit-pc.com/download/face-modules/documents/face-modules-hw-specifications.pdf">http://fit-pc.com/download/face-modules/documents/face-modules-hw-specifications.pdf</a> |
| AMD Virtualization Technology | <a href="http://sites.amd.com/uk/business/it-solutions/virtualization/Pages/amd-v.aspx">http://sites.amd.com/uk/business/it-solutions/virtualization/Pages/amd-v.aspx</a>               |
|                               |   |

### 1.3 Terms and Acronyms

Table 2 – Terms and Acronyms

| Term        | Definition   |
|-------------|--|
| APM         | Advanced Power Management  |
| APU         | Accelerated Processing Unit  |
| B2B         | Board to Board (connectors)  |
| BER         | Bit error rate   |
| bps         | Bits per second  |
| BT          | Bluetooth  |
| CAN         | Controller Area Network  |
| Codec       | Coder decoder  |
| DDR         | Dual data rate   |
| DMA         | Direct Memory Access   |
| DSP         | Digital signal processor   |
| FACE Module | <b>F</b> unction <b>A</b> nd <b>C</b> onnectivity <b>E</b> xtension Module |
| FCH         | Platform Controller Hub  |
| FM-xxxx     | FACE Module – <i>connectivity options</i>                                  |
| GB/s        | Gigabytes per second   |
| GPIO        | General-purpose input/output   |
| GT/s        | Giga Transfers per second (throughput)                                     |
| HW          | Hardware   |
| JTAG        | Joint Test Action Group (ANSI/ICEEE Std. 1149.1-1990)                      |
| kbps        | Kilobits per second  |
| LAN         | Local Area Network   |
| MB/s        | Megabytes per second   |
| Mbps        | Megabits per second  |
| MT/s        | Mega Transfers per second (throughput)                                     |
| NVM         | Non Volatile Memory  |
| OTP         | One Time Programmable  |
| PCM         | Pulse-coded Modulation   |
| PEG         | PCI Express Graphics   |
| Rx          | Receive  |
| SCH         | System Controller Hub  |
| SDRAM       | Synchronous dynamic random access memory                                   |
| SoC         | System-on-Chip   |
| SPI         | Serial peripheral interface  |
| Tx          | Transmit   |
| UART        | Universal asynchronous receiver transmitter                                |
| USB         | Universal serial bus   |
| USB-OTG     | Universal serial bus on-the-go   |
| USIM        | UMTS subscriber interface module   |
| VCTCXO      | Voltage-controlled temperature-compensated crystal oscillator              |
| WLAN        | Wireless Local Area Network  |
| XO          | Crystal oscillator   |

## 2 System Overview

### 2.1 Highlights

Fit-PC3 and fit-PC3i are fully functional miniature computers based on AMD Embedded G-Series 64-bit dual core processor family.

Together with powerful AMD Radeon HD graphics engine, rich peripherals and connectivity options, completely fanless design delivers outstanding performance at lowest power consumption. The product offered in two processors SKUs, offering low-end and mid-end processing power. Fit-PC3 and fit-PC3i differs in a set of proposed connectivity and I/O options, as 2<sup>nd</sup> video output technology, number of LAN ports, Serial RS232 connectivity and readiness for cellular communication.

Performance Value ratio, low-power, rich I/O, miniature rugged design and cost competitiveness position fit-PC3 and fit-PC3i as an attractive solution for a wide range of applications – industrial control and automation, networking and communications infrastructures, media players and media centers, IPTV, infotainment system, digital signage and smart kiosks, gaming or small-footprint desktop replacement.

### 2.2 Specifications

**Table 3 – Platform Specifications**

| Feature               | Specifications   |
|-----------------------|--|
| Processor             | AMD Embedded G-Series (FT1): G-T56N/G-T40E   |
|                       | Dual core 64-bit   |
|                       | Clock speed 1GHz – 1.65GHz <b>(Note 1)</b>   |
|                       | 18W TDP (Pro models)   |
|                       | 6.4W TDP (LP models)   |
| Chipset               | AMD Fusion Controller Hub (FCH) A55E   |
| Memory                | Up to 16GB (2x 8GB) DDR3/DDR3L-1066/1333   |
|                       | 2x SO-DIMM 204-pin DDR3/DDR3L SDRAM memories   |
| Storage               | 1x SATA up to 6 Gbps (SATA 3.0) for internal 2.5" HDD/SSD, HDD to be used 5400rpm only |
|                       | 1x mSATA slot up to 6 Gbps (SATA 3.0)  |
|                       | 2x eSATA ports up to 6 Gbps (SATA 3.0) (fit-PC3 only)                                  |
| Advanced Technologies | AMD Virtualization Technology  |
| Operating Systems     | Windows XP/7/8, 32-bit and 64-bit  |
|                       | Linux 32-bit and 64-bit  |
|                       | Embedded OS  |

**Table 4 – Display and Graphics Specifications**

| Feature        | Specifications   |                                    |
|----------------|--|------------------------------------|
|                | fit-PC3  | fit-PC3i                           |
| GPU            | AMD Radeon HD 6320/ HD 6250 (Pro/LP models)<br>Dual display mode supported |                                    |
| Video Output 1 | HDMI 1.4a up to 1920 x 1200 @ 60Hz   | HDMI 1.4a up to 1920 x 1200 @ 60Hz |
| Video Output 2 | DisplayPort 1.1a up to 2560 x 1600 @ 60Hz                                  | HDMI 1.4a up to 1920 x 1200 @ 60Hz |

**Table 5 – Audio Specifications**

| Feature      | Specifications   |
|--------------|--|
| Codec        | Realtek ALC888-VC2 HD audio codec  |
| Audio Output | Analog stereo output<br>Digital 7.1+2 channels S/PDIF output<br>3.5mm jack |
| Audio Input  | Analog stereo Microphone input<br>Digital S/PDIF input<br>3.5mm jack       |

**Table 6 – Networking Specifications**

| Feature  | Specifications  |  |
|----------|---|--|
|          | fit-PC3   | fit-PC3i   |
| LAN      | 1x GbE LAN ports (extendable up to 5)<br><br>LAN1: Realtek RTL8111F-CG GbE controller (RJ-45)<br>LAN2: N/A<br><br>LAN3-6: Depends on FACE Module<br><b>(Note 2)</b> | 2x GbE LAN ports (extendable up to 6)<br><br>LAN1: Realtek RTL8111F-CG GbE controller (RJ-45)<br>LAN2: Realtek RTL8111F-CG GbE controller (RJ-45)<br>LAN3-6: Depends on FACE Module<br><b>(Note 2)</b> |
| Wireless | WLAN 802.11 b/g/n (2.4GHz Qcom Q802XRN5B module)<br>Bluetooth 3.0 + HS  |  |

**Table 7 – Connectivity Specifications**

| Feature     | Specifications   |                            |
|-------------|--|----------------------------|
|             | fit-PC3  | fit-PC3i                   |
| USB         | 6x USB 2.0 <b>(Note 3)</b><br>2x USB 3.0                                 | 8x USB 2.0 <b>(Note 3)</b> |
| Serial      | 1x RS232 serial communication<br>COM1: Serial port (u mini serial)       | N/A                        |
| Special I/O | N/A  | 1x micro SIM slot (6 pins) |
| Expansion   | Half-size mini-PCIe socket<br>Full-size mini-PCIe socket <b>(Note 5)</b> |                            |

**Table 8 – Mechanical and Environmental Specifications**

| Feature                | Specifications  |
|------------------------|---|
| Input Voltage          | Unregulated 10 – 15VDC input <b>(Note 6)</b>  |
| Power Consumption      | 9W – 24W (Pro models)<br>7W – 15W (LP models)   |
| Operating Temperatures | 1. Commercial<br>HDD models: 0°C – 50°C<br>SSD models: 0°C – 70°C<br>2. Extended (TE)<br>SSD models only: -20°C – 70°C<br>3. Industrial (TI)<br>SSD models only: -40°C – 70°C |
| Enclosure Material     | Die Cast Aluminum   |
| Cooling                | Passive Cooling Fanless Design  |
| Dimensions             | 19cm x 16cm x 4cm (Pro models)<br>19cm x 16cm x 2.5cm (LP models)   |
| Weight                 | 1100/1050gr (Pro/LP models respectively)  |

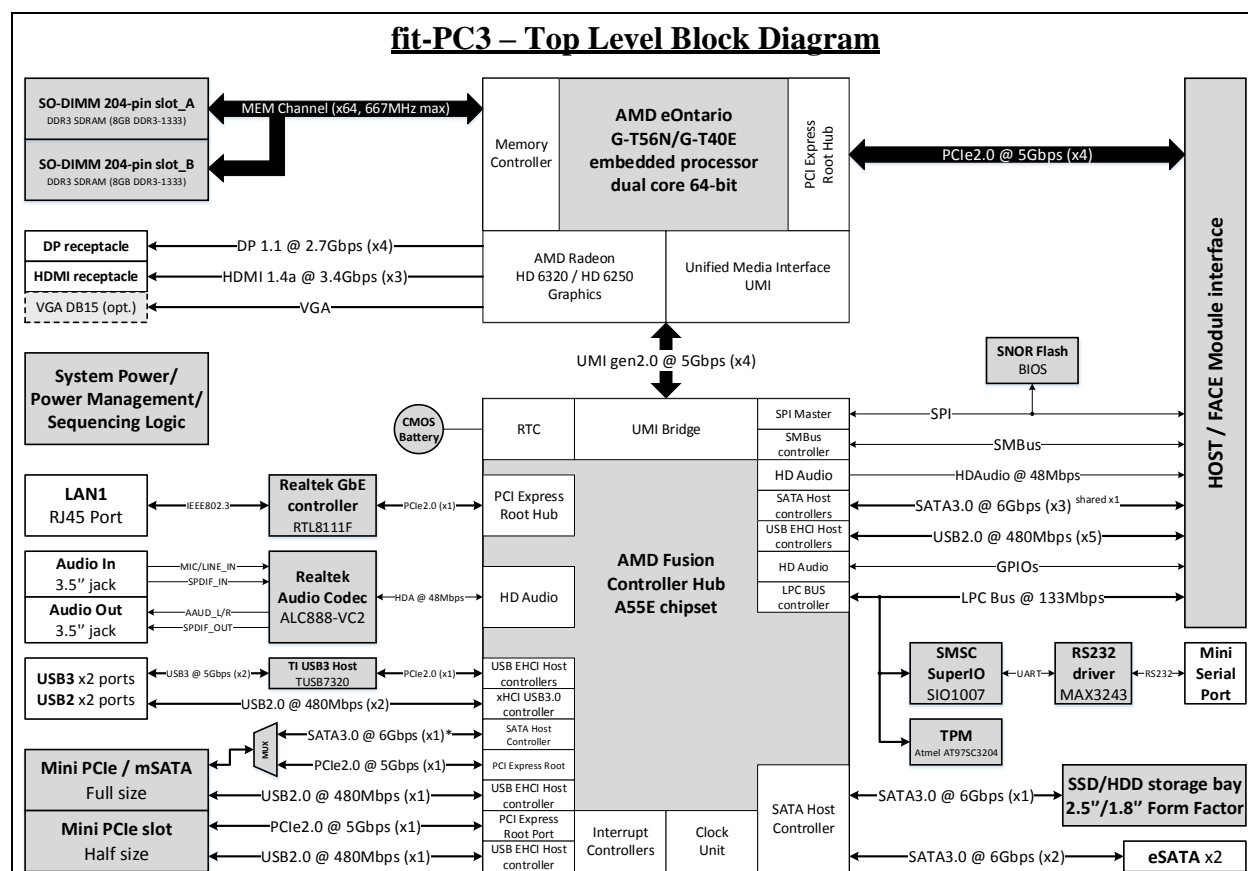
**Notes:**

- For full processors specifications based on fit-PC3/3i model, please refer to models and platform SKU **Table 9**.
- Option for additional 4x GbE LAN ports. LAN3-6 based on FACE Module installed:
  - FM-4USB: N/A
  - FM-1LAN: LAN3 RTL8111F-CG GbE controller (RJ-45), LAN4-6: N/A
  - FM-4LAN: Intel 82574 GbE Controller (RJ-45)
  - FM-POE: Intel 82574 or I211AT GbE Controller (RJ-45)
- Up to 4x additional USB2.0 on front panel based on FACE Module installed.
- FACE Module HW specifications document - Table 1.
- Shared with mSATA. Refer to **Figure 17**.
- Nominal input voltage: 12V

## 2.3 System Block Diagram

Fit-PC3 and fit-PC3i systems Top Level Block Diagrams are shown below. Later chapters in this document describe functions and entities shown in the below diagrams.

Figure 1 – fit-PC3 Top Level Block Diagram





## 3 Platform

---

### 3.1 Processor

The AMD Embedded G-Series processor is the world's first integrated circuit to combine a low-power CPU and a discrete-level GPU into a single embedded Accelerated Processing Unit (APU). This unprecedented level of graphics integration builds a new foundation for high performance multi-media content delivery in a small form factor and power efficient platform for a broad range of embedded designs. Based on a power-optimized core, the AMD Embedded G-Series platform delivers levels of performance in a compact BGA package that is ideal for low power designs in embedded applications.

#### 3.1.1 Processor Features

This section lists the features and design capabilities of the AMD Embedded G-Series processor:

- Two high performance integrated x86 execution cores
- A 32-kB instruction and 32-KB data first-level cache (L1) for each core
- A 512-kB shared instruction / data second-level cache (L2) for each core
- Compatible with Existing 32-bit x86 and 64-bit AMD64 Code Base
  - Support for SSE, SSE2, SSE3, SSE4A, SSSE3, MMX™, and legacy x86 instructions
- AMD 64-bit floating-point accelerator
- AMD Virtualization™ technology (AMD-V™)
- Integrated Memory Controller
  - 64-bit DDR3 SDRAM controller operating at throughputs up to 1333 MT/s
  - Theoretical max BW of 8.53 GB/s assuming DDR3 SDRAM 1066 MT/s
  - Theoretical max BW of 10.65 GB/s assuming DDR3 SDRAM 1333 MT/s
- Integrated graphics processor

## 3.2 Graphics Processor

This section lists the graphics features available for the AMD Embedded G-Series processor.

### 3.2.1 Graphics Features

- AMD Radeon HD 6320 GPU Core architecture for Pro models
- AMD Radeon HD 6250 GPU Core architecture for LP models
- Dedicated graphics memory controller
- 2D Acceleration
  - Highly-optimized 128-bit engine, capable of processing multiple pixels per clock
- 3D Acceleration
  - DirectX® 11 compliant, including full speed 32-bit floating point per component operations
  - Support for OpenCL™ 1.1
  - Support for OpenGL 3.2 and 2.1
- Motion Video Acceleration Features
  - Dedicated hardware (UVD 3) for H.264, MPEG4 Part 2, VC-1, and MPEG2 decode
  - Microsoft DirectX video acceleration (DXVA) API (application programming interface) for Windows operating system
  - Video scaling and YCrCb to RGB color space conversion for video playback and fully adjustable color controls
  - Motion adaptive and vector based de-interlacing filter eliminates video artifacts caused by displaying interlaced video on non-interlaced displays, and by analyzing image and using optimal de-interlacing functions on a per-pixel basis
  - HD HQV and SD HQV support: noise removal, detail enhancement, color enhancement, cadence detection, sharpness, and advanced de-interlacing
  - Super up-conversion for SD to HD resolutions

### 3.2.2 Display Interface

Display interface is fully integrated inside the Accelerated Processing Unit (APU). The APU houses memory interface, display planes, pipes, transcoders and display interface. The number of planes, pipes, and transcoders decide the number of simultaneous and concurrent display devices that can be driven on a platform. Fit-PC3/3i APU system architecture provides one Analog and two Digital Ports. Each Digital Port can transmit data according to one or more protocols. Fit-PC3 Digital Ports configured to drive natively HDMI/DVI and DisplayPort\*. Fit-PC3i Digital Ports configured to drive two HDMI/DVI displays. Each digital port has control signals that may be used to control, configure and/or determine the capabilities of an external device. Fit-PC3/3i design supports one, two or three simultaneous independent and concurrent display configurations, when two displays supported natively and for additional 3<sup>rd</sup> display provision is given.

For further display interface information refer to sections 5.3 and 5.4 .

### 3.2.3 APU PCI Express\* Controller

The APU provides up to 4 PCI Express Root Ports, supporting the PCI Express Base Specification, Revision 2.0. Each Root Port x1 lane supports up to 5 Gbps bandwidth in each direction (10 Gbps concurrent). APU supports 4x1 or 1x4 PCI Express link. Supports L0s and L1 link power states for power saving.

### 3.3 Chipset

The FCH provides extensive I/O support. Functions and capabilities include:

- Unified Media Interface (UMI)
- PCI Express\* Base Specification, Rev 2.0 support up to x4 ports with transfers up to 5 GT/s
- PCI Local Bus Specification, Revision 2.3 support for 33 MHz PCI operations
- 4 OHCI and 3 EHCI host controllers to support 14x USB2.0 ports and 2x USB1.1 ports
- Enhanced DMA controller, interrupt controller, and timer functions
- Integrated SATA host controllers within dependent DMA operation on six ports
- System Management Bus (SMBus) controller, with additional support for I2C devices
- Integrated Clock Controller
- Low Pin Count (LPC) interface
- High Definition Audio

### 3.3.1 Unified Media Interface (UMI)

Unified Media Interface (UMI) is the chip-to-chip connection between the processor and FCH. This high-speed interface integrates advanced priority-based servicing allowing for concurrent traffic and true isochronous transfer capabilities. Base functionality is completely software-transparent, permitting current and legacy software to operate normally.

- 1-, 2-, or 4-lane Unified Media Interface connecting the FCH with the APU
- Automatic detection of lane configuration on boot-up
- Dynamic lane width up/down configuration on detecting bandwidth requirement
- Supports transfer rate of up to 5.0 GT/s per lane
- Clock speed can be locked at 2.5 GHz for power saving

### 3.3.2 FCH PCI Express\* Controller

The FCH provides up to 4 PCI Express Root Ports, supporting the PCI Express Base Specification, Revision 2.0. Each Root Port x1 lane supports up to 5 Gbps bandwidth in each direction (10 Gbps concurrent). PCI Express Root Ports can independently be configured to support four x1s, two x2s, one x2 and two x1s, or one x4 port widths. Supports L0s and L1 link power states for power saving.

Refer to section 5.1 for detailed feature set.

### 3.3.3 PCI Host Bus Controller

The PCI Bridge supports up to four PCI slots. The PCI Bridge runs at 33 MHz and can support CLKRUN# function with individual clock override (option for not stopping specific PCICLK). In addition, it has the capability to hide individual PCI devices. The FCH has a strapping option that allows loading of the boot codes from the PCI bus on the very first boot (first boot after RSMRST#). Subsequent boots will revert back to the ROM selection determined by the ROM straps or PMIO programming. This allows system manufacturers to populate the motherboard with a blank flash device (for BIOS) and use this option to program it. This is particularly useful for systems built without a socket for the BIOS ROM.

- Supports PCI bus at 33MHz
- Supports PCI Rev. 2.3 specification
- Supports up to 4 bus master devices
- Supports 40-bit addressing
- Interrupt steering supported for plug-n-play devices
- Supports concurrent PCI operations
- BIOS/hardware support to hide PCI device
- Supports spread spectrum

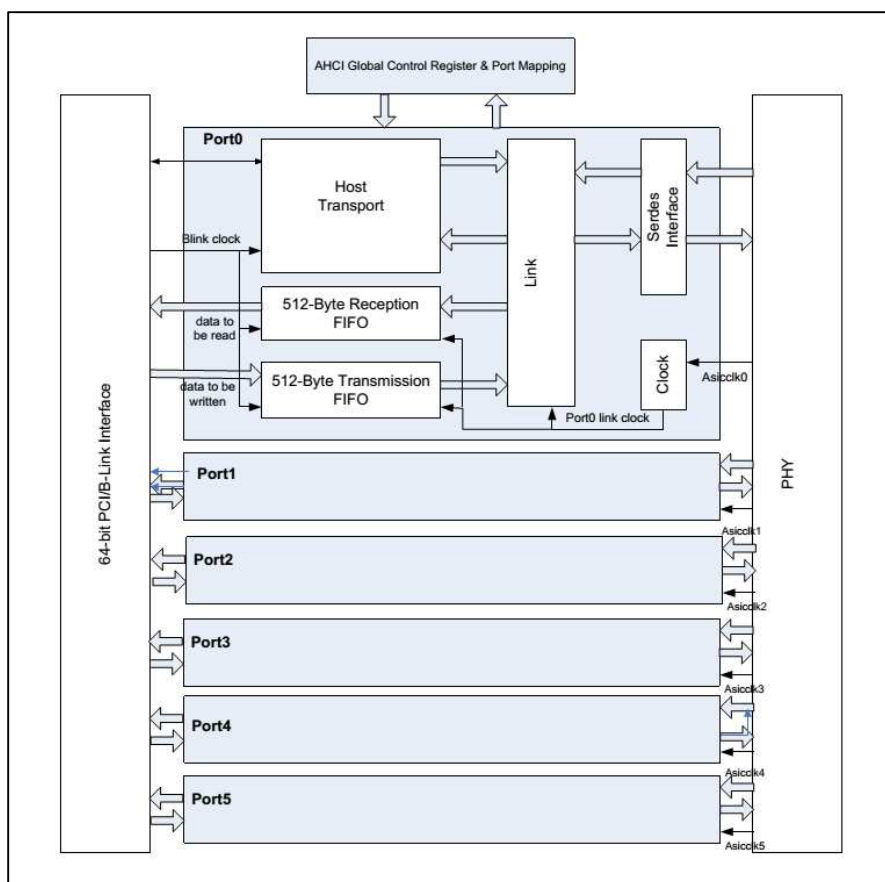
### 3.3.4 Serial ATA (SATA) Controller

The integrated Serial ATA controller processes host commands and transfers data between the host and Serial ATA devices. It supports six independent Serial ATA channels. Each channel has its own Serial ATA bus and supports one Serial ATA device. With respect to the transfer rate, the integrated SATA controller supports First generation (1.5 Gbps), Second generation (3 Gbps), and Third generation (6 Gbps) SATA ports. Refer to **Figure 3** for FCH SATA block structure.

The SATA controller can operate in three modes:

- All six channels are configured as SATA AHCI mode.
- All six channels are configured as IDE mode. In this configuration, the SATA controller is configured into two IDE controllers, with the programming interface of channel 0 to 3 under the first IDE controller, and that of channel 4 and 5 under the second IDE controller.
- Four channels (channel 0 to 3) are configured as SATA AHCI and two channels (channel 4 and 5) are configured as IDE mode. In this configuration, the programming interface of channel 4 and 5 are under the IDE controller.

**Figure 3 – Block Diagram for the SATA Module**



### 3.3.4.1 AHCI

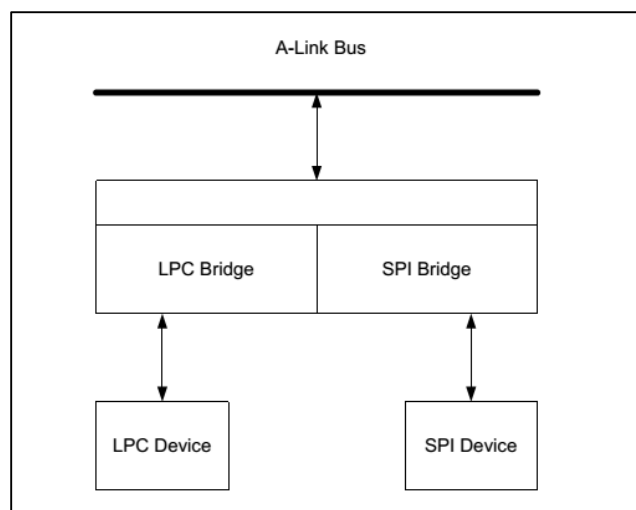
The FCH provides hardware support for Advanced Host Controller Interface (AHCI), a standardized programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices—each device is treated as a master—and hardware assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug. AHCI requires appropriate software support (such as, an AHCI driver) and for some features, hardware support in the SATA device or additional platform hardware.

### 3.3.5 Low Pin Count (LPC) Bridge

The Low Pin Count (LPC) bus interface is a cost-efficient, low-speed interface designed to support low-speed legacy (ISA, X-bus) devices. The LPC interface essentially eliminates the need of ISA and X-bus in the system. A typical setup of the system with LPC interface is shown in **Figure 4**. Here the ISA bus is internal to FCH and is used for connecting to the legacy Direct Memory Access (DMA) logic. The LPC host controller is typically integrated into the FCH. It connects to the internal A-Link bus on one side and the LPC and Serial Peripheral Interface (SPI) buses on the other side.

The ISA interface is only used for legacy DMA operation.

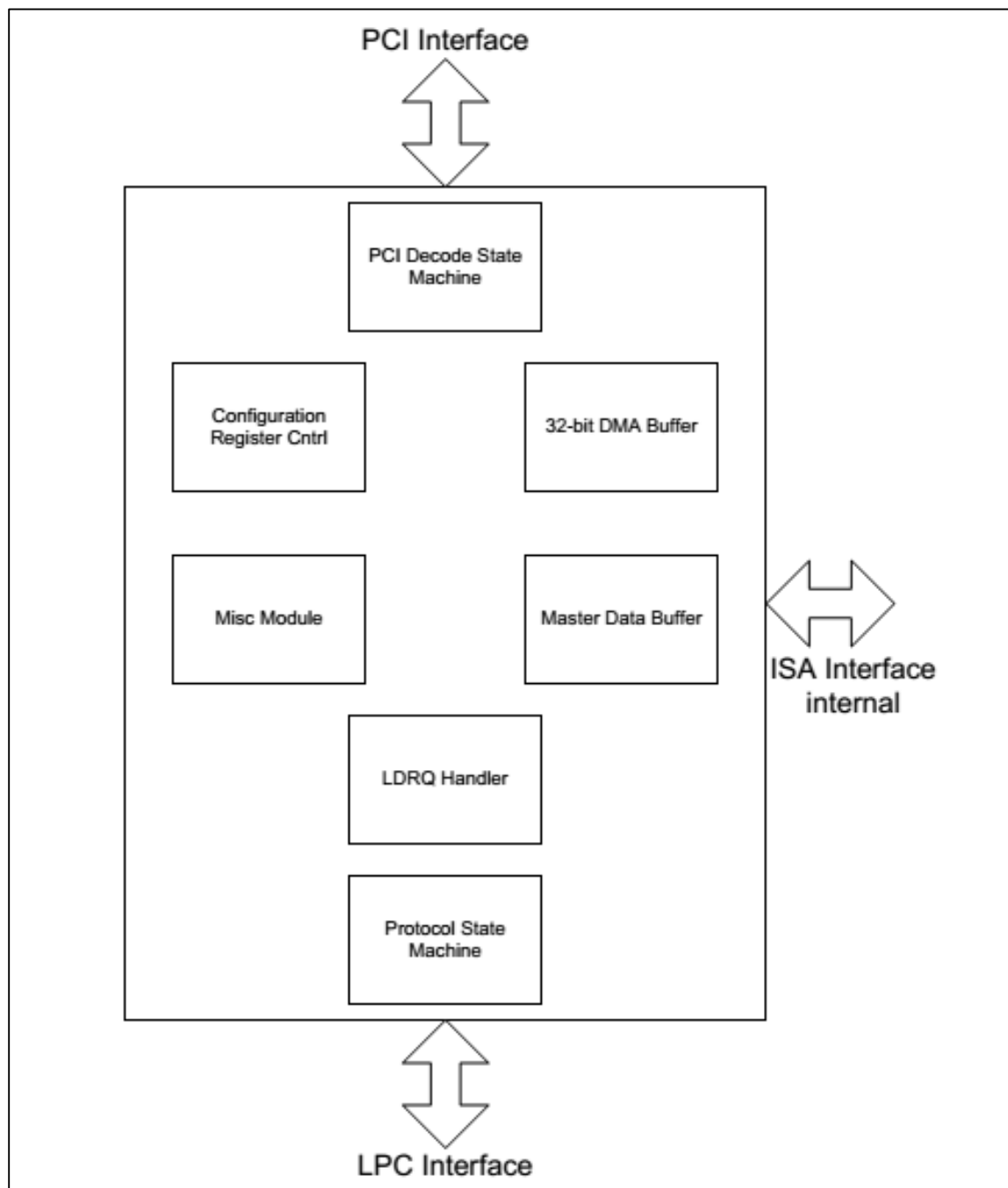
**Figure 4 – Typical LPC Bus System**



Examples of LPC devices include Super I/O (disk controller, keyboard controller), BIOS RAM, audio, Trusted Platform Module (TPM), and system management controller. A BIOS ROM can also be populated on the SPI interface. The Hudson-E1 FCH can support an LPC or SPI type BIOS ROM.

LPC host controller has the A-Link bus on one side and the LPC bus on the other. The host controller supports memory and I/O read/write, DMA read/write, and bus master memory I/O read/write. It supports up to two bus masters and seven DMA channels.

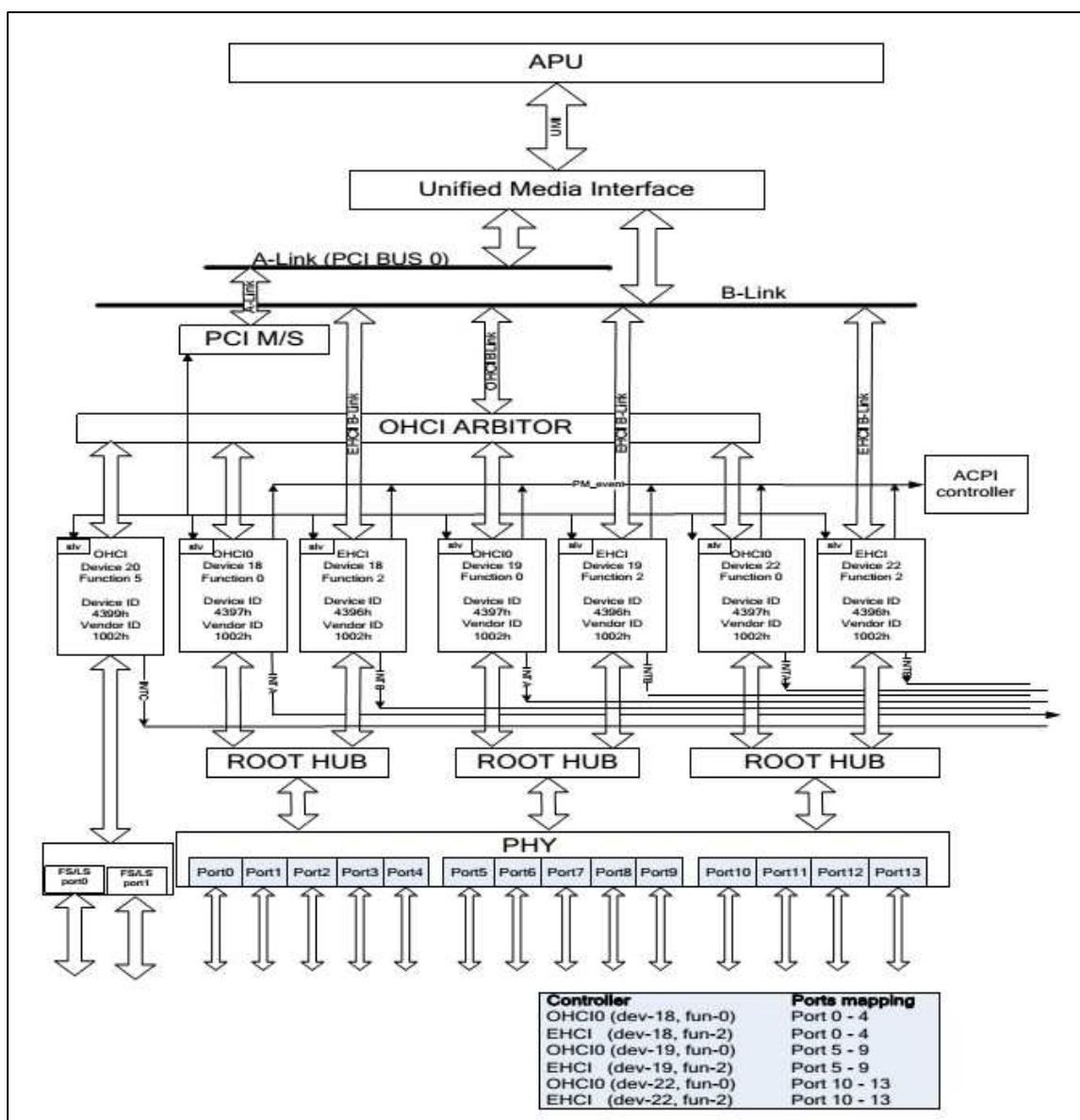
Figure 5 – Block Diagram of LPC Module



### 3.3.6 Universal Serial Bus (USB) Controllers

The FCH contains 4 OHCI and 3 EHCI host controllers to support 14 USB 2.0 ports that support USB high-speed signaling and 2 dedicated USB 1.1 ports. High-speed USB 2.0 allows data transfers up to 480 Mbps. Supports ACPI S1 ~ S4, USB keyboard/mouse functionality for legacy Operating Systems, USB debug port and individual port disable capability.

Figure 6 – USB Controllers Block Diagram

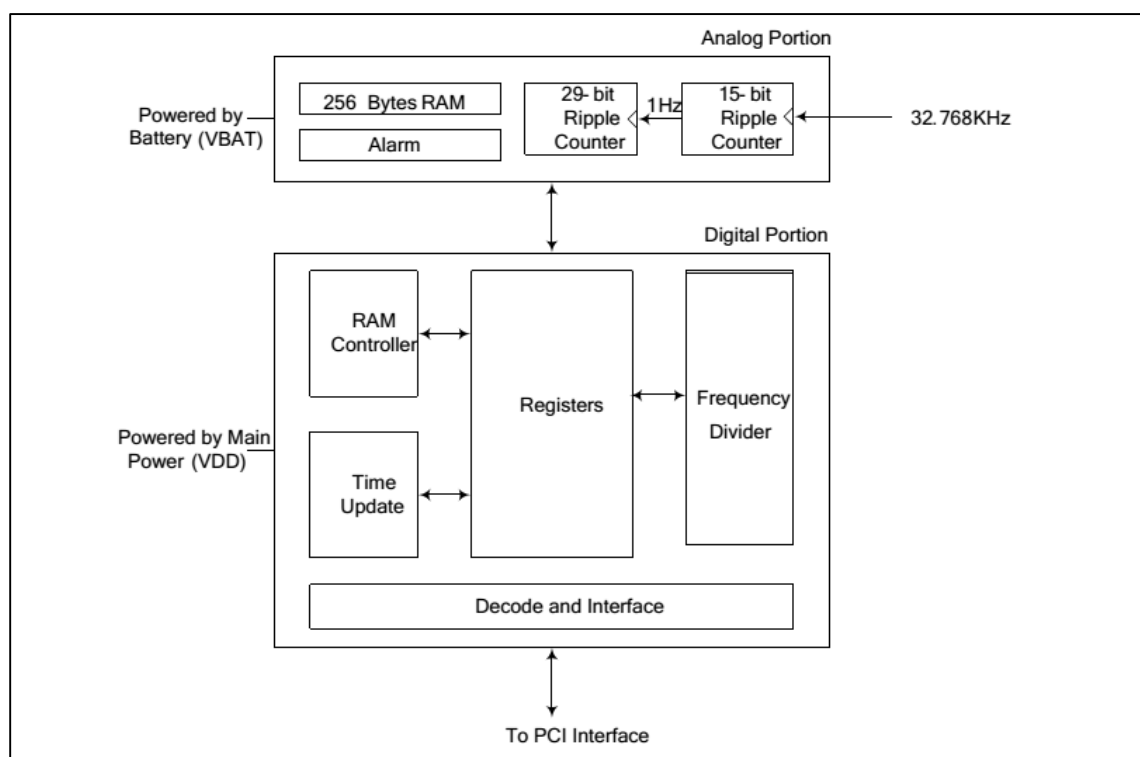


### 3.3.7 RTC

The Real Time Clock (RTC) updates the computer's time and generates interrupts for periodic events and pre-set alarm. The RTC also makes hardware leap year corrections. The FCH's RTC includes a 256-byte CMOS RAM, which is used to store the configuration of a computer such as the number and type of disk drive, graphics adapter, base memory, checksum value, etc.

The internal RTC is made of two parts—one part is an analog circuit, powered by a battery VBAT, and the other is a digital circuit, powered by a main power VDD. **Figure 7** shows the block diagram of the internal RTC. The FCH has added hardware-based daylight saving feature and makes adjustments (spring forward or fall back) at the designated dates/times. Both the date and hour for the daylight and standard time are fully programmable, allowing for different daylight saving dates and hours for different parts of the world.

**Figure 7 – RTC Block Diagram**



### 3.3.8 GPIO

Various general purpose inputs and outputs are provided for custom system design. Refer to section 6.3.

### 3.3.9 System Management Bus (SMBus)

The FCH contains SMBus Host interface that allows the processor to communicate with SMBus slaves. This interface is compatible with most I2C devices.

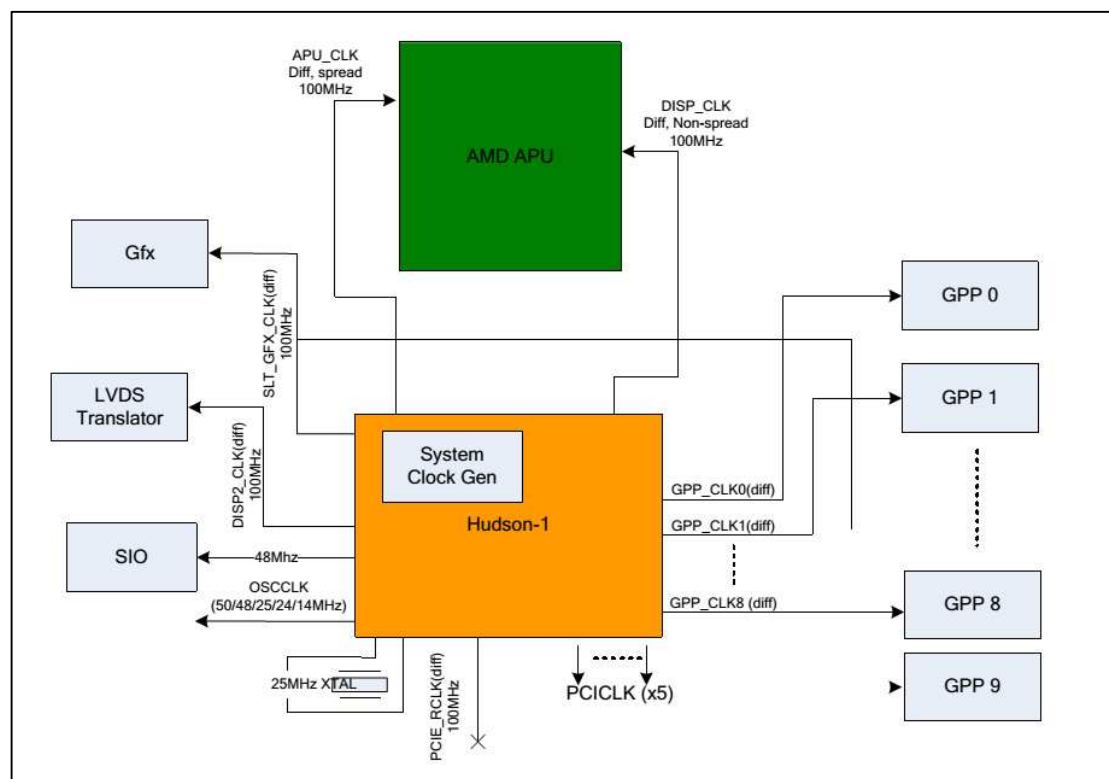
### 3.3.10 High Definition Audio Controller

The High Definition (HD) Audio Controller communicates with the external HD Audio codec over the HD Audio Link. The FCH HD Audio Controller consists of four independent output DMA engines and four independent input DMA engines that are used to move data between system memory and the external codec. The controller can support up to four audio or modem codec in any combinations.

### 3.3.11 Integrated Clock Controller

The FCH Hudson-E1 has an integrated system clock generator that can be used to generate the required system clocks, thus eliminating the need for an external clock generator. However, it does support a mode of operation that allows an external clock generator to be used in the system. The clock generator mode is selected by a power-on configuration strap. A simplified block diagram of the clock distribution for the integrated clock mode is shown in **Figure 8**.

**Figure 8 – System Clock Generation**



If FCH is in external clock mode, the clock sources it requires are a 25MHz crystal as internal PLL clock source, a 32-KHz crystal for the RTC, and a 100MHz differential clock pair for the PCIe reference clocks. In addition to the PCIe clocks, the chipset also uses the 100-MHz clock to generate various internal clocks. If Hudson-E1 is set to integrated clock mode, only a 25MHz crystal for master reference and a 32-KHz crystal for the RTC are required. Hudson-E1 will then generate all the system clocks needed, which include the APU reference clocks, the graphics clocks, the 25MHz clock for SATA, the 48MHz clocks for USB, and so on.

## 3.4 System Memory

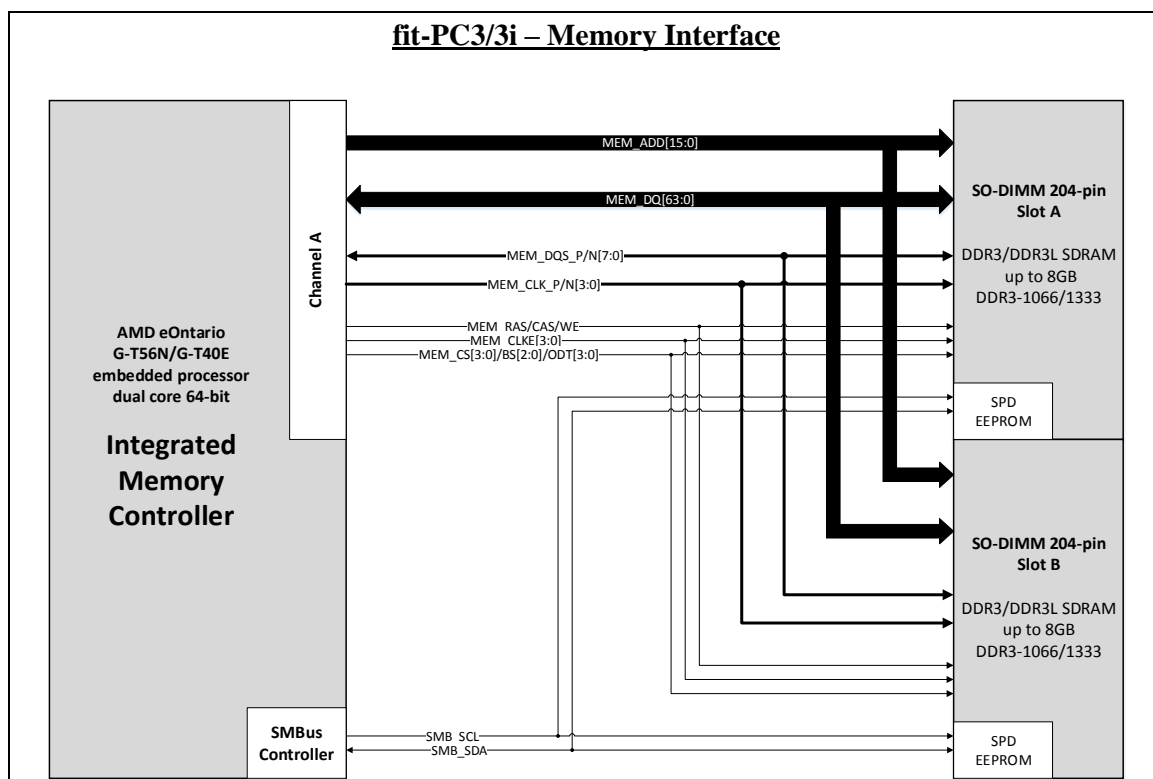
### 3.4.1 Processor Integrated Memory Controller

Processor's Integrated Memory Controller (IMC) supports DDR3 and DDR3L protocols with single 64-bit wide channel, accessing one or two DIMMs. The IMC supports one or two, unbuffered non-ECC DDR3/DDR3L 204-pin SO-DIMMs.

G-T56N supports both DDR3/DDR3L-1066 and DDR3/DDR3L-1333 memories speeds.

G-T40E supports up to DDR3/DDR3L-1066 memories speeds.

**Figure 9 – Memory Interface**



Fit-PC3/3i system architecture provides support for 1.5V (DDR3) and 1.35V (DDR3L) power supplied SO-DIMMs. The adjustment of power rail for the memories and Memory Host Controller IOs is performed automatically without user or BIOS intervention. During boot SMBus Host Controller reads serial presence-detect (SPD) EEPROM on each SO-DIMM and adjust the voltage according to memory type. In case DDR3/DDR3L mixed memory modules are placed, the BUCK regulator will generate 1.5V output voltage, which may cause undesired behavior or permanent damage of the modules, unless DDR3L memory is tolerant to such voltages.

**Note:** It is important to keep both slots populated with the same memory technology.

### 3.4.2 System Supported Memory

- DDR3 SDRAM memory with unbuffered SO-DIMM 204-pin modules
- Up to 16GB (2x 8GB) DDR3/DDR3L-1066/1333
- Supports up to two dual-rank SO-DIMMs
- Non-ECC, Unbuffered DDR3 SO-DIMMs only
- System Memory Interface I/O Voltage of 1.5V and 1.35V
- DDR3 SDRAM SO-DIMMs running at 1.5 V and 1.35V
- Single 64-bit wide channel
- Theoretical maximum memory bandwidth of:
  - 8.53 GB/s assuming DDR3 SDRAM 1066 MT/s
  - 10.65 GB/s assuming DDR3 SDRAM 1333 MT/s
- 1Gb, 2Gb, and 4Gb DDR3 SDRAM device technologies are supported
  - Standard 1-Gb, 2-Gb, and 4-Gb technologies and addressing are supported for x16 and x8 devices. There is no support for memory modules with different technologies or capacities on opposite sides of the same memory module. If one side of a memory module is populated, the other side is either identical or empty.
- On-Die Termination (ODT)

**Table 10 – Supported Memory Technologies**

| Raw Card Version | DIMM Capacity | DRAM Device Technology | DRAM Organization | # of DRAM Devices | # of Physical Device Ranks | # of Row/Col Address Bits | # of Banks Inside DRAM | Page Size |
|------------------|---------------|------------------------|-------------------|-------------------|----------------------------|---------------------------|------------------------|-----------|
| A                | 2 GB          | 2 Gb                   | 128 M x 16        | 8                 | 2                          | 14/10                     | 8                      | 8K        |
|                  | 4 GB          | 4 Gb                   | 256 M x 16        | 8                 | 2                          | 15/10                     | 8                      | 8K        |
| B                | 1 GB          | 1 Gb                   | 128 M x 8         | 8                 | 1                          | 14/10                     | 8                      | 8K        |
|                  | 2 GB          | 2 Gb                   | 256 M x 8         | 8                 | 1                          | 15/10                     | 8                      | 8K        |
|                  | 4 GB          | 4 Gb                   | 512 M x 8         | 8                 | 1                          | 16/10                     | 8                      | 8K        |
| C                | 1 GB          | 2 Gb                   | 128 M x 16        | 4                 | 1                          | 14/10                     | 8                      | 8K        |
|                  | 2 GB          | 4 Gb                   | 256 M x 16        | 4                 | 1                          | 15/10                     | 8                      | 8K        |
| F                | 2 GB          | 1 Gb                   | 128 M x 8         | 16                | 2                          | 14/10                     | 8                      | 8K        |
|                  | 4 GB          | 2 Gb                   | 256 M x 8         | 16                | 2                          | 15/10                     | 8                      | 8K        |
|                  | 8 GB          | 4 Gb                   | 512 M x 8         | 16                | 2                          | 16/ 10                    | 8                      | 8K        |

**Table 11 – Supported Max Memory Size per SO-DIMM**

| Platform | Package | Memory      | Max Size per DIMM [GB] |
|----------|---------|-------------|------------------------|
| Mobile   | rPGA    | SODIMM RC A | 4                      |
|          |         | SODIMM RC B | 4                      |
|          |         | SODIMM RC C | 2                      |
|          |         | SODIMM RC F | 8                      |

### 3.4.3 System Memory Timing Support

The IMC supports the following Speed Bins, CAS Write Latency (CWL), and command signal mode timings on the main memory interface:

- tCL = CAS Latency
- tRCD = Activate Command to READ or WRITE Command delay
- tRP = PRECHARGE Command Period
- CWL = CAS Write Latency
- Command Signal modes = 1N indicates a new command may be issued every clock and 2N indicates a new command may be issued every 2 clocks. Command launch mode programming depends on the transfer rate and memory configuration.

**Table 12 – DDR3 System Memory Timing Support**

| Segment                         | Transfer Rate (MT/s) | tCL (tCK) | tRCD (tCK) | tRP (tCK) | CWL (tCK) | DPC | CMD Mode |
|---------------------------------|----------------------|-----------|------------|-----------|-----------|-----|----------|
| Dual Core Standard Voltage (SV) | 1066                 | 7         | 7          | 7         | 6         | 1   | 1N/2N    |
|                                 |                      | 8         | 8          | 8         | 6         | 1   | 1N/2N    |
|                                 | 1333                 | 9         | 9          | 9         | 7         | 1   | 1N/2N    |

### 3.4.4 System Memory Organization Modes

The IMC supports single-channel organization mode only.

### 3.4.5 Rules for Populating Memory Slots

The frequency and latency timings of the system memory is the lowest supported frequency and slowest supported latency timings of all memory SO-DIMM modules placed in the system.

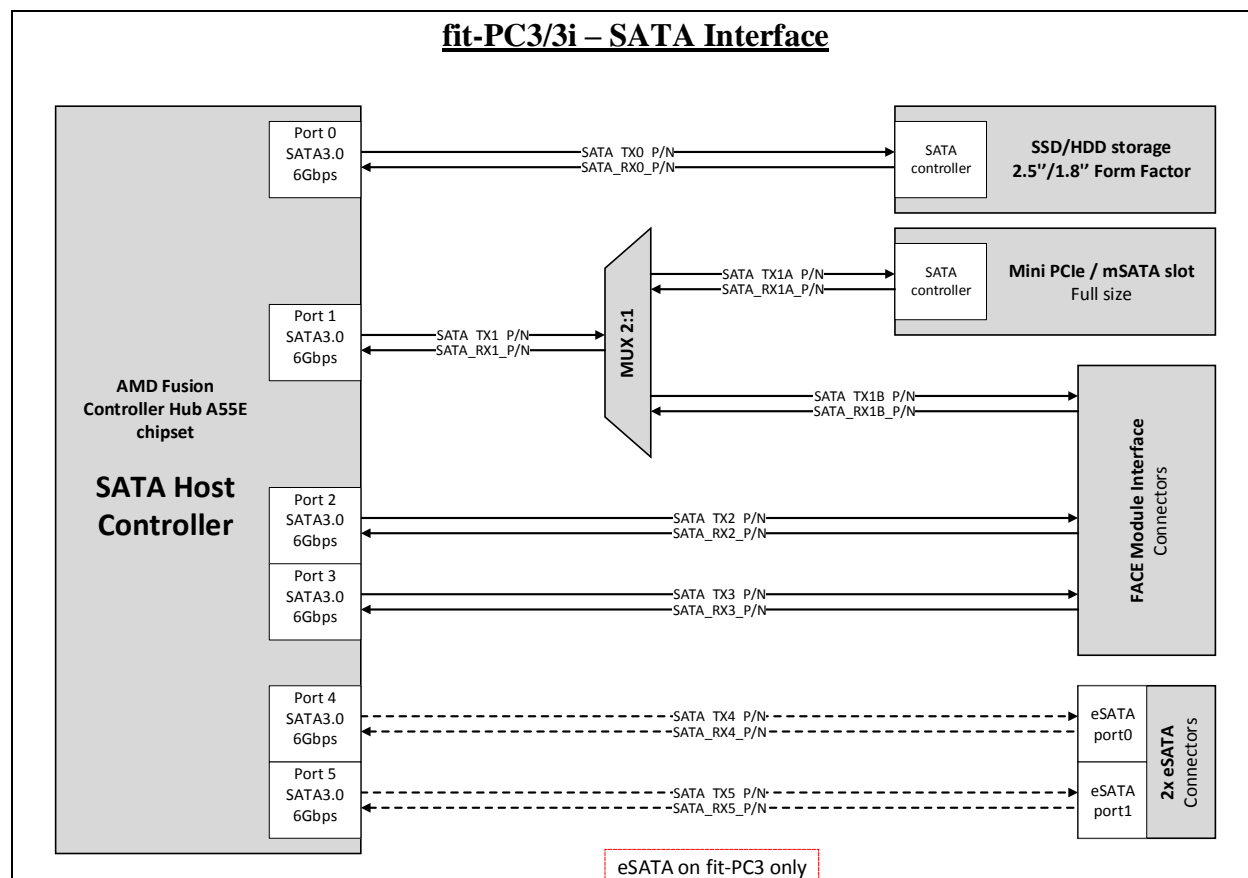
### 3.5 Storage

Fit-PC3 and fit-PC3i supports various types of storage devices due to advanced FCH SATA Host Controller capabilities and I/O availability, described in section 3.3.4. Supported devices include HDD and SSD storage devices in 2.5" form factor. HDD limited to 5400rpm only due to power dissipation reasons. mSATA NAND Flash solid state drive modules supported as well and share mini PCIe full size slot. For detailed system architecture refer to section 6.1 .

In addition, fit-PC3 offers two eSATA connectors, available on the back panel which allow connection of external storage drives. eSATA connectivity provide signaling only, when power to the external drives must be supplied externally.

Fit-PC3 and fit-PC3i, SATA system diagram is show in **Figure 10 – SATA Interface**.

**Figure 10 – SATA Interface**



### 3.5.1 Certified storage devices

#### 3.5.1.1 HDD examples

Table 13 – WD Scorpio Blue HDD series

| Specifications                                  | 1 TB                   | 1 TB                                     | 750 GB                 | 750 GB                                   | 500 GB                                   |
|---|------------------------|--|------------------------|--|--|
| Model number                                    | WD10SPCX               | WD10JPVX<br>WD10JPVT                     | WD7500LPCX             | WD7500BPVX<br>WD7500BPVT                 | WD5000LPVX<br>WD5000LPVT                 |
| Interface                                       | SATA 6 Gb/s            | SATA 6 Gb/s (JPVX)<br>SATA 3 Gb/s (JPVT) | SATA 6 Gb/s            | SATA 6 Gb/s (BPVX)<br>SATA 3 Gb/s (BPVT) | SATA 6 Gb/s (LPVX)<br>SATA 3 Gb/s (LPVT) |
| Formatted capacity <sup>1</sup>                 | 1,000,204 MB           | 1,000,204 MB                             | 750,156 MB             | 750,156 MB                               | 500,107 MB                               |
| User sectors per drive                          | 1,953,525,168          | 1,953,525,168                            | 1,465,149,168          | 1,465,149,168                            | 976,773,168                              |
| Advanced Format (AF)                            | Yes                    | Yes                                      | Yes                    | Yes                                      | Yes                                      |
| Form factor                                     | 2.5-inch               | 2.5-inch                                 | 2.5-inch               | 2.5-inch                                 | 2.5-inch                                 |
| RoHS compliant <sup>2</sup>                     | Yes                    | Yes                                      | Yes                    | Yes                                      | Yes                                      |
| <b>Performance</b>                              |                        |  |                        |  |  |
| Data transfer rates                             |                        |  |                        |  |  |
| Interface speed                                 | 6 Gb/s                 | 6 Gb/s (JPVX)<br>3 Gb/s (JPVT)           | 6 Gb/s                 | 6 Gb/s (BPVX)<br>3 Gb/s (BPVT)           | 6 Gb/s (LPVX)<br>3 Gb/s (LPVT)           |
| Internal transfer rate (max)                    | 140 MB/s               | 144 MB/s                                 | 140 MB/s               | 138 MB/s                                 | 147 MB/s                                 |
| Cache (MB)                                      | 16                     | 8  | 16                     | 8  | 8  |
| Average latency (ms)                            | 5.5                    | 5.5                                      | 5.5                    | 5.5                                      | 5.5                                      |
| Rotational speed (RPM)                          | 5400                   | 5400                                     | 5400                   | 5400                                     | 5400                                     |
| Average drive ready time (sec)                  | 2.8                    | 3.0 (JPVX) / <3.5 (JPVT)                 | 2.8                    | 3.0 (BPVX) / 4.0 (BPVT)                  | 2.8 (LPVX) / <3.5 (LPVT)                 |
| <b>Reliability/Data Integrity</b>               |                        |  |                        |  |  |
| Load/unload cycles <sup>3</sup>                 | 600,000                | 600,000                                  | 600,000                | 600,000                                  | 600,000                                  |
| Non-recoverable read errors per bits read       | <1 in 10 <sup>14</sup> | <1 in 10 <sup>14</sup>                   | <1 in 10 <sup>14</sup> | <1 in 10 <sup>14</sup>                   | <1 in 10 <sup>14</sup>                   |
| Limited warranty (years) <sup>4</sup>           | 2                      | 2  | 2                      | 2  | 2  |
| <b>Power Management</b>                         |                        |  |                        |  |  |
| 5VDC ±10% (A, peak)                             | 1.00                   | 1.00 (JPVX) / 0.900 (JPVT)               | 1.00                   | 1.00 (BPVX) / 0.975 (BPVT)               | 1.00 (LPVX) / 0.900 (LPVT)               |
| Average power requirements (W)                  |                        |  |                        |  |  |
| Read/Write                                      | 1.7                    | 1.4                                      | 1.7                    | 1.6                                      | 1.4                                      |
| Idle  | 0.57                   | 0.59                                     | 0.57                   | 0.65                                     | 0.55                                     |
| Standby/Sleep                                   | 0.18                   | 0.18                                     | 0.18                   | 0.20                                     | 0.13                                     |
| <b>Environmental Specifications<sup>5</sup></b> |                        |  |                        |  |  |
| Temperature (°C)                                |                        |  |                        |  |  |
| Operating                                       | 0 to 60                | 0 to 60                                  | 0 to 60                | 0 to 60                                  | 0 to 60                                  |
| Non-operating                                   | -40 to 65              | -40 to 65                                | -40 to 65              | -40 to 65                                | -40 to 65                                |
| Shock (Gs)                                      |                        |  |                        |  |  |
| Operating (2 ms, read)                          | 350                    | 400                                      | 350                    | 350                                      | 400                                      |
| Non-operating                                   | 1000 (2 ms)            | 1000 (2 ms)                              | 1000 (2 ms)            | 1000 (2 ms)                              | 1000 (2 ms)                              |
| Acoustics (dBA) <sup>6</sup>                    |                        |  |                        |  |  |
| Idle  | 20                     | 24                                       | 20                     | 24                                       | 17                                       |
| Seek (average)                                  | 21                     | 25                                       | 21                     | 25                                       | 22                                       |
| <b>Physical Dimensions</b>                      |                        |  |                        |  |  |
| Height (in./mm, max)                            | 0.28/7.0               | 0.374/9.50                               | 0.28/7.0               | 0.374/9.50                               | 0.28/7.0                                 |
| Length (in./mm, max)                            | 3.94/100.20            | 3.94/100.20                              | 3.94/100.20            | 3.94/100.20                              | 3.94/100.20                              |
| Width (in./mm, ± .01 in.)                       | 2.75/69.85             | 2.75/69.85                               | 2.75/69.85             | 2.75/69.85                               | 2.75/69.85                               |
| Weight (lb./kg, ± 10%)                          | 0.21/0.09              | 0.27/0.12                                | 0.21/0.09              | 0.34/0.15                                | 0.20/0.09                                |

Table 14 – WD Scorpio Blue HDD series (cont.)

| Specifications                                  | 500 GB                 | 500 GB                 | 320 GB                                   | 320 GB                 | 250 GB                                   | 250 GB                 |
|---|------------------------|------------------------|--|------------------------|--|------------------------|
| Model number                                    | WD5000MPCK             | WD5000BPVT             | WD3200LPVX<br>WD3200LPVT                 | WD3200BPVT             | WD2500LPVX<br>WD2500LPVT                 | WD2500BPVT             |
| Interface                                       | SATA 6 Gb/s            | SATA 3 Gb/s            | SATA 6 Gb/s (LPVX)<br>SATA 3 Gb/s (LPVT) | SATA 3 Gb/s            | SATA 6 Gb/s (LPVX)<br>SATA 3 Gb/s (LPVT) | SATA 3 Gb/s            |
| Formatted capacity <sup>1</sup>                 | 500,107 MB             | 500,107 MB             | 320,072 MB                               | 320,072 MB             | 250,059 MB                               | 250,059 MB             |
| User sectors per drive                          | 976,773,168            | 976,773,168            | 625,142,448                              | 625,142,448            | 488,397,168                              | 488,397,168            |
| Advanced Format (AF)                            | Yes                    | Yes                    | Yes                                      | Yes                    | Yes                                      | Yes                    |
| Form factor                                     | 2.5-inch               | 2.5-inch               | 2.5-inch                                 | 2.5-inch               | 2.5-inch                                 | 2.5-inch               |
| RoHS compliant <sup>2</sup>                     | Yes                    | Yes                    | Yes                                      | Yes                    | Yes                                      | Yes                    |
| <b>Performance</b>                              |                        |                        |  |                        |  |                        |
| Data transfer rates                             |                        |                        |  |                        |  |                        |
| Interface speed                                 | 6 Gb/s                 | 3 Gb/s                 | 6 Gb/s (LPVX)<br>3 Gb/s (LPVT)           | 3 Gb/s                 | 6 Gb/s (LPVX)<br>3 Gb/s (LPVT)           | 3 Gb/s                 |
| Internal transfer rate (max)                    | 145 MB/s               | 136 MB/s               | 147 MB/s (LPVX)<br>109 MB/s (LPVT)       | 116 MB/s               | 147 MB/s (LPVX)<br>109 MB/s (LPVT)       | 116 MB/s               |
| Cache (MB)                                      | 16                     | 8                      | 8  | 8                      | 8  | 8                      |
| Average latency (ms)                            | 5.5                    | 5.5                    | 5.5                                      | 5.5                    | 5.5                                      | 5.5                    |
| Rotational speed (RPM)                          | 5400                   | 5400                   | 5400                                     | 5400                   | 5400                                     | 5400                   |
| Average drive ready time (sec)                  | 2.8                    | 4.0                    | 2.8 (LPVX) / <3.5 (LPVT)                 | 4.0                    | 2.8 (LPVX) / <3.5 (LPVT)                 | 4.0                    |
| <b>Reliability/Data Integrity</b>               |                        |                        |  |                        |  |                        |
| Load/unload cycles <sup>3</sup>                 | 600,000                | 600,000                | 600,000                                  | 600,000                | 600,000                                  | 600,000                |
| Non-recoverable read errors per bits read       | <1 in 10 <sup>14</sup> | <1 in 10 <sup>14</sup> | <1 in 10 <sup>14</sup>                   | <1 in 10 <sup>14</sup> | <1 in 10 <sup>14</sup>                   | <1 in 10 <sup>14</sup> |
| Limited warranty (years) <sup>4</sup>           | 2                      | 2                      | 2  | 2                      | 2  | 2                      |
| <b>Power Management</b>                         |                        |                        |  |                        |  |                        |
| 5VDC ±10% (A, peak)                             | 0.900                  | 0.950                  | 1.00 (LPVX) / 0.900 (LPVT)               | 1.00                   | 1.00 (LPVX) / 0.900 (LPVT)               | 1.00                   |
| Average power requirements (W)                  |                        |                        |  |                        |  |                        |
| Read/Write                                      | 1.5                    | 1.6                    | 1.4                                      | 2.5                    | 1.4                                      | 2.5                    |
| Idle  | 0.55                   | 0.65                   | 0.55                                     | 0.85                   | 0.55                                     | 0.85                   |
| Standby/Sleep                                   | 0.15                   | 0.20                   | 0.13                                     | 0.20                   | 0.13                                     | 0.20                   |
| <b>Environmental Specifications<sup>5</sup></b> |                        |                        |  |                        |  |                        |
| Temperature (°C)                                |                        |                        |  |                        |  |                        |
| Operating                                       | 0 to 60                | 0 to 60                | 0 to 60                                  | 0 to 60                | 0 to 60                                  | 0 to 60                |
| Non-operating                                   | -40 to 65              | -40 to 65              | -40 to 65                                | -40 to 65              | -40 to 65                                | -40 to 65              |
| Shock (Gs)                                      |                        |                        |  |                        |  |                        |
| Operating (2 ms, read)                          | 400                    | 350                    | 400                                      | 350                    | 400                                      | 350                    |
| Non-operating                                   | 1000 (2 ms)            | 1000 (2 ms)            | 1000 (2 ms)                              | 1000 (2 ms)            | 1000 (2 ms)                              | 1000 (2 ms)            |
| Acoustics (dBA) <sup>6</sup>                    |                        |                        |  |                        |  |                        |
| Idle  | 15                     | 22                     | 17                                       | 22                     | 17                                       | 22                     |
| Seek (average)                                  | 17                     | 25                     | 22                                       | 25                     | 22                                       | 25                     |
| <b>Physical Dimensions</b>                      |                        |                        |  |                        |  |                        |
| Height (in./mm, max)                            | 0.20/5.0               | 0.374/9.50             | 0.28/7.0                                 | 0.374/9.50             | 0.28/7.0                                 | 0.374/9.50             |
| Length (in./mm, max)                            | 3.95/100.30            | 3.94/100.20            | 3.94/100.20                              | 3.94/100.20            | 3.94/100.20                              | 3.94/100.20            |
| Width (in./mm, ±.01 in.)                        | 2.75/69.85             | 2.75/69.85             | 2.75/69.85                               | 2.75/69.85             | 2.75/69.85                               | 2.75/69.85             |
| Weight (lb./kg, ± 10%)                          | 0.16/0.07              | 0.22/0.10              | 0.20/0.09                                | 0.22/0.10              | 0.20/0.09                                | 0.22/0.10              |

Table 15 – Hitachi CinemaStar C5K750 HDD models

|   |  |   |
|---|--|---|
| <b>Model(s)</b>                               |  | HCC547575A9E380<br>HCC547564A9E380<br>HCC547550A9E380 |
| <b>Configuration</b>                          |  |   |
| Interface                                     |  | SATA 3Gb/s  |
| Capacity (GB) <sup>1</sup>                    |  | 750 / 640 / 500                                       |
| Sector size (bytes) <sup>2</sup>              |  | 512e  |
| Recording zones                               |  | 24  |
| Max. areal density (Gbits/sq. in.)            |  | 492   |
| <b>Performance</b>                            |  |   |
| Data buffer (MB) <sup>3</sup>                 |  | 8   |
| Rotational speed (RPM)                        |  | 5400  |
| Latency average (ms)                          |  | 5.5   |
| Media transfer rate (Mbits/sec, max.)         |  | 996   |
| Interface transfer rate (MB/sec, max.)        |  | 300   |
| Seek time, read (ms, typical) <sup>4</sup>    |  | 15  |
| <b>Reliability</b>                            |  |   |
| Load/unload cycles                            |  | 600,000   |
| Power on Hours (POH) per month                |  | 730   |
| Availability <sup>5</sup> (hrs/day x days/wk) |  | 24x7  |
| <b>Power</b>                                  |  |   |
| Requirement                                   |  | +5 VDC (+/-5%)  |
| Startup (W, peak, max.)                       |  | 3.5   |
| Operating <sup>6</sup> (W, avg.)              |  | 1.5   |
| Low power idle (W, avg.)                      |  | 0.5   |
| <b>Physical size</b>                          |  |   |
| z-height (mm)                                 |  | 9.5   |
| Dimensions (width x depth, mm)                |  | 70 x 100  |
| Weight (g, typical)                           |  | 102   |
| <b>Environmental (operating)</b>              |  |   |
| Shock (half-sine wave)                        |  | 400G (2ms), 225G (1ms)                                |
| Operating temperature <sup>7</sup>            |  | 0° to 70° C   |
| <b>Environmental (non-operating)</b>          |  |   |
| Shock (half-sine wave)                        |  | 1000G (1ms)   |
| Ambient temperature                           |  | -40° to 65° C   |
| <b>Acoustics (A-weighted sound power)</b>     |  |   |
| Idle (Bels, typical)                          |  | 2.4   |
| Seek (Bels, typical)                          |  | 2.5   |

Table 16 – Seagate Momentus HDD series

## Seagate® Momentus® 2.5" Internal Drive

Instant Add-on Storage

**Interface** SATA

**Capacities** 250GB, 320GB, 500GB, 640GB, 750GB

### Momentus LP Drive – Energy Efficient, High Capacity Storage

Engineered specifically for low-power applications, the Momentus LP internal drive has a 5400RPM spindle speed and a 8MB cache to provide energy-efficient performance at whisper-quiet acoustic levels. With reduced power consumption and heat generation, this drive will reduce power costs up to 50% over the life of the system compared to standard drives. It is optimized for standard laptops and small form factor PCs.

- 5400RPM
- 8MB cache
- SATA 3Gb/s interface with Native Command Queueing
- QuietStep™ technology enables ultra-quiet load/unload acoustics
- Perpendicular recording technology increases performance and reliability

### 3.5.1.2 mSATA SSD examples

Table 17 – Micron mSATA NAND Flash SSD

|  |  |
|--|--|
|   | <b>M500 mSATA NAND Flash SSD<br/>Features</b>  |
| <h2>M500 mSATA NAND Flash SSD</h2>   |  |
| <b>MTFDDAT120MAV, MTFDDAT240MAV,<br/>MTFDDAT480MAV</b>   |  |
| <b>Features</b>  | <ul style="list-style-type: none"> <li>• Reliability <ul style="list-style-type: none"> <li>– MTTF: 1.2 million device hours<sup>3</sup></li> <li>– Static and dynamic wear leveling</li> <li>– Uncorrectable bit error rate (UBER): &lt;1 sector per 10<sup>15</sup> bits read</li> </ul> </li> <li>• Low power consumption <ul style="list-style-type: none"> <li>– 150mW TYP<sup>4</sup></li> </ul> </li> <li>• Endurance: Total bytes written (TBW) – 72TB</li> <li>• Capacity<sup>5</sup> (unformatted): 120GB, 240GB, 480GB</li> <li>• Mechanical <ul style="list-style-type: none"> <li>– mSATA connector: 3.3V ±5%</li> <li>– Caseless design: 50.80mm x 29.85mm x 3.75mm</li> <li>– Weight: 10g (MAX)</li> </ul> </li> <li>• Secure firmware update with digitally signed firmware image</li> <li>• Operating temperature <ul style="list-style-type: none"> <li>– Commercial (0°C to +70°C)<sup>6</sup></li> </ul> </li> </ul> |
| <ul style="list-style-type: none"> <li>• Micron® 20nm MLC NAND Flash</li> <li>• RoHS-compliant package</li> <li>• SATA 6 Gb/s interface</li> <li>• TCG/Opal 2.0-compliant self-encrypting drive (SED)</li> <li>• Hardware-based AES-256 encryption engine</li> <li>• ATA modes supported <ul style="list-style-type: none"> <li>– PIO mode 3, 4</li> <li>– Multiword DMA mode 0, 1, 2</li> <li>– Ultra DMA mode 0, 1, 2, 3, 4, 5</li> </ul> </li> <li>• Industry-standard, 512-byte sector size support</li> <li>• Device Sleep (DEVSLEEP), extreme low power mode</li> <li>• Native command queuing support with 32-command slot support</li> <li>• ATA-8 ACS2 command set compliant</li> <li>• ATA security feature command set and password login support</li> <li>• Secure erase (data page) command set: fast and secure erase</li> <li>• Sanitize device feature set support</li> <li>• Self-monitoring, analysis, and reporting technology (SMART) command set</li> <li>• Windows 8 drive telemetry</li> <li>• Adaptive thermal monitoring</li> <li>• Performance<sup>1, 2</sup> <ul style="list-style-type: none"> <li>– PCMark® Vantage (HDD test suite score): up to 80,000</li> <li>– Sequential 128KB READ: up to 500 MB/s</li> <li>– Sequential 128KB WRITE: up to 400 MB/s</li> <li>– Random 4KB READ: up to 80,000 IOPS</li> <li>– Random 4KB WRITE: up to 80,000 IOPS</li> <li>– READ/WRITE latency: 5ms/25ms (MAX)</li> </ul> </li> </ul> | <p>Notes:</p> <ol style="list-style-type: none"> <li>1. Typical I/O performance numbers as measured fresh-out-of-box (FOB) using Iometer with a queue depth of 32 and write cache enabled.</li> <li>2. 4KB transfers used for READ/WRITE latency values.</li> <li>3. The product achieves a mean time to failure (MTTF) based on population statistics not relevant to individual units.</li> <li>4. Active average power measured during execution of MobileMark® with DIPM (device-initiated power management) enabled.</li> <li>5. 1GB = 1 billion bytes; formatted capacity is less.</li> <li>6. Drive on-board sensor temperature.</li> </ol>   |
| <p><b>Warranty:</b> Contact your Micron sales representative for further information regarding the product, including product warranties.</p>  |  |

Table 18 – ACPI CMS2G-M SSD

| Specification                |  |
|------------------------------|--|
| Model Name                   | CMS2G-M  |
| Interface                    | SATA III 6Gb/s compatible                                |
| NAND Flash Type              | MLC  |
| Connector Type               | miniPCle mSATA   |
| External DRAM Buffer         | Yes  |
| Capacity                     | 32GB~256GB   |
| Sequential R/W (128KB, Typ.) | Max 530/330 MB/s   |
| Random R/W (4KB, Typ.)       | Max 94K/75K IOPS   |
| Temperature                  | Operating Temp.: 0°C~+70°C<br>Storage Temp.: -40°C~+90°C |
| TRIM                         | Support  |
| S.M.A.R.T. (Health Monitor)  | Support  |
| Security Tool                | -  |
| MTBF                         | > 1.2 million hours                                      |
| Vibration (Operating)        | 20G Peak, 7~2000Hz                                       |
| Shock                        | 1500G, 0.5ms   |
| Dimension (LxWxH)            | 50.8*29.85*3.7mm   |
| Weight                       | 8 gram   |
| Warranty                     | 3 Year   |

## 4 Peripherals

---

### 4.1 USB3.0 Host Controller

Fit-PC3/3i system architecture features USB3.0 connectivity via dedicated Host Controller from Texas Instruments. TUSB7320 is a USB 3.0 xHCI compliant host controller that supports up to four downstream ports. The TUSB7320 interfaces to the host system via a PCIe x1 Gen 2 interface and provides Super Speed, high-speed, full-speed, or low-speed connections on the downstream USB ports.

The TUSB7320 target applications such as desktop and mobile computers, workstations, servers, Add-In Cards and Express Cards implementations and PCI Express based embedded applications.

- **Main Features**
  - USB 3.0 Compliant xHCI Host Controller
  - PCIe x1 Gen2 interface
  - Two downstream ports (USB3.0 and USB2.0 combined)
  - Requires no external flash for default configuration
  - Optional serial EEPROM for custom configuration
  - Internal Spread Spectrum generation
  - Adaptive receiver equalizer
- **Each Downstream Port**
  - May be independently enabled or disabled
  - Has adjustments for transmit swing, De-Emphasis, and Equalization settings
  - May be marked as Removable/Non-Removable
  - Has independent power control and overcurrent detection

## 4.2 Network

The following section provides information about fit-PC3 and fit-PC3i main network components and features.

### 4.2.1 Realtek RTL8111F GbE Controller

Fit-PC3 system architecture incorporates single LAN and fit-PC3i incorporate dual LAN1 and LAN2 implemented with Realtek RTL8111F Gigabit Ethernet Controller. RTL8111F combines a triple-speed IEEE 802.3 compliant Media Access Controller (MAC) with a triple-speed Ethernet transceiver, PCI Express bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8111F offers high-speed transmission over CAT 5 UTP cable.

The RTL8111F supports PCI Express 1.1 bus interface for host communications with power management, and is compliant with the IEEE 802.3u specification for 10/100Mbps Ethernet and the IEEE 802.3ab specification for 1000Mbps Ethernet. It also supports an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space. The RTL8111F features embedded One-Time-Programmable (OTP) memory to replace the external EEPROM.

Advanced Configuration Power management Interface (ACPI) – power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM) – is supported to achieve the most efficient power management possible. In addition to the ACPI feature, remote Wake on LAN is supported in both ACPI and APM (Advanced Power Management) environments.

The RTL8111F is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms and embedded applications.

#### 4.2.1.1 Realtek RTL8111F Features

Realtek RTL8111F Gigabit Ethernet controller main features show below:

- Integrated 10/100/1000 transceiver
- Auto-Negotiation with Next Page capability
- Supports PCI Express 1.1
- Supports pair swap/polarity/skew correction
- Crossover Detection & Auto-Correction
- Wake-on-LAN and remote wake-up support
- Supports Full Duplex flow control (IEEE 802.3x)
- Supports jumbo frame to 9K bytes
- Fully compliant with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab
- Supports IEEE 802.1P Layer 2 Priority Encoding
- Supports IEEE 802.1Q VLAN tagging
- Supports IEEE 802.3az-2010 (EEE)
- Embedded OTP memory can replace the external EEPROM
- Supports power down/link down power saving/PHY disable mode

- Built-in switching regulator
- Supports Customized LEDs
- Supports 1-Lane 2.5Gbps PCI Express Bus
- Supports hardware ECC (Error Correction Code) function
- Supports hardware CRC (Cyclic Redundancy Check) function

#### 4.2.1.2 LAN Ports LEDs notifications

LAN ports LEDs status notifications shown in the table below:

**Table 19 – LAN ports LEDs status notification**

| LED color | Mode  | Function         |
|-----------|-------|------------------|
| Yellow    | Blink | Activity         |
| Green     | On    | 10/100/1000 Mbps |

### 4.3 Wireless Networks

Fit-PC3 and fit-PC3i current official WLAN + Bluetooth module is Qcom's Q802XRN5B, in a mini PCIe half size form factor. The Q802XRN5B is highly integrated 2.4GHz single band IEEE 802.11b/g/n and Bluetooth 3.0, in a single Realtek RTL8723AE chip with a single PCI-E interface. The integration enhances coordination between 802.11 and Bluetooth, with dynamic power control reducing power consumption, and packet traffic arbitration offering coexistence performance unattainable by two chip solutions.

**Note:** Any other mini PCIe half size RF module can be installed and with relevant driver package can provide wireless infrastructure for the system. Q802XRN5B module uses single PCIe as Host interface for both WLAN and BT communication.

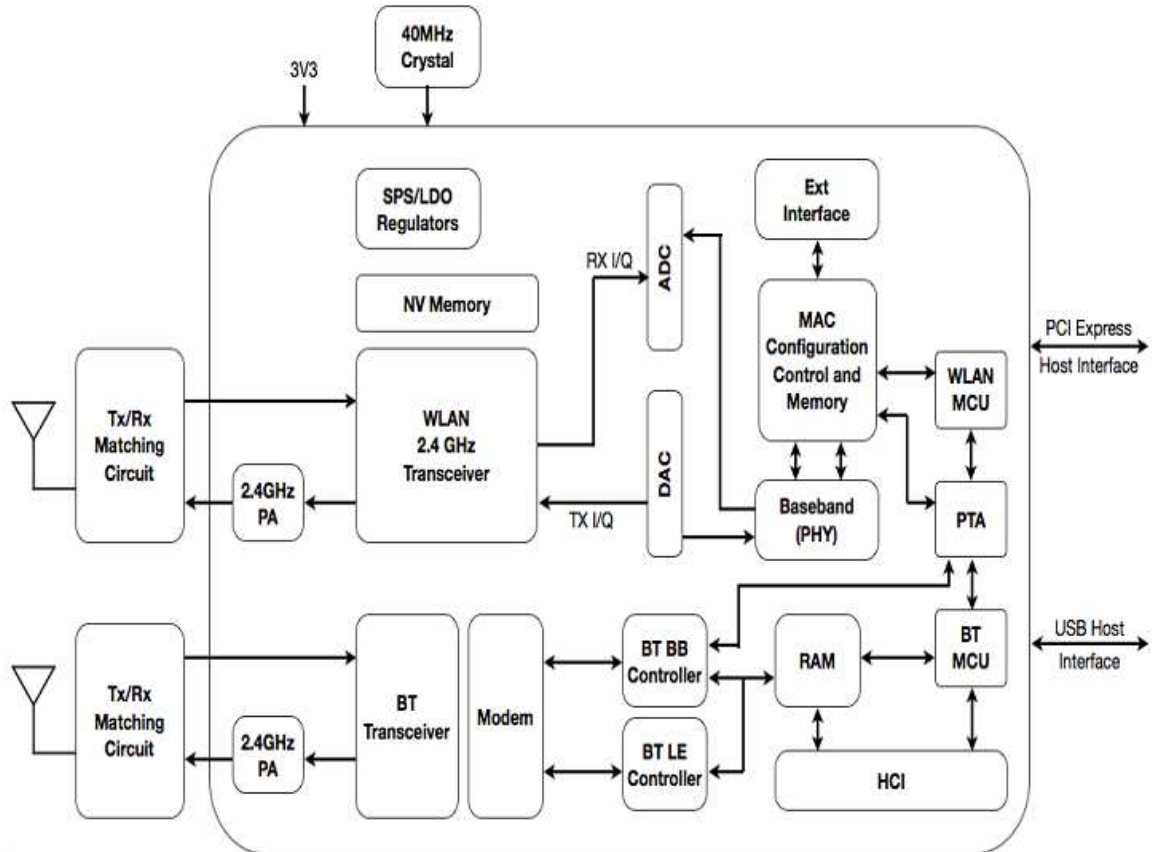
Modules with 2 Host interfaces can be used as well, when PCI Express Host interface used for communication with WLAN part of a baseband chip and USB Host interface used for communication with BT part of a baseband chip.

### 4.4 Wireless Module Features

- Realtek RTL8723AE WLAN + BT
- One Transmit and one Receive path (1T1R)
- 20MHz and 40MHz bandwidth transmission
- Compatible with 802.11n specification
- 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- IEEE 802.11b/g/n compatible WLAN
- IEEE 802.11e QoS Enhancement (WMM)
- IEEE 802.11h TPC, Spectrum Measurement
- Short Guard Interval (400ns)
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- Bluetooth 3.0+HS/2.1+EDR Compliant
- Bluetooth Low Energy supported

- Enhanced BT/WIFI Coexistence Control to improve transmission quality in different profiles

Figure 11 – Wireless Module Q802XRN5B Block Diagram



#### 4.4.1 WLAN

Table 20 – WLAN Channel Assignment

| Channel | Frequency | FCC (US) | IC (CA) | ETSI (EU) | Japan (JP) |
|---------|-----------|----------|---------|-----------|------------|
| 1       | 2412MHz   | V        | V       | V         | V          |
| 2       | 2417MHz   | V        | V       | V         | V          |
| 3       | 2422MHz   | V        | V       | V         | V          |
| 4       | 2427MHz   | V        | V       | V         | V          |
| 5       | 2432MHz   | V        | V       | V         | V          |
| 6       | 2437MHz   | V        | V       | V         | V          |
| 7       | 2442MHz   | V        | V       | V         | V          |
| 8       | 2447MHz   | V        | V       | V         | V          |
| 9       | 2452MHz   | V        | V       | V         | V          |
| 10      | 2457MHz   | V        | V       | V         | V          |
| 11      | 2462MHz   | V        | V       | V         | V          |
| 12      | 2467MHz   |          |         | V         | V          |
| 13      | 2472MHz   |          |         | V         | V          |
| 14      | 2484MHz   |          |         |           | V          |

KEY: US = United States, CA = Canada, EU = European Countries (except France and Spain)

JP = Japan. Many countries and region are currently revising the channel assignment.

V = Supported

#### 4.4.2 Bluetooth

Table 21 – BT Channel Assignment

| Channel      | Frequency       | RF Channel              |
|--------------|-----------------|-------------------------|
| Europe & USA | 2400~2483.5 MHz | Freq.=2402+k MHz k=0~78 |
| Japan        | 2400~2483.5 MHz | Freq.=2402+k MHz k=0~78 |

Most Europe area except Spain and France.

#### 4.4.3 Security

- Complete Security Features- WEP64/128, WPA, WPA2, 802.1x and 802.11i
- Cisco CCx Compliant

## 4.5 Audio

Fit-PC3 and fit-PC3i systems support analog and digital inputs/outputs via standard 3.5" audio jacks. For system audio specifications refer to **Table 5 – Audio Specifications**.

### 4.5.1 Audio Codec General Description

Fit-PC3 and fit-PC3i incorporates Realtek ALC888S-VC2 audio codec. ALC888S-VC2 is a high-performance 7.1+2 Channel High Definition Audio Codec with two independent S/PDIF outputs. It features ten DAC channels that simultaneously support 7.1 sound playback, plus independent stereo sound output (multiple streaming) through the front panel stereo outputs, and integrate two stereo ADCs that can support a stereo microphone, and feature Acoustic Echo Cancellation (AEC), Beam Forming (BF), and Noise Suppression (NS) for voice applications.

The ALC888S-VC2 supports 16/20/24-bit S/PDIF input and output functions with sampling rate of up to 192 kHz, offering easy connection of PCs to high quality consumer electronic products such as digital decoders and Minidisk devices. In addition to the standard (primary) S/PDIF output function, the ALC888S features another independent (secondary) S/PDIF-OUT output and converters that transport digital audio output to a High Definition Media Interface (HDMI) transmitter (becoming more common in high-end PCs).

All analog IO are input and output capable, and headphone amplifiers are also integrated at each analog output. All analog IOs can be re-tasked according to user's definitions, or automatically switched.

The ALC888S-VC2 supports host audio controller from the AMD FCH chipset, and also from any other HDA compatible audio controller. With EAX/Direct Sound 3D/I3DL2/A3D compatibility, and excellent software utilities like environment sound emulation, multiple-band software equalizer and dynamic range control, optional Dolby® Digital Live, DTS® CONNECT™, and Dolby® Home Theater programs, the ALC888S provides an excellent home entertainment package and game experience for PC users.

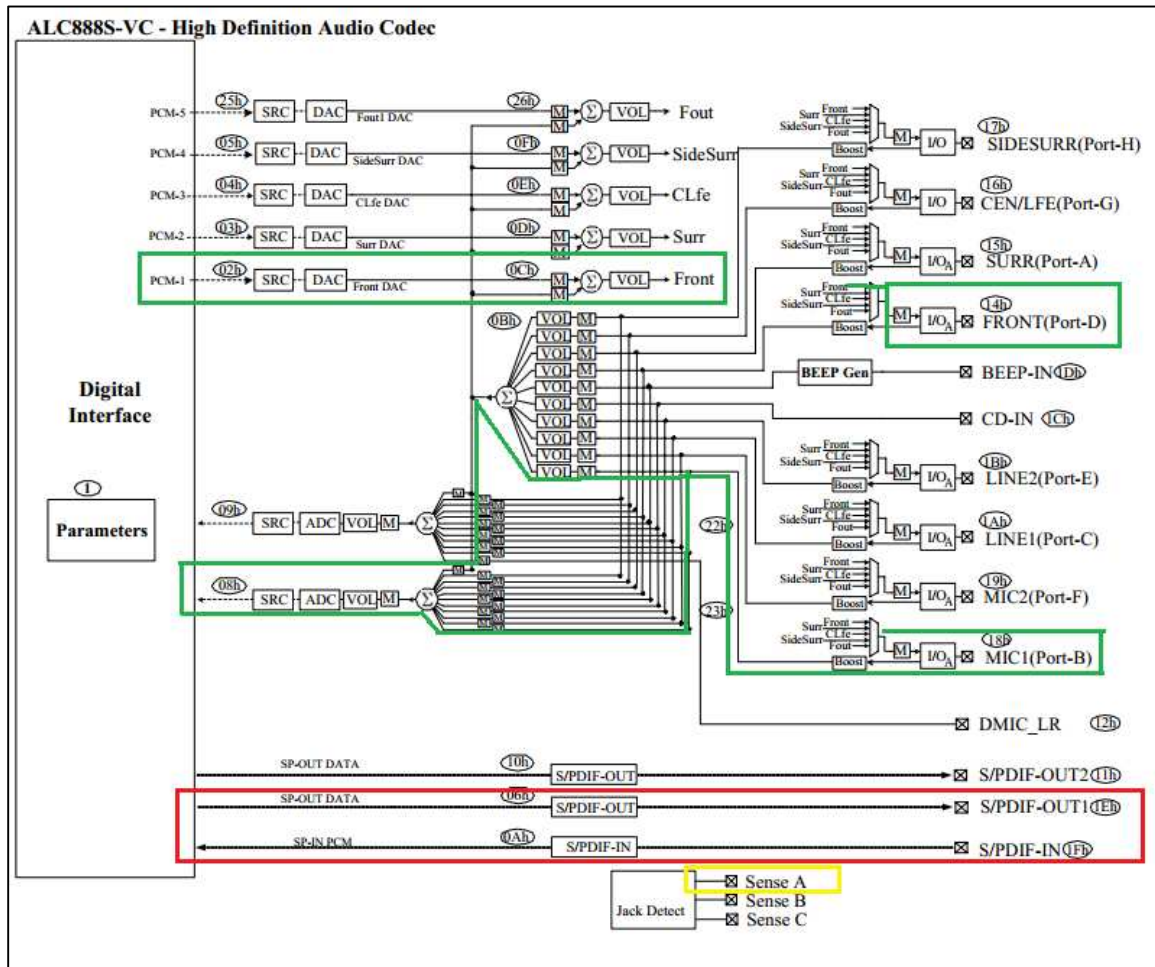
The ALC888S-VC2 meets the current WLP3.10 (Windows Logo Program) and future WLP requirements that become effective from 01 June 2008 (See Enhanced Features section below). The ALC888S-VC2 also conforms to Intel's Audio Codec low power state white paper and is ECR compliant.

### 4.5.2 Audio Codec Features

- Meets premium audio requirements for Microsoft WLP 3.10
- High-performance DACs with 97dB SNR (A-Weighting), ADCs with 90dB SNR (A-Weighting)
- Ten DAC channels support 16/20/24-bit PCM format for 7.1 sound playback, plus 2 channels of independent stereo sound output (multiple streaming) through the front panel output
- Two stereo ADCs support 16/20/24-bit PCM format recording simultaneously
- All DACs supports 16/20/24-bit, 44.1k/48k/96k/192kHz sample rate
- All ADCs supports 16/20/24-bit, 44.1k/48k/96k/192kHz sample rate

- Two independent S/PDIF-OUT converters support 16/20/24-bit, 4.1k/48k/88.2k/96k/192kHz sample rate. One converter for normal S/PDIF output, the other outputs an independent digital stream to the HDMI transmitter
- One S/PDIF-IN converter supports 44.1k/48k/96k/192k Hz sample rate
- Two jack detection pins each designed to detect up to 4 jacks
- Extra jack detection pin for CD input when it is used as an optional line level input, S/PDIF input and output
- Supports legacy analog mixer architecture
- Wide range (–80dB ~ +42dB) volume control with 1.5dB resolution of analog to analog mixer gain
- Software selectable boost gain (+10/+20/+30dB) for analog microphone input
- All analog jacks are stereo input and output re-tasking for analog plug & play
- Built-in headphone amplifiers for each re-tasking jack
- Support stereo digital microphone interface to improve voice quality
- Integrates high pass filter to cancel DC offset generated from digital microphone
- Support low voltage IO for HDA Link (1.5V~3.3V)
- Intel low power ECR compliant, supports power status control for each analog converter and pin widgets, supports jack detection and wake up event in D3 mode

Figure 12 – Audio Codec Functional Block Diagram



The markers in the **Figure 12** apply to audio functionality implemented in Fit-PC3 and fit-PC3i systems and summarized below:

1. Audio Jack Detect function implemented via Sense A:
2. Analog audio output: Port D, FRONT\_HOUT\_R/L (detect via 5k)
3. Analog audio input: Port B, MIC\_IN\_R/L (detected via 20k)
4. Digital audio output: S/PDIF-OUT1
5. Digital audio input: S/PDIF-IN

## 4.6 Super-I/O Controller

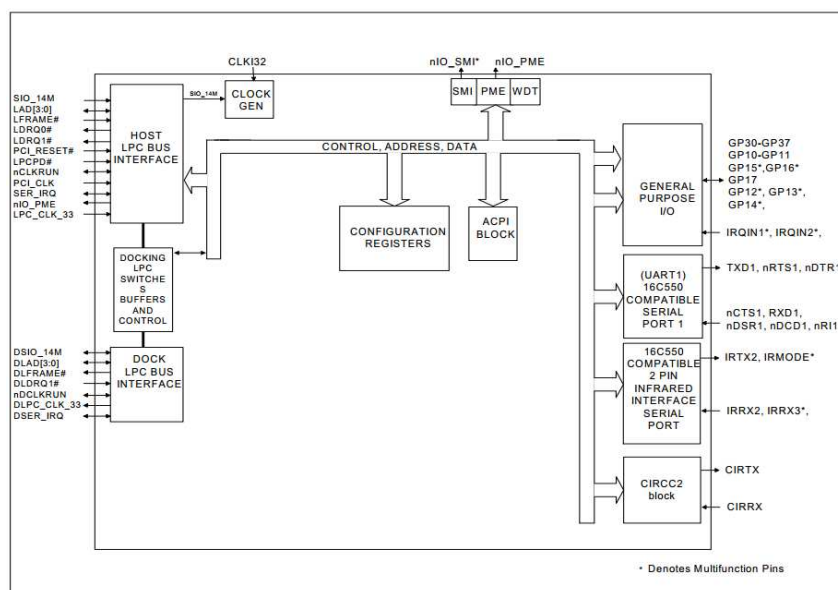
Fit-PC3 design provides RS232 serial communication between Data Terminal Equipment (Host) and Data Communication Equipment (Device) by the means of Super-I/O Controller SMSC SIO1007, which implements LPC Bus to UART Bridge. The SIO1007 implements the LPC interface with the LPC PortSwitch interface. The LPC PortSwitch interface is a hot switchable external docking LPC interface. It also features a full 16bit internally decoded address bus, a Serial IRQ interface with PCI clock support, relocatable configuration ports and three DMA channel options.

The SIO1007 incorporates one complete 8-pin UART. In addition SIO1007 provides a second UART to support a serial Infrared interface that complies with IrDA v1.2 (Fast IR) and several other popular IR formats.

### ■ Main Features

- One full function Serial port
- High Speed UART with Send/Receive 16-Byte FIFOs
- Support 230k and 460k Baud rates
- Programmable baud rate generator
- Modem control circuit
- IR communication controller
- LPC bus Host interface
- LPC PortSwitch interface
- Two IRQ input pins
- PC99a and ACPI 1.0 Compliant
- Intelligent Auto Power Management
- 16x GPIOs

**Figure 13 – SMSC SIO1007 Super-I/O Controller functional block diagram**



## 5 Interfaces

---

### 5.1 PCI Express\*

This section describes the PCI Express interface capabilities of the processor. See the PCI Express Base Specification for details of PCI Express. The processor has one PCI Express controller that can support one external x4 PCI Express Graphics or General Purpose Device. The primary PCI Express Graphics port is referred to as PEG 0.

#### 5.1.1 PCI Express\* Architecture

Compatibility with the PCI addressing model is maintained to ensure that all existing applications and drivers may operate unchanged.

The PCI Express configuration uses standard mechanisms as defined in the PCI Plug-and-Play specification. The processor external graphics ports support Gen 2 speed. The 4-lane PCI Express\* graphics port can operate at either 2.5 GT/s, 5 GT/s.

PCI Express\* Gen 1.1 and Gen 2 uses 8b/10b encoding scheme.

#### 5.1.2 PCI Express\* Specifications

- The port may negotiate down to narrower widths.  
Support for x4/x1 widths for a single PCI Express\* mode.
- 2.5 GT/s and 5.0 GT/s PCI Express\* frequencies are supported.
- Gen1 Raw bit-rate on the data pins of 2.5 GT/s, resulting in a real bandwidth per pair of 250 MB/s given the 8b/10b encoding used to transmit data across this interface. This also does not account for packet overhead and link maintenance.
- Maximum theoretical bandwidth on the interface of 1.25 GB/s in each direction simultaneously, for an aggregate of 2.5 GB/s when x4 Gen 1.
- Gen 2 Raw bit-rate on the data pins of 5.0 GT/s, resulting in a real bandwidth per pair of 500 MB/s given the 8b/10b encoding used to transmit data across this interface. This also does not account for packet overhead and link maintenance.
- Maximum theoretical bandwidth on the interface of 2.5 GB/s in each direction simultaneously, for an aggregate of 5 GB/s when x4 Gen 2.
- PCI Express\* reference clock is 100-MHz differential clock.
- Power Management Event (PME) functions.
- Dynamic width capability.
- Polarity inversion.
- Supports Half Swing “low-power/low-voltage”.

Note: The AMD processor and FCH does not support PCI Express\* Hot-Plug.

### 5.1.3 Mini PCI Express\* Edge Connector

Table 22 – mini PCI Express edge connector pinout

| mini PCI Express edge connector |                 |   |       |                    |   |                   |
|---------------------------------|-----------------|---|-------|--------------------|---|-------------------|
| Pin #                           | Pin Name        | Signal Description  | Pin # | Pin Name           | Signal Description  |                   |
| 1                               | WAKE#           | Open drain, active low signal driven low by a mini PCIe card to reactivate the PCIe link        | 2     | 3.3Vaux            | 3.3V power rail   |                   |
| 3                               | COEX1/Reserved  | Reserved for future wireless coexistence control interface between radios (if needed)           | 4     | GND                | Ground connection   |                   |
| 5                               | COEX2/Reserved  |   | 6     | 1.5V               | 1.5V power rail   |                   |
| 7                               | CLKREQ#         | Clock request - open drain, active low driven by mini PCIe card to request PCIe reference clock | 8     | UIM_PWR/Reserved   | The UIM signals are defined on the system connector to provide the interface between the removable User Identity Module (UIM) Interface - an extension of SIM and WWAN. |                   |
| 9                               | GND             | Ground connection   | 10    | UIM_DATA/Reserved  |   |                   |
| 11                              | REFCLK-         | PCI Express differential reference clock (100 MHz)  | 12    | UIM_CLK/Reserved   |   |                   |
| 13                              | REFCLK+         |   | 14    | UIM_RESET/Reserved |   |                   |
| 15                              | GND             | Ground connection   | 16    | UIM_VPP/Reserved   |   |                   |
| Mechanical Notch Key            |                 |   |       |                    |   |                   |
| 17                              | Reserved/UIM_C8 | Reserved  | 18    | GND                | Ground connection   |                   |
| 19                              | Reserved/UIM_C4 | Reserved  | 20    | W_DISABLE#         | Active low signal when asserted by the system disable radio operation. Reserved for future use.   |                   |
| 21                              | GND             | Ground connection   | 22    | PERST#             | Asserted when power is switched off and also can be used by the system to force HW reset  |                   |
| 23                              | PERn0           | PCI Express differential receive pair   | 24    | 3.3Vaux            | 3.3V power rail   |                   |
| 25                              | PERp0           |   | 26    | GND                | Ground connection   |                   |
| 27                              | GND             | Ground connection   | 28    | 1.5V               | 1.5V power rail   |                   |
| 29                              | GND             | Ground connection   | 30    | SMB_CLK            | Optional SMBus two-wire interface for Host/mini PCIe module communication   |                   |
| 31                              | PETn0           | PCI Express differential transmit pair  | 32    | SMB_DATA           |   |                   |
| 33                              | PETp0           |   | 34    | GND                | Ground connection   |                   |
| 35                              | GND             | Ground connection   | 36    | USB_D-             | USB Host Interface  |                   |
| 37                              | GND             | Ground connection   | 38    | USB_D+             |   |                   |
| 39                              | 3.3Vaux         | 3.3V power rail   | 40    | GND                | Ground connection   |                   |
| 41                              | 3.3Vaux         | 3.3V power rail   | 42    | LED_WWAN#          | Active low output signals are provided to allow status indications to users via system provided LEDs  |                   |
| 43                              | GND             | Ground connection   | 44    | LED_WLAN#          |   |                   |
| 45                              | Reserved        | Reserved for future second PCI Express Lane   | 46    | LED_WPAN#          |   |                   |
| 47                              | Reserved        |   | 48    | 1.5V               |   | 1.5V power rail   |
| 49                              | Reserved        |   | 50    | GND                |   | Ground connection |
| 51                              | Reserved        |   | 52    | 3.3Vaux            |   | 3.3V power rail   |

## 5.2 Unified Media Interface (UMI)

Unified Media Interface (UMI) connects the processor and the FCH.

### 5.2.1 UMI Specifications

- UMI 2.0 support
- Four lanes in each direction
- GT/s point-to-point UMI interface to FCH is supported
- Raw bit-rate on the data pins of 5.0 Gbps, resulting in a real bandwidth per pair of 500 MB/s given the 8b/10b encoding used to transmit data across this interface. Does not account for packet overhead and link maintenance.
- Maximum theoretical bandwidth on interface of 2 GB/s in each direction simultaneously, for an aggregate of 4 GB/s when UMI x4
- Shares 100-MHz PCI Express\* reference clock
- DC coupling – no capacitors between the processor and the FCH
- Polarity inversion
- FCH end-to-end lane reversal across the link
- Supports Half Swing “low-power/low-voltage”

## 5.3 Digital Display Interface

The FCH can drive a number of digital interfaces natively. The Digital Ports can be configured to drive HDMI, DVI, DisplayPort, and Embedded DisplayPort. Fit-PC3/3i system architecture provide HDMI/DVI and/or DisplayPort interfaces on its digital video outputs.

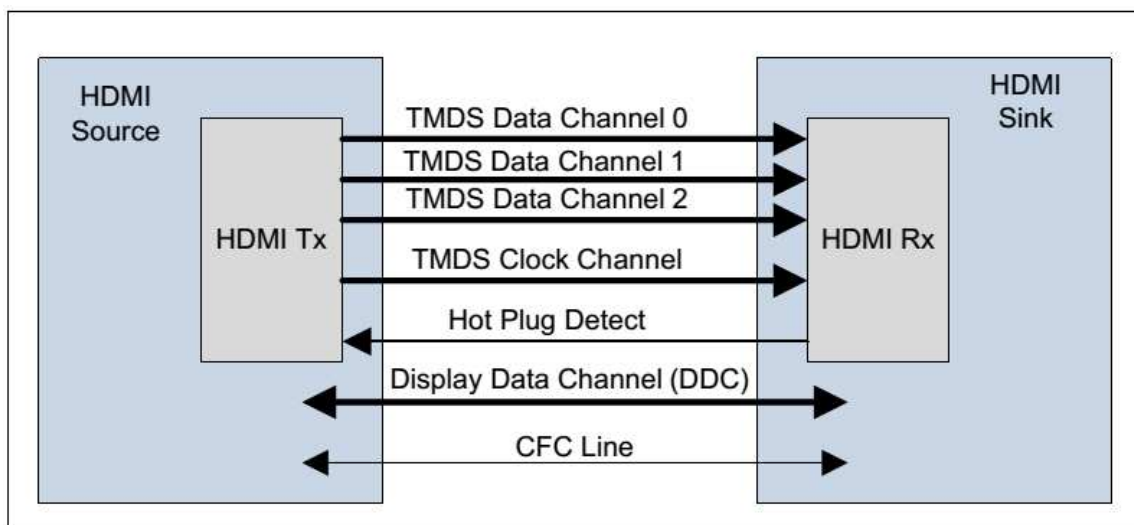
### 5.3.1 High Definition Multimedia Interface (HDMI)

The High-Definition Multimedia Interface (HDMI) is provided for transmitting uncompressed digital audio and video signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays. It can carry high quality multi-channel audio data and all standard and high-definition consumer electronics video formats. HDMI display interface connecting the FCH and display devices utilizes transition minimized differential signaling (TMDS) to carry audiovisual information through the same HDMI cable.

HDMI includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control) which is not supported by the FCH. As shown in **Figure 14** the HDMI cable carries four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA DDC. The DDC is used by an HDMI Source to determine the capabilities and characteristics of the Sink.

Audio, video and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels. The digital display data signals driven natively through the FCH are AC coupled and needs level shifting to convert the AC coupled signals to the HDMI compliant digital signals. FCH HDMI interface is designed as per High-Definition Multimedia Interface Specification 1.4a.

Figure 14 – HDMI Link Diagram



### 5.3.1.1 HDMI Connector

**Table 23** shows the pin assignments of the HDMI external connector on a downstream port on a Source device (fit-PC3/3i), and **Table 24** signal description on the HDMI port.

**Table 23 – Downstream Port HDMI Connector Pinout**

| Pin # | Signal            | Pin # | Signal            |
|-------|-------------------|-------|-------------------|
| 1     | TMDS_DATA2+       | 2     | TMDS_DATA2 Shield |
| 3     | TMDS_DATA2-       | 4     | TMDS_DATA1+       |
| 5     | TMDS_DATA1 Shield | 6     | TMDS_DATA1-       |
| 7     | TMDS_DATA0+       | 8     | TMDS_DATA0 Shield |
| 9     | TMDS_DATA0-       | 10    | TMDS_CLK+         |
| 11    | TMDS_CLK Shield   | 12    | TMDS_CLK-         |
| 13    | CEC               | 14    | Reserved          |
| 15    | DDC_SCL           | 16    | DDC_SDA           |
| 17    | GND               | 18    | PWR_5V            |
| 19    | HPD               |       |                   |

**Table 24 – Downstream Port HDMI Connector Signal Description**

| Pin # | Signal            | Source Direction | Description                       |
|-------|-------------------|------------------|-----------------------------------|
| 1     | TMDS_DATA2+       | Out              | Data differential pair 2 - Link 1 |
| 2     | TMDS_DATA2 Shield | -                |                                   |
| 3     | TMDS_DATA2-       | Out              |                                   |
| 4     | TMDS_DATA1+       | Out              | Data differential pair 1 - Link 1 |
| 5     | TMDS_DATA1 Shield | -                |                                   |
| 6     | TMDS_DATA1-       | Out              |                                   |
| 7     | TMDS_DATA0+       | Out              | Data differential pair 0 - Link 1 |
| 8     | TMDS_DATA0 Shield | -                |                                   |
| 9     | TMDS_DATA0-       | Out              |                                   |
| 10    | TMDS_CLK+         | Out              | Clock differential pair - Link 1  |
| 11    | TMDS_CLK Shield   | -                |                                   |
| 12    | TMDS_CLK-         | Out              |                                   |
| 13    | CEC               | In/Out           | Consumer Electronics Control      |
| 14    | Reserved          | -                |                                   |
| 15    | DDC_SCL           | Out              | EDID Communication channel        |
| 16    | DDC_SDA           | In/Out           |                                   |
| 17    | GND               | -                |                                   |
| 18    | PWR_5V            | Out              | Power                             |
| 19    | HPD               | In               | Hot Plug Detect                   |

### 5.3.2 Digital Video Interface (DVI)

The FCH Digital Ports can be configured to drive DVI-D. DVI uses TMDS for transmitting data from the transmitter to the receiver which is similar to the HDMI protocol but without the audio and CEC. Refer to the HDMI section for more information on the signals and data transmission. To drive DVI-I through the back panel the VGA DDC signals is connected along with the digital data and clock signals from one of the Digital Ports. The digital display data signals driven natively through the FCH are AC coupled and needs level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

### 5.3.3 Display Port Interface (DP)

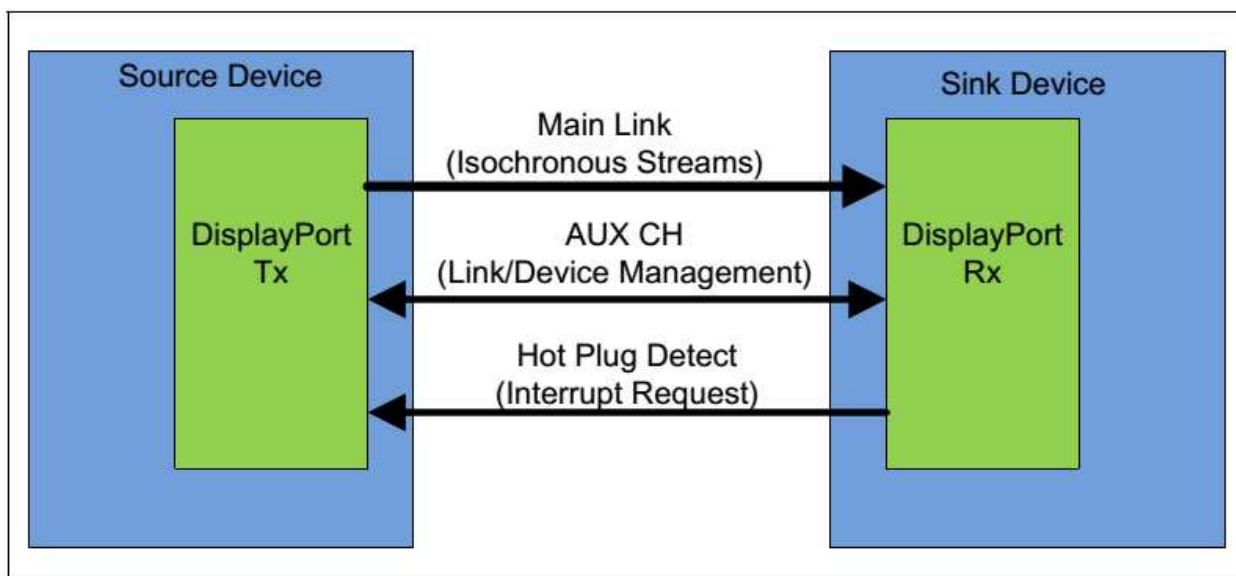
DisplayPort is a digital communication interface that utilizes differential signaling to achieve a high bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays. DisplayPort is also suitable for display connections between consumer electronics devices such as high definition optical disc players, set top boxes, and TV displays.

A DisplayPort consists of a Main Link, Auxiliary channel, and a Hot Plug Detect signal. The Main Link is a unidirectional, high-bandwidth, and low latency channel used for transport of

isochronous data streams such as uncompressed video and audio. The Auxiliary Channel (AUX CH) is a half-duplex bidirectional channel used for link management and device control. The Hot Plug Detect (HPD) signal serves as an interrupt request for the sink device.

FCH is designed as per VESA DisplayPort Standard Version 1.1a.





















**Figure 15 – DP Link Diagram**



### 5.3.3.1 DisplayPort Connector

**Table 25** shows the pin assignments of the DisplayPort external connector on a downstream port on a Source device (fit-PC3/3i) and **Table 26** show the pin assignments of the DisplayPort external connector on an upstream port on a Sink device (DisplayPort Monitor).





















**Table 25 – Downstream Port DP Connector Pinout**

| Pin Number | Signal Type          | Pin Name        | Mating Row Contact Location | Vertically Opposed Connector's Front View   |
|------------|----------------------|-----------------|-----------------------------|---|
| 1          | Out                  | ML_Lane 0(p)    | Top                         |    |
| 2          | GND                  | GND             | Bottom                      |    |
| 3          | Out                  | ML_Lane 0 (n)   | Top                         |    |
| 4          | Out                  | ML_Lane 1 (p)   | Bottom                      |    |
| 5          | GND                  | GND             | Top                         |    |
| 6          | Out                  | ML_Lane 1 (n)   | Bottom                      |    |
| 7          | Out                  | ML_Lane 2 (p)   | Top                         |    |
| 8          | GND                  | GND             | Bottom                      |    |
| 9          | Out                  | ML_Lane 2 (n)   | Top                         |    |
| 10         | Out                  | ML_Lane 3 (p)   | Bottom                      |    |
| 11         | GND                  | GND             | Top                         |    |
| 12         | Out                  | ML_Lane 3 (n)   | Bottom                      |   |
| 13         | CONFIG (see note 1)  | CONFIG1         | Top                         |  |
| 14         | CONFIG (see note 1)  | CONFIG2         | Bottom                      |  |
| 15         | I/O                  | AUX CH (p)      | Top                         |  |
| 16         | GND                  | GND             | Bottom                      |  |
| 17         | I/O                  | AUX CH (n)      | Top                         |  |
| 18         | In                   | Hot Plug Detect | Bottom                      |  |
| 19         | RTN                  | Return          | Top                         |  |
| 20         | PWR Out (see note 2) | DP_PWR          | Bottom                      |  |

Notes:

1. Pins 13 and 14 must be connected to ground through a pull-down device. External devices and cable assemblies must be designed to not rely on a low impedance ground path from these pins.
2. Pin 20, PWR Out, must provide +3.3V+/-10% with a maximum current of 500mA and a minimum power capability of 1.5 watts.

Table 26 – Upstream Port DP Connector Pinout

| Pin Number | Signal Type            | Pin Name        | Mating Row Contact Location | Vertically Opposed Connector's Front View   |   |
|------------|------------------------|-----------------|-----------------------------|---|---|
| 1          | In                     | ML_Lane 3(n)    | Top                         |    |   |
| 2          | GND                    | GND             | Bottom                      |   |    |
| 3          | In                     | ML_Lane 3 (p)   | Top                         |    |   |
| 4          | In                     | ML_Lane 2 (n)   | Bottom                      |   |    |
| 5          | GND                    | GND             | Top                         |    |   |
| 6          | In                     | ML_Lane 2 (p)   | Bottom                      |   |    |
| 7          | In                     | ML_Lane 1 (n)   | Top                         |    |   |
| 8          | GND                    | GND             | Bottom                      |   |    |
| 9          | In                     | ML_Lane 1 (p)   | Top                         |    |   |
| 10         | In                     | ML_Lane 0 (n)   | Bottom                      |   |    |
| 11         | GND                    | GND             | Top                         |    |   |
| 12         | In                     | ML_Lane 0 (p)   | Bottom                      |   |    |
| 13         | CONFIG (see note 1)    | CONFIG1         | Top                         |    |   |
| 14         | CONFIG (see note 1)    | CONFIG2         | Bottom                      |   |    |
| 15         | I/O                    | AUX CH (p)      | Top                         |    |   |
| 16         | GND                    | GND             | Bottom                      |   |    |
| 17         | I/O                    | AUX CH (n)      | Top                         |   |   |
| 18         | Out                    | Hot Plug Detect | Bottom                      |   |   |
| 19         | RTN                    | Return          | Top                         |  |   |
| 20         | Power Out (see note 2) | DP_PWR          | Bottom                      |   |  |

Notes:

1. Pins 13 and 14 must be connected to ground through a pull-down device. External devices and cable assemblies must be designed to not rely on a low impedance ground path from these pins.
2. Pin 20, PWR Out, must provide +3.3 volts  $\pm 10\%$  with a maximum current of 500mA and a minimum power capability of 1.5 watts.

**Table 27** shows the wiring of an external cable connector assembly.

**Table 27 – Display Port Cable**

| Receptacle On Source Device |                 |      |             | DisplayPort Standard Cable |      |              |                 |                |      |                 |         | Receptacle on the Sink Device |                 |         |  |
|-----------------------------|-----------------|------|-------------|----------------------------|------|--------------|-----------------|----------------|------|-----------------|---------|-------------------------------|-----------------|---------|--|
|                             |                 |      |             | Source Side Plug           |      | Cable Wiring |                 | Sink Side Plug |      |                 |         |                               |                 |         |  |
| At SOURCE                   |                 | Pin# | At SOURCE   |                            | Pin# | Pin#         | At SINK         |                | Pin# | Sink End Dongle |         | Pin#                          | Sink End Dongle |         |  |
| Signal Type                 |                 |      | Signal Type |                            |      |              | Signal Type     |                |      | Signal Type     |         |                               |                 |         |  |
| Out                         | ML_Lane 0(p)    | 1    | Out         | ML_Lane 0(p)               | 1    | 1            | ML_Lane 3 (n)   | In             | 1    | ML_Lane 3 (n)   | In      | 1                             | ML_Lane 3 (n)   | In      |  |
|                             | GND             | 2    | GND         | GND                        | 2    | 2            | GND             | GND            | 2    | GND             | GND     | 2                             | GND             | GND     |  |
| Out                         | ML_Lane 0 (n)   | 3    | Out         | ML_Lane 0 (n)              | 3    | 3            | ML_Lane 3 (p)   | In             | 3    | ML_Lane 3 (p)   | In      | 3                             | ML_Lane 3 (p)   | In      |  |
| Out                         | ML_Lane 1 (p)   | 4    | Out         | ML_Lane 1 (p)              | 4    | 4            | ML_Lane 2 (n)   | In             | 4    | ML_Lane 2 (n)   | In      | 4                             | ML_Lane 2 (n)   | In      |  |
| GND                         | GND             | 5    | GND         | GND                        | 5    | 5            | GND             | GND            | 5    | GND             | GND     | 5                             | GND             | GND     |  |
| Out                         | ML_Lane 1 (n)   | 6    | Out         | ML_Lane 1 (n)              | 6    | 6            | ML_Lane 2 (p)   | In             | 6    | ML_Lane 2 (p)   | In      | 6                             | ML_Lane 2 (p)   | In      |  |
| Out                         | ML_Lane 2 (p)   | 7    | Out         | ML_Lane 2 (p)              | 7    | 7            | ML_Lane 1 (n)   | In             | 7    | ML_Lane 1 (n)   | In      | 7                             | ML_Lane 1 (n)   | In      |  |
| GND                         | GND             | 8    | GND         | GND                        | 8    | 8            | GND             | GND            | 8    | GND             | GND     | 8                             | GND             | GND     |  |
| Out                         | ML_Lane 2 (n)   | 9    | Out         | ML_Lane 2 (n)              | 9    | 9            | ML_Lane 1 (p)   | In             | 9    | ML_Lane 1 (p)   | In      | 9                             | ML_Lane 1 (p)   | In      |  |
| Out                         | ML_Lane 3 (p)   | 10   | Out         | ML_Lane 3 (p)              | 10   | 10           | ML_Lane 0 (n)   | In             | 10   | ML_Lane 0 (n)   | In      | 10                            | ML_Lane 0 (n)   | In      |  |
| GND                         | GND             | 11   | GND         | GND                        | 11   | 11           | GND             | GND            | 11   | GND             | GND     | 11                            | GND             | GND     |  |
| Out                         | ML_Lane 3 (n)   | 12   | Out         | ML_Lane 3 (n)              | 12   | 12           | ML_Lane 0 (p)   | In             | 12   | ML_Lane 0 (p)   | In      | 12                            | ML_Lane 0 (p)   | In      |  |
| CONFIG                      | CONFIG1         | 13   | CONFIG      | CONFIG1                    | 13   | 13           | CONFIG1         | CONFIG         | 13   | CONFIG1         | CONFIG  | 13                            | CONFIG1         | CONFIG  |  |
| CONFIG                      | CONFIG2         | 14   | CONFIG      | CONFIG2                    | 14   | 14           | CONFIG2         | CONFIG         | 14   | CONFIG2         | CONFIG  | 14                            | CONFIG2         | CONFIG  |  |
| I/O                         | AUX_CH (p)      | 15   | I/O         | AUX_CH (p)                 | 15   | 15           | AUX_CH (p)      | I/O            | 15   | AUX_CH (p)      | I/O     | 15                            | AUX_CH (p)      | I/O     |  |
| GND                         | GND             | 16   | GND         | GND                        | 16   | 16           | GND             | GND            | 16   | GND             | GND     | 16                            | GND             | GND     |  |
| I/O                         | AUX_CH (n)      | 17   | I/O         | AUX_CH (n)                 | 17   | 17           | AUX_CH (n)      | I/O            | 17   | AUX_CH (n)      | I/O     | 17                            | AUX_CH (n)      | I/O     |  |
| In                          | Hot Plug Detect | 18   | In          | Hot Plug Detect            | 18   | 18           | Hot Plug Detect | Out            | 18   | Hot Plug Detect | Out     | 18                            | Hot Plug Detect | Out     |  |
| PWR RTN                     | Return DP_PWR   | 19   |             | Return DP_PWR              | 19   | 19           | Return DP_PWR   |                | 19   | Return DP_PWR   | PWR RTN | 19                            | Return DP_PWR   | PWR RTN |  |
| PWR Out                     | DP_PWR          | 20   |             | DP_PWR                     | 20   | 20           | DP_PWR          |                | 20   | DP_PWR          | PWR Out | 20                            | DP_PWR          | PWR Out |  |

## 5.4 Analog Display Interface

The Analog Port provides RGB signal output along with a HSYNC and VSYNC signal. There is an associated Display Data Channel (DDC) signal pair that is implemented using GPIO pins dedicated to the Analog Port. The intended target device is for a monitor with a VGA connector. Display devices such as LCD panels with analog inputs may work satisfactory but no functionality added to the signals to enhance that capability.

### 5.4.1 VGA DB15 Connector

For an analog interface fit-PC3 and fit-PC3i system design provisions standard DB15 female connector.

**Table 28 – VGA DB15 Connector**

| Pin # | Signal    | Source Direction | Description                      |
|-------|-----------|------------------|----------------------------------|
| 1     | VGA_RED   | Out              | Analog red information           |
| 2     | VGA_GREEN | Out              | Analog green information         |
| 3     | VGA_BLUE  | Out              | Analog blue information          |
| 4     | NC        | -                |                                  |
| 5     | GND       | -                | Ground                           |
| 6     | GND       | -                | Ground                           |
| 7     | GND       | -                | Ground                           |
| 8     | GND       | -                | Ground                           |
| 9     | 5V        | Out              | Power                            |
| 10    | GND       | -                | Ground                           |
| 11    | NC        | -                |                                  |
| 12    | DDC_SDA   | In/Out           | EDID Communication Channel Data  |
| 13    | VGA_HSYNC | Out              | Horizontal sync signal           |
| 14    | VGA_VSYNC | Out              | Vertical sync signal             |
| 15    | DDC_SCL   | Out              | EDID Communication Channel Clock |
| 16    | CHASSIS   | -                |                                  |
| 17    | CHASSIS   | -                |                                  |

**Note:** VGA DB15 connector is not assembled by default but available for custom orders with MOQ (minimum order quantity) > 100 units.

## 5.5 RS232 Serial Interface

Fit-PC3 design provide RS232 serial communication port (COM1) and support seven RS232 signal set by the means of Super-I/O Controller described in 4.6 and RS232/UART line driver transceiver device. Due to small dimension physical port is implemented with ultra mini serial connector with the pinout in the table below.

**Note:** Fit-PC3i design doesn't implement RS232 communication.

**Figure 16 – COM1 Serial Port Pinout**

| Pin # | Signal   | Host Direction | Description  |
|-------|----------|----------------|--|
| 1     | COM1_TX  | Out            | Transmit Data –<br>Carries data from DTE to DCE                                    |
| 2     | COM1_RTS | Out            | Request To Send –<br>DTE requests the DCE prepare to receive data                  |
| 3     | COM1_RX  | In             | Receive Data –<br>Carries data from DCE to DTE                                     |
| 4     | COM1_CTS | In             | Clear To Send –<br>Indicates DCE is ready to accept data                           |
| 5     | COM1_DTR | Out            | Data Terminal Ready –<br>Indicates presence of DTE to DCE                          |
| 6     | COM1_DSR | In             | Data Set Ready –<br>DCE is ready to receive commands or data                       |
| 7     | COM1_RI  | In             | Ring Indicator –<br>DCE has detected an incoming ring signal on the telephone line |
| 8     | GND      | -              | Ground   |

## 6 Miscellaneous Features

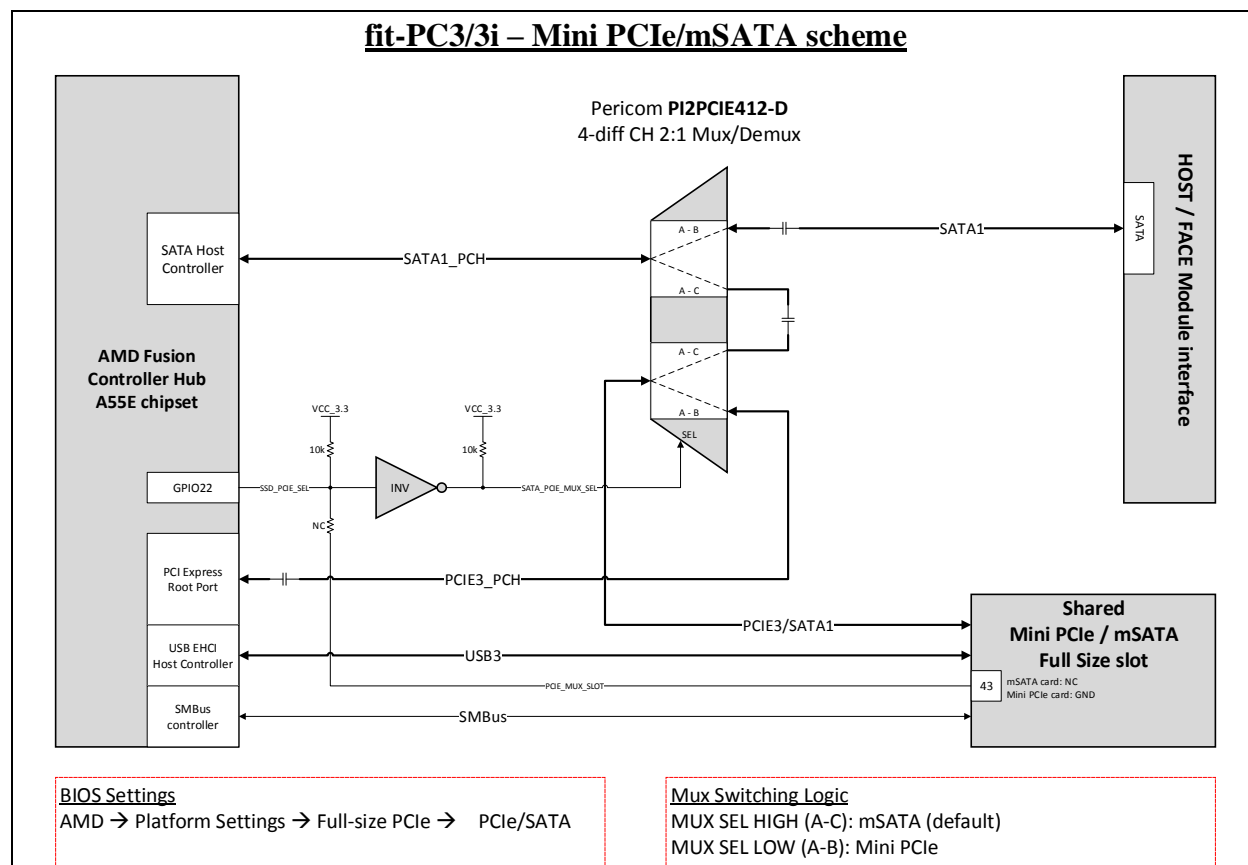
### 6.1 Mini PCI Express/mSATA sharing

Fit-PC3 and fit-PC3i advanced platform components and Compulab's flexible system design offers extremely high utilization of different functionalities and mechanical Form Factors to be implemented on the same HW.

Mini PCIe and mSATA share the same slot, and allow the flexibility to install both storage and PCI express devices. PCI Express/SATA interface switching implemented with 4-channel differential bi-directional multiplexer/de-multiplexer as shown in **Figure 17**.

**Note:** Proper functionality requires BIOS configuration to set the MUX to desired connectivity option (mSATA by default).

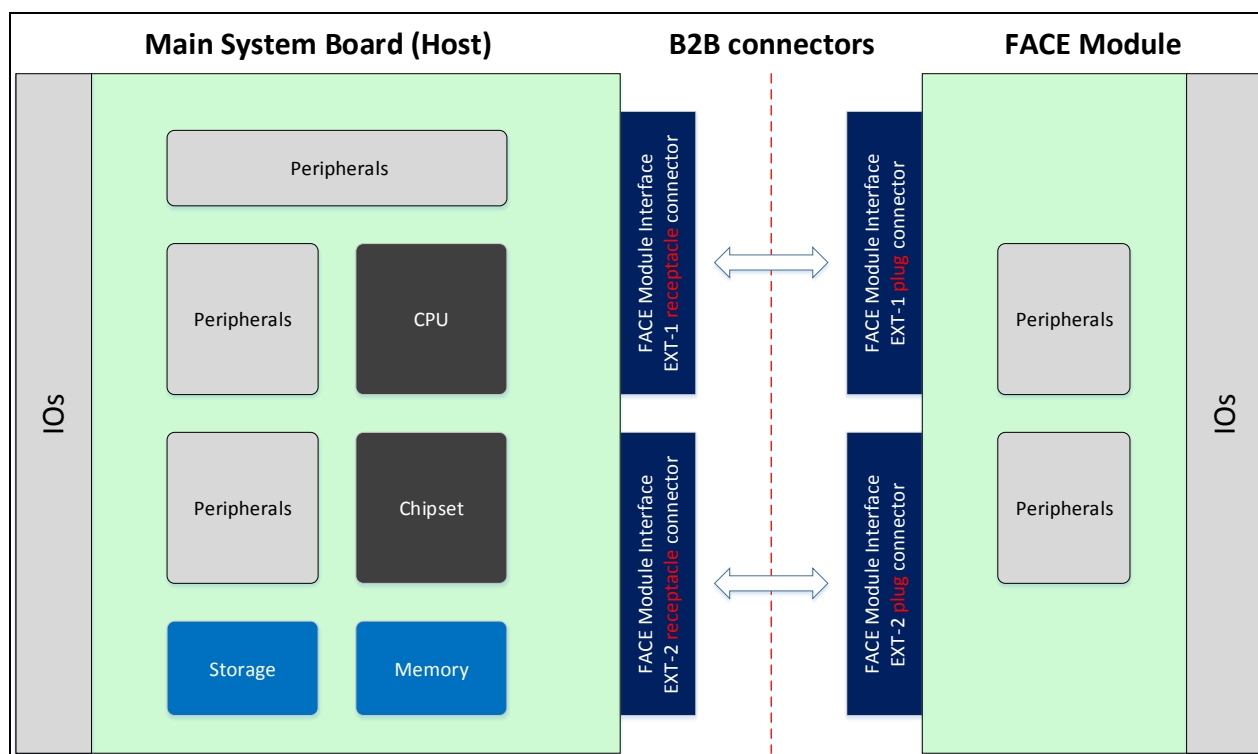
Figure 17 – fit-PC3/3i PC Mini PCIe/mSATA scheme



## 6.2 FACE Module Interface

FACE Module (**F**unction **A**nd **C**onnectivity **E**xtension Module) designed as additional/optional system board providing extended functionality and IO connectivity options. The interface between main system board and FACE module implemented with high speed, low pitch, and high pin count board-to-board connectors (B2B). Connectors' pinout including signals mapping and description described later in this chapter.

Figure 18 – FACE Module concept



### 6.2.1 Extension Connectors

Complete B2B receptacle and plug connector's specifications shown in the tables below.

**Table 29 – B2B receptacle connector HOST side**

| Item            | Option A    | Option B    | Option C          |
|-----------------|-------------|-------------|-------------------|
| Manufacturer    | FCI         | Tyco        | Oupiin            |
| PN              | 61082-10260 | 5-5179180-4 | 2382-100C00DP1T-M |
| Type            | Receptacle  | Receptacle  | Receptacle        |
| Positions       | 2x50        | 2x50        | 2x50              |
| Pitch           | 0.8mm       | 0.8mm       | 0.8mm             |
| Current rating  | 0.5A        | 0.5A        | 0.5A              |
| Height          | 7.7mm       | 7.7mm       | 7.7mm             |
| Stacking height | 12mm        | 12mm        | 12mm              |

**Table 30 – B2B plug connector FACE Module side**

| Item            | Option A    | Option B    | Option C          |
|-----------------|-------------|-------------|-------------------|
| Manufacturer    | FCI         | Tyco        | Oupiin            |
| PN              | 61083-10460 | 3-5177986-4 | 2381-100C00DP4T-M |
| Type            | Plug        | Plug        | Plug              |
| Positions       | 2x50        | 2x50        | 2x50              |
| Pitch           | 0.8mm       | 0.8mm       | 0.8mm             |
| Current rating  | 0.5A        | 0.5A        | 0.5A              |
| Height          | 7.7mm       | 7.7mm       | 7.7mm             |
| Stacking height | 12mm        | 12mm        | 12mm              |

## 6.2.2 Connectors Pinout

The tables below provide complete pinout of extension connectors EXT1, EXT2 and signals mapping.

**Table 31 – EXT1 connector HOST side pinout**

| EXT-1 connector HOST side |            |   |       |                |   |
|---------------------------|------------|---|-------|----------------|---|
| Pin #                     | Pin Name   | Signal Description  | Pin # | Pin Name       | Signal Description  |
| A1                        | GND        | Ground connection   | B1    | GND            | Ground connection   |
| A2                        | SATA2_TX+  | SATA3.0 differential transmit pair 2  | B2    | SATA0_TX+/CLK+ | Host PCIe CLK output differential pair - 100MHz PCIe Gen2 to PCIe devices |
| A3                        | SATA2_TX-  |   | B3    | SATA0_TX-/CLK- |   |
| A4                        | IR_RX      | IR UART receive signal  | B4    | SATA0_LED      | SATA activity LED indicator   |
| A5                        | SATA2_RX+  | SATA3.0 differential receive pair 2   | B5    | SATA0_RX+/CLK+ | Host PCIe CLK output differential pair - 100MHz PCIe Gen2 to PCIe devices |
| A6                        | SATA2_RX-  |   | B6    | SATA0_RX-/CLK- |   |
| A7                        | GND        | Ground connection   | B7    | VSSBY          | 5V power domain   |
| A8                        | SATA3_TX+  | SATA3.0 differential transmit pair 3  | B8    | SATA1_RX+      | SATA3.0 differential receive pair 1; Host signal shared with mini PCIe    |
| A9                        | SATA3_TX-  |   | B9    | SATA1_RX-      |   |
| A10                       | SMB_ALERT# | SMBus Alert used to wake the system   | B10   | DEBUG1         | Reserved debug signal   |
| A11                       | SATA3_RX+  | SATA3.0 differential receive pair 3   | B11   | SATA1_TX+      | SATA3.0 differential transmit pair 1; Host signal shared with mini PCIe   |
| A12                       | SATA3_RX-  |   | B12   | SATA1_TX-      |   |
| A13                       | VSSBY      | 5V power domain   | B13   | VSSBY          | 5V power domain   |
| A14                       | SMB_CLK    | SMBus host clock output. Connect to SMBus slave.                                | B14   | USB3_P         | USB Host interface 3  |
| A15                       | SMB_DAT    | SMBus bidirectional data. Connect to SMBus slave.                               | B15   | USB3_N         |   |
| A16                       | HDA_RST#   | High Definition Audio host reset  | B16   | USB_OC_2_3#    | USB Overcurrent Indicator for lanes 2/3                                   |
| A17                       | HDA_SYNC   | High Definition Audio host sync   | B17   | USB2_P         | USB Host interface 2  |
| A18                       | HDA_BITCLK | High Definition Audio host bit clock out 24MHz                                  | B18   | USB2_N         |   |
| A19                       | HDA_SDOOUT | High Definition Audio serial host data out                                      | B19   | VSSBY          | 5V power domain   |
| A20                       | HDA_SDIN1  | High Definition Audio serial host data in1                                      | B20   | Reserved       | Reserved for internal test purposes                                       |
| A21                       | HDA_SDIN0  | High Definition Audio serial host data in0                                      | B21   | Reserved       | Reserved for internal test purposes                                       |
| A22                       | DEBUG3     | Reserved debug signal   | B22   | LPC_SERIRQ     | Serial Interrupt Request  |
| A23                       | GND        | Ground connection   | B23   | LPC_CLK        | Single Ended 33MHz CLK host out to PCI devices                            |
| A24                       | USB0_P     | USB Host interface lane 0   | B24   | LPC_FRAME#     | LPC interface frame signal  |
| A25                       | USB0_N     |   | B25   | GND            | Ground connection   |
| A26                       | USB_OC0_1# | USB Overcurrent Indicator for lanes 0/1   | B26   | Reserved       | Reserved for internal use only  |
| A27                       | USB1_P     | USB Host interface 1  | B27   | Reserved       | Reserved for internal use only  |
| A28                       | USB1_N     |   | B28   | Reserved       | Reserved for internal use only  |
| A29                       | GND        | Ground connection   | B29   | Reserved       | Reserved for internal use only  |
| A30                       | LPC_AD0    | LPC bus multiplexed command, address and data. Internal PU provided on LPC[3:0] | B30   | Reserved       | Reserved for internal use only  |
| A31                       | LPC_AD1    |   | B31   | RESET#         | Active Low Platform Reset driven by the Host                              |
| A32                       | LPC_AD2    |   | B32   | PCIE_CLK+      | Host PCIe CLK output differential pair - 100MHz PCIe Gen2 to PCIe devices |
| A33                       | LPC_AD3    |   | B33   | PCIE_CLK-      |   |

|     |            |  |     |               |   |
|-----|------------|--|-----|---------------|---|
| A34 | GND        | Ground connection  | B34 | EXT_PRSENT#   | Clock Request for PCI Express 100 MHz Clocks  |
| A35 | PCIE_TX3+  | PCI Express (x1) Gen2 (up to 5Gbps) differential transmit pair 3                             | B35 | PCIE_RX3+     | PCI Express (x1) Gen2 (up to 5Gbps) differential receive pair 3                             |
| A36 | PCIE_TX3-  |  | B36 | PCIE_RX3-     |   |
| A37 | PCIE_WAKE# | PCI Express Wake Event from Device to Host   | B37 | SPI_EXT_CNTRL | SPI interface external control signal   |
| A38 | PCIE_TX2+  | PCI Express (x1) Gen2 (up to 5Gbps) differential transmit pair 2                             | B38 | PCIE_RX2+     | PCI Express (x1) Gen2 (up to 5Gbps) differential receive pair 2                             |
| A39 | PCIE_TX2-  |  | B39 | PCIE_RX2-     |   |
| A40 | GND        | Ground connection  | B40 | GND           | Ground connection   |
| A41 | PCIE_TX1+  | PCI Express (x1) Gen2 (up to 5Gbps) differential transmit pair 1                             | B41 | PCIE_RX1+     | PCI Express (x1) Gen2 (up to 5Gbps) differential receive pair 1                             |
| A42 | PCIE_TX1-  |  | B42 | PCIE_RX1-     |   |
| A43 | PWRBTN#    | System power button signal   | B43 | SLP#          | Assert LP state S3 (sleep) active low signal  |
| A44 | PCIE_TX0+  | Host CPU PEG (x1) - PCIe Gen3 (up to 8Gbps) differential transmit pair for external graphics | B44 | PCIE_RX0+     | Host CPU PEG (x1) - PCIe Gen3 (up to 8Gbps) differential receive pair for external graphics |
| A45 | PCIE_TX0-  |  | B45 | PCIE_RX0-     |   |
| A46 | RESERVED   | Reserved debug signal  | B46 | RESERVED      | Reserved debug signal   |
| A47 | VCC_12V    | Main 12V power domain  | B47 | VCC_12V       | Main 12V power domain   |
| A48 | VCC_12V    |  | B48 | VCC_12V       |   |
| A49 | VCC_12V    |  | B49 | VCC_12V       |   |
| A50 | VCC_12V    |  | B50 | VCC_12V       |   |

Table 32 – EXT2 connector HOST side pinout

| EXT-2 connector HOST side |                    |  |       |                       |  |
|---------------------------|--------------------|--|-------|-----------------------|--|
| Pin #                     | Pin Name           | Signal Description   | Pin # | Pin Name              | Signal Description   |
| A1                        | GND                | Ground connection  | B1    | GND                   | Ground connection  |
| A2                        | PEG_RX0+/RSVD0     | PCI Express (x1) Gen2 (up to 5Gbps) differential transmit pair 2 | B2    | PEG_TX0+/RSVD6        | PCI Express (x1) Gen2 (up to 5Gbps) differential transmit pair 2 |
| A3                        | PEG_RX0-/RSVD1     |  | B3    | PEG_TX0-/RSVD7        |  |
| A4                        | DGPU_PRSENT#/RSVD3 | XGPIOD0 (FCH GPIO145)  | B4    | DGPU_PWREN#/RSVD8     |  |
| A5                        | PEG_RX1+/RSVD4     | PCI Express (x1) Gen2 (up to 5Gbps) differential transmit pair 3 | B5    | PEG_TX1+/RSVD9        | PCI Express (x1) Gen2 (up to 5Gbps) differential transmit pair 3 |
| A6                        | PEG_RX1-/RSVD5     |  | B6    | PEG_TX1-/RSVD10       |  |
| A7                        | GND                | Ground connection  | B7    | GND                   | Ground connection  |
| A8                        | PEG_RX2+/RSVD11    | Not Connected  | B8    | PEG_TX2+/RSVD16       | Reserved   |
| A9                        | PEG_RX2-/RSVD12    |  | B9    | PEG_TX2-/RSVD17       |  |
| A10                       | DGPU_PWROK/RSVD13  | XGPIOD1 (FCH GPIO146)  | B10   | DGPU_HOLD_RST#/RSVD18 | XGPIO1 (FCH GPIO1)   |
| A11                       | PEG_RX3+/RSVD14    | Not Connected  | B11   | PEG_TX3+/RSVD19       | Not Connected  |
| A12                       | PEG_RX3-/RSVD15    |  | B12   | PEG_TX3-/RSVD20       | XGPIO4 (FCH GPIO4)   |
| A13                       | GND                | Ground connection  | B13   | GND                   | Ground connection  |
| A14                       | PEG_RX4+/RSVD21    | XGPIOD5 (FCH GPIO144)  | B14   | PEG_TX4+/RSVD26       | XGPIO5 (FCH GPIO5)   |
| A15                       | PEG_RX4-/RSVD22    | XGPIOD6 (FCH GPIO147)  | B15   | PEG_TX4-/RSVD27       | XGPIO6 (FCH GPIO6)   |

|     |                         |  |     |                       |  |
|-----|-------------------------|--|-----|-----------------------|--|
| A16 | DGPU_SELECT#/RSVD23     | XGPIOD3 (FCH GPIO149)                        | B16 | DGPU_HPD_INTR#/RSVD28 | XGPIO3 (FCH GPIO3)   |
| A17 | PEG_RX5+/RSVD24         | XGPIOD8 (FCH GPIO129)                        | B17 | PEG_TX5+/RSVD29       | XGPIO7 (FCH GPIO7)   |
| A18 | PEG_RX5-/RSVD25         | XGPIOD9 (FCH GPIO130)                        | B18 | PEG_TX5-/RSVD30       | XGPIO8 (FCH GPIO8)   |
| A19 | V5SBY                   | 5V power domain                              | B19 | V5SBY                 | 5V power domain  |
| A20 | PEG_RX6+/RSVD31         | XS5GPIO0 (FCH GPIO201)                       | B20 | PEG_TX6+/RSVD36       | XGPIO9 (FCH GPIO9)   |
| A21 | PEG_RX6-/RSVD32         | XS5GPIO1 (FCH GPIO202)                       | B21 | PEG_TX6-/RSVD37       | XGPIO10 (FCH GPIO10)   |
| A22 | DGPU_PWM_SELECT#/RSVD33 | XGPIOD4 (FCH GPIO150)                        | B22 | SPARE/eDP_HDP         | NC   |
| A23 | PEG_RX7+/RSVD34         | XS5GPIO3 (FCH GPIO204)                       | B23 | PEG_TX7+/RSVD38       | XGPIO11 (FCH GPIO11)   |
| A24 | PEG_RX7-/RSVD35         | XS5GPIO4 (FCH GPIO205)                       | B24 | PEG_TX7-/RSVD39       | XGPIO12 (FCH GPIO12)   |
| A25 | GND                     | Ground connection                            | B25 | GND                   | Ground connection  |
| A26 | LVDS_A0+/eDP_TX0+       | Not Connected                                | B26 | PEG_CLK+/RSVD40       | Host PCIe differential CLK output - 100MHz PCIe Gen2 to PCIe device  |
| A27 | LVDS_A0-/eDP_TX0-       |  | B27 | PEG_CLK-/RSVD41       |  |
| A28 | LVDS_A1+/eDP_TX1+       | Not Connected                                | B28 | LVDS_BKLT_CTRL        | Panel Backlight Brightness Control   |
| A29 | LVDS_A1-/eDP_TX1-       |  | B29 | COM1_DCR              | Full RS232 interface from Host to DCE device (shared with back panel COM port and only single may be used) |
| A30 | LVDS_A2+/eDP_TX2+       | Not Connected                                | B30 | COM1_TX               |  |
| A31 | LVDS_A2-/eDP_TX2-       |  | B31 | COM1_DCD              |  |
| A32 | GND                     | Ground connection                            | B32 | GND                   | Ground connection  |
| A33 | LVDS_A3+/eDP_TX3+       | Not Connected                                | B33 | COM1_DTR              | Full RS232 interface from Host to DCE device (shared with back panel COM port and only single may be used) |
| A34 | LVDS_A3-/eDP_TX3-       |  | B34 | COM1_RTS              |  |
| A35 | LVDS_VDD_EN             | LVDS Panel Power Enable                      | B35 | COM1_RX               |  |
| A36 | LVDS_ACLK+/eDP_AUX+     | Not Connected                                | B36 | COM1_CTS              |  |
| A37 | LVDS_ACLK-/eDP_AUX-     |  | B37 | COM1_RI               |  |
| A38 | GND                     | Ground connection                            | B38 | LVDS_BKLT_EN          | LVDS Backlight Enable  |
| A39 | LVDS_CTRL_CLK           | SMB2_SCLK (general purpose bus)              | B39 | LVDS_I2C_CLK          | APU_SID (Sideband-Temperature Sensor Interface Clock)  |
| A40 | LVDS_CTRL_DATA          | SMB2_SDA (general purpose bus)               | B40 | LVDS_I2C_DAT          | APU_SID (Sideband-Temperature Sensor Interface Data)   |
| A41 | PEG_CLK_REQ#/RSVD42     | Clock Request Signal for PCIe Graphics (PEG) | B41 | GND                   | Ground connection  |
| A42 | USB3_TX0_P              | GPIO_FANTACH1                                | B42 | USB3_TX0_P            | USB1.1 Host interface 1  |
| A43 | USB3_TX0_N              | GPIO_FANTACH2                                | B43 | USB3_TX0_N            |  |
| A44 | GND                     | Ground connection                            | B44 | NC                    | XPWM_GPIO0 (FCH GPIO197)   |
| A45 | USB3_RX0_P              | USB Host interface 13                        | B45 | USB3_RX0_P            | USB1.1 Host interface 0  |
| A46 | USB3_RX0_N              |  | B46 | USB3_RX0_N            |  |
| A47 | USB_OC_4_5#             | USB Overcurrent Indicator for lanes 2/3      | B47 | SPARE0                | Host chipset spare GPIO  |
| A48 | USB4_P                  | USB Host interface 5                         | B48 | VCC_12V               | Main 12V power domain  |
| A49 | USB4_N                  |  | B49 | VCC_12V               |  |
| A50 | GND                     | Ground connection                            | B50 | VCC_12V               |  |

### 6.3 Custom Design GPIOs

Fit-PC3/3i incorporates general purpose input output signals for user application implementations and custom system design. The GPIOs were selected and configured to provide convenient in/out functionality.

**Table 33 – Custom Design GPIO table**

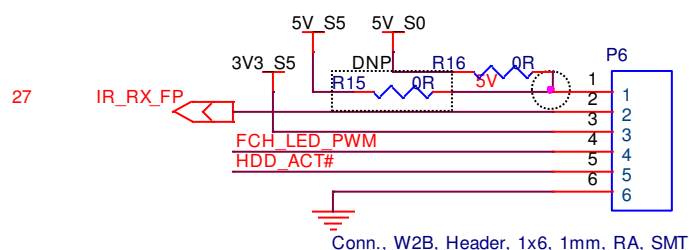
| FCH GPIO | Signal        | Direction | Default Drive | Default Pull (PU/PD) | EXT2 pin# |
|----------|---------------|-----------|---------------|----------------------|-----------|
| GPIO1    | XGPIO1        | Out       | Low           | No Pull              | B10       |
| GPIO3    | XGPIO3        | Out       | High          | FUNCTION0/AD3        | B16       |
| GPIO4    | XGPIO4        | Out       | High          | No Pull              | B12       |
| GPIO5    | XGPIO5        | Out       | High          | No Pull              | B14       |
| GPIO6    | XGPIO6        | Out       | High          | FUNCTION0/AD6        | B15       |
| GPIO7    | XGPIO7        | Out       | High          | No Pull              | B17       |
| GPIO8    | XGPIO8        | Out       | High          | No Pull              | B18       |
| GPIO9    | XGPIO9        | In        | -             | No Pull              | B20       |
| GPIO10   | XGPIO10       | In        | -             | No Pull              | B21       |
| GPIO11   | XGPIO11       | Out       | High          | No Pull              | B23       |
| GPIO12   | XGPIO12       | Out       | High          | No Pull              | B24       |
| GPIO57   | GPIO_FANTACH1 | Out       | High          | No Pull              | A42       |
| GPIO58   | GPIO_FANTACH2 | In        | -             | PU                   | A43       |
| GPIOD129 | XGPIOD8       |           |               |                      | A17       |
| GPIOD130 | XGPIOD9       |           |               |                      | A18       |
| GPIOD144 | XGPIOD5       |           |               |                      | A14       |
| GPIOD146 | XGPIOD1       |           |               |                      | A10       |
| GPIOD147 | XGPIOD6       |           |               |                      | A15       |
| GPIOD149 | XGPIOD3       |           |               |                      | A16       |
| GPIOD150 | XGPIOD4       |           |               |                      | A22       |
| GPIO197  | XPWM_GPIO0    |           |               | FUNCTION0/PWM        | B44       |
| GPIO201  | XS5GPIO0      | Out       | High          | PU/FUNCTION0         | A20       |
| GPIO202  | XS5GPIO1      | Out       | High          | PU/FUNCTION0         | A21       |
| GPIO204  | XS5GPIO3      | Out       | High          | PU/FUNCTION0         | A23       |
| GPIO205  | XS5GPIO4      | Out       | High          | PU/FUNCTION0         | A24       |

## 6.4 Misc Use Connector

Fit-PC3/3i offers custom use connector with the following connectivity options:

**Table 34 – Misc Use Connector**

| Pin # | Signal      | Source Direction | Description                              |
|-------|-------------|------------------|--|
| 1     | 5V          | Out              | 5V power                                 |
| 2     | IR_OUT      | In               | IR sensor output                         |
| 3     | 3.3V        | Out              | 3.3V power                               |
| 4     | FCH_LED_PWM | -                | Board LED cathode (for external control) |
| 5     | HDD_ACT#    | -                | SATA LED cathode (for external control)  |
| 6     | GND         | -                | Ground                                   |



## 7 Advanced Technologies

---

### 7.1 AMD Virtualization Technology

Virtualization helps companies save money and increase agility. But it can also impose some serious CPU and memory demands on your hardware. You need a computing platform that can provide a robust and scalable environment for virtualization while maintaining power efficiency.

AMD Virtualization (AMD-V™) Technology is a set of hardware extensions to the x86 system architecture that allows you to better utilize your resources, which make your servers, clients, and datacenters more effective.

AMD-V™ is designed to help simplify virtualization solutions, enabling a more satisfying user experience and near native application performance. AMD-V technology includes features such as:

- **Virtualization extensions to the x86 instruction set** – Enables software to more efficiently create virtual machines so that multiple operating systems and their applications can run simultaneously on the same computer.
- **Tagged TLB** – Hardware features that facilitate efficient switching between virtual machines for better application responsiveness.
- **Rapid Virtualization Indexing (RVI)** – Helps accelerate the performance of many virtualized applications by enabling hardware-based virtual machine memory management.
- **AMD-V™ Extended Migration** - Hardware feature that helps virtualization software enable live migration of virtual machines between all available AMD Opteron™ processor generations.
- **I/O Virtualization** - Enables direct device access by a virtual machine, bypassing the hypervisor for improved application performance and improved isolation of virtual machines for increased integrity and security.

## 8 Power Management

---

### 8.1 Power Manager

In fit-PC3 and fit-PC3i system architecture Fusion Controller Hub (FCH) responsible for all Power Management functionality and activity.

Power management and its HW/FW defined by Compulab's system architecture and AMD platform architecture. It is responsible for power management and housekeeping functionality in the platform. It interfaces with processor, chipset, system power supplies and power sequencing logic. It is essential part for proper system operation.

## 9 Electrical Characteristics

### 9.1 Absolute Maximum Ratings

Operating the fit-PC3/3i under conditions beyond its absolute maximum ratings may damage the device. Absolute maximum ratings are limiting values to be considered individually when all other parameters are within their specified operating ranges. Functional operation and specification compliance under any absolute maximum condition, or after exposure to any of these conditions, are not guaranteed or implied. Exposure may affect device reliability.

**Table 35 – Absolute Maximum Ratings**

| Parameter                 | Min | Typ. | Max | Unit |
|---------------------------|-----|------|-----|------|
| Main power supply voltage | 8.5 | -    | 16  | V    |

### 9.2 Recommended Operating Conditions

Operating conditions include parameters that are under the control of the user: power-supply voltage and ambient temperature. The fit-PC3/3i meets all performance specifications when used within the recommended operating conditions, unless otherwise noted.

**Table 36 – Recommended Operating Condition**

| Parameter                 | Min | Typ. | Max | Unit |
|---------------------------|-----|------|-----|------|
| Main power supply voltage | 10  | 12   | 15  | V    |

### 9.3 DC Electrical Characteristics

**Table 37 – DC Electrical Characteristics**

| Parameter           | Operating Conditions | Min  | Typ. | Max | Unit |
|---------------------|----------------------|------|------|-----|------|
| 3.3V Digital I/O    |                      |      |      |     |      |
| V <sub>IH</sub>     | GPIOs                | 1.5  | -    | -   | V    |
| V <sub>IL</sub>     |                      | -    | -    | 1.5 | V    |
| V <sub>OH</sub>     |                      | 2.4  | -    | -   | V    |
| V <sub>OL</sub>     |                      | -    | -    | 0.4 | V    |
| RS232               |                      |      |      |     |      |
| TX Voltage Swing    |                      | ±5.0 | ±5.4 | -   | V    |
| Input Voltage Range |                      | -25  | -    | 25  | V    |

### 9.4 Power Supply

Fit-PC3/3i wall power supply:

- Input: 100-240VAC 50/60Hz
- Output: 12VDC 3A, 36W

## 10 Mechanical Characteristics

### 10.1 Mechanical Drawings

#### 10.1.1 Fit-PC3 Pro

Figure 19 – fit-PC3 Pro Isometric Front



Figure 20 – fit-PC3 Pro Isometric Back



Figure 21 – fit-PC3 Pro Front Panel

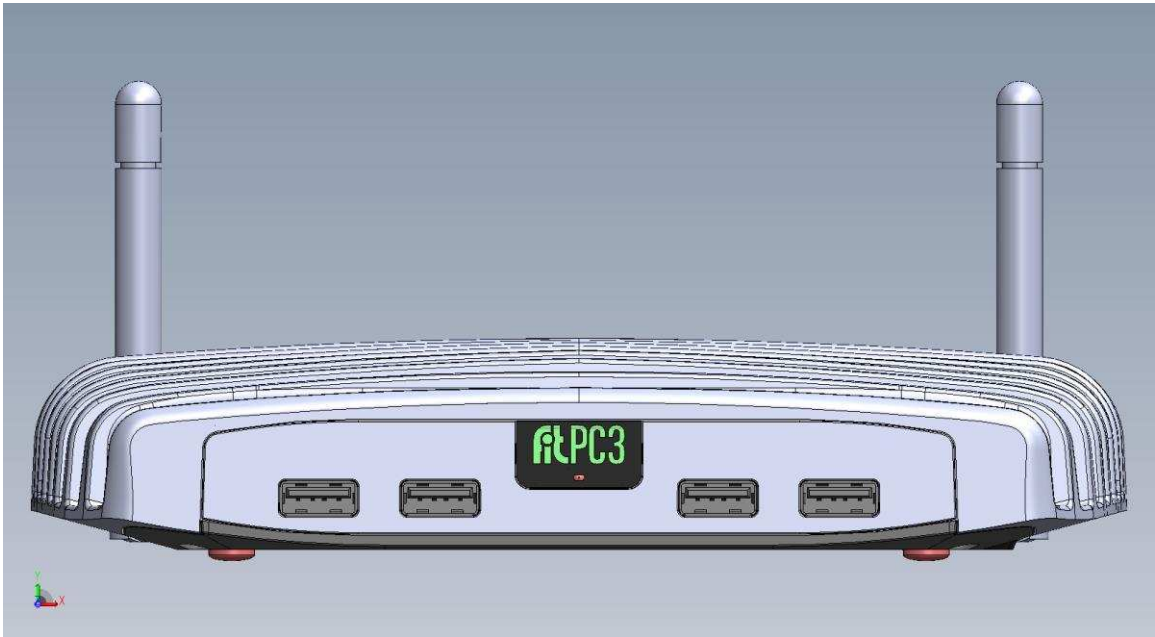
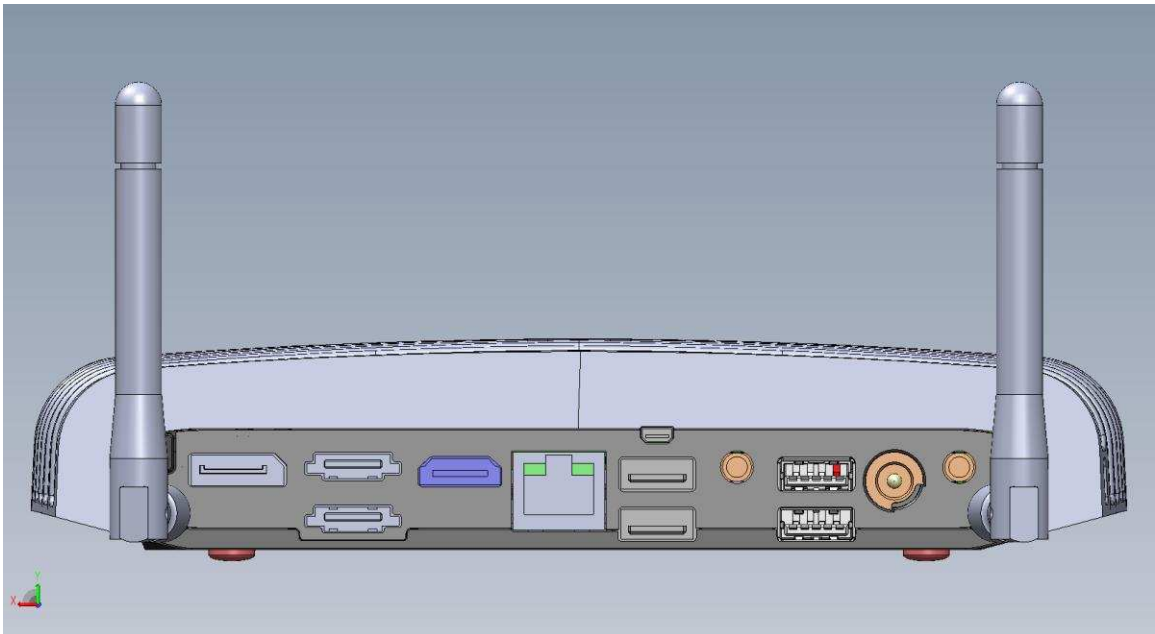
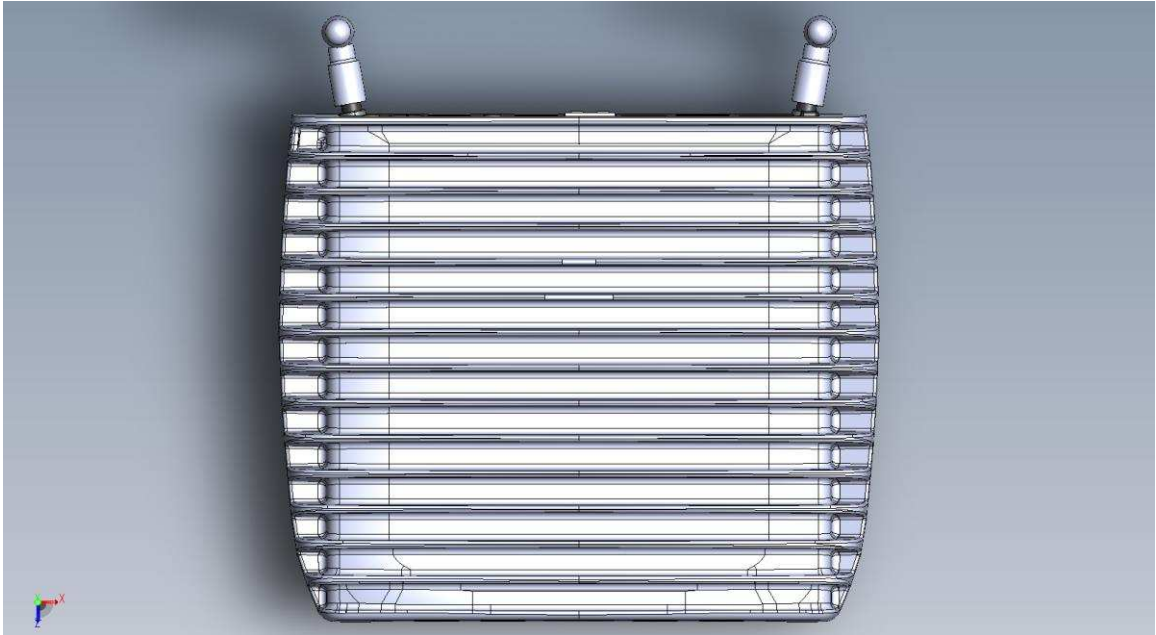


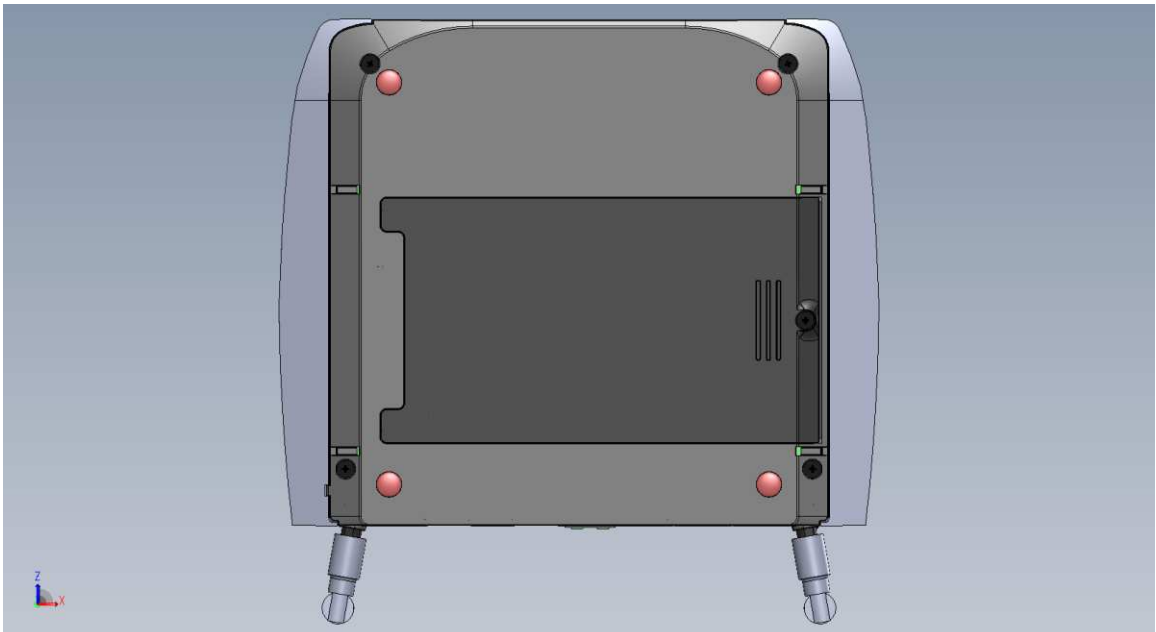
Figure 22 – fit-PC3 Pro Back Panel



**Figure 23 – fit-PC3 Pro Top**



**Figure 24 – fit-PC3 Pro Bottom**



### 10.1.2 Fit-PC3 LP

Figure 25 – fit-PC3 LP Isometric Front



Figure 26 – fit-PC3 LP Isometric Back



Figure 27 – fit-PC3 LP Front Panel

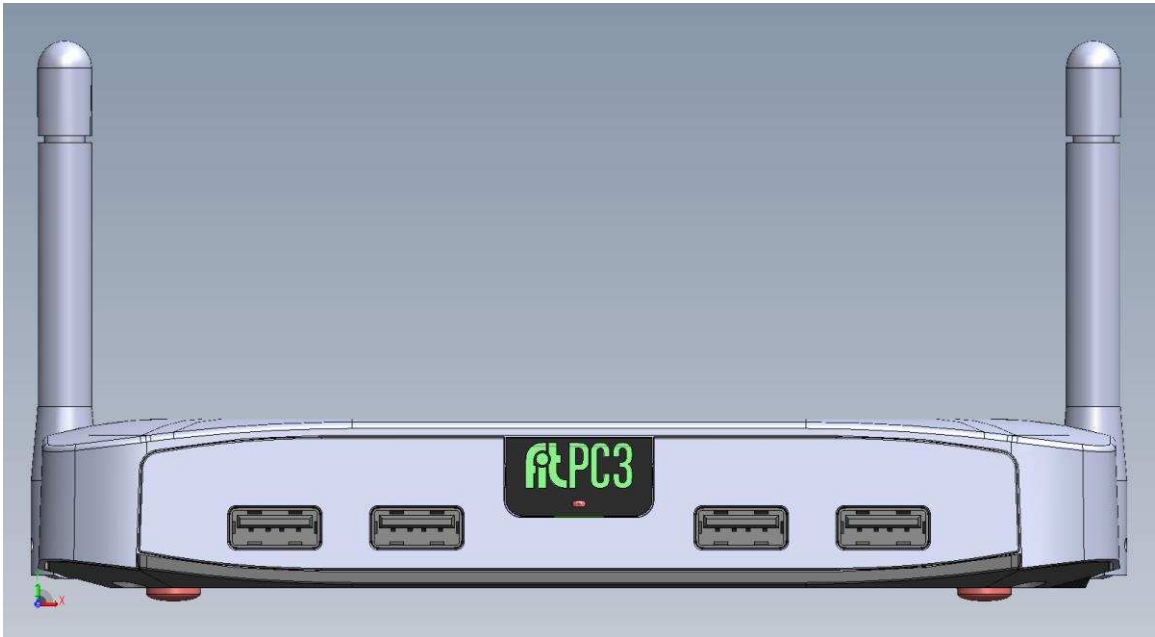
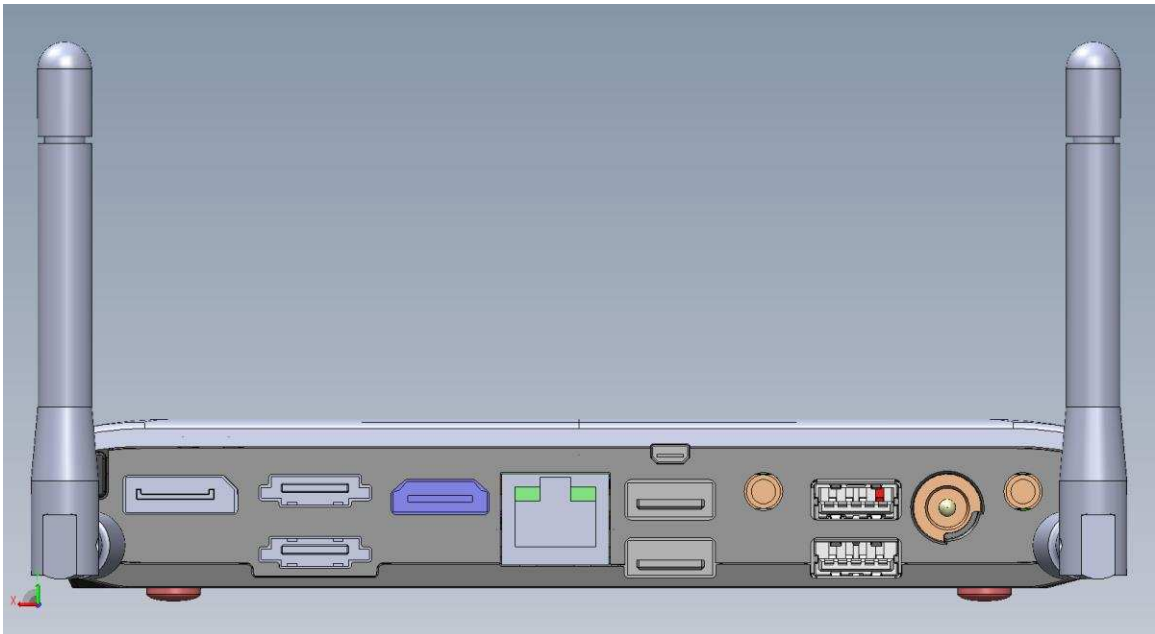
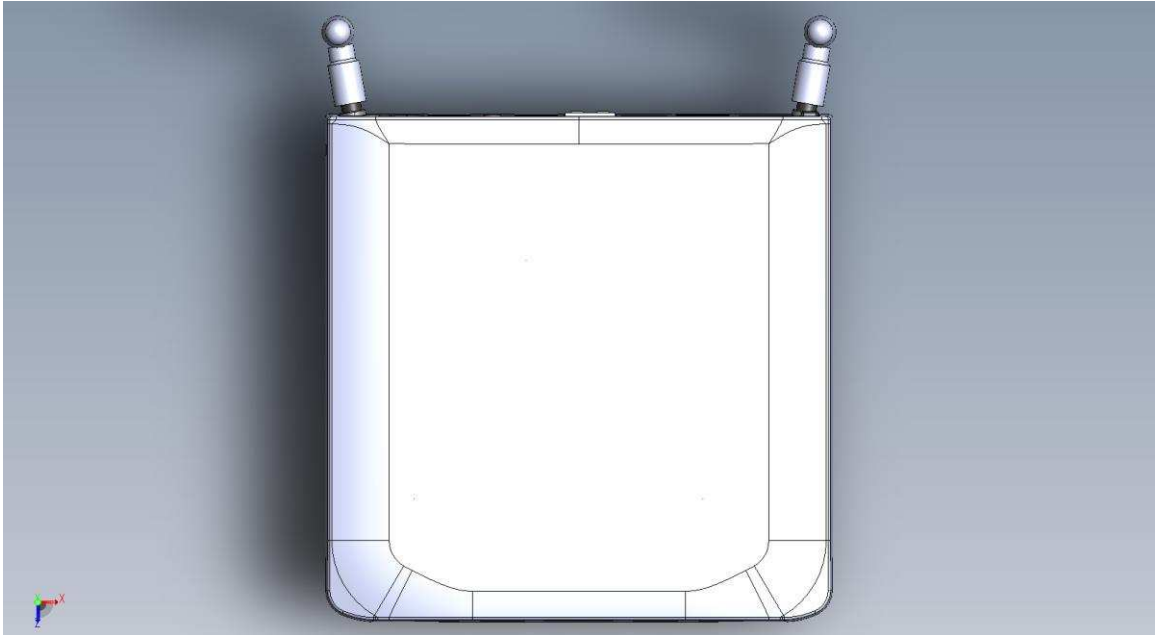


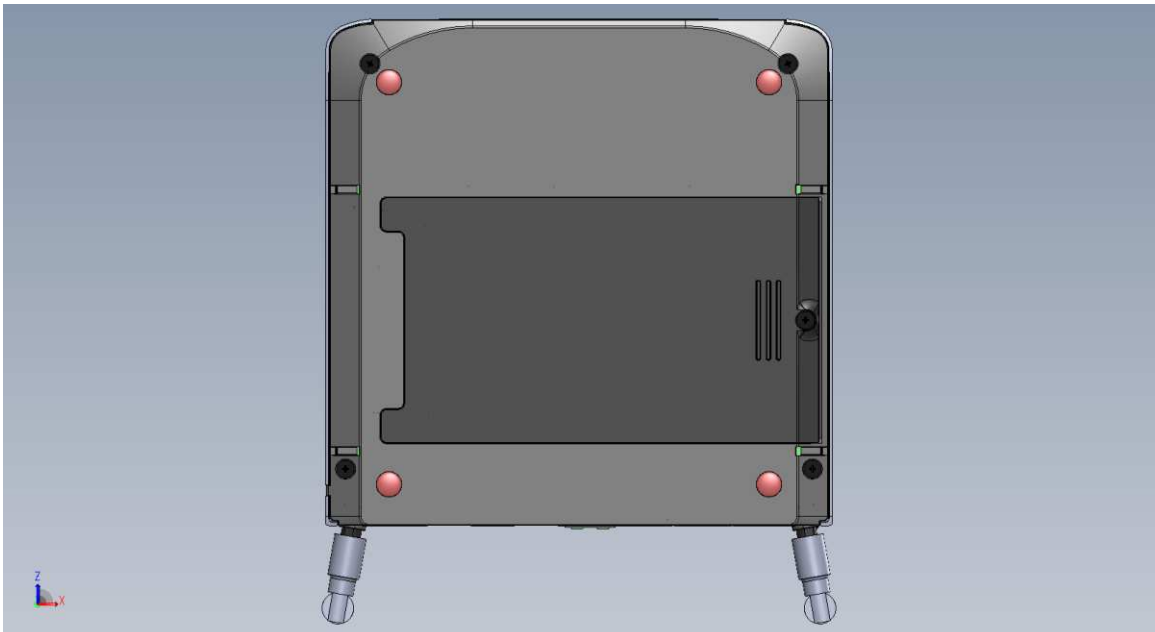
Figure 28 – fit-PC3 LP Back Panel



**Figure 29 – fit-PC3 LP Top**



**Figure 30 – fit-PC3 LP Bottom**



### 10.1.3 Fit-PC3i

Fit-PC3i differs from fit-PC3 mechanical design on its back panel, due to different connectivity options provided.

**Figure 31 – fit-PC3i Pro Back Panel**

**TBD**

#### 10.1.4 Single Board Computer

Single Board Computers or Open Chassis platforms based on fit-PC3 and fit-PC3i HW available for system integration and industrial business applications. Available in both variations with or without FACE Module. SBC HW should be thermally coupled to a passive or active cooling system in order to guarantee proper operation and maximal performance.

SBC supplied with a heat plate in order to simplify system integration and provide an easy way to attach it to a heat sink.

**Note:** Heat plate alone does NOT guarantee sufficient cooling in order to provide maximal performance, therefore in order to avoid system throttling or thermal shut down in worst cases, system integrators must supply additional system cooling method.

##### 10.1.4.1 With FACE Module

Figure 32 – SBC-FITPC3 Mechanical Drawing with FACE Module

TBD

##### 10.1.4.2 Without FACE Module

Figure 33 – SBC-FITPC3 Mechanical Drawing without FACE Module

TBD

## 10.2 Environmental

fit-PC3 and fit-PC3i models available in 3 operating temperature grades – Commercial, Extended and Industrial. Please refer to the table below:

**Table 38 – Operating Temperature Grades**

| Operating Conditions | Op. Temp. grades |               |                 |
|----------------------|------------------|---------------|-----------------|
|                      | Commercial       | Extended (TE) | Industrial (TI) |
| HDD models           | 0°C – 50°C       | N/A           | N/A             |
| SSD models           | 0°C – 70°C       | -20°C – 70°C  | -40°C – 70°C    |

## 11 Resources

---

For more CompuLab resources please use the following links:

1. Fit-PC website:  
<http://www.fit-pc.com/web/>
2. fit-PC3 website:  
<http://www.fit-pc.com/web/products/fit-pc3/>
3. Wiki pages for additional documentation and driver download:  
[http://www.fit-pc.com/wiki/index.php/Main\\_Page](http://www.fit-pc.com/wiki/index.php/Main_Page)
4. Forum:  
<http://www.fit-pc.com/forum/viewforum.php?f=71>