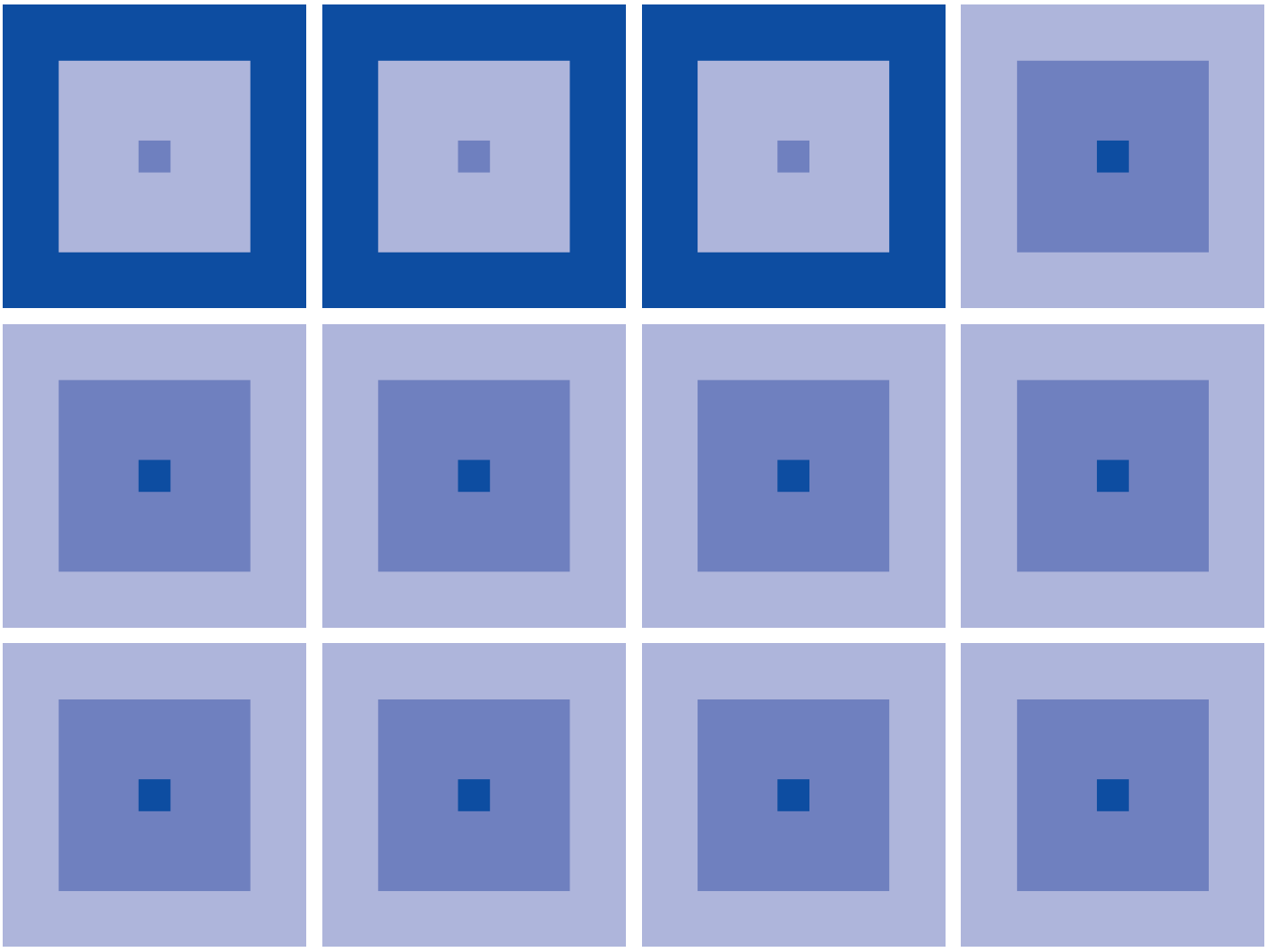
MF424-21

EPSON

LCD driver with RAM

S1D15000 Series

Technical Manual



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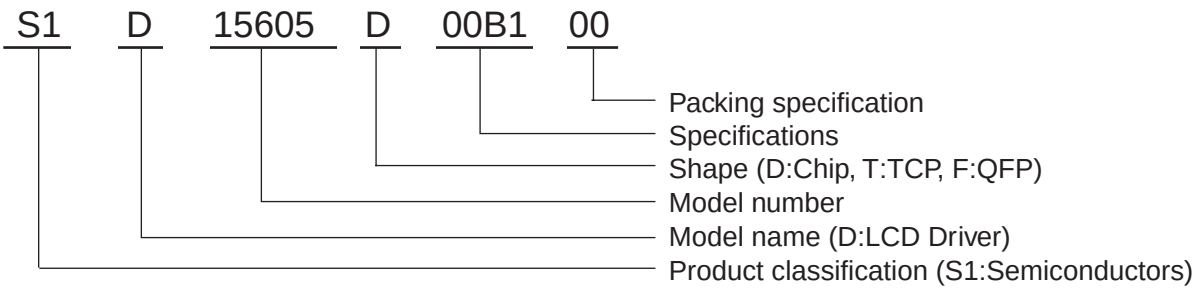
The information of the product number change

Starting April 1, 2001 the product number will be changed as listed below. To order from April 1, 2001 please use the new product number. For further information, please contact Epson sales representative.

Configuration of product number

●DEVICES (Example : S1D15605D00B100)



Comparison table between new and previous number

Previous number	New number
SED1510D0C	S1D15100D00C*
SED1510F0C	S1D15100F00C*
SED1520DAA	S1D15200D10A*
SED1520DAB	S1D15200D10B*
SED1520F0A	S1D15200F00A*
SED1520FAA	S1D15200F10A*
SED1521F0A	S1D15201F00A*
SED1521FAA	S1D15201F10A*
SED1522F0A	S1D15202F00A*
SED1522FAA	S1D15202F10A*
SED1526F0A	S1D15206F00A*
SED1526FAA	S1D15206F10A*
SED1526FBA	S1D15206F11A*
SED1526FEA	S1D15206F14A*
SED1526FEY	S1D15206F14Y*
SED1526T0A	S1D15206T00A*
SED1528DBB	S1D15208D11B*
SED1528F0A	S1D15208F00A*
SED1530D0A	S1D15300D00A*
SED1530D0B	S1D15300D00B*
SED1540D0A	S1D15400D00A*
SED1540D0B	S1D15400D00B*
SED1540F0A	S1D15400F00A*
SED1560D0B	S1D15600D00B*

Previous number	New number
SED1560DAB	S1D15600D10B*
SED1561D0B	S1D15601D00B*
SED1561DAB	S1D15601D10B*
SED1562D0B	S1D15602D00B*
SED1565D0B	S1D15605D00B*
SED1565D1B	S1D15605D01B*
SED1565D2B	S1D15605D02B*
SED1565DBB	S1D15605D11B*
SED1565DBE	S1D15605D11E*
SED1565T0*	S1D15605T00**
SED1565T0B	S1D15605T00B*
SED1566D0B	S1D15606D00B*
SED1566D1B	S1D15606D01B*
SED1566D2B	S1D15606D02B*
SED1566DBB	S1D15606D11B*
SED1566T0*	S1D15606T00**
SED1567D0B	S1D15607D00B*
SED1567D1B	S1D15607D01B*
SED1567D2B	S1D15607D02B*
SED1567DBB	S1D15607D11B*
SED1567T0*	S1D15607T00**
SED1568D0B	S1D15608D00B*
SED1568DBB	S1D15608D11B*
SED1569D0B	S1D15609D00B*

Previous number	New number
SED1569D$_{BB}$	S1D15609D11B*
SED1570D$_{0A}$	S1D15700D00A*
SED1570D$_{0B}$	S1D15700D00B*
SED1575D$_{0B}$	S1D15705D00B*
SED1575D$_{3B}$	S1D15705D03B*
SED1575D$_{AB}$	S1D15705D10B*
SED1575T$_{0}$*	S1D15705T00**
SED1575T$_{0A}$	S1D15705T00A*
SED1575T$_{3}$*	S1D15705T03**
SED1577D$_{0B}$	S1D15707D00B*
SED1577D$_{3B}$	S1D15707D03B*
SED1577T$_{0}$*	S1D15707T00**
SED1577T$_{3}$*	S1D15707T03**
SED1578D$_{0B}$	S1D15708D00B*
SED157AD$_{0B}$	S1D15710D00B*
SED157AD$_{AB}$	S1D15710D10B*
SED157AD$_{BB}$	S1D15710D11B*
SED157AT$_{0A}$	S1D15710T00A*
SED15A6D$_{0B}$	S1D15A06D00B*
SED15A6D$_{1B}$	S1D15A06D01B*
SED15A6D$_{2B}$	S1D15A06D02B*
SED15A6T$_{0}$*	S1D15A06T00**
SED15B1D$_{0B}$	S1D15B01D00B*
SED15B1D$_{1B}$	S1D15B01D01B*
SED15B1D$_{2B}$	S1D15B01D02B*
SED15B1T$_{0}$*	S1D15B01T00**

S1D15100 Series

S1D15200 Series

S1D15210 Series

S1D15206 Series

S1D15300 Series

S1D15400 Series

S1D15600/601/602 Series

S1D15605 Series

S1D15700 Series

S1D15705 Series

S1D15710 Series

S1D15A06 Series

S1D15B01 Series

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S1D15000 Series
Selection Guide

■ LCD drivers with RAM for small- and medium-sized displays

Ultra-low power consumption and on-chip RAM make this series ideal for compact LCD-based equipment.

S1D15000 (SED1500) series

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Segment	Common	Display RAM (bits)	Microprocessor interface	Frequency (KHz)	Package	Application/additional features
S1D15100D00C* (SED1510D0C)	0.9 to 6.0	1.8 to 6.0	1/4	32	4	128 bit	Serial	18(internal)	Al pad chip	Small segment-type LCD display. Common and data interface.
S1D15100F00C* (SED1510F0C)									QFP12-48pin	
S1D15200***** (SED1520***)	2.4 to 7.0	3.5 to 13	1/8 to 1/32	61	16	2,560 bit	8 bit	18(internal, external) or 2(external)	Chip, TCP	After service parts
S1D15201***** (SED1521***)	2.4 to 7.0	3.5 to 13	1/8 to 1/32	80	–	2,560 bit	8 bit	18(internal, external) or 2(external)	Chip, TCP	After service parts
S1D15202***** (SED1521***)	2.4 to 7.0	3.5 to 13	1/8 to 1/32	69	8	2,560 bit	8 bit	18(internal, external) or 2(external)	Chip, TCP	After service parts
S1D15206D**A* (SED1526D*A)	2.4 to 6.0	3.5 to Supply voltage ×3	1/8,1/9, 1/16,1/17	80	17	80×33 bit	8-bit parallel or Serial	20	Al pad chip	DC/DC×3 (S1D15206*00**•VREG) (S1D15206*14**•no VREG)
S1D15206D**B* (SED1526D*B)									Au bump chip	
S1D15206F**A* (SED1526F*A)									QFP5-128pin	
S1D15206T**A* (SED1526T*A)									TCP	
S1D15208D**A* (SED1528D*A)	2.4 to 6.0	3.5 to Supply voltage ×3	1/32,1/33	64	33	80×33 bit	8-bit parallel or Serial	20	Al pad chip	DC/DC×3 (S1D15208*00**•VREG) (S1D15208*14**•no VREG)
S1D15208D**B* (SED1528D*B)									Au bump chip	
S1D15208F**A* (SED1528F*A)									QFP5-128pin	
S1D15208T**A* (SED1528T*A)									TCP	
S1D15300D00A* (SED1530D0A)	2.4 to 6.0	4.5 to 16	1/32,1/33	100	33	132×65 bit	8-bit parallel or Serial	–	Al pad chip	Built-in power circuit for LCD (DC/DC×4) S1D15300D00**(SED1530*0*) Common : Right side S1D15300*10**(SED1530*A*) Common : Both side
S1D15300D10A* (SED1530DAA)									Al pad chip	
S1D15300D00B* (SED1530D0B)									Au bump chip	
S1D15300D10B* (SED1530DAB)									Au bump chip	
S1D15300T10A* (SED1530TAA)									TCP	
S1D15301D00A* (SED1531D0A)	2.4 to 6.0	4.5 to 16	1/64,1/65	132	–	132×65 bit	8-bit parallel or Serial	–	Al pad chip	Built-in power circuit for LCD (DC/DC×4) S1D15301*00**(SED1531*0*) Common : Right side
S1D15301D00B* (SED1531D0B)									Au bump chip	
S1D15301T00A* (SED1531T0A)									TCP	
S1D15302D00A* (SED1532D0A)	2.4 to 6.0	4.5 to 16	1/64,1/65	100	33	132×65 bit	8-bit parallel or Serial	–	Al pad chip	Built-in power circuit for LCD (DC/DC×4) S1D15302*00**(SED1532*0*) Common : Right side S1D15302*11**(SED1532*B*) Common : Left side
S1D15302D11A* (SED1532DBA)									Al pad chip	
S1D15302D00B* (SED1532D0B)									Au bump chip	
S1D15302D11B* (SED1532DBB)									Au bump chip	
S1D15302T00A* (SED1532T0A)									TCP	
S1D15302T11A* (SED1532TBA)									TCP	

TCP : Tape Carrier Package

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Segment	Common	Display RAM (bits)	Microprocessor interface	Frequency (KHz)	Package	Application/additional features
S1D15303D15B* (SED1533DFB)	2.4 to 6.0	4.5 to 16	1/17	116	17	132×65 bit	8-bit parallel or Serial	–	Au bump chip	Built-in power circuit for LCD (DC/DC×4) Common : Left side no VREF
S1D15400D00A* (SED1540D0A)	2.4 to 7.0	3.5 to 11	1/3, 1/4	73	3, 4	2,560 bit	8-bit parallel	18(internal), 4(external)	Al pad chip	
S1D15400D00B* (SED1540D0B)									Au bump chip	
S1D15400F00A* (SED1540F0A)									QFP5-100pin	
S1D15600D00A* (SED1560D0A)	2.4 to 6.0	6.0 to 16	1/48,1/49, 1/64,1/65	102	65	166×65 bit	8-bit parallel or Serial	18	Al pad chip	Built-in power circuit for LCD (DC/DC×3) S1D15600*00B* (SED1560*0B) : 1/9 bias S1D15600*10B* (SED1560*AB) : 1/7 bias
S1D15600D10A* (SED1560DAA)									Al pad chip	
S1D15600D00B* (SED1560D0B)									Au bump chip	
S1D15600D10B* (SED1560DAB)									Au bump chip	
S1D15600T00B* (SED1560T0B)									TCP	
S1D15600T26A* (SED1560TQA)									QTCP	
S1D15601D00A* (SED1561D0A)	2.4 to 6.0	6.0 to 16	1/24,1/25, 1/32,1/33	134	33	166×65 bit	8-bit parallel or Serial	18	Al pad chip	Built-in power circuit for LCD (DC/DC×3) S1D15601*00B* (SED1561*0B) : 1/7 bias S1D15601*10B* (SED1561*AB) : 1/5 bias
S1D15601D00B* (SED1561D0B)									Au bump chip	
S1D15601D10B* (SED1561DAB)									Au bump chip	
S1D15601T00B* (SED1561T0B)									TCP	
S1D15601T10B* (SED1561TAB)									TCP	
S1D15601T26A* (SED1561TQA)									QTCP	
S1D15602D00A* (SED1562D0A)	2.4 to 6.0	6.0 to 16	1/16,1/17 (1/5 bias)	150	17	166×65 bit	8-bit parallel or Serial	18	Al pad chip	Built-in power circuit for LCD (DC/DC×3)
S1D15602D00B* (SED1562D0B)									Au bump chip	
S1D15602T00B* (SED1562T0B)									TCP	
S1D15602T26A* (SED1562TQA)									QTCP	
S1D15605D11B* (SED1565DBB)	1.8 to 5.5	4.5 to 16	1/65 (1/7,1/9 bias)	132	65	132×65 bit	8-bit parallel or Serial	33	Au bump chip	Built-in power circuit for LCD (DC/DC×4)
S1D15605D00B* (SED1565D0B)									Au bump chip	
S1D15605D01B* (SED1565D1B)									Au bump chip	
S1D15605D02B* (SED1565D2B)									Au bump chip	
S1D15605T00A* (SED1565T0A)									TCP	
S1D15605T00B* (SED1565T0B)									TCP	
S1D15605T00C* (SED1565T0C)									TCP	

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Segment	Common	Display RAM (bits)	Microprocessor interface	Frequency (KHz)	Package	Application/additional features
S1D15606D11B* (SED1566DBB)	1.8 to 5.5	4.5 to 16	1/49 (1/6,1/8 bias)	132	49	132×65 bit	8-bit parallel or Serial	33	Au bump chip	Built-in power circuit for LCD (DC/DC×4)
S1D15606D00B* (SED1566D0B)									Au bump chip	
S1D15606D01B* (SED1566D1B)									Au bump chip	
S1D15606D02B* (SED1566D2B)									Au bump chip	
S1D15606T00A* (SED1566T0A)									TCP	
S1D15607D11B* (SED1567DBB)	1.8 to 5.5	4.5 to 16	1/33 (1/5,1/6 bias)	132	33	132×65 bit	8-bit parallel or Serial	33	Au bump chip	Built-in power circuit for LCD (DC/DC×4)
S1D15607D00B* (SED1567D0B)									Au bump chip	
S1D15607D01B* (SED1567D1B)									Au bump chip	
S1D15607D02B* (SED1567D2B)									Au bump chip	
S1D15607T00B* (SED1567T0B)									TCP	
S1D15607T00C* (SED1567T0C)									TCP	
S1D15608D11B* (SED1568DBB)	1.8 to 5.5	4.5 to 16	1/55 (1/6,1/8 bias)	132	55	132×65 bit	8-bit parallel or Serial	33	Au bump chip	Built-in power circuit for LCD (DC/DC×4)
S1D15608D00B* (SED1568D0B)									Au bump chip	
S1D15609D11B* (SED1569DBB)	1.8 to 5.5	4.5 to 16	1/53 (1/6,1/8 bias)	132	53	132×65 bit	8-bit parallel or Serial	33	Au bump chip	Built-in power circuit for LCD (DC/DC×4)
S1D15609D00B* (SED1569D0B)									Au bump chip	
S1D15609T**** (SED1569TXX*)									TCP	
S1D15A06D00B* (SED15A6D0B)	1.8 to 5.5	4.5 to 16	1/55	102	55	102×65 bit	8-bit parallel or Serial	33	Au bump chip	Reduced ext. parts Built-in power circuit.
S1D15A06T00A* (SED15A6T0A*)									TCP	
S1D15B01D00B* (SED15B1D0B)	1.8 to 5.5	4.5 to 16	1/65	132	65	132×65 bit	8-bit parallel or Serial	33	Au bump chip	Built-in self-refreshing function.
S1D15B01T00A* (SED15B1T0A)									TCP	
S1D15E00D00B* (SED15E0D0B)	1.8 to 3.6	3.2 to 10	1/100	132	100	132×100 bit	Serial	Can be select	Au bump chip	4-line MLS driving
S1D15E00T00A* (SED15E0T0A)									TCP	
S1D15705D00B* (SED1575D0B)	3.6 to 5.5	4.5 to 16	1/65	168	65	200×65 bit	8-bit parallel or Serial	22	Au bump chip	Built-in power circuit for LCD (DC/DC×4)
S1D15705D03B* (SED1575D3B)	2.4 to 3.6									
S1D15705T00A* (SED1575T0A)	3.6 to 5.5	4.5 to 16	1/65	168	65	200×65 bit	8-bit parallel or Serial	22	TCP	Built-in power circuit for LCD (DC/DC×4)
S1D15705T03A* (SED1575T3A)	2.4 to 3.6									
S1D15707D00B* (SED1577D0B)	3.6 to 5.5	4.5 to 16	1/33	200	33	200×65 bit	8-bit parallel or Serial	22	Au bump chip	Built-in power circuit for LCD (DC/DC×4)
S1D15707D03B* (SED1577D3B)	2.4 to 3.6									
S1D15707T00A* (SED1577T0A)	3.6 to 5.5	4.5 to 16	1/33	200	33	200×65 bit	8-bit parallel or Serial	22	TCP	Built-in power circuit for LCD (DC/DC×4)
S1D15707T03A* (SED1577T3A)	2.4 to 3.6									
S1D15710D00B* (SED157AD0B)	1.8 to 5.5	4.5 to 18	1/65	224	65	224×65 bit	8-bit parallel or Serial	22	Au bump chip	Built-in power circuit for LCD
S1D15710T00A* (SED157AT0A*)									TCP	

TCP : Tape Carrier Package

1. S1D15100 Series

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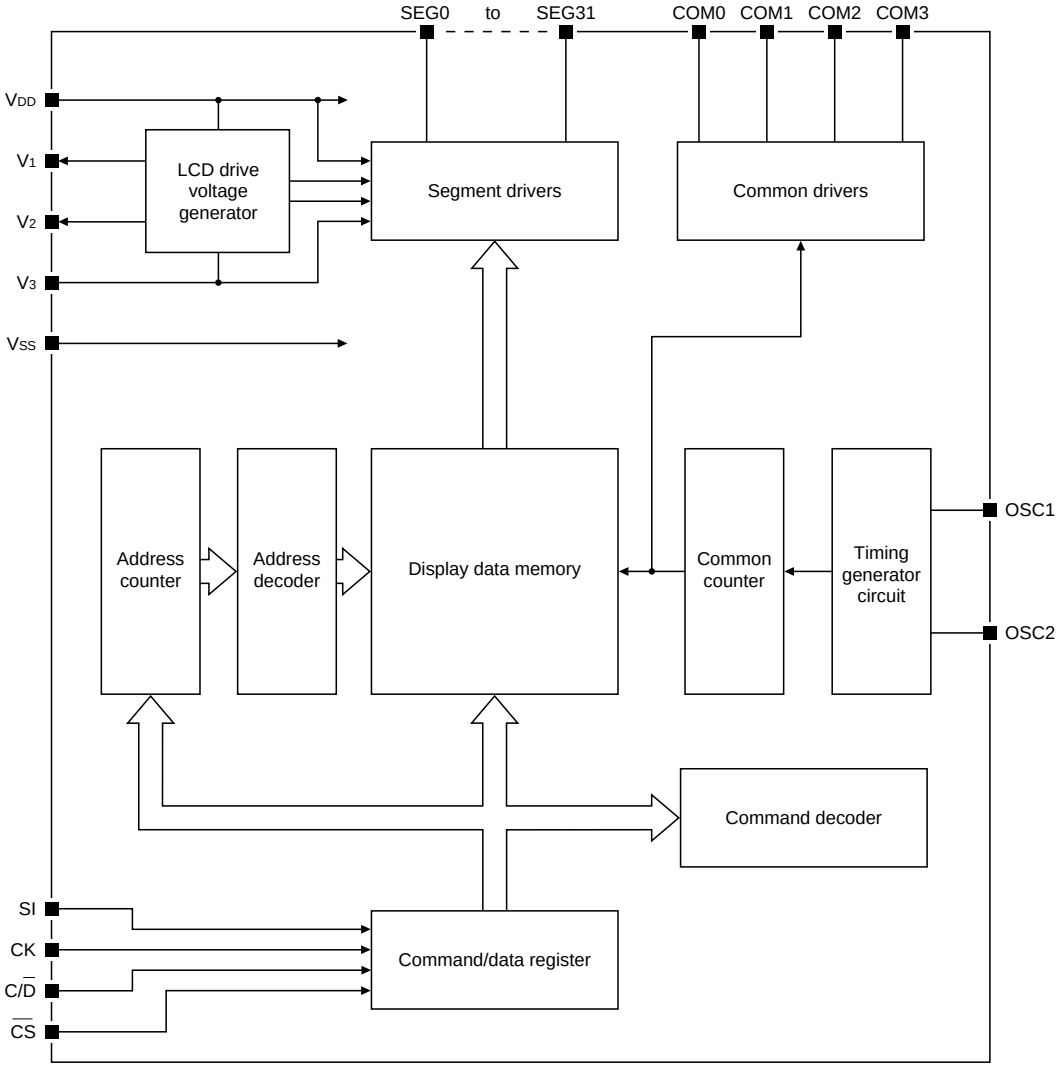
1. DESCRIPTION

The S1D15100Series is a segment driver IC for 1/4-duty LCD panels. It features 150 μW maximum power dissipation and a wide operating supply voltage range, making it ideal for use in battery-powered devices. The S1D15100 series incorporates an LCD driving power circuit and allows simple configuration of the interface with a microcomputer, achieving a handy type unit at low cost.

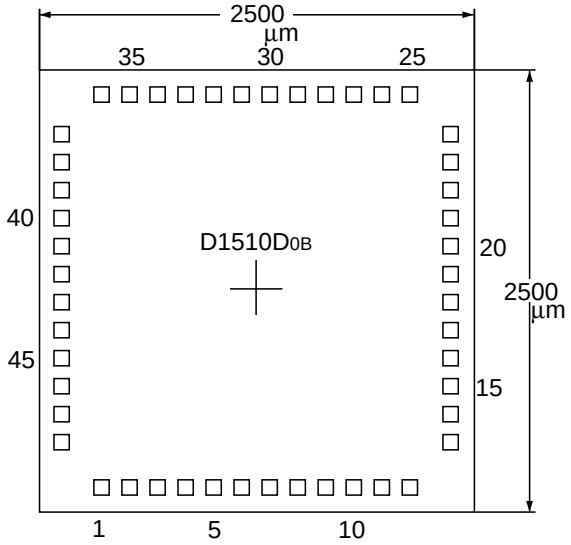
2. FEATURES

- 1/4-duty LCD segment driver
- 150 μW maximum power dissipation
- Serial data interface
- 128 bits of display data RAM
- On-chip oscillator
- LCD drive voltage generator
- Four common driver outputs
- 32 segment driver outputs
- 0.9 to 6.0 V supply for logic circuitry operation
- 1.8 to 6.0 V supply for LCD driver operation
- Series specification
  S1D15100D00C∗: chip (Al pad)
  S1D15100F00C∗ : QFP12-48pin

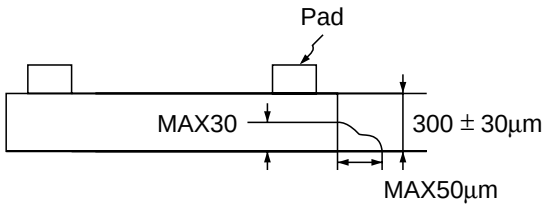
3. BLOCK DIAGRAM



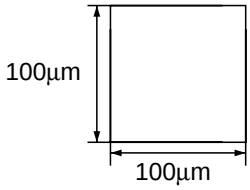
4. PAD LAYOUT AND COORDINATES (S1D15100D00C*)



Sectional dimensions



Size of pad opening



Chip size: 2500µm × 2500µm
Chip pitch: 525µm

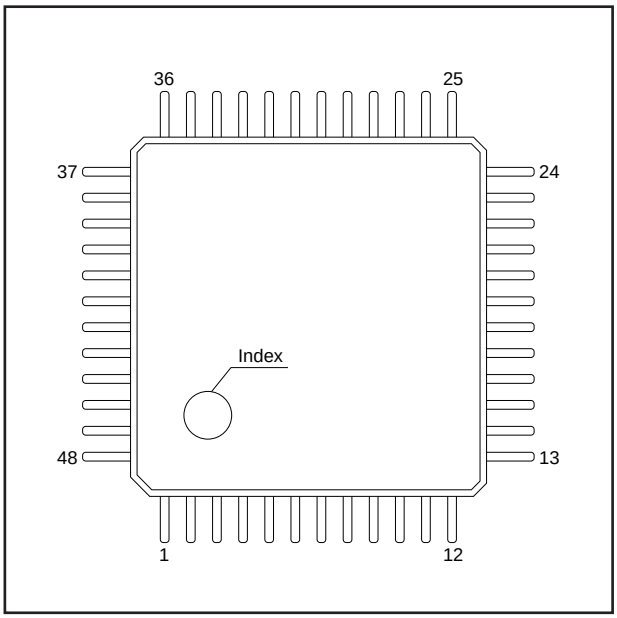
Pad center coordinates

Unit: µm

No.	Pin name	X coordinate	Y coordinate	No.	Pin name	X coordinate	Y coordinate
1	OSC1	-898	-1091	25	SEG 8	898	1091
2	OSC2	-738	-1091	26	SEG 9	738	1091
3	V1	-578	-1091	27	SEG 10	578	1091
4	V2	-418	-1091	28	SEG 11	418	1091
5	V3	-258	-1091	29	SEG 12	258	1091
6	V_{SS}	-98	-1091	30	SEG 13	98	1091
7	V_{DD}	63	-1091	31	SEG 14	-63	1091
8	CK	223	-1091	32	SEG 15	-223	1091
9	$\overline{SI}$	383	-1091	33	SEG 16	-383	1091
10	$\overline{CS}$	543	-1091	34	SEG 17	-543	1091
11	C/$\overline{D}$	703	-1091	35	SEG 18	-703	1091
12	COM0	863	-1091	36	SEG 19	-863	1091
13	COM1	1091	-898	37	SEG 20	-1091	898
14	COM2	1091	-738	38	SEG 21	-1091	738
15	COM3	1091	-578	39	SEG 22	-1091	578
16	V_{REG}	1091	-418	40	SEG 23	-1091	418
17	SEG 0	1091	-258	41	SEG 24	-1091	258
18	SEG 1	1091	-98	42	SEG 25	-1091	98
19	SEG 2	1091	63	43	SEG 26	-1091	-63
20	SEG 3	1091	224	44	SEG 27	-1091	-223
21	SEG 4	1091	383	45	SEG 28	-1091	-383
22	SEG 5	1091	543	46	SEG 29	-1091	-543
23	SEG 6	1091	703	47	SEG 30	-1091	-703
24	SEG 7	1091	863	48	SEG 31	-1091	-863

Origin: Center of the chip
Chip size: 2,500 × 2,500

5. PINOUT (S1D15100F00C*)



No.	Name	No.	Name	No.	Name
1	OSC1	17	SEG0	33	SEG16
2	OSC2	18	SEG1	34	SEG17
3	V_1	19	SEG2	35	SEG18
4	V_2	20	SEG3	36	SEG19
5	V_3	21	SEG4	37	SEG20
6	V_{SS}	22	SEG5	38	SEG21
7	V_{DD}	23	SEG6	39	SEG22
8	CK	24	SEG7	40	SEG23
9	SI	25	SEG8	41	SEG24
10	$\overline{CS}$	26	SEG9	42	SEG25
11	C/$\overline{D}$	27	SEG10	43	SEG26
12	COM0	28	SEG11	44	SEG27
13	COM1	29	SEG12	45	SEG28
14	COM2	30	SEG13	46	SEG29
15	COM3	31	SEG14	47	SEG30
16	V_{REG}	32	SEG15	48	SEG31

6. PIN DESCRIPTION

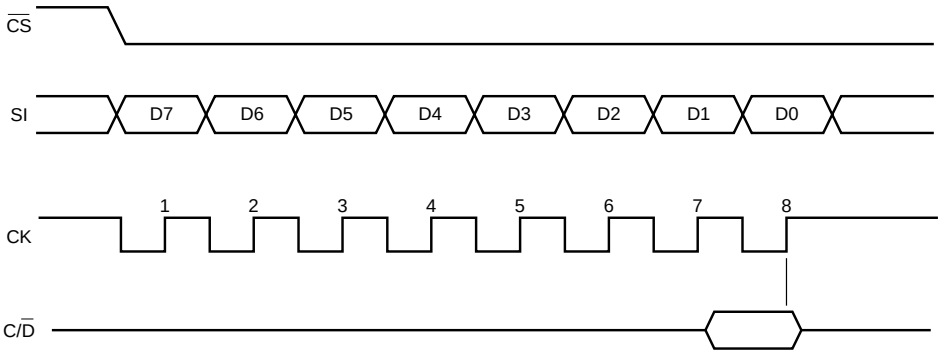
Pin Name	I/O	Description	Q'ty
V_{DD}	Power supply	Plus power terminal. Common to the microcomputer power terminal V_{CC}.	1
V_{SS}	Power supply	Minus power supply. A 0V terminal to be connected to the system GND.	1
V_1 V_2	O	Power level monitor terminal for liquid crystal drive. The levels $V_1 = 1/3 \times V_3$ and $V_2 = 2/3 \times V_3$ are generated from the inside of S1D15100F00C*.	2
V_3	Power supply	Power terminal for liquid crystal drive. Potential relations: $V_{DD} > V_3$.	1
SI	I	Serial data input. Input of display data and of commands to control operation of S1D15100F00C*. When display data is input, the relations between display data input and segment ON/OFF are as follows: SI input "0" $\rightarrow$ OFF, SI input "1" $\rightarrow$ ON	1
CK	I	Shift clock input of serial data (SI input). SI input data is read bit by bit in the serial register at the CK input leading edge.	1
C/$\overline{D}$	I	Identification of SI input as data or command (in case of S1D15100F00C* only). The LOW level indicates data, and the HIGH level does commands.	1
$\overline{CS}$	I	Chip select signal input (in case of S1D15100F00C* only). When $\overline{CS}$ input is changed from the HIGH level to the LOW level, S1D15100F00C* can accept SI inputs. The CK counter is set to the initial state when the $\overline{CS}$ input is changed from the HIGH level to the LOW level.	1
OSC1 OSC2	I O	Oscillation resistance connection terminal	2
SEG0 to SEG31	O	Segment signal for liquid crystal drive	32
COM0 to COM3	O	Common signal for liquid crystal drive	4
V_{REG}	O	Test terminal. Keep it open.	1

Total 48

7. FUNCTIONAL DESCRIPTION

Command/Data Register

◊ The command/data register consists of an 8-bit serial register and a 3-bit CK counter.
◊ When $\overline{CS}$ input changes from the HIGH level to the LOW level, S1D15100 Serise comes to accept SI inputs. Also, the CK counter is initialized when $\overline{CS}$ input changes from the HIGH level to the LOW level. S1D15100 Serise always accepts SI inputs. When the built-in timing generator (CR oscillator) starts oscillating, the CK counter is initialized.
◊ The serial register takes in serial data D7, D6, ... D0 in this order from the SI terminal on the rising edge of the CK. At the same time, the CK counter starts counting the serial clock. The CK counter, when counting 8 on the serial clock, returns to the initial state.
◊ So, serial data is taken in to the serial register in 8 bits and is processed.
◊ When the CK counter counts 8 of shift clock input (CK input) (reads the input 8-bit serial data), the serial data taken in the command/data register is output to the display data memory (RAM) if the input serial data is a display data, or is output to the command decoder if it is a command data.
◊ S1D15100 Serise identifies input serial data (SI input) as display data or command data judging from C/$\overline{D}$ input. It displays display data when C/$\overline{D}$ input is LOW level or command data when the input is HIGH level.
◊ S1D15100 Serise reads and identifies C/$\overline{D}$ input at the timing on the rising edge of 8xn of shift clock input (CK input) from the $\overline{CS}$ = LOW level. (n=1, 2, 3, ...)

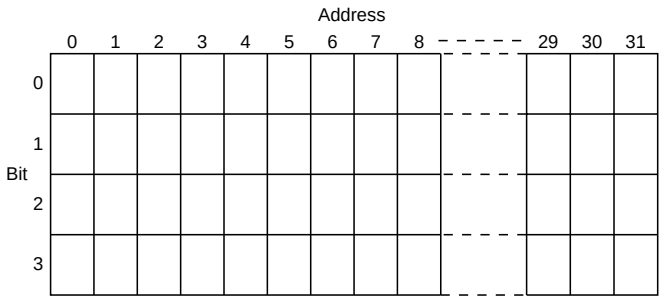


Command Decoder

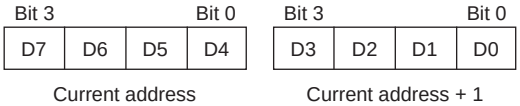
◊ When the command/data register data specifies any command (when C/$\overline{D}$ input is HIGH level when serial data is input), the command decoder takes in and decode the data of the command/data register to control S1D15100F00C∗.

Display Data Memory

The format of the 32 × 4-bit memory is shown in the following figure.



Each 8-bit display data byte loaded from the command/data register is stored in two consecutive addresses as shown in the following figure. The upper four bits are stored at the location specified by the address counter, and the lower four bits, at the next location. The address counter is automatically incremented by two.



A single 4-bit word can be written to memory using the Data Memory Write command as shown in the following figure. The lower four bits are stored at the location specified by the address counter. The address counter is automatically incremented by one.

1	0	0	✻	D3	D2	D1	D0

Bit 3 Bit 0

D3	D2	D1	D0

Address = n

Note

✻ = don't care

◊ The display data memory address is automatically incremented by 2 when a 8-bit display data (C/$\overline{D}$ = LOW level) is stored, or incremented by 1 when a 4-bit data is stored by the display data re-write command.

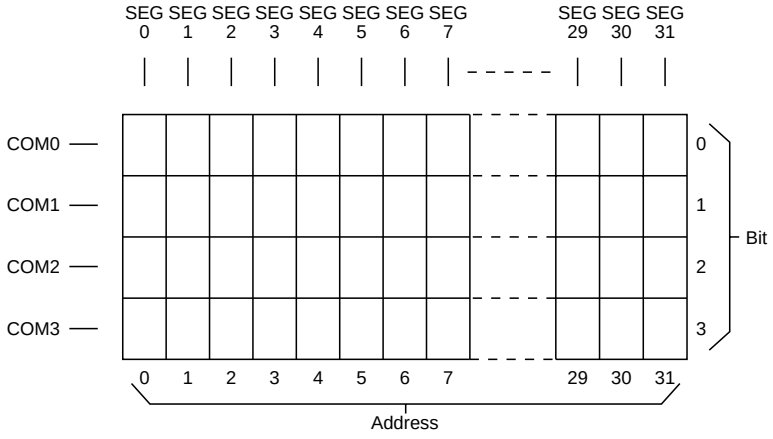
◊ After the display data is written in the RAM, the RAM address is held as shown below unless the address is reset:

After writing a 8-bit display data ...
the final write address is incremented by 2.

After rewriting a 4-bit display data ...
the final rewrite address is incremented by 1.

◊ Data in the display data memory synchronizes with the COM0 to COM3 signals and is output in 32 bits to the segment driver.

The relations of the display data memory, the segment terminal and common signal selection timing are as follows:



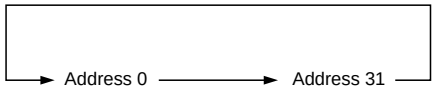
Address Counter

◊ The address counter is a presettable type to give 5-bit addresses to the display data memory.

◊ In case of S1D15100 Serise, any address can be set when the address set command is used.

◊ In case of S1D15100 Serise, set addresses are automatically incremented by 2 when an 8-bit display data is stored (C/$\overline{D}$ = LOW level), or incremented by 1 when a 4-bit data is stored by the display data memory rewrite command.

◊ The address decoder, after counting Address 31, counts 0 at the next counting and repeats as follows:

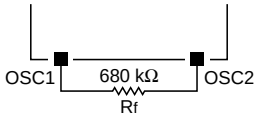


Address Decoder

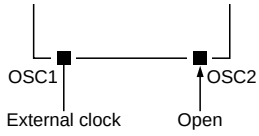
The address decoder sets addresses 0 to 31 of the display data memory where the display data of address counter is written.

Timing Generator

A low-power oscillator can be constructed using an external feedback resistor as shown in the following figure.



Alternatively, an 18 kHz external clock can be input on OSC1, and OSC2 left open, as shown in the following figure.



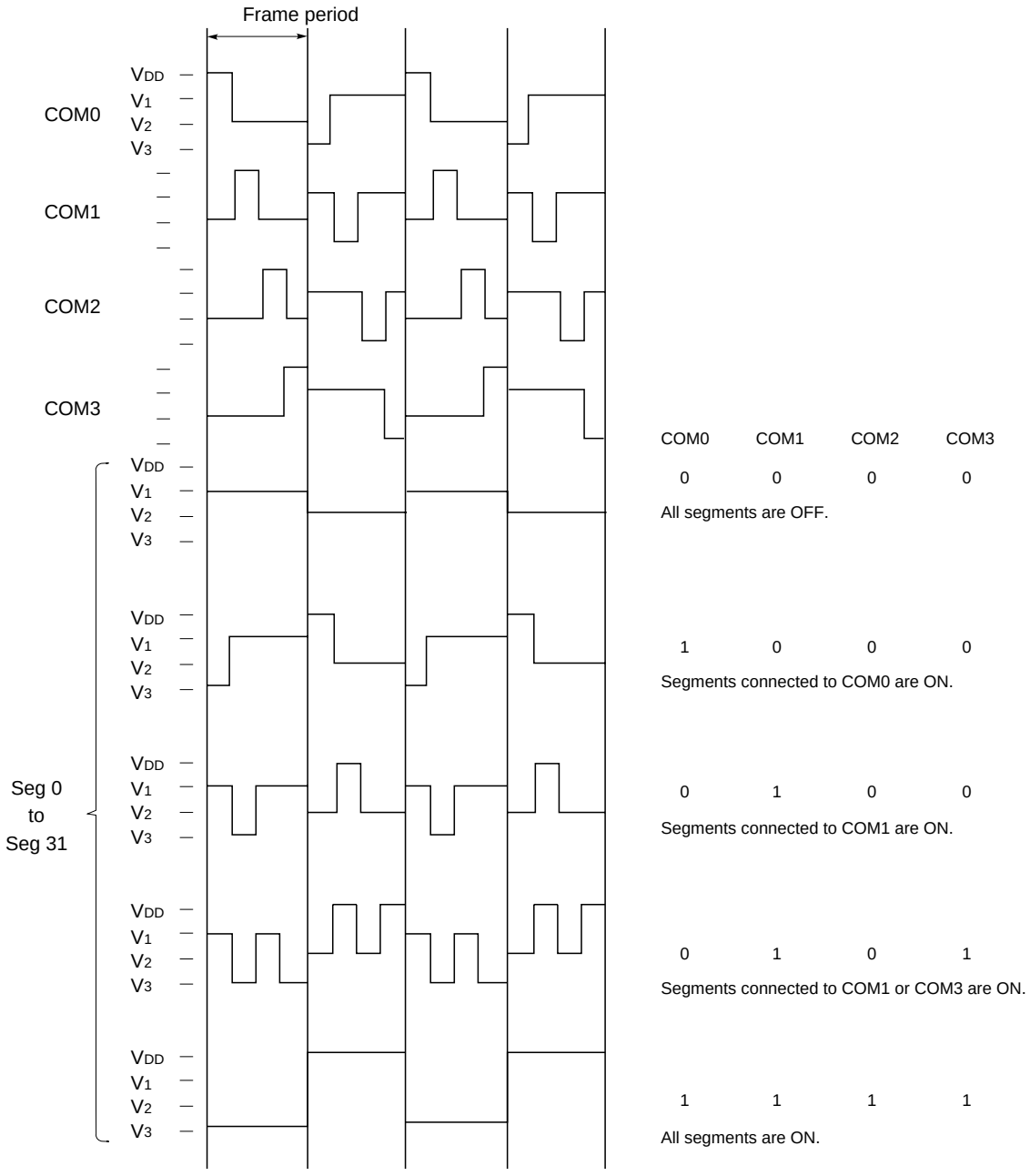
Common Counter

The timing generator clock signal is frequency-divided by the common counter to generate both the common drive timing and the alternating frame timing.

Segment and Common Drivers

The 32 segment drivers and the four common drivers are 4-level outputs that switch between V_{DD} and the V1, V2 and V3 LCD driver voltage levels.

The output states are determined by the display data values and the common counter as shown in the following figure. The outputs are used to drive a 1/3-bias, 1/4-duty LCD panel.



8. COMMANDS

The S1D15100F00C∗ samples C/$\overline{D}$ on every eighth rising edge of CK. If C/$\overline{D}$ is HIGH, the command/data register contents are latched into the command decoder. The command decoder executes the following six commands.

Address Set

Set the address counter to the value specified by D0 to D4.

0	0	0	D4	D3	D2	D1	D0

Addresses are incremented by 2 each time a display data (8-bit) is input. The relations between D4 to D0 and addresses are as follows:

D4	D3	D2	D1	D0	Address
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
1	1	1	0	0	28
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31

Display ON

Turn all LCD segments ON. The display memory data is not affected.

0	0	1	∗	∗	∗	∗	∗

Note: ∗ = don't care

Display OFF

Turn all LCD segments OFF. The display memory data is not affected.

0	1	0	∗	∗	∗	∗	∗

Note: ∗ = don't care

Display Start

Return to normal display mode. The display memory data is output to the display.

0	1	1	∗	∗	∗	∗	∗

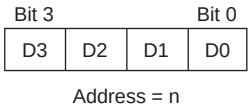
Note: ∗ = don't care

Memory Write

Store the data D0 to D3 at the location specified by the address counter. The address counter is automatically incremented by one. The other display memory locations are not affected.

1	0	0	∗	D3	D2	D1	D0

Data are allocated to each bit of the display data memory as follows:



Note: ∗ = don't care

Reset

Reset the S1D15100F00C∗. The S1D15100F00C∗ then enters normal operating mode, and the display turns OFF.

1	1	0	∗	∗	∗	∗	∗

Note: ∗ = don't care

9. SUPPLY VOLTAGES

In addition to V_{DD}, there are three LCD supply voltages: V_1 , V_2 and V_3. V_3 is supplied externally, whereas V_1 and V_2 are generated internally. V_1, V_2 and V_3 are given by the following equations.

$V_1 = V_{DD} – 1/3V_{LCD}$

$V_2 = V_{DD} – 2/3V_{LCD}$

$V_3 = V_{DD} – V_{LCD}$

where V_{LCD} is the LCD drive voltage. The voltages must be such that

$V_{DD} \geq V_1 \geq V_2 \geq V_3$

LCD supply voltage connections when the LCD drive supply is connected to V_{SS} are shown in figure 1, and the connections when the drive supply is independent of V_{SS}, in Figure 2.

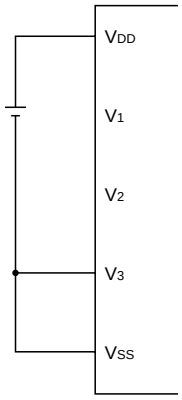


Figure 1. LCD drive supply connected to V_{SS}

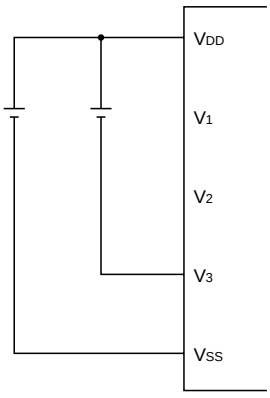
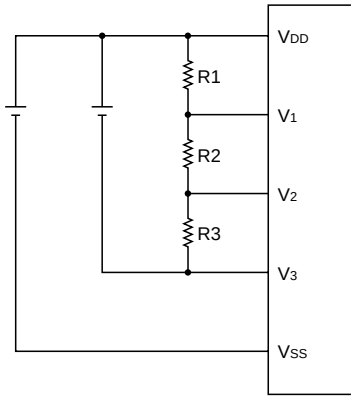


Figure 2. LCD drive supply not connected to V_{SS}

When there is a lot of distortion in the LCD drive waveforms, connect bleeder resistors as shown in the following figure.



10. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{SS}	–7.0 to 0.3	V
LCD supply voltage range	V_3	–7.0 to 0.3	V
Input voltage range	V_I	V_{SS} –0.3 to 0.3	V
Output voltage range	V_O	V_{SS} –0.3 to 0.3	V
Power dissipation	P_D	250	mW
Operating temperature range	T_{opg}	–20 to 75	°C
Storage temperature range	T_{stg}	–65 to 150	°C
Soldering temperature (10 sec at leads)	T_{sol}	260	°C
Heat resistance		400 • 10	°C•Min

Note: All voltages shown are specified on a V_{DD} = 0 V basis.

11. DC ELECTRICAL CHARACTERISTICS

V_{DD} = 0V, V_{SS} = –5.0 ±0.5 V, Ta = –20 to 75 °C unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Supply voltage	V_{SS}		–6.0	—	–0.9	V
LCD supply voltages	V_1		—	1/3 × V3	—	V
	V_2		—	2/3 × V3	—	
	V_3		–6.0	—	–1.8	
Quiescent supply current	I_{DDQ}	V_{SS} = –6.0 V, V_{IN} = V_{DD}	—	0.05	1.0	µA
Supply current	I_{DD1}	Display mode, R_f = 680 KΩ, V_{SS} = –5.0 V	—	20.0	30.0	µA
	I_{DD2}	Input mode, V_{SS} = –5.0 V, f_{ck} = 200 kHz	—	100	250	
LOW-level input voltage	V_{IL}		V_{SS}	—	0.8 V_{SS}	V
HIGH-level input voltage	V_{IH}		0.2 V_{SS}	—	V_{DD}	V
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$	—	0.05	2.0	µA
SEG0 to SEG31 and COM0 to COM3 LOW-level output voltage	V_{OL}	I_{OL} = 0.1 mA	—	—	V_{SS}+ 0.4	V
SEG0 to SEG31 and COM0 to COM3 HIGH-level output voltage	V_{OH}	I_{OH} = –0.1 mA	–0.4	—	—	V
Output leakage current	I_{LO}	$V_{SS} \le V_{OUT} \le V_{DD}$	—	0.05	5.0	µA
Oscillator frequency	f_{OSC}	V_{SS} = –5.0 V, R_f = 680 ±2% kΩ	—	18	—	kHz
		V_{SS} = –3.0 V, R_f =680 ±2% kΩ	—	16	—	
Input terminal capacity	C_I	Ta = 25°C, f = 1 MHz	—	5.0	8.0	pF
SEG0 to SEG31 and COM0 to COM3 ON resistance *1	R_{ON}	V_3 = –5.0 V, I ΔVON I = 0.1 V, Ta = 25 °C	—	5.0	7.5	kΩ
		V_3 = –0.3 V, I ΔVON I = 0.1 V, Ta = 25 °C	—	10.0	50.	

*1 The internal power impedance is not included in the LCD driver on resistance (R_{ON}).

12. AC ELECTRICAL CHARACTERISTICS

V_{DD} = 0 V, V_{SS} = –5.0 ±0.5 V, Ta = –20 to 75 °C

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
CK period	t_{CYC}		900	—	—	ns
CK LOW-level pulsewidth	t_{PWL1}		400	—	—	ns
CK HIGH-level pulsewidth	t_{PWH1}		400	—	—	ns
SI to CK setup time	t_{DW1}		100	—	—	ns
CK to SI hold time	t_{DH1}		200	—	—	ns
$\overline{CS}$ LOW-level puisewidth	t_{PWL2}	$t_{PWL2} \geq 8t_{CYC}$	7200*1	—	—	ns
$\overline{CS}$ HIGH-level pulsewidth	t_{PWH2}		400	—	—	ns
$\overline{CS}$ to CK setup time	t_{DW2}	Referenced to the rising edge of the first CK cycle.	100	—	—	ns
CK to $\overline{CS}$ hold time	t_{DH2}	Referenced to the rising edge of the eighth CK cycle.	200	—	—	ns
C/$\overline{D}$ to CK setup time	t_{DW3}	Referenced to the rising edge of the eighth CK cycle.	9	—	—	µs
CK to C/$\overline{D}$ hold time	t_{DH3}	Referenced to the rising edge of the eighth CK cycle.	1	—	—	µs
Rise time	t_r		—	—	50	ns
Fall time	t_f		—	—	50	ns

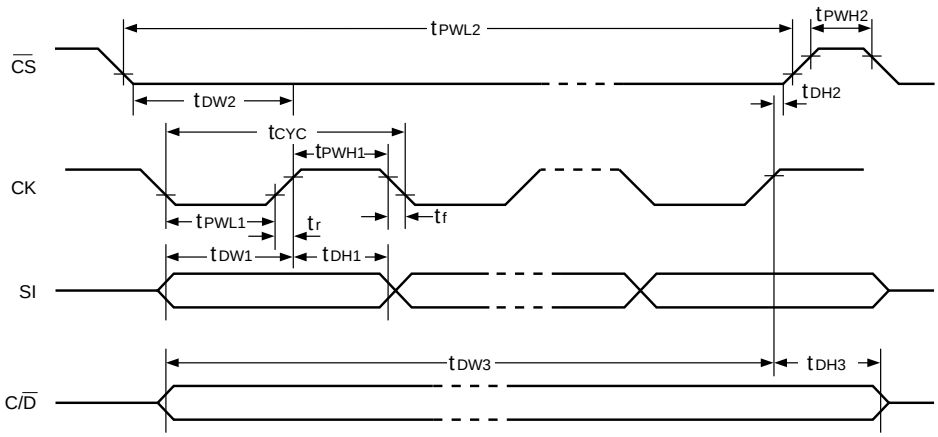
*1 $t_{CYC} \times 8$

V_{DD} = 0 V, V_{SS} = –6.0 to –1.5 V, Ta = –20 to 75 °C

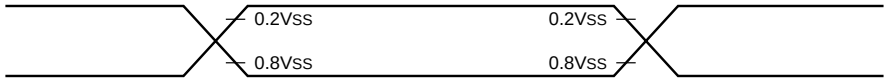
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
CK period	t_{CYC}		10	—	—	µs
CK LOW-level puisewidth	t_{PWL1}		4.5	—	—	µs
CK HIGH-level pulsewidth	t_{PWH1}		4.5	—	—	µs
SI to CK setup time	t_{DW1}		1.2	—	—	µs
CK to SI hold time	t_{DH1}		2.3	—	—	µs
$\overline{CS}$ LOW-level pulsewidth	t_{PWL2}	$t_{PWL2} \geq 8t_{CYC}$	80*1	—	—	µs
$\overline{CS}$ HIGH-level pulsewidth	t_{PWH2}		4.5	—	—	µs
$\overline{CS}$ to CK setup time	t_{DW2}	Referenced to the rising edge of the first CK cycle.	1.2	—	—	µs
CK to $\overline{CS}$ hold time	t_{DH2}	Referenced to the rising edge of the eighth CK cycle.	2.3	—	—	µs
C/$\overline{D}$ to CK setup time	t_{DW3}	Referenced to the rising edge of the eighth CK cycle.	100	—	—	µs
CK to C/$\overline{D}$ hold time	t_{DH3}	Referenced to the rising edge of the eighth CK cycle.	11	—	—	µs
Rise time	t_r		—	—	50	ns
Fall time	t_f		—	—	50	ns

*1 $t_{CYC} \times 8$

Timing Chart



Timing measurement



2. S1D15200 Series

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1. DESCRIPTION

The S1D15200 series of dot matrix LCD drivers are designed for the display of characters and graphics. The drivers generate LCD drive signals derived from bit mapped data stored in an internal RAM.
The drivers are available in two configurations
The S1D15200 series drivers incorporate innovative circuit design strategies to achieve very low power dissipation at a wide range of operating voltages.
These features give the designer a flexible means of implementing small to medium size LCD displays for compact, low power systems.

- The S1D15200 which is able to drive two lines of twelve characters each.
- The S1D15201 which is able to drive 80 segments for extention.
- The S1D15202 which is able to drive one line of thirteen characters each.

2. FEATURES

- Fast 8-bit MPU interface compatible with 80- and 68-family microcomputers
- Many command set
- Total 80 (segment + common) drive sets
- Low power — 30 μW at 2 kHz external clock
- Wide range of supply voltages
  V_{DD} – V_{SS}: –2.4 to –7.0 V
  V_{DD} – V5: –3.5 to –13.0 V
- Low-power CMOS

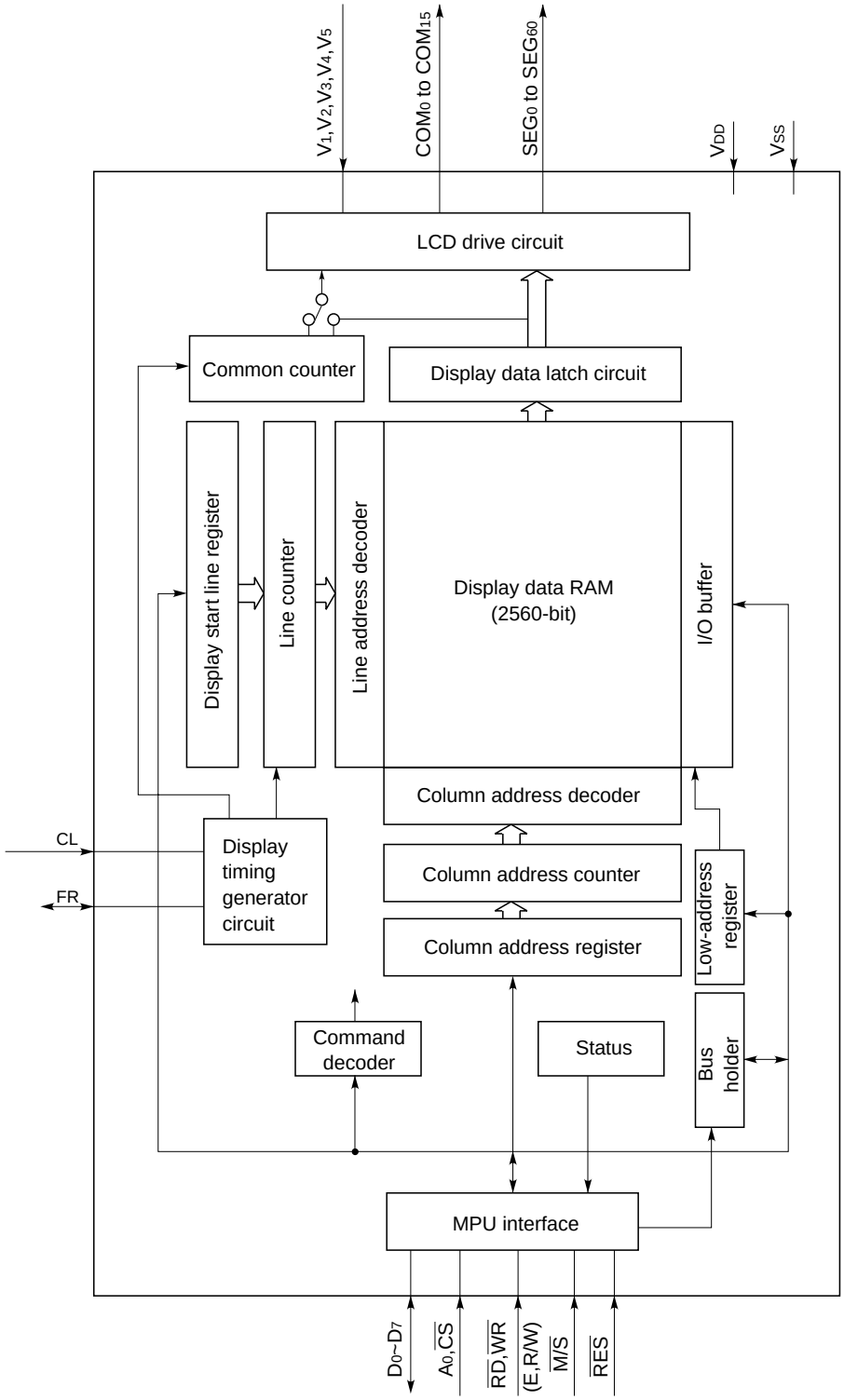
Line-up

Product Name	Clock Frequency		Applicable Driver	Number of SEG Drivers	Number of CMOS Drivers	Duty
	On-Chip	External				
S1D15200∗00∗∗	18 kHz	18 kHz	S1D15200∗00∗∗, S1D15201∗00∗∗	61	16	1/16, 1/32
S1D15201∗00∗∗	—	18 kHz	S1D15200∗00∗∗, S1D15202∗00∗∗	80	0	1/8 to 1/32
S1D15202∗00∗∗	18 kHz	18 kHz	S1D15202∗00∗∗, S1D15201∗00∗∗	69	8	1/8, 1/16
S1D15200∗10∗∗	—	2 kHz	S1D15200∗10∗∗, S1D15201∗10∗∗	61	16	1/16, 1/32
S1D15201∗10∗∗	—	2 kHz	S1D15200∗10∗∗, S1D15200∗10∗∗	80	0	1/8 to 1/32
S1D15202∗10∗∗	—	2 kHz	S1D15200∗10∗∗, S1D15201∗10∗∗	69	8	1/8, 1/16

- Package code (For example S1D15200)
  S1D15200T : TCP
  S1D15200F∗∗∗∗ : PKG
    - S1D15200F∗∗A∗ (QFP5-100pin)
    - S1D15200F∗∗C∗ (QFP15-100pin)
  S1D15200D∗∗∗∗ : Chip
    - S1D15200D∗∗A∗ (Al-pad)
    - S1D15200D∗∗B∗ (Au-bump)
    - S1D15200D∗∗E∗ (Au-bump)

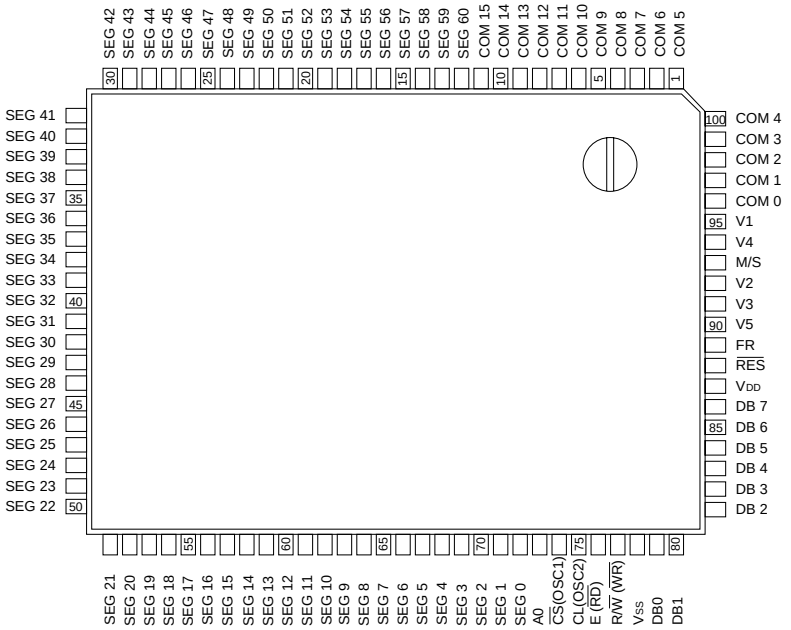
3. BLOCK DIAGRAM

An example of S1D15200∗10A∗:

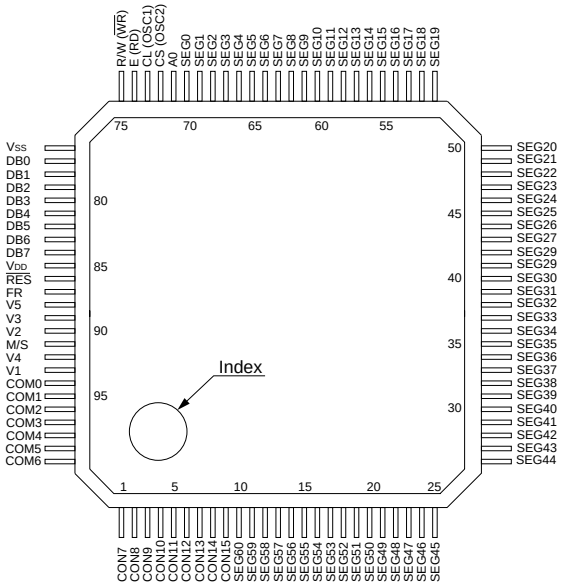


4. PIN LAYOUT

QFP5



QFP15



Note: This is an example of S1D15200F pin assignment. The modified pin names are given below.

Product Name	Pin/Pad Number					
	74	75	96 to 100, 1 to 11	93	94	95
S1D15200F00A*	OSC1	OSC2	COM0 to COM15*	M/S	V4	V1
S1D15201F00A*	CS	CL	SEG76 to SEG61	SEG79	SEG78	SEG77
S1D15202F00A*	OSC1	OSC2	COM0 to 7, SEG68 to 61	M/S	V4	V1
S1D15200F10A*	CS	CL	COM0 to COM15*	M/S	V4	V1
S1D15201F10A*	CS	CL	SEG76 to SEG61	SEG79	SEG78	SEG77
S1D15202F10A*	CS	CL	COM0 to 7, SEG68 to 61	M/S	V4	V1

S1D15200: Common outputs COM0 to COM15 of the master LSI correspond to COM31 to COM16 of the slave LSI.
S1D15202: Common outputs COM0 to COM15 of the master LSI correspond to COM15 to COM8 of the slave LSI.

5. PAD

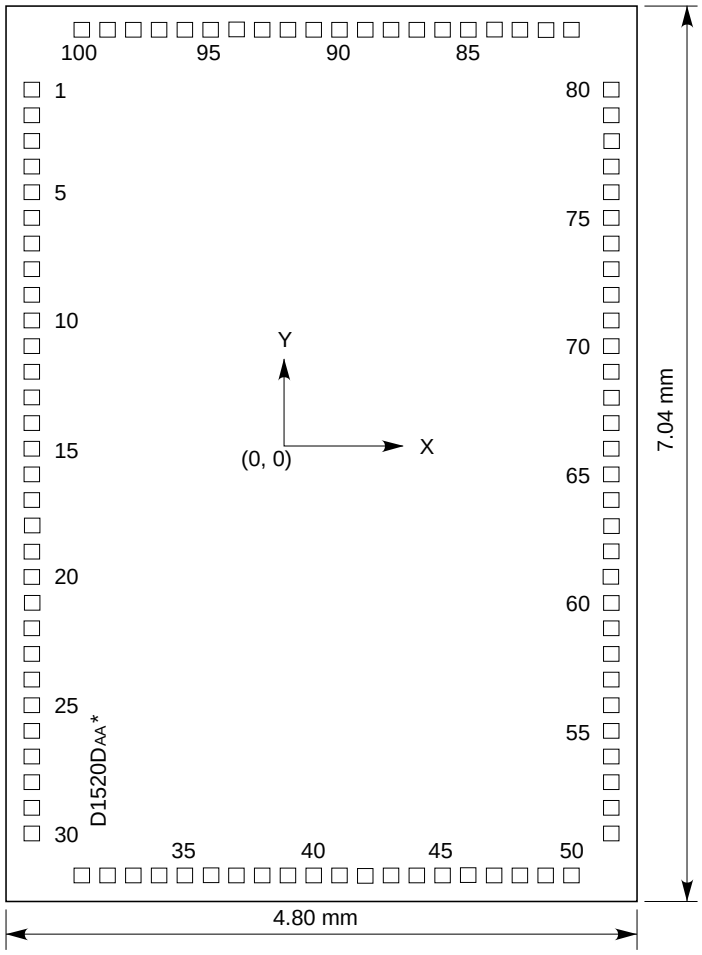
Pad Layout

Chip specifications of AL pad package

Chip size: 4.80×7.04×0.400 mm
Pad pitch: 100×100 μm

Chip specifications of gold bump package

Chip size: 4.80×7.04×0.525 mm
Bump pitch: 199 μm (Min.)
Bump height: 22.5 μm (Typ.)
Bump size: 132×111 μm (±20 μm) for mushroom model
116×92 μm (±4 μm) for vertical model



Note: An example of S1D15200D10A⋆ die numbers is given. These numbers are the same as the bump package.

Pad Center Coordinates

An example of S1D15200D10** pin names is given. The asterisk (*) can be A for AL pad package or B for gold bump package.

S1D15200D10B* Pad Center Coordinates

Pad No.	Pin Name	X	Y
1	COM5	159	6507
2	COM6	159	6308
3	COM7	159	6108
4	COM8	159	5909
5	COM9	159	5709
6	COM10	159	5510
7	COM11	159	5310
8	COM12	159	5111
9	COM13	159	4911
10	COM14	159	4712
11	COM15	159	4512
12	SEG60	159	4169
13	SEG59	159	3969
14	SEG58	159	3770
15	SEG57	159	3570
16	SEG56	159	3371
17	SEG55	159	3075
18	SEG54	159	2876
19	SEG53	159	2676
20	SEG52	159	2477
21	SEG51	159	2277
22	SEG50	159	2078
23	SEG49	159	1878
24	SEG48	159	1679
25	SEG47	159	1479
26	SEG46	159	1280
27	SEG45	159	1080
28	SEG44	159	881
29	SEG43	159	681
30	SEG42	159	482
31	SEG41	504	159
32	SEG40	704	159
33	SEG39	903	159
34	SEG38	1103	159
35	SEG37	1302	159
36	SEG36	1502	159
37	SEG35	1701	159
38	SEG34	1901	159
39	SEG33	2100	159
40	SEG32	2300	159
41	SEG31	2499	159
42	SEG30	2699	159
43	SEG29	2898	159
44	SEG28	3098	159
45	SEG27	3297	159
46	SEG26	3497	159
47	SEG25	3696	159
48	SEG24	3896	159
49	SEG23	4095	159
50	SEG22	4295	159
51	SEG21	4641	482
52	SEG20	4641	681
53	SEG19	4641	881
54	SEG18	4641	1080
55	SEG17	4641	1280
56	SEG16	4641	1479
57	SEG15	4641	1679
58	SEG14	4641	1878
59	SEG13	4641	2078
60	SEG12	4641	2277
61	SEG11	4641	2477
62	SEG10	4641	2676
63	SEG9	4641	2876
64	SEG8	4641	3075
65	SEG7	4641	3275
66	SEG6	4641	3474
67	SEG5	4641	3674
68	SEG4	4641	3948
69	SEG3	4641	4148
70	SEG2	4641	4347
71	SEG1	4641	4547
72	SEG0	4641	4789
73	A0	4641	5048
74	CS	4641	5247
75	CL	4641	5447
76	E ($\overline{RD}$)	4641	5646
77	R/W ($\overline{WR}$)	4641	5846
78	V_{SS}	4641	6107
79	DB0	4641	6307
80	DB1	4641	6506
81	DB2	4295	6884
82	DB3	4095	6884
83	DB4	3896	6884
84	DB5	3696	6884
85	DB6	3497	6884
86	DB7	3297	6884
87	V_{DD}	3098	6884
88	$\overline{RES}$	2898	6884
89	FR	2699	6884
90	V_5	2499	6884
91	V_3	2300	6884
92	V_2	2100	6884
93	M/S	1901	6884
94	V_4	1701	6884
95	V_1	1502	6884
96	COM0	1302	6884
97	COM1	1103	6884
98	COM2	903	6884
99	COM3	704	6884
100	COM4	504	6884

The other S1D15200 series packages have the different pin names as shown.

Package/Pad No.	74	75	96 to 100, 1 to 11	93	94	95
S1D15200D00**	OSC1	OSC2	COM0 to COM15 *	M/S	V_4	V_1
S1D15202D00**	OSC1	OSC2	COM0 to 7, SEG68 to 61	M/S	V_4	V_1
S1D15202D10**	OSC1	OSC2	COM0 to 7, SEG68 to 61	M/S	V_4	V_1
S1D15201D00**	CS	CL	SEG76 to SEG61	SEG79	SEG78	SEG77
S1D15201D10**	CS	CL	SEG76 to SEG61	SEG79	SEG78	SEG77

6. PIN DESCRIPTION

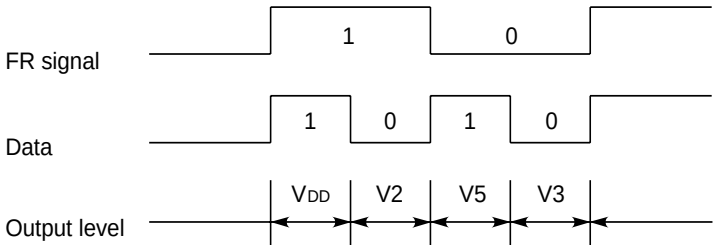
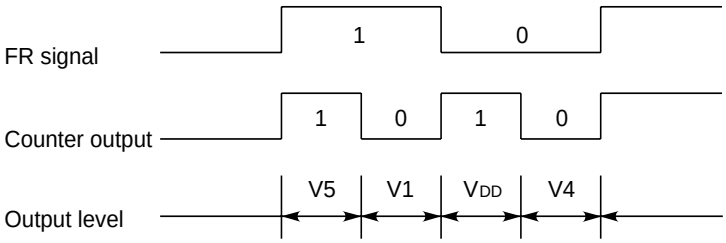
(1) Power Supply Pins

Name	Description
V_{DD}	Connected to the +5Vdc power. Common to the V_{CC} MPU power pin.
V_{SS}	0 Vdc pin connected to the system ground.
V_1, V_2, V_3, V_4, V_5	Multi-level power supplies for LCD driving. The voltage determined for each liquid crystal cell is divided by resistance or it is converted in impedance by the op amp, and supplied. These voltages must satisfy the following: $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$

(2) System Bus Connection Pins

D7 to D0	Three-state I/O. The 8-bit bidirectional data buses to be connected to the 8- or 16-bit standard MPU data buses.
A0	Input. Usually connected to the low-order bit of the MPU address bus and used to identify the data or a command. A0=0: D0 to D7 are display control data. A0=1: D0 to D7 are display data.
$\overline{RES}$	Input. When the $\overline{RES}$ signal goes ⊓⊔⊓ the 68-series MPU is initialized, and when it goes ⊔⊓⊔ , the 80-series MPU is initialized. The system is reset during edge sense of the $\overline{RES}$ signal. The interface type to the 68-series or 80-series MPU is selected by the level input as follows: High level: 68-series MPU interface Low level: 80-series MPU interface
$\overline{CS}$	Input. Active low. Effective for an external clock operation model only. An address bus signal is usually decoded by use of chip select signal, and it is entered. If the system has a built-in oscillator, this is used as an input pin to the oscillator amp and an Rf oscillator resistor is connected to it. In such case, the $\overline{RD}$, $\overline{WR}$ and E signals must be ORed with the $\overline{CS}$ signals and entered.
E ($\overline{RD}$)	• If the 68-series MPU is connected: Input. Active HIGH. Used as an enable clock input of the 68-series MPU. • If the 80-series MPU is connected: Input. Active LOW. The $\overline{RD}$ signal of the 80-series MPU is entered in this pin. When this signal is kept low, the SED1520 data bus is in the output status.
R/W ($\overline{WR}$)	• If the 68-series MPU is connected: Input. Used as an input pin of read control signals (if R/W is HIGH) or write control signals (if LOW). • If the 80-series MPU is connected: Input. Active LOW. The $\overline{WR}$ signal of the 80-series MPU is entered in this pin. A signal on the data bus is fetched at the rising edge of $\overline{WR}$ signal.

(3) LCD Drive Circuit Signals

<table>
<tr><th>Name</th><th>Description</th></tr>
<tr><td>CL</td><td>Input. Effective for an external clock operation model only.
This is a display data latch signal to count up the line counter and common counter at each signal falling and rising edges. If the system has a built-in oscillator, this is used as an output pin of the oscillator amp and an Rf oscillator resistor is connected to it.</td></tr>
<tr><td>FR</td><td>Input/output.
This is an I/P pin of LCD AC signals, and connected to the M terminal of common driver.
<u>I/O selection</u>
• Common oscillator built-in model: Output if M/S is 1; Input if M/S is 0.
• Dedicate segment model: Input</td></tr>
<tr><td>SEGn</td><td>Output.
The output pin for LCD column (segment) driving. A single level of V_{DD}, V_2, V_3 and V_5 is selected by the combination of display RAM contents and RF signal.
 
</td></tr>
<tr><td>COMn</td><td>Output.
The output pin for LCD common (low) driving. A single level of V_{DD}, V_1, V_4 and V_5 is selected by the combination of common counter output and RF signal. The slave LSI has the reverse common output scan sequence than the master LSI.
 
</td></tr>
<tr><td>M/S</td><td>Input.
The master or slave LSI operation select pin for the S1D15200 or S1D15202. Connected to V_{DD} (to select the master LSI operation mode) or V_{SS} (to select the slave LSI operation mode).
When this M/S pin is set, the functions of FR, COM0 to COM15, OSC1 ($\overline{CS}$), and OSC2 (CL) pins are changed.
<table>
<tr><th></th><th>M/S</th><th>FR</th><th>COM output</th><th>OSC1</th><th>OSC2</th></tr>
<tr><td rowspan="2">S1D15200F00A*</td><td>V_{DD}</td><td>Output</td><td>COM0 to COM15</td><td>Input</td><td>Output</td></tr>
<tr><td>V_{SS}</td><td>Input</td><td>COM31 to COM16</td><td>NC</td><td>Input</td></tr>
<tr><td rowspan="2">S1D15202F00A*</td><td>V_{DD}</td><td>Output</td><td>COM0 to COM7</td><td>Input</td><td>Output</td></tr>
<tr><td>V_{SS}</td><td>Input</td><td>COM15 to COM8</td><td>NC</td><td>Input</td></tr>
</table>
* The slave driver has the reverse common output scan sequence than the master driver.</td></tr>
</table>

7. FUNCTION DESCRIPTION

System Bus

MPU interface

1. Selecting an interface type

The S1D15200 series transfers data via 8-bit bidirectional data buses (D0 to D7). As its Reset pin has the MPU interface select function, the 80-series MPU or the 68-series MPU can directly be connected to the MPU bus by the selection of HIGH or LOW $\overline{RES}$ signal level after reset (see Table 1).
When the $\overline{CS}$ signal is high, the S1D15200 series is disconnected from the MPU bus and set to stand by. However, the reset signal is entered regardless of the internal setup status.

Table 1

$\overline{RES}$ signal input level	MPU type	A0	E	R/W	CS	D0 to D7
⊓⊔ Active	68-series	↑	↑	↑	↑	↑
⊔⊓ Active	80-series	↑	$\overline{RD}$	$\overline{WR}$	↑	↑

(1) Data transfer

The S1D15200 and S1D15201 drivers use the A0, E (or $\overline{RD}$) and R/$\overline{W}$ (or $\overline{WR}$) signals to transfer data between the system MPU and internal registers. The combinations used Access to Display Date RAM and Internal Registers are given in the table blow.

This means that a dummy read cycle has to be executed at the start of every series of reads. See Figure 1.
No dummy cycle is required at the start of a series of writes as data is transferred automatically from the input latch to its destination.

Table 2

Common	68 MPU	80 MPU		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read display data
1	0	1	0	Write display data
0	1	0	1	Read status
0	0	1	0	Write to internal register (command)

In order to match the timing requirements of the MPU with those of the display data RAM and control registers all data is latched into and out of the driver. This introduces a one cycle delay between a read request for data and the data arriving. For example when the MPU executes a read cycle to access display RAM the current contents of the latch are placed on the system data bus while the desired contents of the display RAM are moved into the latch.

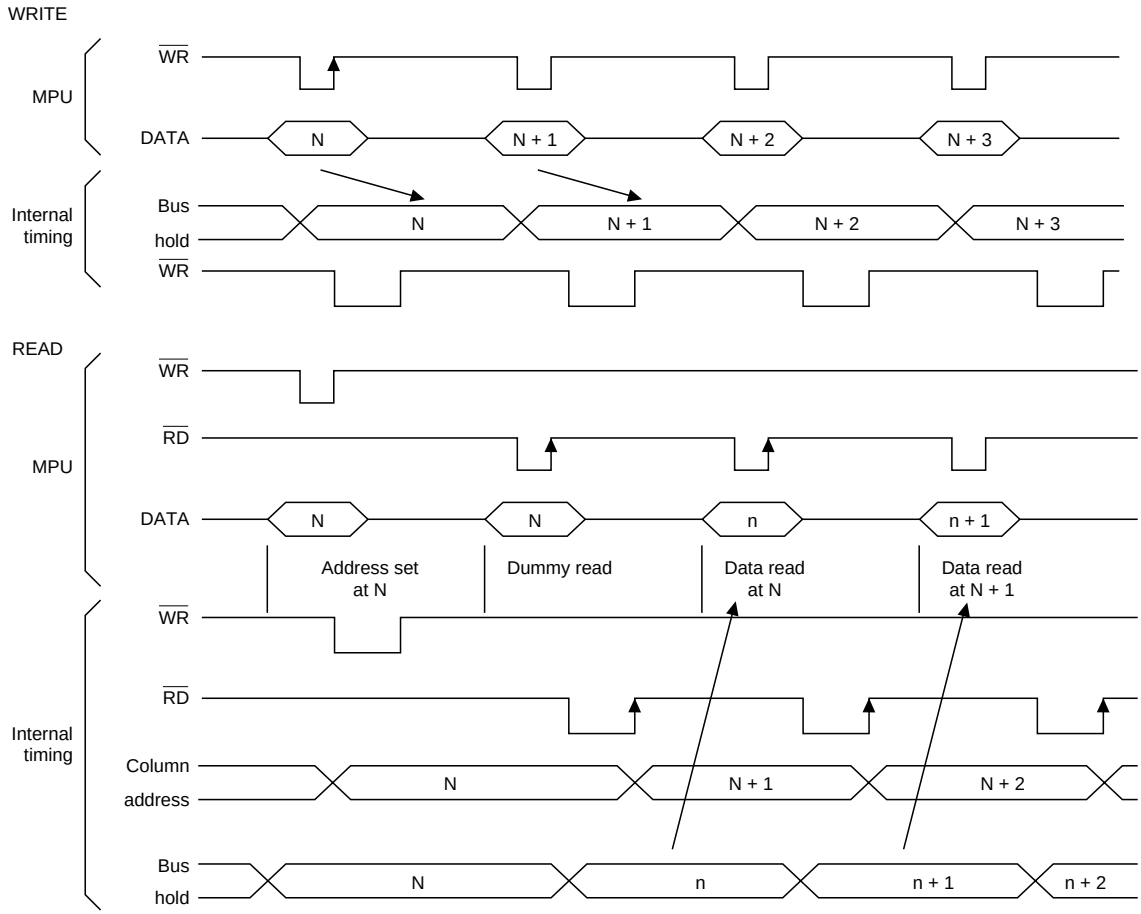


Figure 1 Bus Buffer Delay

(2) Busy flag

When the Busy flag is logical 1, the S1D15200 series is executing its internal operations. Any command other than Status Read is rejected during this time. The Busy flag is output at pin D7 by the Status Read command. If an appropriate cycle time (tcyc) is given, this flag needs not be checked at the beginning of each command and, therefore, the MPU processing capacity can greatly be enhanced.

(3) Display Start Line and Line Count Registers

The contents of this register form a pointer to a line of data in display data RAM corresponding to the first line of the display (COM0), and are set by the Display Start Line command. See section 3.

The contents of the display start line register are copied into the line count register at the start of every frame, that is on each edge of FR. The line count register is incremented by the CL clock once for every display line, thus generating a pointer to the current line of data, in display data RAM, being transferred to the segment driver circuits.

(4) Column Address Counter

The column address counter is a 7-bit presettable counter that supplies the column address for MPU access to the display data RAM. See Figure 2. The counter is incremented by one every time the driver receives a Read or Write Display Data command. Addresses above 50H are invalid, and the counter will not increment past this value. The contents of the column address counter are set with the Set Column Address command.

(5) Page Register

The page resiter is a 2-bit register that supplies the page address for MPU access to the display data RAM. See Figure 2. The contents of the page register are set by the Set Page Register command.

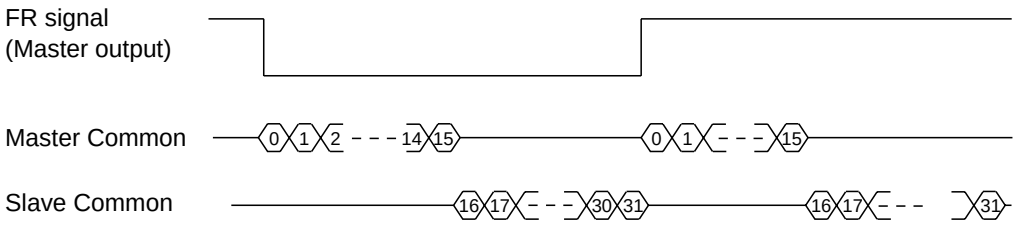
(6) Display Data RAM

The display data RAM stores the LCD display data, on a 1-bit per pixel basis. The relation-ship between display data, display address and the display is shown in Figure 2.

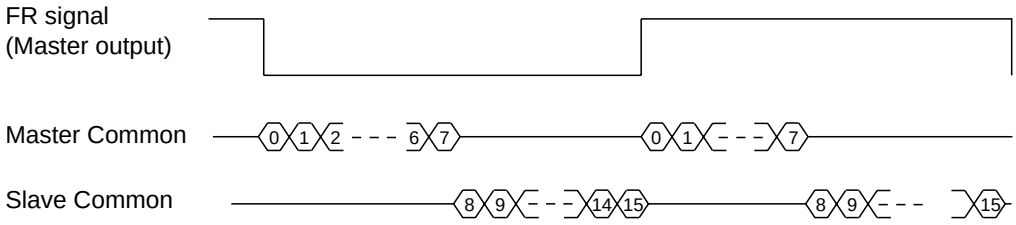
(7) Common Timing Generator Circuit

Generates common timing signals and FR frame signals from the CL basic clock. The 1/16 or 1/32 duty (for S1D15200) or 1/8 or 1/16 duty (for S1D15202) can be selected by the Duty Select command. If the 1/32 duty is selected for the S1D15200 and 1/16 duty is selected for the S1D15202, the 1/32 and 1/16 duties are provided by two chips consisting of the master and slave chips in the common multi-chip mode.

S1D15200



S1D15220



(8) Display Data Latch Circuit

This latch stores one line of display data for use by the LCD driver interface circuitry. The output of this latch is controlled by the Display ON/OFF and Static Drive ON/OFF commands.

(9) LCD Driver Circuit

The LCD driver circuitry generates the 80 4-level signals used to drive the LCD panel, using output from the display data latch and the common timing generator circuitry.

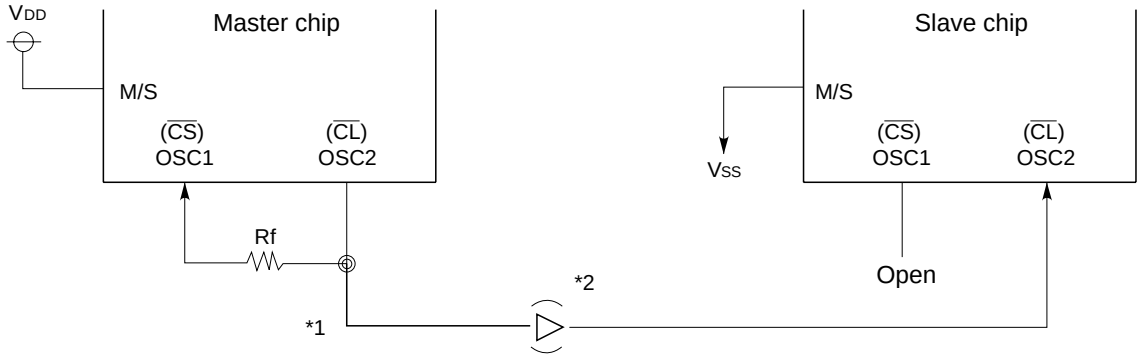
(10) Display Timing Generator

This circuit generates the internal display timing signal using the basic clock, CL, and the frame signals, FR. FR is used to generate the dual frame AC-drive waveform (type B drive) and to lock the line counter and common timing generator to the system frame rate. CL is used to lock the line counter to the system line scan rate. If a system uses both S1D15200 or S1D15202 and S1D15201 they must have the same CL frequency rating.

(11) Oscillator Circuit (S1D15200*0A Only)

A low power-consumption CR oscillator for adjusting the oscillation frequency using Rf oscillation resistor only. This circuit generates a display timing signal. Some of S1D15200 and S1D15202 series models have a built-in oscillator and others use an external clock. This difference must be checked before use.
Connect the Rf oscillation resistor as follows. To suppress the built-in oscillator circuit and drive the MPU using an external clock, enter the clock having the same phase as the OSC2 of mater chip into OSC2 of the slave chip.

- MPU having a built-in oscillator



*1 If the parasitic capacitance of this section increases, the oscillation frequency may shift to the lower frequency. Therefore, the Rf oscillation frequency must be reduced below the specified level.
*2 A CMOS buffer is required if the oscillation circuit is connected to two or more slave MPU chips.

- MPU driven with an external clock

(12) Reset Circuit

Detects a rising or falling edge of an $\overline{RES}$ input and initializes the MPU during power-on.

- Initialization status
  1. Display is off.
  2. Display start line register is set to line 1.
  3. Static drive is turned off.
  4. Column address counter is set to address 0.
  5. Page address register is set to page 3.
  6. 1/32 duty (S1D15200) or 1/16 duty (S1D15202) is selected.
  7. Forward ADC is selected (ADC command D0 is 1 and ADC status flag is 1).
  8. Read-modify-write is turned off.

The input signal level at $\overline{RES}$ pin is sensed, and an MPU interface mode is selected as shown on Table 1. For the 80-series MPU, the $\overline{RES}$ input is passed through the inverter and the active high reset signal must be entered. For the 68-series MPU, the active low reset signal must be entered.
As shown for the MPU interface (reference example), the $\overline{RES}$ pin must be connected to the Reset pin and reset at the same time as the MPU initialization.
If the MPU is not initialized by the use of $\overline{RES}$ pin during power-on, an unrecoverable MPU failure may occur.
When the Reset command is issued, initialization

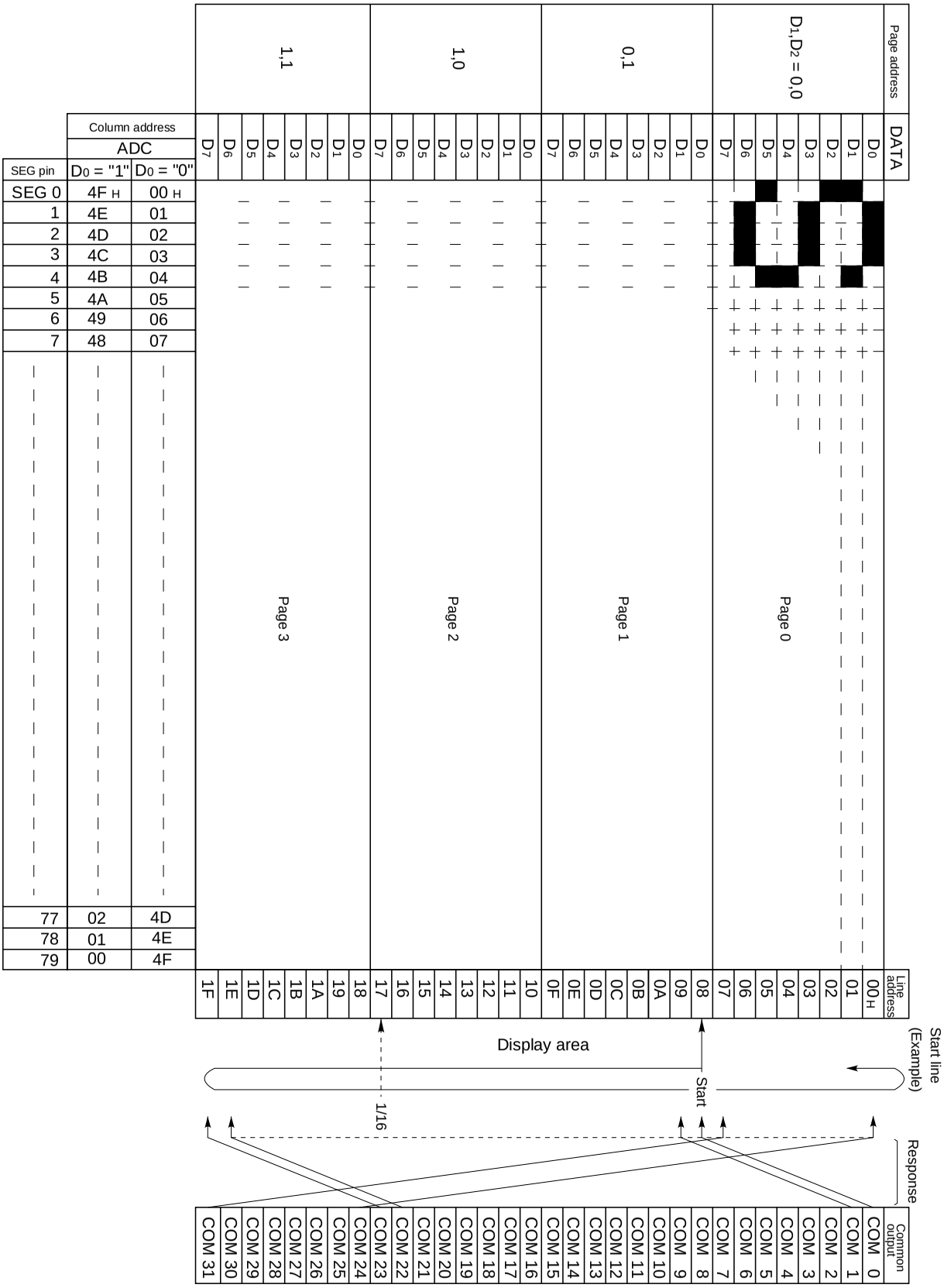


Figure 2 Display Data RAM Addressing

1/5 bias, 1/16 duty
1/6 bias, 1/32 duty

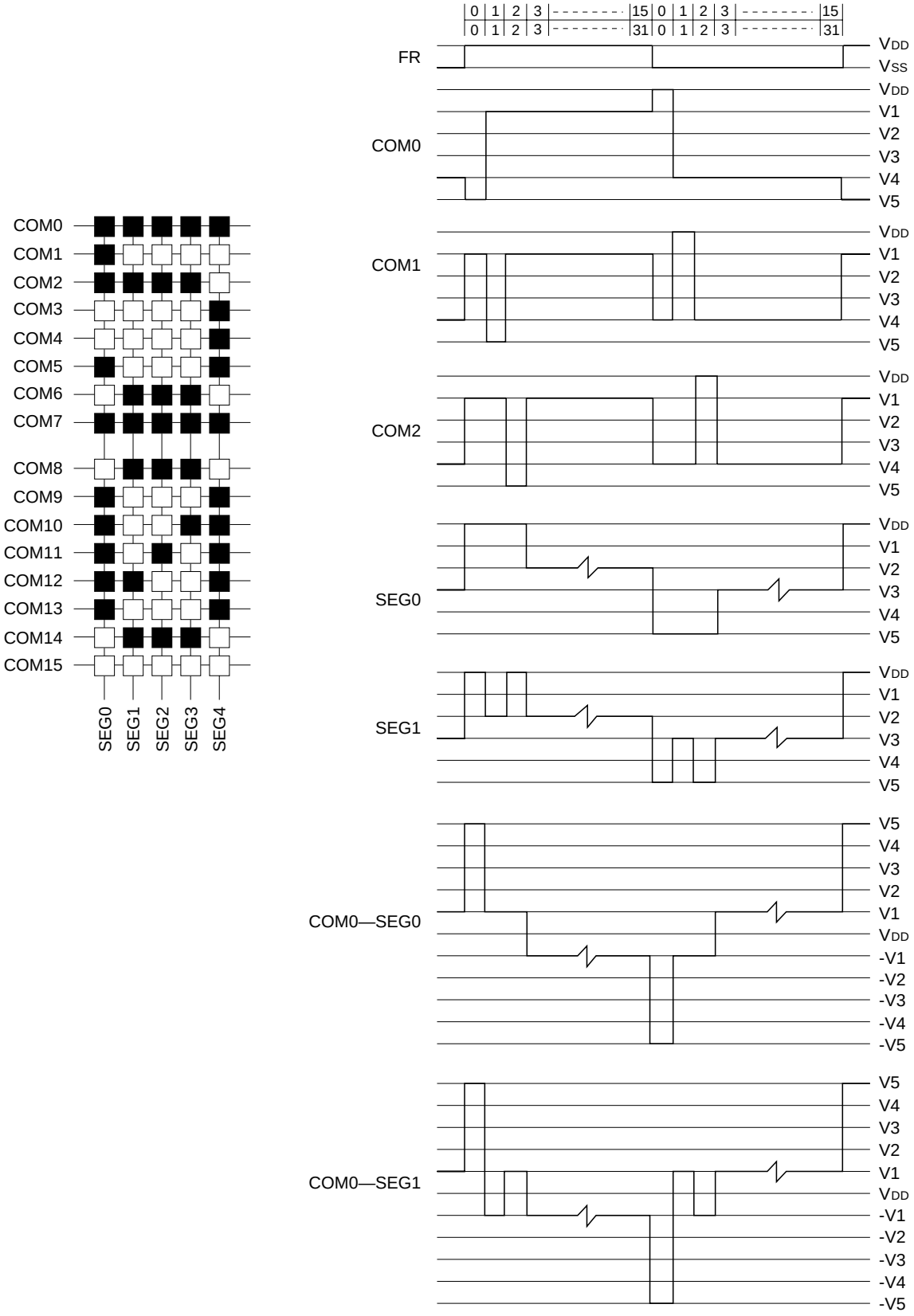


Figure 4 LCD drive waveforms example

8. COMMANDS

Table 3

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
(1) Display On/OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns display on or off. 1: ON, 0: OFF
(2) Display start line	0	1	0	1	1	0Display start address (0 to 31)						Specifies RAM line corresponding to top line of display.
(3) Set page address	0	1	0	1	0	1	1	1	0	Page (0 to 3)		Sets display RAM page in page address register.
(4) Set column (segment) address	0	1	0	0	Column address (0 to 79)							Sets display RAM column address in column address register.
(5) Read status	0	0	1	Busy	ADC	ON/OFF	Reset	0	0	0	0	Reads the following status: BUSY 1: Busy 0: Ready ADC 1: CW output 0: CCW output ON/OFF 1: Display off 0: Display on RESET 1: Being reset 0: Normal
(6) Write display data	1	1	0	Write data								Writes data from data bus into display RAM.
(7) Read display data	1	0	1	Read data								Reads data from display RAM onto data bus.
(8) Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	0: CW output, 1: CCW output
(9) Static drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects static driving operation. 1: Static drive, 0: Normal driving
(10) Select duty	0	1	0	1	0	1	0	1	0	0	0/1	Selets LCD duty cycle 1: 1/32, 0: 1/16
(11) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-modify-write ON
(12) End	0	1	0	1	1	1	0	1	1	1	0	Read-modify-write OFF
(13) Reset	0	1	0	1	1	1	0	0	0	1	0	Software reset

Command Description

Table 3 is the command table. The S1D15200 series identifies a data bus using a combination of A0 and R/W ($\overline{RD}$ or $\overline{WR}$) signals. As the MPU translates a command in the internal timing only (independent from the external clock), its speed is very high. The busy check is usually not required.

(1) Display ON/OFF

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	1	1	1	D	AEH, AFH

This command turns the display on and off.

- D=1: Display ON
- D=0: Display OFF

(2) Display Start Line

This command specifies the line address shown in Figure 3 and indicates the display line that corresponds to COM0. The display area begins at the specified line address and continues in the line address increment direction. This area having the number of lines of the specified display duty is displayed. If the line address is changed dynamically by this command, the vertical smooth scrolling and paging can be used.

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	0	A_4	A_3	A_2	A_1	A_0	C0H to DFH

This command loads the display start line register.

A_4	A_3	A_2	A_1	A_0	Line Address
0	0	0	0	0	0
0	0	0	0	1	1
		:			:
		:			:
1	1	1	1	1	31

See Figure 2.

(3) Set Page Address

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified. The display status is not changed even when the page address is changed.

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	1	1	0	A_1	A_0	B8H to BBH

This command loads the page address register.

A_1	A_0	Page
0	0	0
0	1	1
1	0	2
1	1	3

See Figure 2.

(4) Set Column Address

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by 1 each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 80, and the page address is not changed continuously.

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	0	A_6	A_5	A_4	A_3	A_2	A_1	A_0	00H to 4FH

This command loads the column address register.

A_6	A_5	A_4	A_3	A_2	A_1	A_0	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				:
			:				:
1	0	0	1	1	1	1	79

(5) Read Status

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Reading the command I/O register (A0=0) yields system status information.

- The busy bit indicates whether the driver will accept a command or not.
  Busy=1: The driver is currently executing a command or is resetting. No new command will be accepted.
  Busy=0: The driver will accept a new command.
- The ADC bit indicates the way column addresses are assigned to segment drivers.
  ADC=1: Normal. Column address n → segment driver n.
  ADC=0: Inverted. Column address 79-u → segment driver u.
- The ON/OFF bit indicates the current status of the display.
  It is the inverse of the polarity of the display ON/OFF command.
  ON/OFF=1: Display OFF
  ON/OFF=0: Display ON
- The RESET bit indicates whether the driver is executing a hardware or software reset or if it is in normal operating mode.
  RESET=1: Currently executing reset command.
  RESET=0: Normal operation

(6) Write Display Data

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	Write data							

Writes 8-bits of data into the display data RAM, at a location specified by the contents of the column address and page address registers and then increments the column address register by one.

(7) Read Display Data

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	Read data							

Reads 8-bits of data from the data I/O latch, updates the contents of the I/O latch with display data from the display data RAM location specified by the contents of the column address and page address registers and then increments the column address register.
After loading a new address into the column address register one dummy read is required before valid data is obtained.

(8) Select ADC

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	0	0	0	D	A0H, A1H

This command selects the relationship between display data RAM column addresses and segment drivers.
D=1: SEG0 ← column address 4FH, … (inverted)
D=0: SEG0 ← column address 00H, … (normal)
This command is provided to reduce restrictions on the placement of driver ICs and routing of traces during printed circuit board design. See Figure 2 for a table of segments and column addresses for the two values of D.

(9) Static Drive ON/OFF

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	0	1	0	D	A4H, A5H

Forces display on and all common outputs to be selected.
D=1: Static drive on
D=0: Static drive off

(10) Select Duty

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	1	0	0	D	A8H, A9H

This command sets the duty cycle of the LCD drive and is only valid for the S1D15200F and S1D15202F. It is invalid for the S1D15201F which performs passive operation. The duty cycle of the S1D15201F is determined by the externally generated FR signal.

	S1D15200	S1D15202
D=1:	1/32 duty cycle	1/16 duty cycle
D=0:	1/16 duty cycle	1/8 duty cycle

When using the S1D15200F00A∗, S1D15202F00A∗ (having a built-in oscillator) and the S1D15201F00A∗ continuously, set the duty as follows:

		S1D15201F00A∗
S1D15200F00A∗	1/32	1/32
	1/16	1/16
S1D15202F00A∗	1/16	1/32
	1/8	1/16

(11) Read-Modify-Write

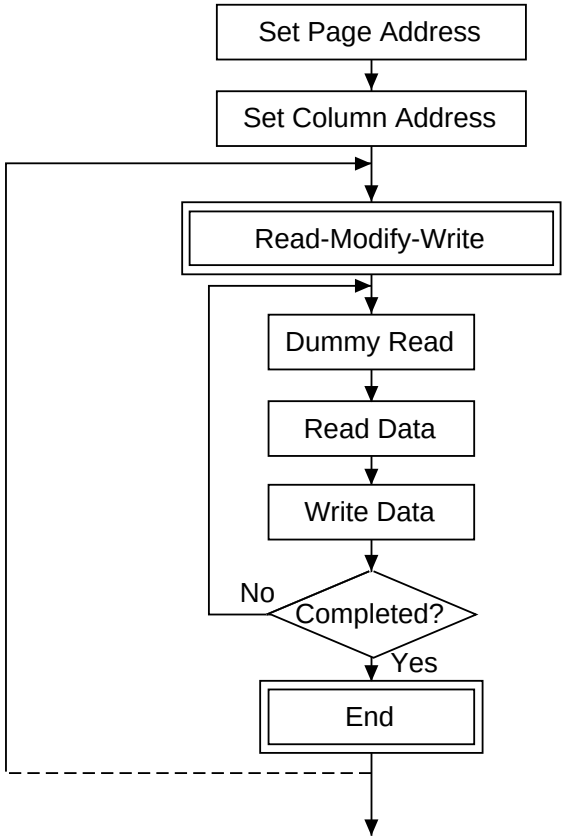
A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	0	0	0	0	E0H

This command defeats column address register auto-increment after data reads. The current conetents of the column address register are saved. This mode remains active until an End command is received.

- Operation sequence during cursor display

When the End command is entered, the column address is returned to the one used during input of Read-Modify-Write command. This function can reduce the load of MPU when data change is repeated at a specific display area (such as cursor blinking).

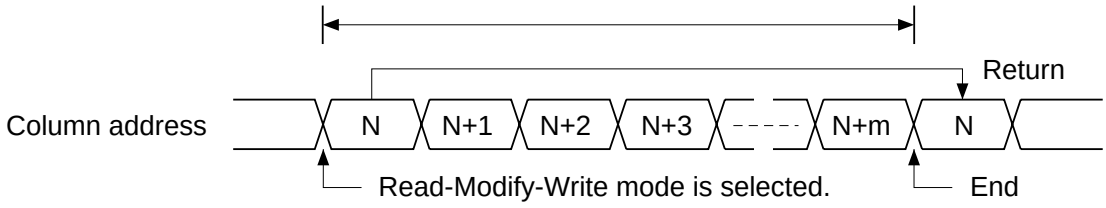
* Any command other than Data Read or Write can be used in the Read-Modify-Write mode. However, the Column Address Set command cannot be used.



(12) End

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	1	1	1	0	EEH

This command cancels read-modify-write mode and restores the contents of the column address register to their value prior to the receipt of the Read-Modify-Write command.



(13) Reset

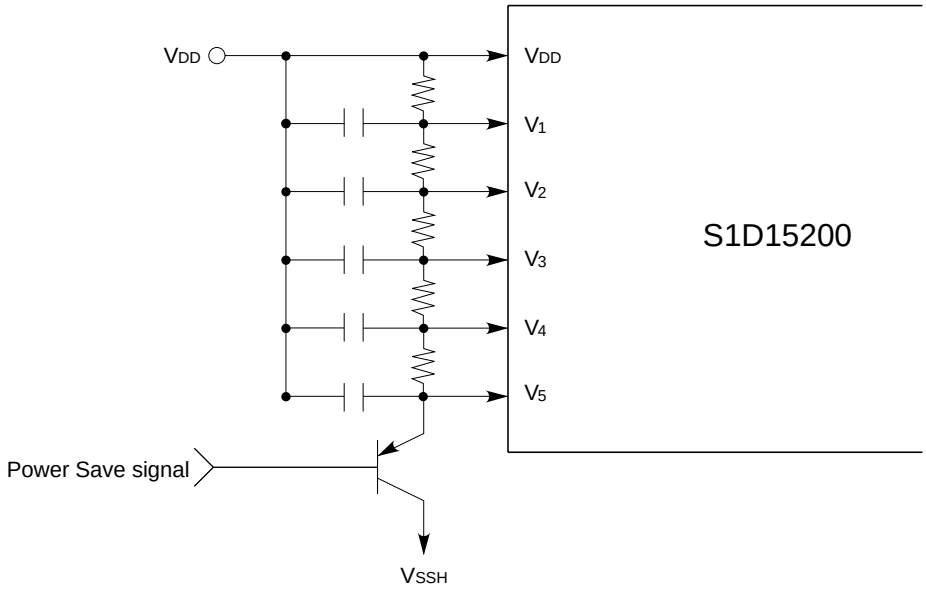
A_0	$\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	0	0	1	0	E2H

This command clears
- the display start line register.
- and set page address register to 3 page.
  It does not affect the contents of the display data RAM.

When the power supply is turned on, a Reset signal is entered in the $\overline{RES}$ pin. The Reset command cannot be used instead of this Reset signal.

(14) Power Save (Combination command)

The Power Save mode is selected if the static drive is turned ON when the display is OFF. The current consumption can be reduced to almost the static current level. In the Power Save mode:
(a) The LCD drive is stopped, and the segment and common driver outputs are set to the V_{DD} level.
(b) The external oscillation clock input is inhibited, and the OSC2 is set to the floating mode.
(c) The display and operation modes are kept.
The Power Save mode is released when the display is turned ON or when the static drive is turned OFF. If the LCD drive voltage is supplied from an external resistance divider circuit, the current passing through this resistor must be cut by the Power Save signal.



If the LCD drive power is generated by resistance division, the resistance and capacitance are determined by the LCD panel size. After the panel size has been determined, reduce the resistance to the level where the display quality is not affected and reduce the power consumption using the divider resistor.

9. ABSOLUTE MAXIMUS RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{SS}	–8.0 to +0.3	V
Supply voltage (2)	V_5	–16.5 to +0.3	V
Supply voltage (3)	V_1, V_4, V_2, V_3	V5 to +0.3	V
Input voltage	V_{IN}	V_{SS}–0.3 to +0.3	V
Output voltage	V_O	V_{SS}–0.3 to +0.3	V
Power dissipation	P_D	250	mW
Operating temperature	T_{opr}	–40 to +85	°C
Storage temperature	T_{stg}	–65 to +150	°C
Soldering temperature time at lead	T_{sol}	260, 10	°C, sec

Notes: 1. All voltages are specified relative to V_{DD} = 0 V.
2. The following relation must be always hold
$V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$
3. Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced by the soldering process, so care should be taken to avoid thermally stressing the package during board assembly.

10. ELECTRICAL CHARCTERISTICS

DC Characteristics

Ta = –20 to 75 °C, V_{DD} = 0 V unless stated otherwise

Parameter		Symbol	Condition		Rating			Unit	Applicable Pin
					Min.	Typ.	Max.		
Operating voltage (1) See note 1.	Recommended	V_{SS}			–5.5	–5.0	–4.5	V	V_{SS}
	Allowable				–7.0	—	–2.4		
Operating voltage (2)	Recommended	V_5			–13.0	—	–3.5	V	V_5 See note 10.
	Allowable				–13.0	—	—		
	Allowable	V_1, V_2			0.6×V_5	—	V_{DD}	V	V_1, V_2
	Allowable	V_3, V_4			V_5	—	0.4×V_5	V	V_3, V_4
High-level input voltage		V_{IHT}			V_{SS}+2.0	—	V_{DD}	V	See note 2 & 3.
		V_{IHC}			0.2×V_{SS}	—	V_{DD}		
		V_{IHT}	V_{SS} = –3 V		0.2×V_{SS}	—	V_{DD}		See note 2 & 3.
		V_{IHC}	V_{SS} = –3 V		0.2×V_{SS}	—	V_{DD}		
Low-level input voltage		V_{ILT}			V_{SS}		V_{SS}+0.8		See note 2 & 3.
		V_{ILC}			V_{SS}		0.8×V_{SS}		
		V_{ILT}	V_{SS} = –3 V		V_{SS}		0.85×V_{SS}		See note 2 & 3.
		V_{ILC}	V_{SS} = –3 V		V_{SS}		0.8×V_{SS}		
High-level output voltage		V_{OHT}	I_{OH} = –3.0 mA		V_{SS}+2.4	—	—	V	OSC2 See note 4 & 5.
		V_{OHC1}	I_{OH} = –2.0 mA		V_{SS}+2.4	—	—		
		V_{OHC2}	I_{OH} = –120 µA		0.2×V_{SS}	—	—		
		V_{OHT}	V_{SS} = –3 V	I_{OH} = –2 mA	0.2×V_{SS}			V	See note 4 & 5. OSC2
		V_{OHC1}	V_{SS} = –3 V	I_{OH} = –2 mA	0.2×V_{SS}				
		V_{OHC2}	V_{SS} = –3 V	I_{OH} = –50 µA	0.2×V_{SS}				

(continued)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Applicable Pin
Low-level output voltage	V_{OLT}	I_{OL} = 3.0 mA		—	—	V_{SS}+0.4	V	OSC2 See note 4 & 5.
	V_{OLC1}	I_{OL} = 2.0 mA		—	—	V_{SS}+0.4		
	V_{OLC2}	I_{OL} = 120 µA		—	—	0.8×V_{SS}		
	V_{OLT}	V_{SS} = –3 V	I_{OL} = 2 mA			0.8×V_{SS}	V	See note 4 & 5. OSC2
	V_{OLC1}	V_{SS} = –3 V	I_{OL} = 2 mA			0.8×V_{SS}		
	V_{OLC2}	V_{SS} = –3 V	I_{OL} = 50 µA			0.8×V_{SS}		
Input leakage current	I_{LI}			–1.0	—	1.0	µA	See note 6.
Output leakage current	I_{LO}			–3.0	—	3.0	µA	See note 7.
LCD driver ON resistance	R_{ON}	Ta = 25 °C	V_5 = –5.0 V	—	5.0	7.5	kΩ	SEG0 to 79, COM0 to 15, See note 11
			V_5 = –3.5 V	—	10.0	50.0		
Static current dissipation	I_{DDQ}	$\overline{CS}$ = CL = V_{DD}		—	0.05	1.0	µA	V_{DD}
Dynamic current dissipation	I_{DD} (1)	During display V_5 = –5.0 V	f_{CL} = 2 kHz	—	2.0	5.0	µA	V_{DD} See note 12, 13 & 14.
			R_f = 1 MΩ	—	9.5	15.0		
			f_{CL} = 18 kHz	—	5.0	10.0		
		During display V_5 = –5 V V_{SS} = –3 V	f_{CL} = 2 kHz		1.5	4.5	µA	V_{DD} See note 12 & 13.
			Rf = 1 MΩ		6.0	12.0		
	I_{DD} (2)	During access t_{cyc} = 200 kHz		—	300	500	µA	See note 8.
		V_{SS} = –3V, During access t_{cyc} = 200 kHz			150	300		
Input pin capacitance	C_{IN}	Ta = 25 °C, f = 1 MHz		—	5.0	8.0	pF	All input pins
Oscillation frequency	f_{OSC}	R_f = 1.0 MΩ ±2%, V_{SS} = –5.0 V		15	18	21	kHz	See note 9.
		R_f = 1.0 MΩ ±2%, V_{SS} = –3.0 V		11	16	21		
Reset time	t_R			1.0	—		µS	$\overline{RES}$ See note 15.

Notes:
1. Operation over the specified voltage range is guaranteed, except where the supply voltage changes suddenly during CPU access.
2. A0, D0 to D7, E (or $\overline{RD}$), R/$\overline{W}$ (or $\overline{WR}$) and $\overline{CS}$
3. CL, FR, M/$\overline{S}$ and $\overline{RES}$
4. D0 to D7
5. FR
6. A0, E (or $\overline{RD}$), R/$\overline{W}$ (or $\overline{WR}$), $\overline{CS}$, CL, M/$\overline{S}$ and $\overline{RES}$
7. When D0 to D7 and FR are high impedance.
8. During continual write acess at a frequency of t_{cyc}. Current consumption during access is effectively proportional to the access frequency.
9. See figure below for details
10. See figure below for details
11. For a voltage differential of 0.1 V between input (V_1, …, V_4) and output (COM, SEG) pins. All voltages within specified operating voltage range.
12. S1D15200∗10∗∗ and S1D15201∗10∗∗ and S1D15202∗10∗∗ only. Does not include transient currents due to stray and panel capacitances.
13. S1D15200∗00∗∗ and S1D15202∗00∗∗ only. Does not include transient currents due to stray and panel capacitances.
14. S1D15201∗00∗∗ only. Does not include transient currents due to stray and panel capacitances.
15. tR (Reset time) represents the time from the RES signal edge to the completion of reset of the internal circuit. Therefore, the S1D15200 series enters the normal operation status after this t_R.

Relationship between fOSC, fFR and Rf, and operating bounds on VSS and V5

*9 • Relationship between oscillation frequency, frames and Rf
(S1D15200F00A∗), (S1D15202F00A∗)

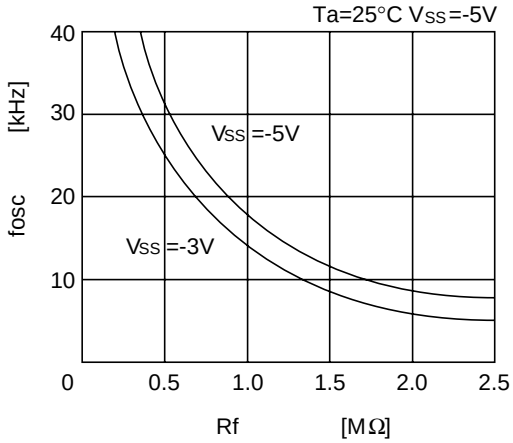


Figure 5 (a)

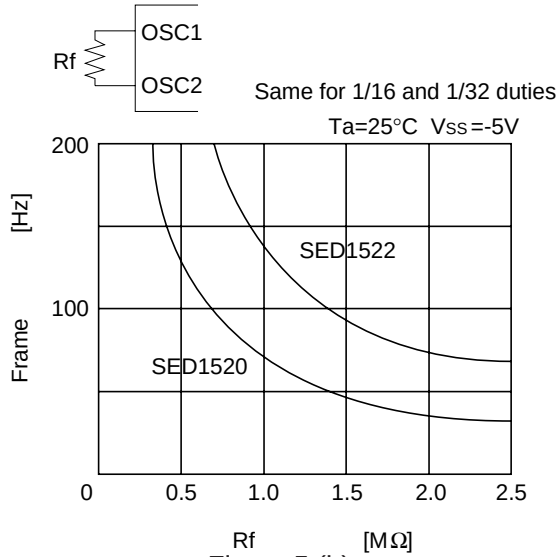


Figure 5 (b)

• Relationship between external clocks (fCL) and frames
(S1D15200F10A∗) , (S1D15202F10A∗)

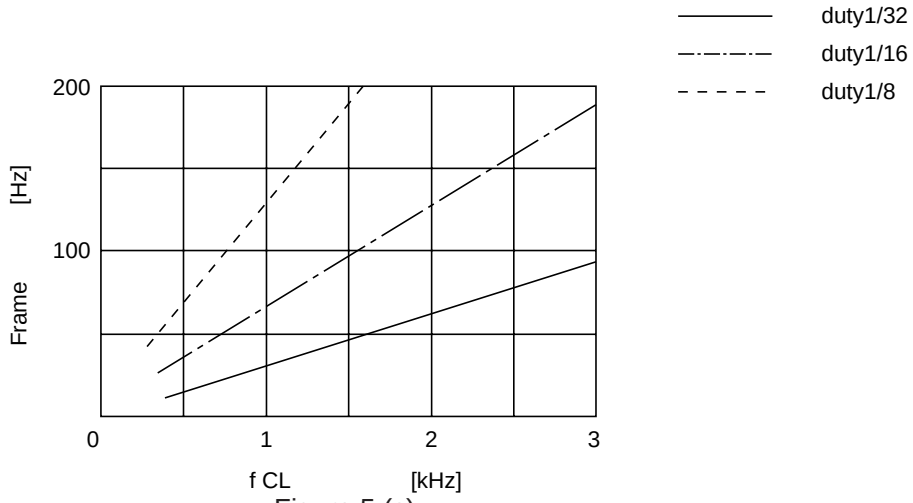


Figure 5 (c)

*10 • Operating voltage range of VSS and V5 systems

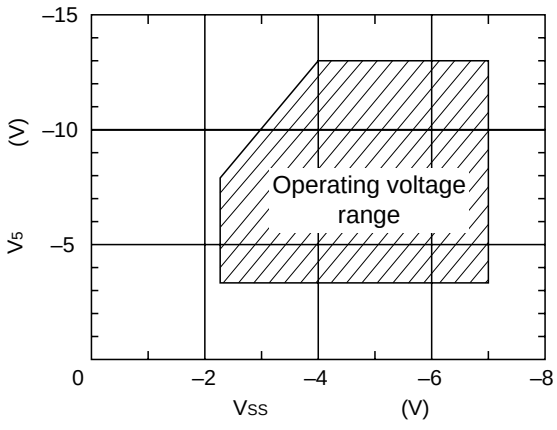
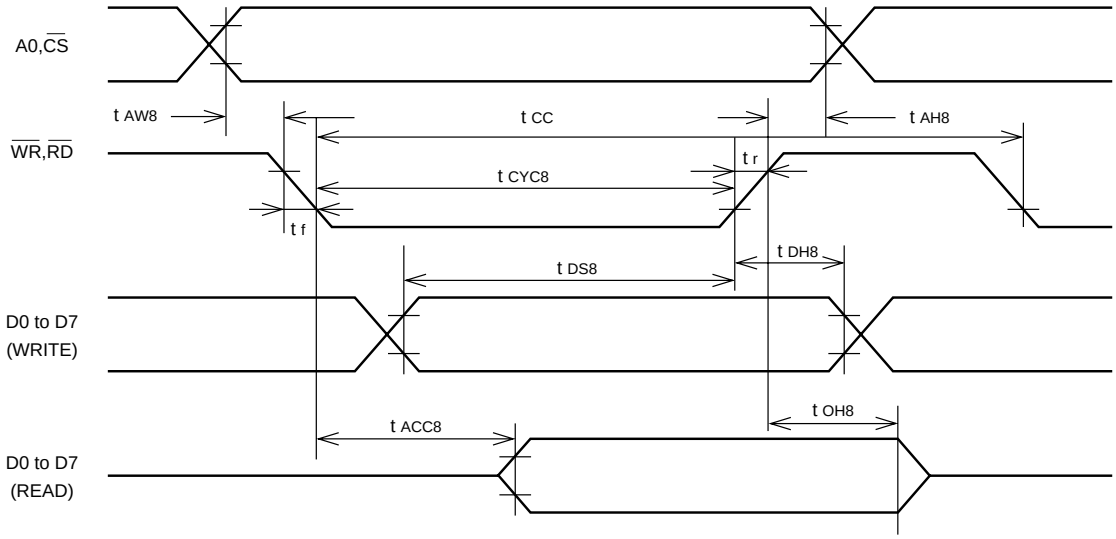


Figure 6

AC Characteristics

- MPU Bus Read/Write I (80-family MPU)



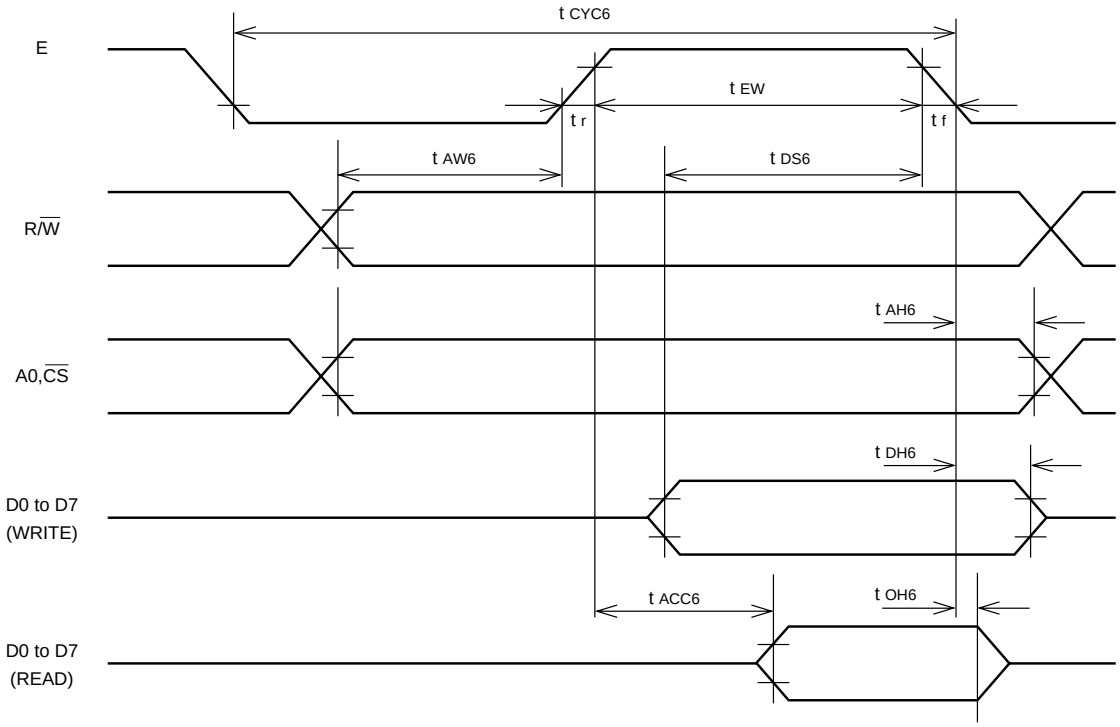
Ta = –20 to 75 ˚C, Vss = –5.0 V ±10% unless stated otherwise

Parameter	Symbol	Condition	Rating		Unit	Signal
			Min.	Max.		
Address hold time	t_{AH8}		10	—	ns	A0, $\overline{CS}$
Address setup time	t_{AW8}		20	—	ns	
System cycle time	t_{CYC8}		1000	—	ns	$\overline{WR}$, $\overline{RD}$
Control pulsewidth	t_{CC}		200	—	ns	
Data setup time	t_{DS8}		80	—	ns	D0 to D7
Data hold time	t_{DH8}		10	—	ns	
$\overline{RD}$ access time	t_{ACC8}	CL = 100 pF	—	90	ns	
Output disable time	t_{CH8}		10	60	ns	
Rise and fall time	t_r, t_f	—	—	15	ns	—

(Vss = –2.7 to –4.5 V, Ta = –20 to +75°C)

Parameter	Symbol	Condition	Rating		Unit	Signal
			Min.	Max.		
Address hold time	t_{AH8}	—	20	—	ns	A0, $\overline{CS}$
Address setup time	t_{AW8}		40	—	ns	
System cycle time	t_{CYC8}	—	2000	—	ns	$\overline{WR}$, $\overline{RD}$
Control pulse width	t_{CC}		400	—	ns	
Data setup time	t_{DS8}	—	160	—	ns	D0 to D7
Data hold time	t_{DH8}		20	—	ns	
$\overline{RD}$ access time	t_{ACC8}	CL = 100 pF	—	180	ns	
Output disable time	t_{CH8}		20	120	ns	
Rise and fall time	t_r, t_f	—	—	15	ns	—

• MPU Bus Read/Write II (68-family MPU)



Ta = –20 to 75 ˚C, VSS = –5 V ±10 unless stated otherwise

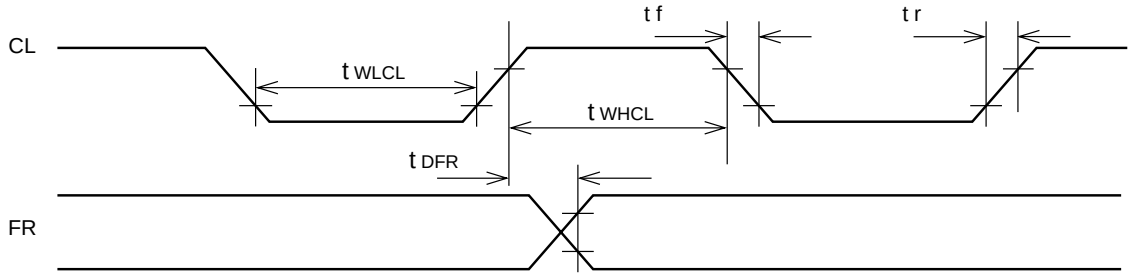
Parameter		Symbol	Condition	Rating		Unit	Signal
				Min.	Max.		
System cycle time		t_{CYC6}		1000	—	ns	A0, CS, R/W
Address setup time		t_{AW6}		20	—	ns	
Address hold time		t_{AH6}		10	—	ns	
Data setup time		t_{DS6}		80	—	ns	D0 to D7
Data hold time		t_{DH6}		10	—	ns	
Output disable time		t_{OH6}	CL = 100 pF	10	60	ns	
Access time		t_{ACC6}		—	90	ns	
Enable pulsewidth	Read	t_{EW}		100	—	ns	E
	Write			80	—	ns	
Rise and fall time		tr, tf	—	—	15	ns	—

(VSS = –2.7 to – 4.5 V, Ta = –20 to +75°C)

Parameter		Symbol	Condition	Rating		Unit	Signal
				Min.	Max.		
System cycle time*1		t_{CYC6}	—	2000	—	ns	A0, CS, R/W
Address setup time		t_{AW6}	—	40	—	ns	
Address hold time		t_{AH6}		20	—	ns	
Data setup time		t_{DS6}	—	160	—	ns	D0 to D7
Data hold time		t_{DH6}		20	—	ns	
Output disable time		t_{OH6}	CL = 100 pF	20	120	ns	
Access time		t_{ACC6}		—	180	ns	
Enable pulse width	Read	t_{EW}	—	200	—	ns	E
	Write			160	—	ns	
Rise and fall time		t_r, t_f	—	—	15	ns	—

Notes: 1. t_{CYC6} is the cycle time of CS. E = H, not the cycle time of E.

• Display Control Signal Timing



Input

Ta = –20 to 75 °C, VSS = –5.0 V ±10% unless stated otherwise

Parameter	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
Low-level pulsewidth	t_{WLCL}		35	—	—	µs	CL
High-level pulsewidth	t_{WHCL}		35	—	—	µs	
Rise time	t_r		—	30	150	ns	
Fall time	t_f		—	30	150	ns	
FR delay time	t_{DFR}		–2.0	0.2	2.0	µs	FR

VSS = –2.7 to –4.5 V, Ta = –20 to +75°C

Parameter	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
Low-level pulse width	t_{WLCL}	—	70	—	—	µs	CL
High-level pulse width	t_{WHCL}	—	70	—	—	µs	
Rise time	t_r	—	—	60	300	ns	
Fall time	t_f	—	—	60	300	ns	
FR delay time	t_{DFR}	—	–4.0	0.4	4.0	µs	FR

Note: The listed input t_{DFR} applies to the S1D15200 and S1D15201 and S1D15202 in slave mode.

Output

Ta = –20 to 75 °C, VSS = –5.0 V ±10% unless stated otherwise

Parameter	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
FR delay time	t_{DFR}	CL = 100 pF	—	0.2	0.4	µs	FR

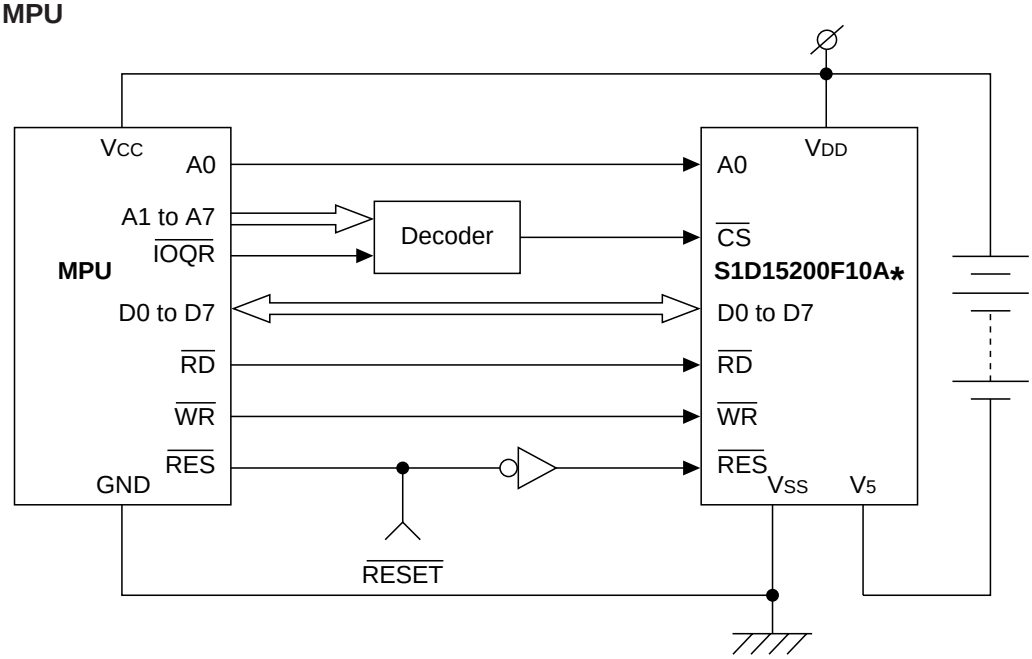
VSS = –2.7 to –4.5 V, Ta = –20 to +75°C

Parameter	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
FR delay time	t_{DFR}	CL = 100 pF	—	0.4	0.8	µs	FR

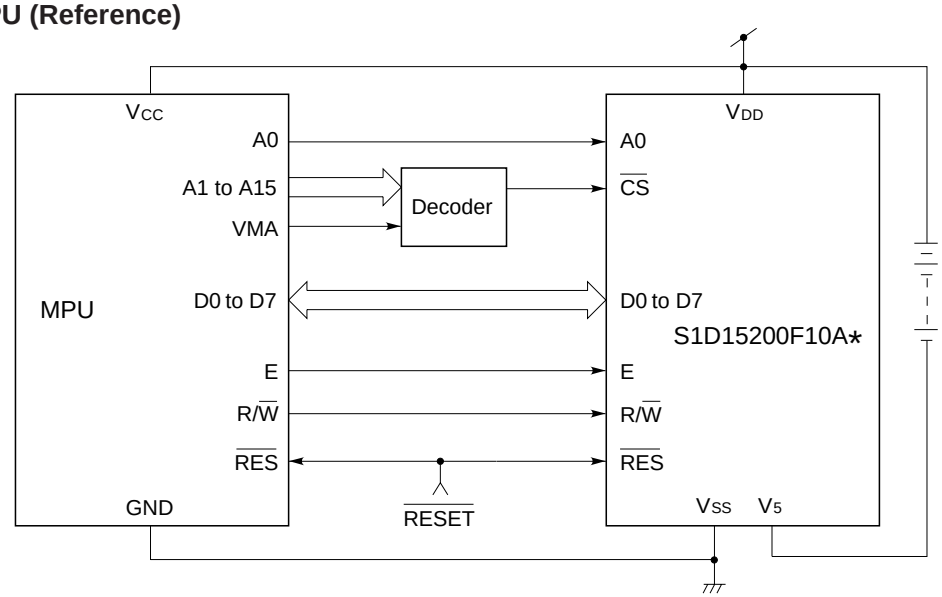
Notes: 1. The listed output t_{DFR} applies to the S1D15200 and S1D15202 in master mode.

11. MPU INTERFACE CONFIGURATION

80 Family MPU

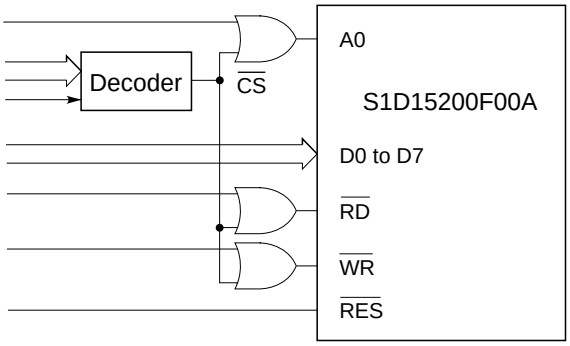


68 Family MPU (Reference)



* Refer to the figure above as to S1D15201.

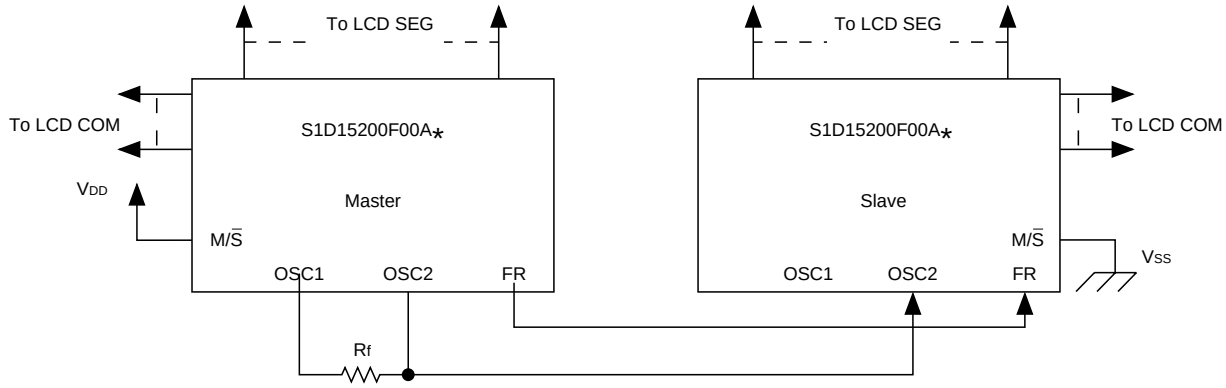
* S1D15200∗00∗∗(internal osillating) does not have $\overline{CS}$ terminal. Input OR output with $\overline{CS}$ signal to AD. $\overline{RD}$(E) $\overline{WR}$(R/$\overline{W}$)terminals as the figure belew.



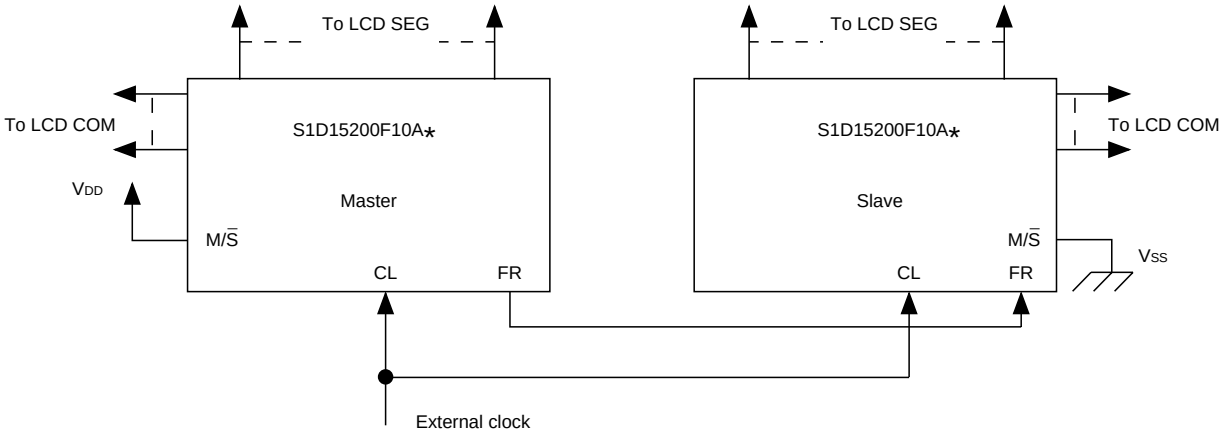
When in use of 80 Family MPU

12. LCD DRIVE INTERGFACE CONFIGURATION

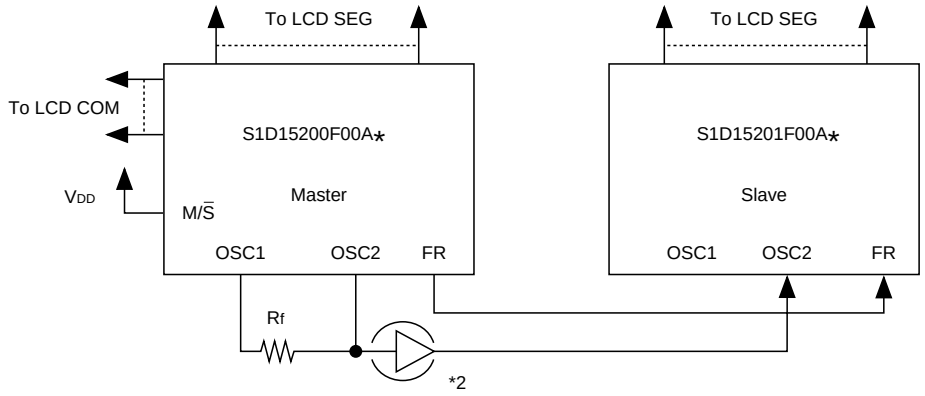
S1D15200F00A∗–S1D15200F00A∗
S1D15202F00A∗–S1D15202F00A∗



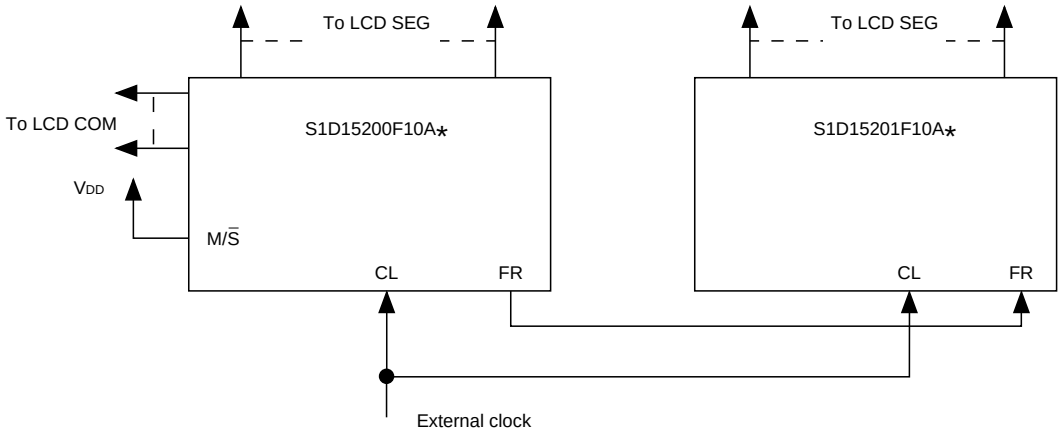
S1D15200F10A∗–S1D15200F10A∗
S1D15202F10A∗–S1D15202F10A∗



S1D15200F00A∗
)–S1D15201F00A∗ (See note 1)
S1D15202F00A∗



S1D15200F10A*–S1D15201F10A*

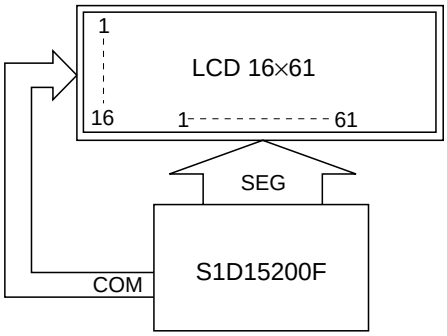


Notes: 1. The duty cycle of the slave must be the same as that for the master.
2. If a system has two or more slave drivers a CMOS buffer will be required.

13. LCD PANEL WIRING EXAMPLE
(THE FULL-DOT LCD PANEL DISPLAYS A CHARACTER IN 6×8 DOTS.)

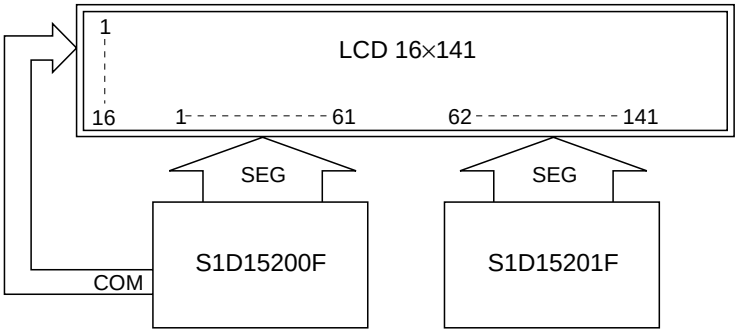
1/16 duty:

- 10 characters × 2 lines



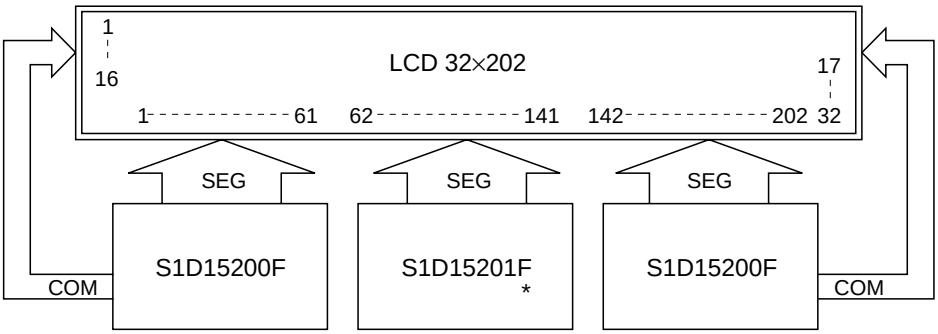
1/16 duty:

- 23 characters × 2 lines



1/32 duty:

- 33 characters × 4 lines



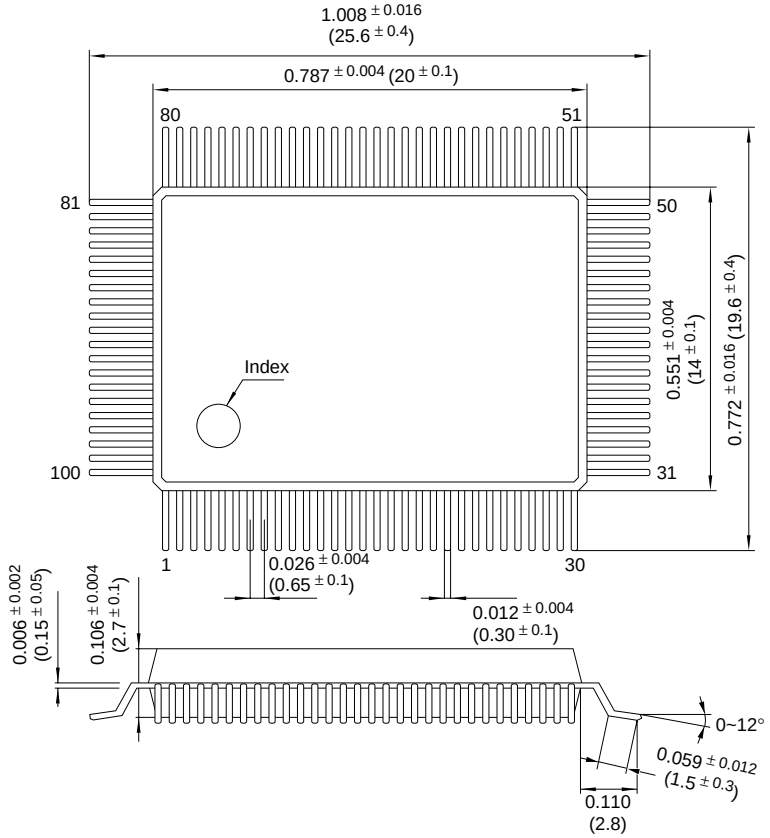
* The S1D15201F can be omitted (the 32×122-dot display mode is selected).

Note: A combination of 10B∗ or 10A∗ type chip (that uses internal clocks) and 00B∗ or 00A∗ type chip (that uses external clocks) is NOT allowed.

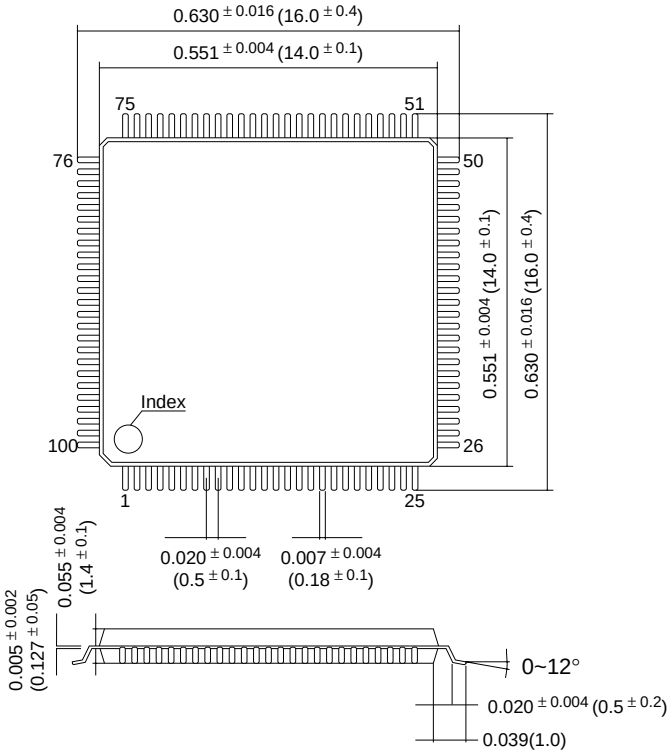
Package Dimensions

• Plastic QFP5–100 pin

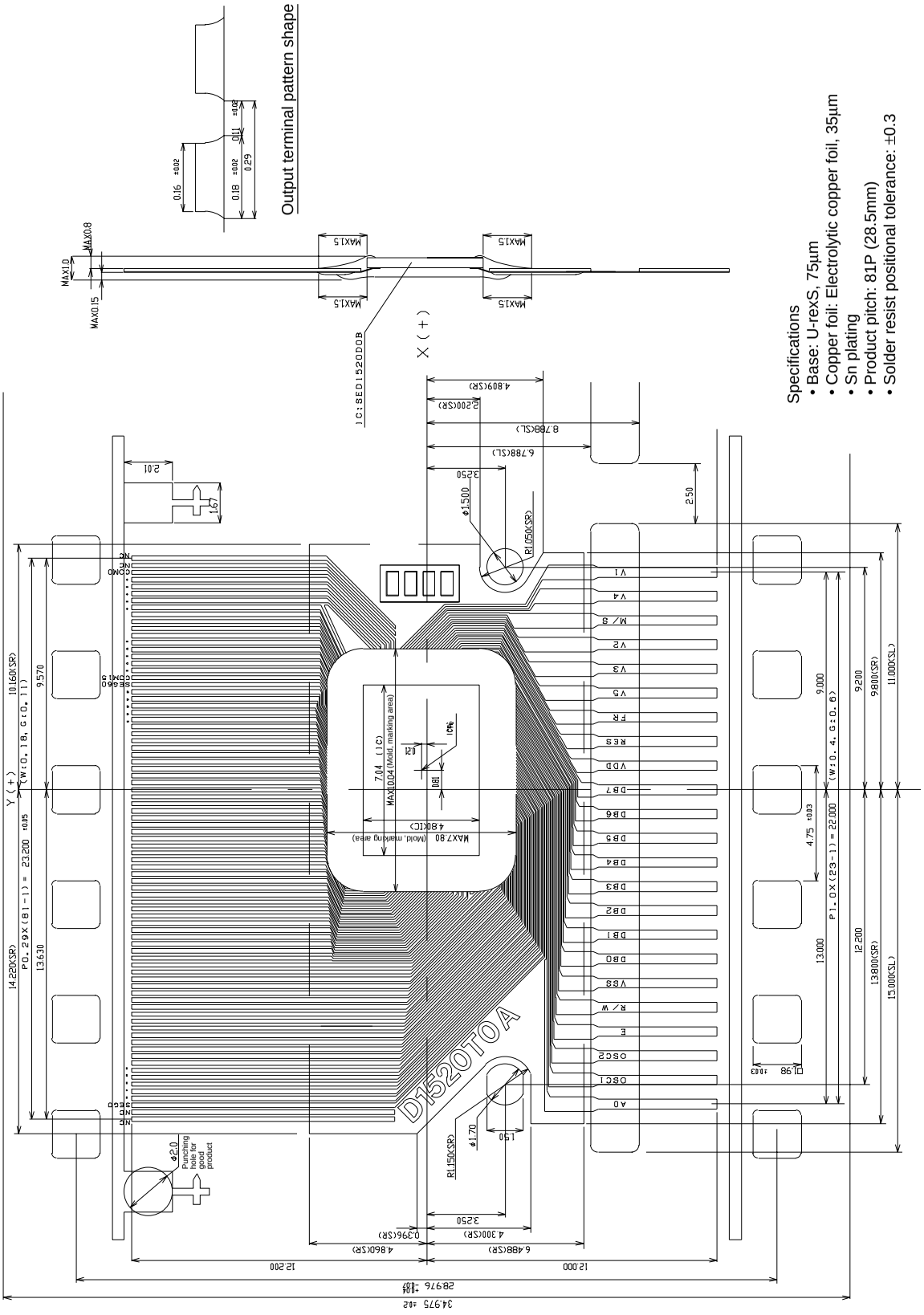
Dimensions: inches (mm)



• Plastic QFP15–100 pin



TCP Dimensions



3. S1D15210 Series

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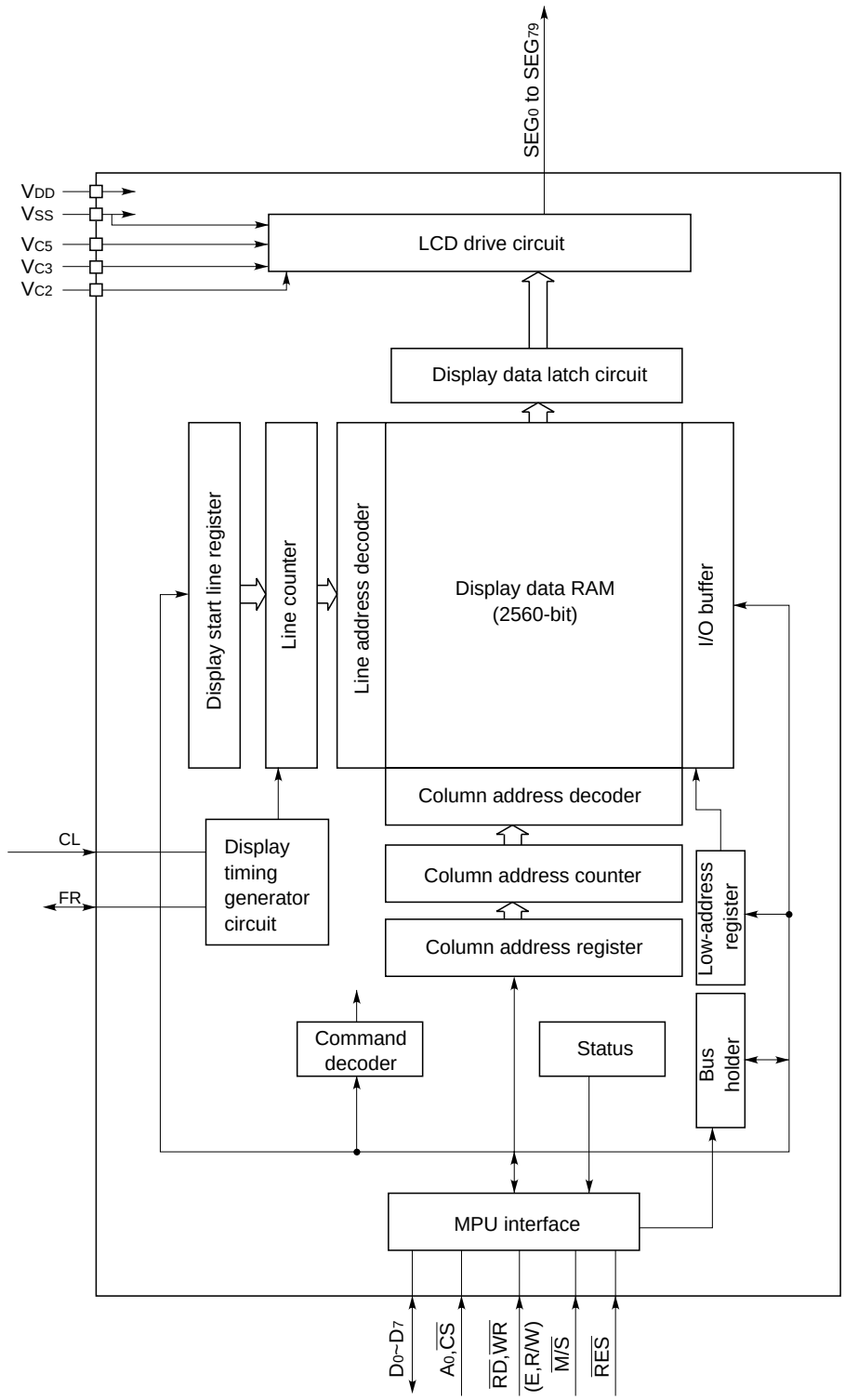
1. DESCRIPTION

The S1D15210 Series of dot matrix LCD drivers are designed for the display of characters and graphics. The drivers generate LCD drive signals derived from bit mapped data stored in an internal RAM.
The S1D15210 Series drivers incorporate innovative circuit design strategies to achieve very low power dissipation at a wide range of operating voltages.

2. FEATURES

- Fast 8-bit MPU interface compatible with 80- and 68-family microcomputers
- 32 × 80 bit RAM
- Many command set
- Total 80 (segment + common) drive sets
- Low power — 30 μW at 2 kHz external clock
- Wide range of supply voltages
  $V_{DD} - V_{SS}$: 2.4V to 6.0 V
  $V_{C5} - V_{SS}$: 3.5V to 6.0 V
- Low-power CMOS
- Al-pad chip:S1D15210D**A*
- Au-bump chip:S1D15210D**B*

3. BLOCK DIAGRAM



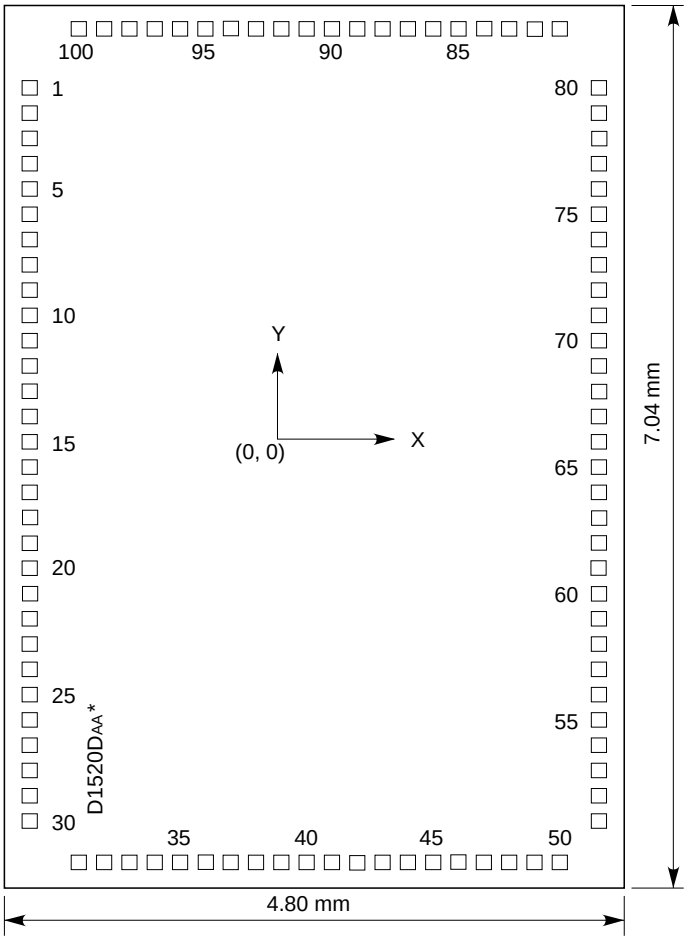
4. PAD LAYOUT

(1) Al-pad chip

Chip size : 4.80×7.04×0.400 mm
Pad pitch (Typ.) : 100×100 µm

(2)Au-bump chip

Bump size : 92×92 µm
Bump height : 22.5 µm



5. PAD CENTER COORDINATES

Pad No.	Pin Name	X	Y
1	SEG71	159	6507
2	SEG70	159	6308
3	SEG69	159	6108
4	SEG68	159	5909
5	SEG67	159	5709
6	SEG66	159	5510
7	SEG65	159	5310
8	SEG64	159	5111
9	SEG63	159	4911
10	SEG62	159	4712
11	SEG61	159	4512
12	SEG60	159	4169
13	SEG59	159	3969
14	SEG58	159	3770
15	SEG57	159	3570
16	SEG56	159	3371
17	SEG55	159	3075
18	SEG54	159	2876
19	SEG53	159	2676
20	SEG52	159	2477
21	SEG51	159	2277
22	SEG50	159	2078
23	SEG49	159	1878
24	SEG48	159	1679
25	SEG47	159	1479
26	SEG46	159	1280
27	SEG45	159	1080
28	SEG44	159	881
29	SEG43	159	681
30	SEG42	159	482
31	SEG41	504	159
32	SEG40	704	159
33	SEG39	903	159
34	SEG38	1103	159
35	SEG37	1302	159
36	SEG36	1502	159
37	SEG35	1701	159
38	SEG34	1901	159
39	SEG33	2100	159
40	SEG32	2300	159
41	SEG31	2499	159
42	SEG30	2699	159
43	SEG29	2898	159
44	SEG28	3098	159
45	SEG27	3297	159
46	SEG26	3497	159
47	SEG25	3696	159
48	SEG24	3896	159
49	SEG23	4095	159
50	SEG22	4295	159
51	SEG21	4641	482
52	SEG20	4641	681
53	SEG19	4641	881
54	SEG18	4641	1080
55	SEG17	4641	1280
56	SEG16	4641	1479
57	SEG15	4641	1679
58	SEG14	4641	1878
59	SEG13	4641	2078
60	SEG12	4641	2277
61	SEG11	4641	2477
62	SEG10	4641	2676
63	SEG9	4641	2876
64	SEG8	4641	3075
65	SEG7	4641	3275
66	SEG6	4641	3474
67	SEG5	4641	3674
68	SEG4	4641	3948
69	SEG3	4641	4148
70	SEG2	4641	4347
71	SEG1	4641	4547
72	SEG0	4641	4789
73	A0	4641	5048
74	$\overline{CS}$	4641	5247
75	CL	4641	5447
76	E ($\overline{RD}$)	4641	5646
77	R/W ($\overline{WR}$)	4641	5846
78	V_{DD}	4641	6107
79	DB0	4641	6307
80	DB1	4641	6506
81	DB2	4295	6884
82	DB3	4095	6884
83	DB4	3896	6884
84	DB5	3696	6884
85	DB6	3497	6884
86	DB7	3297	6884
87	V_{SS}	3098	6884
88	$\overline{RES}$	2898	6884
89	FR	2699	6884
90	VC2	2499	6884
91	VC3	2300	6884
92	VC5	2100	6884
93	SEG79	1901	6884
94	SEG78	1701	6884
95	SEG77	1502	6884
96	SEG76	1302	6884
97	SEG75	1103	6884
98	SEG74	903	6884
99	SEG73	704	6884
100	SEG72	504	6884

6. PIN DESCRIPTION

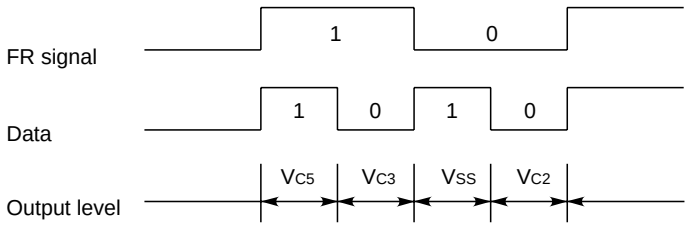
(1) Power Supply Pins

Name	Description
V_{DD}	Connected to the +5Vdc power. Common to the V_{CC} MPU power pin.
V_{SS}	0 Vdc pin connected to the system ground.
V_{C5}, V_{C3}, V_{C2}	Multi-level power supplies for LCD driving. The voltage determined for each liquid crystal cell is divided by resistance or it is converted in impedance by the op amp, and supplied. These voltages must satisfy the following: $V_{C5} \geq V_{C3} \geq V_{C2} \geq V_{SS}$

(2) System Bus Connection Pins

D7 to D0 *1	Three-state I/O. The 8-bit bidirectional data buses to be connected to the 8- or 16-bit standard MPU data buses.
A0	Input. Usually connected to the low-order bit of the MPU address bus and used to identify the data or a command. Low level (0): D0 to D7 are display control data. High level (1): D0 to D7 are display data.
$\overline{RES}$	Input. When the $\overline{RES}$ signal goes ⊓⌴⊓ the 68-series MPU is initialized, and when it goes ⌴⊓⌴ , the 80-series MPU is initialized. The system is reset during edge sense of the RES signal. The interface type to the 68-series or 80-series MPU is selected by the level input as follows: High level: 68-series MPU interface Low level: 80-series MPU interface
$\overline{CS}$	Input. Active low. An address bus signal is usually decoded by use of chip select signal.
E ($\overline{RD}$)	• If the 68-series MPU is connected: Input. Active high. Used as an enable clock input of the 68-series MPU. • If the 80-series MPU is connected: Input. Active low. The RD signal of the 80-series MPU is entered in this pin. When this signal is kept low, the S1D15210 data bus is in the output status.
R/W ($\overline{WR}$) WR (R/W)	• If the 68-series MPU is connected: Input. Used as an input pin of read control signals (if R/W is high) or write control signals (if low). • If the 80-series MPU is connected: Input. Active low. The WR signal of the 80-series MPU is entered in this pin. A signal on the data bus is fetched at the rising edge of WR signal.

(3) LCD Drive Circuit Signals

Name	Description
CL	Input. Effective for an external clock operation model only. This is a display data latch signal to count up the line counter and common counter at each signal falling and rising edges.
FR	Input. This is an input pin of LCD AC signals, and connected to the FR pin of common driver.
SEGn	Output. The output pin for LCD column (segment) driving. A single level of V_{C5}, V_{C3}, V_{C2}, V_{SS} is selected by the combination of display RAM contents and FR signal. 

7. FUNCTION DESCRIPTION

System Bus

(1) MPU interface

Selecting an interface type

The S1D15210 series transfers data via 8-bit bidirectional data buses (D0 to D7). As its Reset pin has the MPU interface select function, the 80-series MPU or the 68-series MPU can directly be connected to the MPU bus by the selection of high or low RES signal level after reset (see Table 1).

When the $\overline{CS}$ signal is high, the S1D15210 series is disconnected from the MPU bus and set to stand by. (However, the reset signal is entered regardless of the internal setup status.)

Table 1

$\overline{RES}$ signal input level	MPU type	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	D0 to D7
Active ⎍⎍⎍	80-series	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	D0 to D7
Active ⎍⎍⎍	68-series	A0	E	R/$\overline{W}$	$\overline{CS}$	D0 to D7

Data transfer

The S1D15210 drivers use the A0, E (or $\overline{RD}$) and R/$\overline{W}$ (or $\overline{WR}$) signals to transfer data between the system MPU and internal registers. The combinations used are given in the table blow.

Table 2

Common	80 MPU		68 MPU	Function
A0	$\overline{RD}$	$\overline{WR}$	R/$\overline{W}$	
1	0	1	1	Read display data
1	1	0	0	Write display data
0	0	1	1	Read status
0	1	0	0	Write to internal register (command)

Access to Display Date Ram and Internal Registers

In order to match the timing requirements of the MPU with those of the display data RAM and control registers all data is latched into and out of the driver.

This introduces a one cycle delay between a read request for data and the data arriving. For example when the MPU executes a read cycle to access display RAM the current contents of the latch are placed on the system data bus while the desired contents of the display RAM are moved into the latch.

This means that a dummy read cycle has to be executed at the start of every series of reads. See Figure 1.

No dummy cycle is required at the start of a series of writes as data is transferred automatically from the input latch to its destination.

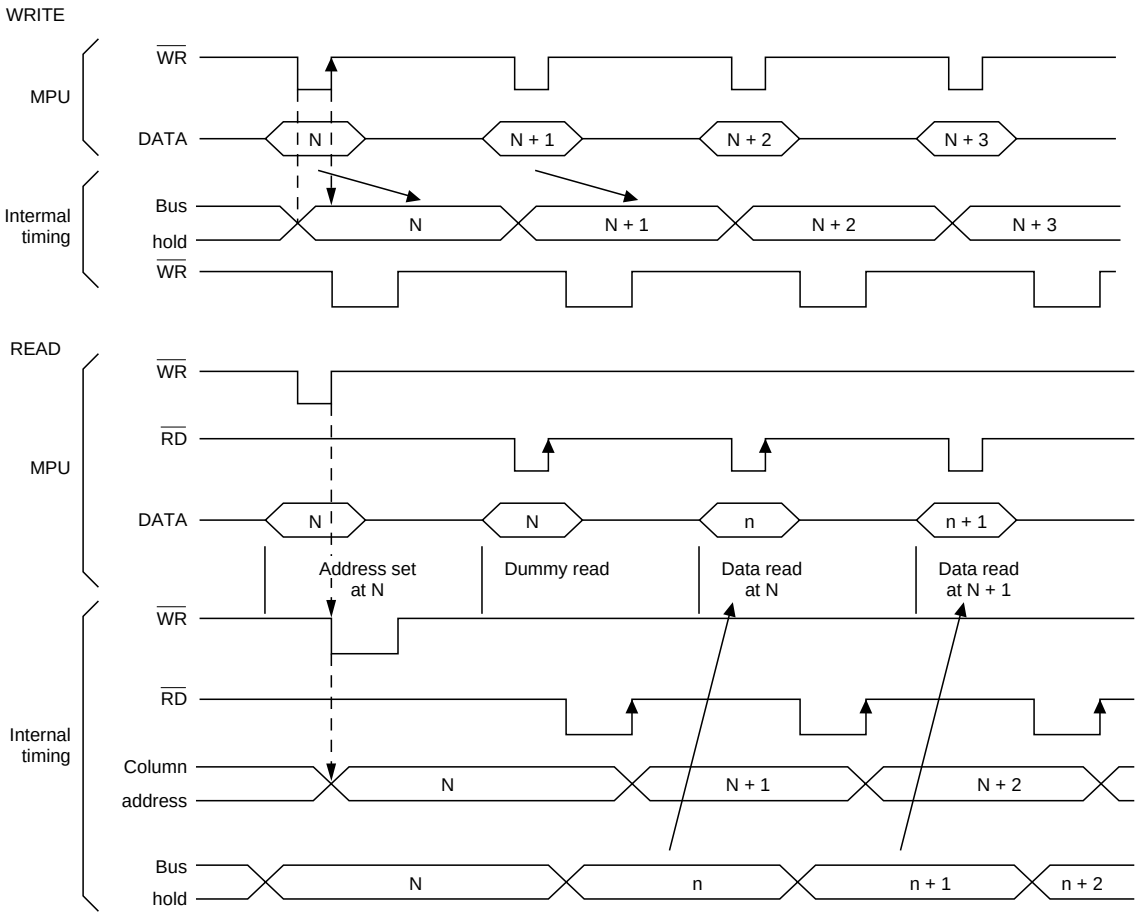


Figure 1 Bus Buffer Delay

(2) Busy flag

When the Busy flag is logical 1, the S1D15200 series is executing its internal operations. Any command other than Status Read is rejected during this time. The Busy flag is output at pin D7 by the Status Read command. If an appropriate cycle time (tcyc) is given, this flag needs not be checked at the beginning of each command and, therefore, the MPU processing capacity can greatly be enhanced.

(3) Display Start Line and Line Count Registers

The contents of this register form a pointer to a line of data in display data RAM corresponding to the first line of the display (COM0), and are set by the Display Start Line command. See section 3.

The contents of the display start line register are copied into the line count register at the start of every frame, that is on each edge of FR. The line count register is incremented by the CL clock once for every display line, thus generating a pointer to the current line of data, in display data RAM, being transferred to the segment driver circuits.

(4) Column Address Counter

The column address counter is a 7-bit presettable counter that supplies the column address for MPU access to the display data RAM. See Figure 2. The counter is incremented by one every time the driver receives a Read or Write Display Data command. Addresses above 50H are invalid, and the counter will not increment past this value. The contents of the column address counter are set with the Set Column Address command.

(5) Page Register

The page resiter is a 2-bit register that supplies the page address for MPU access to the display data RAM. See Figure 3. The contents of the page register are set by the Set Page Register command.

(6) Display Data RAM

The display data RAM stores the LCD display data, on a 1-bit per pixel basis. The relation-ship between display data, display address and the display is shown in Figure 3.

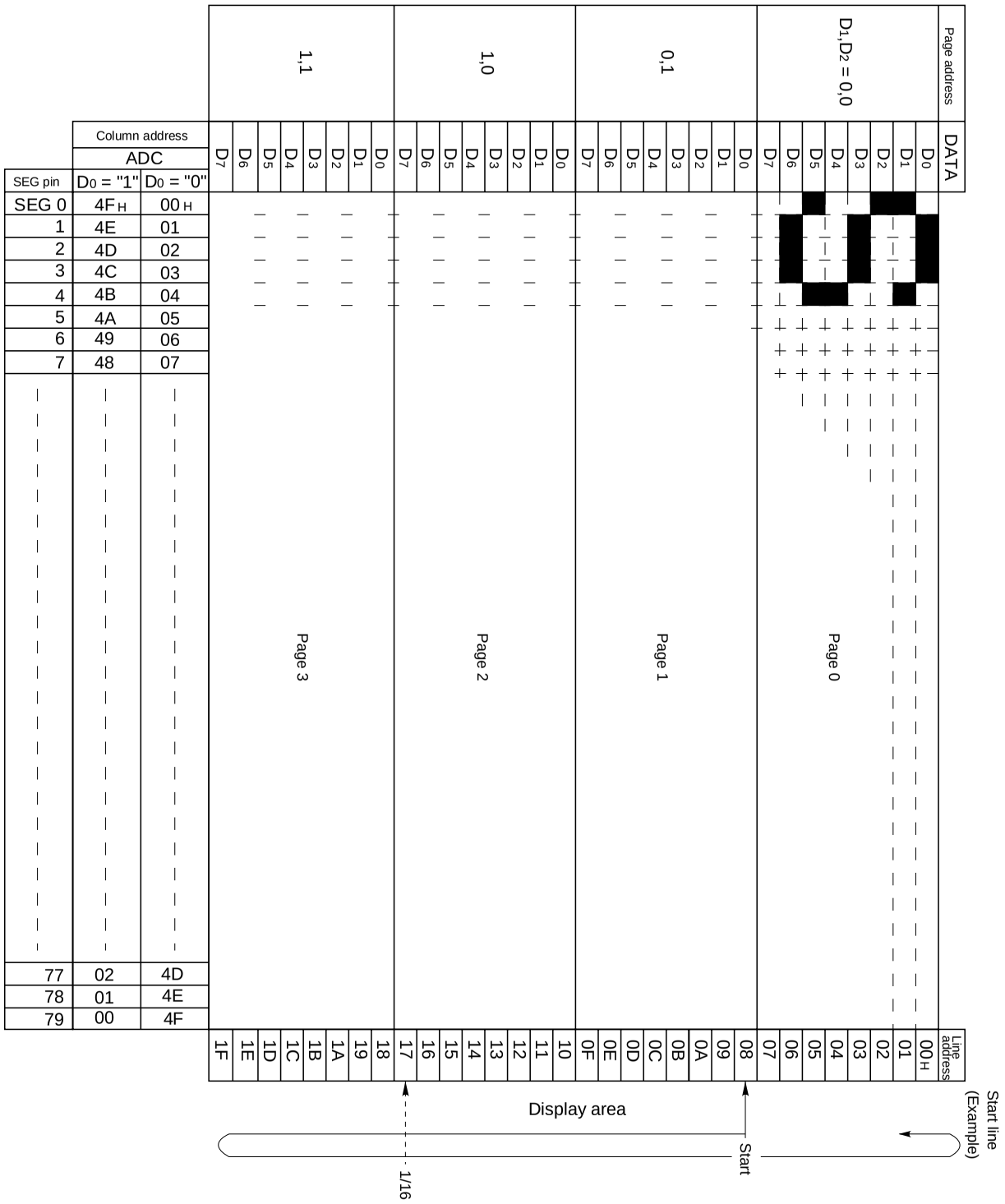
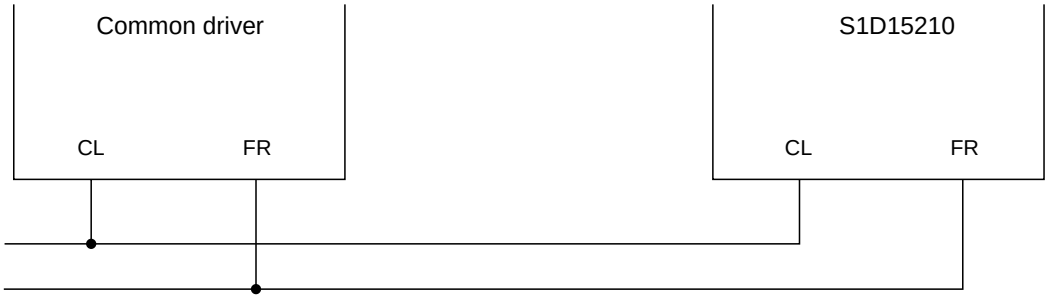


Figure 2 Display Data RAM Addressing

(7) Display Timing Generation Circuit

The master clock CL and the frame signal FR generate internal timing. The master clock CL causes the line counter to operate, which synchronizes with the line counter. Therefore, the master clock CL and the frame signal FR input signals of the same phases as those of the CR and FR signals of the common driver, respectively.



(8) Display Data Latch Circuit

The display data latch circuit is a latch that temporarily memorizes the display data to be output to the liquid crystal drive circuit from the display data RAM for each common period. Display ON/OFF and Display All Lamps ON/OFF commands control the data in this latch. Therefore, data in the display data RAM are never to be modified.

(9) Liquid Crystal Drive Circuit

This circuit comprises 80 sets of multiplexers to generate four-value level for the liquid crystal drive. Various combinations of display data in the display data latch and the FR signals output the liquid crystal waveforms as shown in Fig. 3.

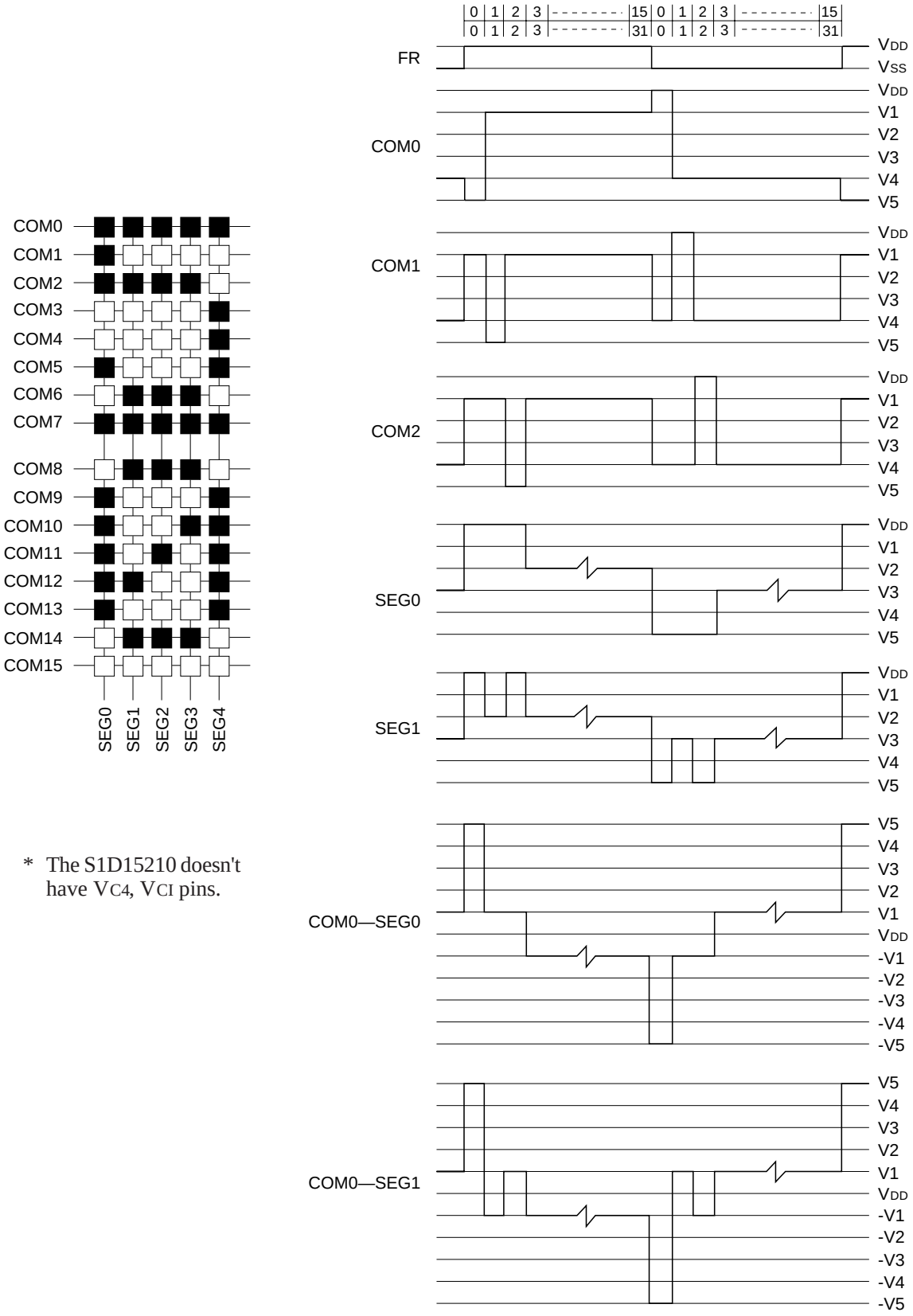
(10) Reset Circuit

This circuit detects the $\overline{RES}$ input rise or fall edge and performs initialization.
~~RES~~ input is level-sensed, then, as shown in Table 1, the MPU interface mode is selected.

When connecting to MPU, the output port of MPU is used and the reset signal is input through software. Otherwise, the circuit is connected to the reset terminal of MPU and the ⎍ reset signal via the inverter is input for 80-system MPU, and the ⎴ reset signal for the 68-system MPU.
$\overline{RES}$ input causes initialization of S1D15210, and initialization of the MPU is performed at the same time. Failure of initialization by the $\overline{RES}$ terminal upon applying power may lead to a status that cannot be released.
If the reset command is used, items 2 and 5 of the following initial settings are to be executed:

(11) Status in Initial Setting

1. Display OFF
2. To set the display start line register on the first line.
3. Display All Lamps OFF
4. To set the column address counter to address 0.
5. To set the page address counter to the third page.
6. ADC select: normal rotation (ADC command = "0", ADC status flag "1")
7. Read/Modify/Write OFF



* The S1D15210 doesn't have V_{C4}, V_{CI} pins.

Figure 4 LCD drive waveforms example

8. COMMANDS

Table 3

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
(1)Display On/OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns display on or off. 1: ON, 0: OFF
(2)Display start line	0	1	0	1	1	0	Display start address (0 to 31)					Specifies RAM line corresponding to top line of display.
(3)Set page address	0	1	0	1	0	1	1	1	0	Page (0 to 3)		Sets display RAM page in page address register.
(4) Set column (segment) address	0	1	0	0	Column address (0 to 79)							Sets display RAM column address in column address register.
(5) Read status	0	0	1	Busy	ADC	ON/OFF	Reset	0	0	0	0	Reads the following status: BUSY 1: Busy 0: Ready ADC 1: CW output 0: CCW output ON/OFF 1: Display off 0: Display on RESET 1: Being reset 0: Normal
(6) Write display data	1	1	0	Write data								Writes data from data bus into display RAM.
(7) Read display data	1	0	1	Read data								Reads data from display RAM onto data bus.
(8) Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	0: CW output, 1: CCW output
(9) All-display ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects static driving operation. 1: Static drive, 0: Normal driving
(10) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-modify-write ON
(11) End	0	1	0	1	1	1	0	1	1	1	0	Read-modify-write OFF
(12) Reset	0	1	0	1	1	1	0	0	0	1	0	Software reset

Table 3 is the command table. The S1D15210 identifies a data bus using a combination of A0 and R/W (RD or WR) signals. As the MPU translates a command in the internal timing only (independent from the external clock), its speed is very high. The busy check is usually not required.

(1) Display ON/OFF

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	1	1	1	D	AEH, AFH

This command turns the display on and off.
- D=1: Display ON
- D=0: Display OFF

(2) Display Start Line

This command specifies the line address shown in Figure 2 and indicates the display line that corresponds to COM0. The display area begins at the specified line address and continues in the line address increment direction. This area having the number of lines of the specified display duty is displayed. If the line address is changed dynamically by this command, the vertical smooth scrolling and paging can be used.

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	0	A_4	A_3	A_2	A_1	A_0	C0H to DFH

This command loads the display start line register.

A_4	A_3	A_2	A_1	A_0	Line Address
0	0	0	0	0	0
0	0	0	0	1	1
		:			:
		:			:
1	1	1	1	1	31

See Figure 2.

(3) Set Page Address

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified. The display status is not changed even when the page address is changed.

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	1	1	0	A_1	A_0	B8H to BBH

This command loads the page address register.

A_1	A_0	Page Address
0	0	0
0	1	1
1	0	2
1	1	3

See Figure 2.

(4) Set Column Address

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by 1 each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 80, and the page address is not changed continuously.

A_0	(E) $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	0	A_6	A_5	A_4	A_3	A_2	A_1	A_0	00H to 4FH

This command loads the column address register.

A_6	A_5	A_4	A_3	A_2	A_1	A_0	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				:
			:				:
1	0	0	1	1	1	1	79

(5) Read Status

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Reading the command I/O register (A0=0) yields system status information.

- The busy bit indicates whether the driver will accept a command or not.
  Busy=1: The driver is currently executing a command or is resetting. No new command will be accepted.
  Busy=0: The driver will accept a new command.
- The ADC bit indicates the way column addresses are assigned to segment drivers.
  ADC=1: Normal. Column address n → segment driver n.
  ADC=0: Inverted. Column address 79-n → segment driver u.
- The ON/OFF bit indicates the current status of the display.
  It is the inverse of the polarity of the display ON/OFF command.
  ON/OFF=1: Display OFF
  ON/OFF=0: Display ON
- The RESET bit indicates whether the driver is executing a hardware or software reset or if it is in normal operating mode.
  RESET=1: Currently executing reset command.
  RESET=0: Normal operation

(6) Write Display Data

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	Write data							

Writes 8-bits of data into the display data RAM, at a location specified by the contents of the column address and page address registers and then increments the column address register by one.

(7) Read Display Data

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	Read data							

Reads 8-bits of data from the data I/O latch, updates the contents of the I/O latch with display data from the display data RAM location specified by the contents of the column address and page address registers and then increments the column address register.
After loading a new address into the column address register one dummy read is required before valid data is obtained.

(8) Select ADC

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	0	0	0	D	A0H, A1H

This command selects the relationship between display data RAM column addresses and segment drivers.
D=1: SEG0 ← column address 4FH, … (inverted)
D=0: SEG0 ← column address 00H, … (normal)
This command is provided to reduce restrictions on the placement of driver ICs and routing of traces during printed circuit board design. See Figure 2 for a table of segments and column addresses for the two values of D.

(9) All Display ON/OFF

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	0	1	0	D	A4H, A5H

Forces display on and all common outputs to be selected.
D=1: All display on
D=0: All display off

(10) Read-Modify-Write

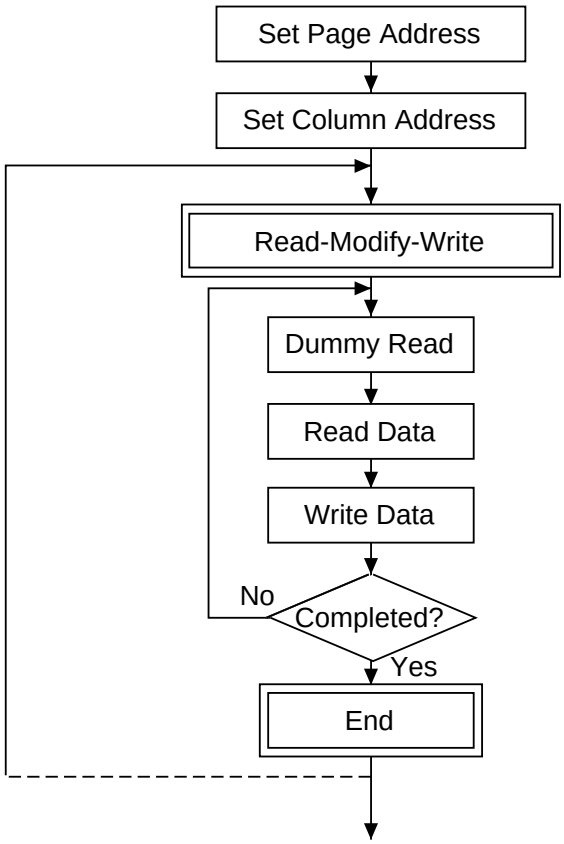
A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	0	0	0	0	E0H

This command defeats column address register auto-increment after data reads. The current conetents of the column address register are saved. This mode remains active until an End command is received.

- Operation sequence during cursor display

When the End command is entered, the column address is returned to the one used during input of Read-Modify-Write command. This function can reduce the load of MPU when data change is repeated at a specific display area (such as cursor blinking).

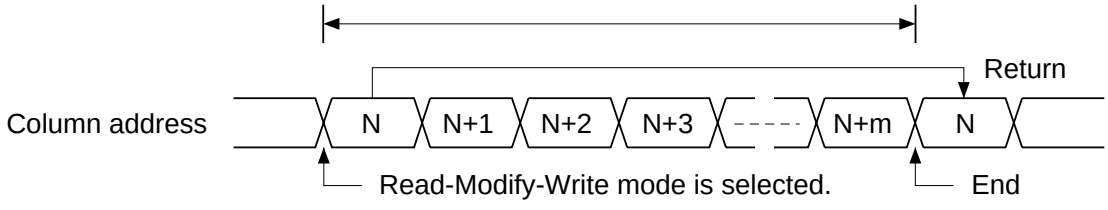
* Any command other than Data Read or Write can be used in the Read-Modify-Write mode. However, the Column Address Set command cannot be used.



(11) End

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	1	1	1	0	EEH

This command cancels read-modify-write mode and restores the contents of the column address register to their value prior to the receipt of the Read-Modify-Write command.



(12) Reset

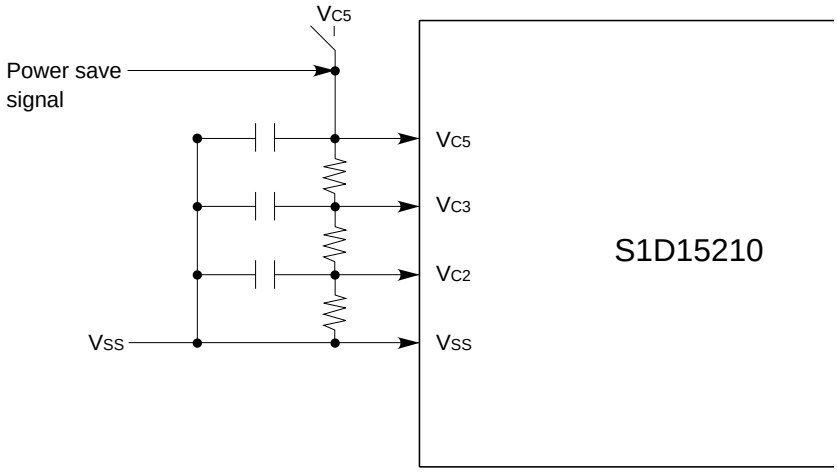
A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	0	0	1	0	E2H

This command clears
- the display start line register.
- and set page address register to 3 page.
  It does not affect the contents of the display data RAM.

When the power supply is turned on, a Reset signal is entered in the $\overline{RES}$ pin. The Reset command cannot be used instead of this Reset signal.

(13) Power Save (Combination command)

The Power Save mode is selected if the static drive is turned ON when the display is OFF. The current consumption can be reduced to almost the static current level. In the Power Save mode:
(a) The LCD drive is stopped, and the segment and common driver outputs are set to the V_{DD} level.
(b) The external oscillation clock input is inhibited, and the OSC2 is set to the floating mode.
(c) The display and operation modes are kept.
The Power Save mode is released when the display is turned ON or when the static drive is turned OFF. If the LCD drive voltage is supplied from an external resistance divider circuit, the current passing through this resistor must be cut by the Power Save signal.



9. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{DD}	–0.3 to +7.0	V
Supply voltage (2)	V_{C5}	–0.3 to +7.0	V
Supply voltage (3)	V_{C3}, V_{C2}	–0.3 to V_{C5}+3	V
Input voltage	V_{IN}	–0.3 to V_{DD} +0.3	V
Output voltage	V_O	–0.3 to V_{DD} +0.3	V
Operating temperature	T_{opr}	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Notes: 1. All voltages are specified relative to V_{SS} = 0 V.
2. The following relation must be always hold
$V_{C5} \geq V_{C3} \geq V_{C2} \geq V_{SS}$
3. Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation under these conditions is not implied.
Moisture resistance of flat packages can be reduced by the soldering process, so care should be taken to avoid thermally stressing the package during board assembly.

10. ELECTRICAL CHARCTERISTICS

DC Characteristics

Ta = –20 to 75 °C, V_{DD} = 0 V unless stated otherwise

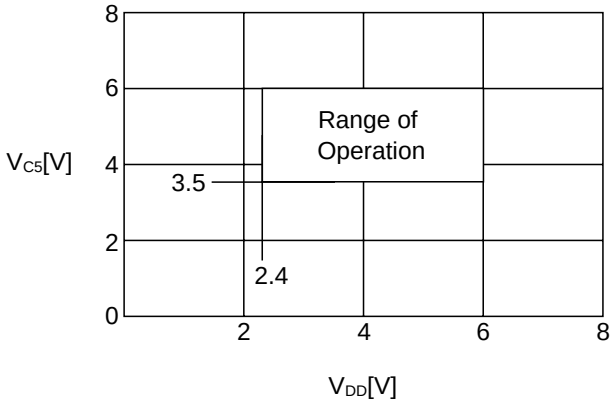
Parameter		Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Applicable Pin
Operating voltage (1) See note 1.	Recommended	V_{DD}			4.5	5.0	5.5	V	V_{DD} *1
	Allowable				2.4	—	6.0		
Operating voltage (2)	Allowable	V_{C5}			3.5	—	6.0	V	V_{C5} *2
	Allowable	V_{C3}			0.5×V_{C5}	—	V_{C5}	V	V_{C3}
	Allowable	V_{C2}			V_{SS}	—	0.5×V_{C5}	V	V_{C2}
High-level input voltage		V_{IH}			0.8×V_{DD}	—	V_{DD}	V	*3
		V_{IL}			V_{SS}	—	0.2×V_{DD}	V	*3
		V_{OH1}	I_{OH} = –1 mA		0.8×V_{DD}	—	V_{DD}	V	*4
		V_{OH2}	V_{DD} = –2.7 V I_{OH} = –0.5mA		0.8×V_{DD}	—	V_{DD}	V	*4
Low-level input voltage		V_{OL1}	I_{OL} = 1 mA		V_{SS}		0.2×V_{DD}	V	*4
		V_{OL2}	V_{DD} = 2.7 V I_{OL} = 0.5 mA		V_{SS}		0.2×V_{DD}	V	*4
Input leakage current		I_{L1}			–1.0	—	1.0	µA	*5
Output leakage current		I_{L2}			–3.0	—	3.0	µA	*6
LCD driver ON resistance		R_{ON}	Ta = 25 °C	V5 = 6.0 V	—	1.3	3.0	kΩ	SEG0 to 79, *7
				V5 = 3.5 V	—	2.5	6.0		

(continued)

Parameter		Symbol	Condition	Rating			Unit	Applicable Pin
				Min.	Typ.	Max.		
Static current dissipation		I_{SSQ}	$\overline{CS}$ = CL = FR = V_{DD}	—	0.01	1.0	µA	V_{SS}
Dynamic current dissipation	During display	I_{SS} (1)	V_{DD} = 5 V V_{C5} = 5 V Ta = 25°C f_{CL} = 2 KHz	—	2.0	5.0	µA	V_{SS} *8
			V_{DD} = 3.0 V V_{C5} = 5 V Ta = 25°C f_{CL} = 2 KHz	—	1.5	4.5	µA	V_{SS} *8
	During access	I_{SS} (2)	V_{DD} = 5 V t_{cyc} = 200 KHz	—	300	500	µA	V_{SS} *9
			V_{DD} = 3.0 V t_{cyc} = 200 KHz	—	150	300		
Input pin capacitance		C_{IN}	Ta = 25 °C, f = 1 MHz	—	5.0	8.0	pF	All input pins

Notes: 1. Although this equipment is capable of withstanding a wide range of operating voltage, it is not designed for withstanding a sudden voltage change while accessing the MPU.

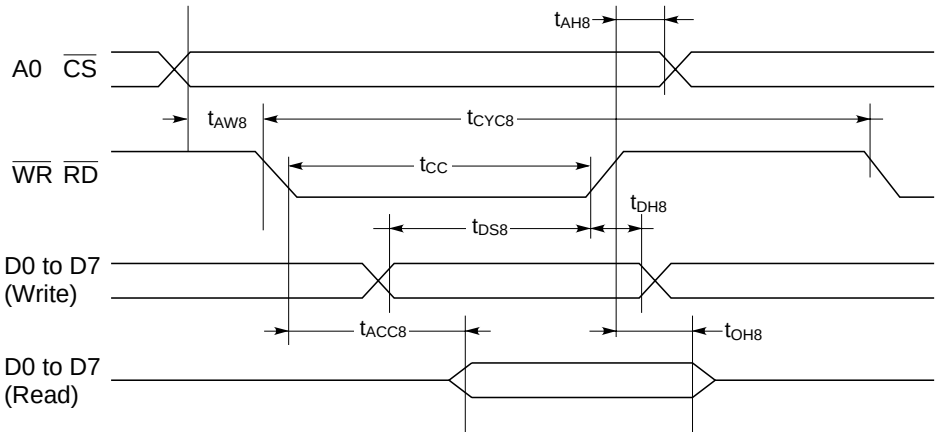
2. Ranges of Operating Voltage for V_{DD} and V_{C5} Systems



3. D0 to D7, A0, $\overline{RES}$, $\overline{CS}$, $\overline{RD}$, (E), $\overline{WR}$, (R/$\overline{W}$), C_L, and FR terminals.
4. D0 to D7 terminals.
5. A0, $\overline{RES}$, $\overline{CS}$, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), and C_L terminals.
6. FR, D0 to D7 (in high impedance status) terminals.
7. These are resistance values obtained when voltage of 0.1 V is applied between the output terminals (SEG) and the respective power terminals (V_{C3}, V_{C2}). These are defined within the range of the operating voltage.
8. This is current consumed by a single IC, not including current required by the LCD panel capacity or by the wiring capacity.
9. This indicates current consumption at the time the pattern of vertical stripes is always wrapped in by the tcyc. Current consumption while accessing roughly proportionate to the tcyc for access. If not accessed, only I_{SS1} is relevant.

Timing Characteristics

- System Bus Read/Write Characteristic 1 (80-system MPU)



(V_{DD} = 5.0 V ± 10%, Ta = –40 to 85°C)

Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time Address set-up time		A0 CS	t_{AH8} t_{AW8}	—	10 20	— —	ns ns
System cycle time		WR RD	t_{CYC8}	—	1000	—	ns
Control pulse width	Write		t_{CC}	—	100	—	ns
	Read				200	—	ns
Data set-up time Data hold time		D0 to D7	t_{DS8} t_{DH8}	—	80 10	— —	ns ns
RD access time Output disable time			t_{ACC8} t_{OH8}	CL = 100 pF	— 10	180 90	ns ns

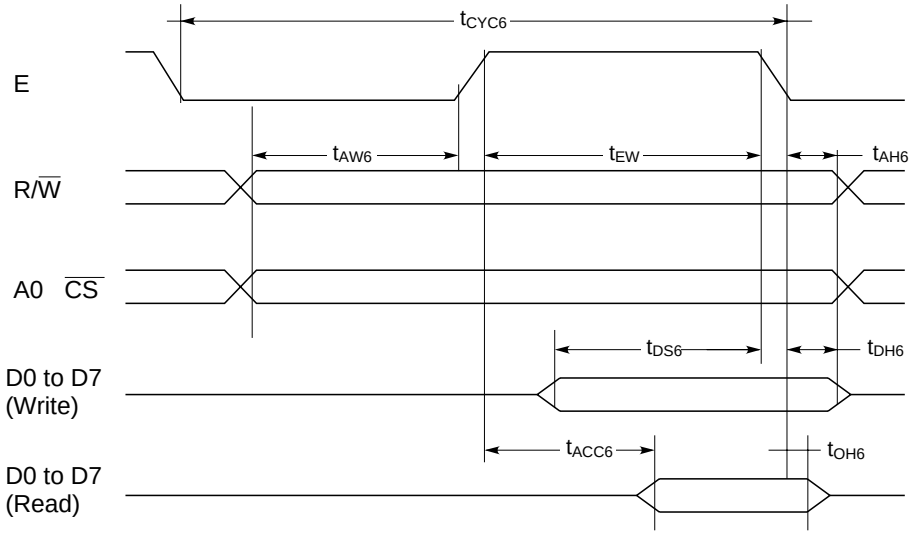
(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time Address set-up time		A0 CS	t_{AH8} t_{AW8}	—	20 40	— —	ns ns
System cycle time		WR RD	t_{CYC8}	—	2000	—	ns
Control pulse width	Write		t_{CC}	—	200	—	ns
	Read				400	—	ns
Data set-up time Data hold time		D0 to D7	t_{DS8} t_{DH8}	—	160 20	— —	ns ns
RD access time Output disable time			t_{ACC8} t_{OH8}	CL = 100 pF	— 20	360 180	ns ns

Note: * The rise time (tr) and fall time (tf) of the input signal are defined within 15 ns. Tr and tf are to define the AC timing of the input waveform, and operates without any problem even when a signal beyond the specification (15 ns) is input. However, it should be noted that the bigger tr and and tf are, the lower the margin for noise becomes.

* All timings are defined based on the standards of 20% and 80% of V_{DD}.

• System Bus Read/Write Characteristic 2 (68-system MPU)



(V_{DD} = 5.0 V ± 10%, Ta = –40 to 85°C)

Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time *1		A0 CS R/W	t_{CYC6}	—	1000	—	ns
Address set-up time Address hold time			t_{AW6} t_{AH6}	—	20 10	— —	ns ns
Data set-up time Data hold time		D0 to D7	t_{DS6} t_{DH6}	—	80 10	— —	ns ns
Output disable time Access time			t_{OH6} t_{ACC6}	CL = 100 pF	10	90 180	ns ns
Enable pulse width	Write	E	t_{EW}	—	100	—	ns
	Read				200	—	ns

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

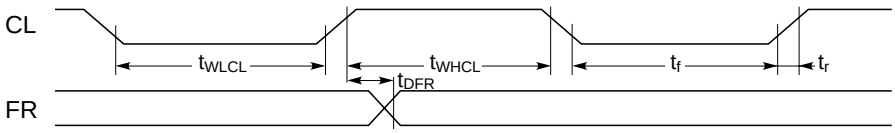
Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time *1		A0 CS R/W	t_{CYC6}	—	2000	—	ns
Address set-up time Address hold time			t_{AW6} t_{AH6}	—	40 20	— —	ns ns
Data set-up time Data hold time		D0 to D7	t_{DS6} t_{DH6}	—	160 20	— —	ns ns
Output disable time Access time			t_{OH6} t_{ACC6}	CL = 100 pF	20	180 360	ns ns
Enable pulse width	Write	E	t_{EW}	—	200	—	ns
	Read				400	—	ns

Notes: 1 "t_{CYC6}" represents the cycle of signal E when $\overline{CS}$ = LOW. If $\overline{CS}$ = HIGH → LOW, it is necessary to secure t_{CYC6} after $\overline{CS}$ = LOW is attained.

Note: * The rise time (tr) and fall time (tf) of the input signal are defined within 15 ns. Tr and tf are to define the AC timing of the input waveform, and operates without any problem even when a signal beyond the specification (15 ns) is input. However, it should be noted that the bigger tr and and tf are, the lower the margin for noise becomes.

* All timings are defined based on the standards of 20% and 80% of V_{DD}.

• Display Control Input Timing



(V_{DD} = 5.0 V ± 10%, Ta = –40 to 85°C)

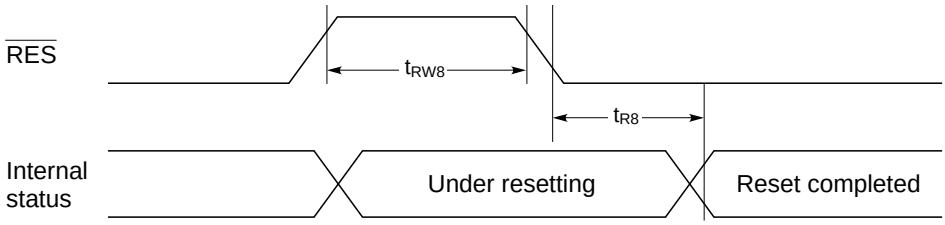
Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Low-level pulse width	CL	tWLCL	—	35	—	—	µs
High-level pulse width		tWHCL	—	35	—	—	µs
Rise time		tr	—	—	30	150	ns
Fall time		tf	—	—	30	150	ns
FR delay time	FR	tDFR	—	–2.0	0.2	2.0	µs

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Low-level pulse width	CL	tWLCL	—	70	—	—	µs
Highlevel pulse width		tWHCL	—	70	—	—	µs
Rise time		tr	—	—	60	300	ns
Fall time		tf	—	—	60	300	ns
FR delay time	FR	tDFR	—	–4.0	0.4	4.0	µs

Note: All timings are defined based on the standards of 20% and 80% of V_{DD}.

• Reset Input Timing (80-system MPU)



(V_{DD} = 5.0 V ± 10%, Ta = –40 to 85°C)

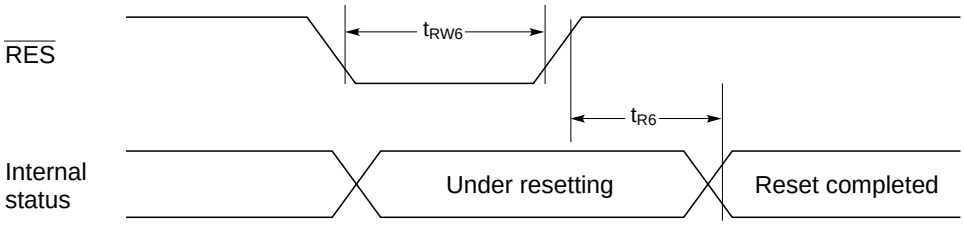
Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_{R8}		2.0	—	—	µs
Reset HIGH pulse width	$\overline{RES}$	t_{RW8}		1.0	—	—	µs

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_{R8}		4.0	—	—	µs
Reset HIGH pulse width	$\overline{RES}$	t_{RW8}		2.0	—	—	µs

Note: * The rise time (tr) and fall time (tf) of the input signal are defined within 15 ns. Tr and tf are to define the AC timing of the input waveform, and operates without any problem even when a signal beyond the specification (15 ns) is input. However, it should be noted that the bigger tr and and tf are, the lower the margin for noise becomes.
* All timings are defined based on the standards of 10% and 90% of V_{DD}.

• Reset Input Timing (68-system MPU)



(V_{DD} = 5.0 V ± 10%, Ta = –40 to 85°C)

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_{R6}		2.0	—	—	µs
Reset LOW pulse width	$\overline{RES}$	t_{RW6}		1.0	—	—	µs

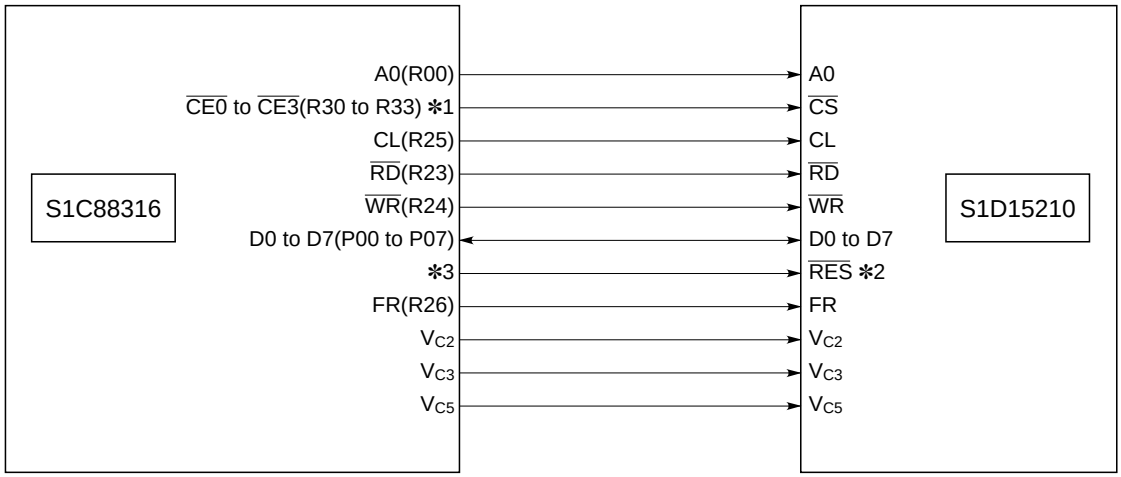
(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_{R6}		4.0	—	—	µs
Reset LOW pulse width	$\overline{RES}$	t_{RW6}		2.0	—	—	µs

Note: * The rise time (tr) and fall time (tf) of the input signal are defined within 15 ns. Tr and tf are to define the AC timing of the input waveform, and operates without any problem even when a signal beyond the specification (15 ns) is input. However, it should be noted that the bigger tr and and tf are, the lower the margin for noise becomes.
* All timings are defined based on the standards of 10% and 90% of V_{DD}.

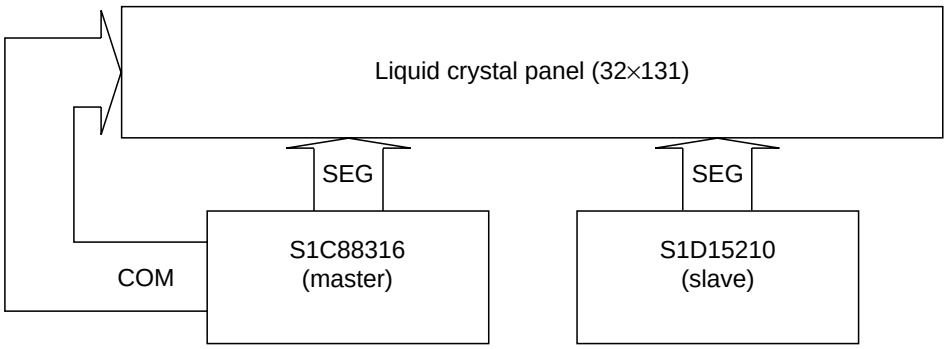
11. EXAMPLE OF CONNECTION

MPU Interface (MPU example: S1C88316)



Notes: 1 See S1C88316 technical Manual for the signals of S1C88316.
2 The reset input for 80-system MPU interface of S1D15210 is the opposite phase of that for the reset input of S1C88316.
3 For the reset input of S1D15210, we recommend that you use the output port of S1C88316 and send the reset signals through software.

EXAMPLE OF CONNECTIONS TO LIQUID CRYSTAL PANEL



4. S1D15206 Series

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1. DESCRIPTION

The S1D15206 series is a single-chip LCD driver for dot-matrix liquid crystal displays (LCD's). It accepts serial or 8-bit parallel display data directly from a microprocessor and stores data in an on-chip display RAM. It can generate an LCD drive signal independent from microprocessor clock.
As the S1D15206 series features the very low power dissipation and wide operating voltage range, it can easily realize a powerful but compact display unit having a small battery.
A single chip of S1D15206 series can drive a 17×80-pixel or 33×64-pixel LCD panel.

(Note: The S1D15206 series are not designed to have EMI resistance.)

2. FEATURES

- Direct data display using the display RAM. When RAM data bit is 0, it is not displayed; when 1, it is displayed.
- Large 80×33-bit RAM capacity
- On-chip LCD driver circuit (97 segment and common drivers)
- High-speed, 8-bit microprocessor interface allowing direct connection to both the 8080 and 6800
- Supported serial interface
- Rich command functions (upward compatible to S1D15200 Series); they are Read/Write Display Data, Display On/Off Switching, Set Page Address, Set Initial Display Line, Set Column Address, Read Status, Static Drive On/Off Switching, Select Duty, Duty+1, Read-Modify-Write, Select Segment Driver Direction, Power Save, Reset, Set Power Control, Set Electronic Controls, Clock Stop.
- On-chip CR oscillator circuit
- On-chip LCD power circuit (The on-chip and external LCD power supplies are software selectable.)
- Very low power consumption
- Flexible power voltages; 2.4 to 6.0 V (V_{DD}-V_{SS}) and -13.0 to -4.0 V (V_{DD}-V5)
- -40 to +85°C wide operating temperature range
- CMOS process
- 128-pin QFP5 package with aluminum pad or Au bump

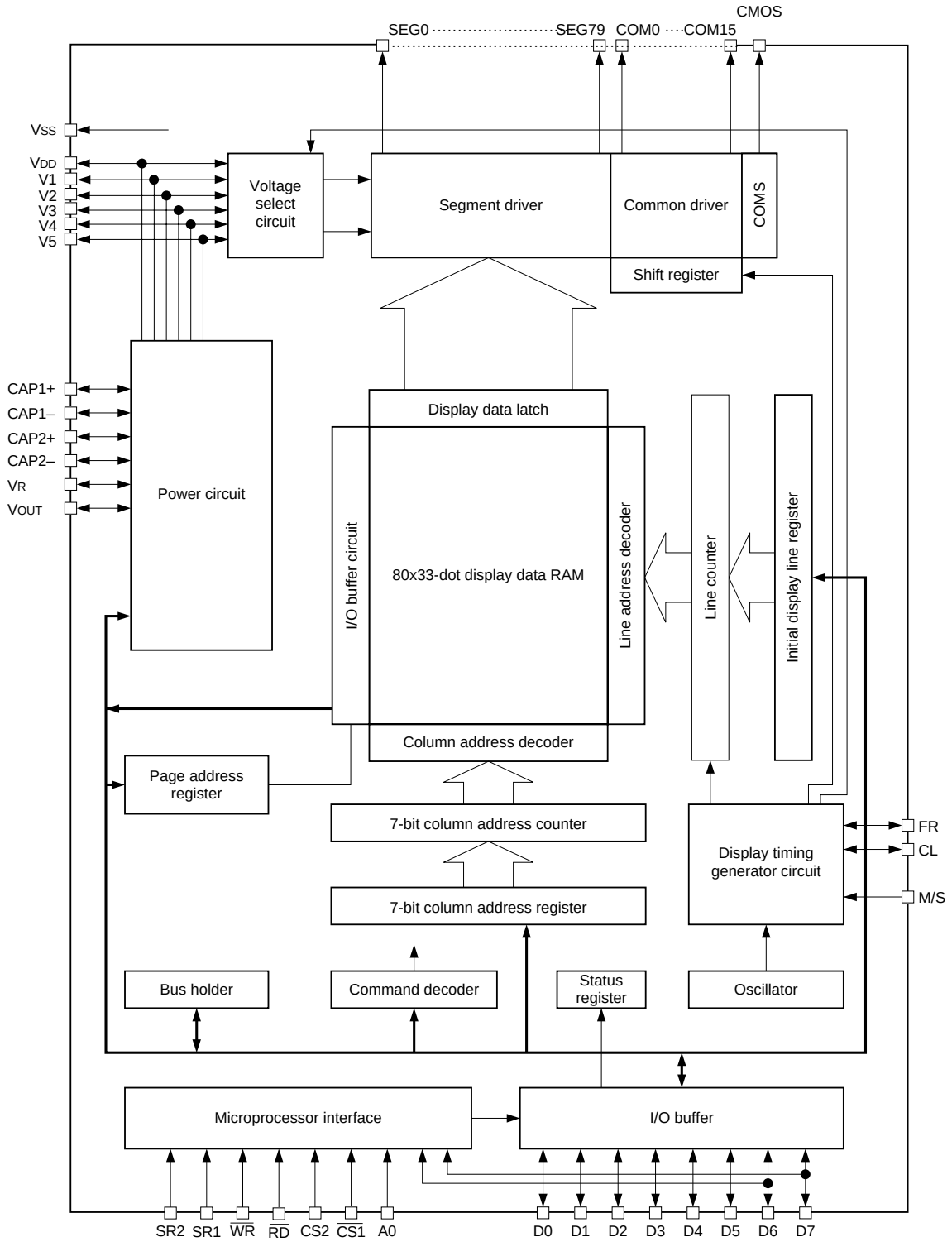
Series Specifications (for 128-pin flat package)

Model	Operating clock (Internal OSC)	f_{CL} (Typ.)	Duty	Segment driver	Common driver	V_{REG} type	COM pin positions	QFP
S1D15206F00A*	20 kHz	2.9	1/8, 1/9, 1/16, 1/17	80	17	Type 1	Type A	5
S1D15206F11A*		5.8						
S1D15206F10A*		2.9					Type B	
S1D15206F14A*		2.9				Type 2	Type A	
S1D15206F14Y*		2.9						26
S1D15208F00A*		2.9	1/32, 1/33	64	33	Type 1		5
S1D15208D11B*		5.8						—

V_{REG} type Type 1 V_{REG} (Built-in power supply regulating voltage)
Temperature gradient: -0.17% /°C
Type 2 V_{REG} (Built-in power supply regulating voltage)
Temperature gradient: 0.00% /°C
COMS pin positions Refer to No. P3 (Package pin layout), No. P4 (PAD layout) and No. P5 (PAD coordinates).

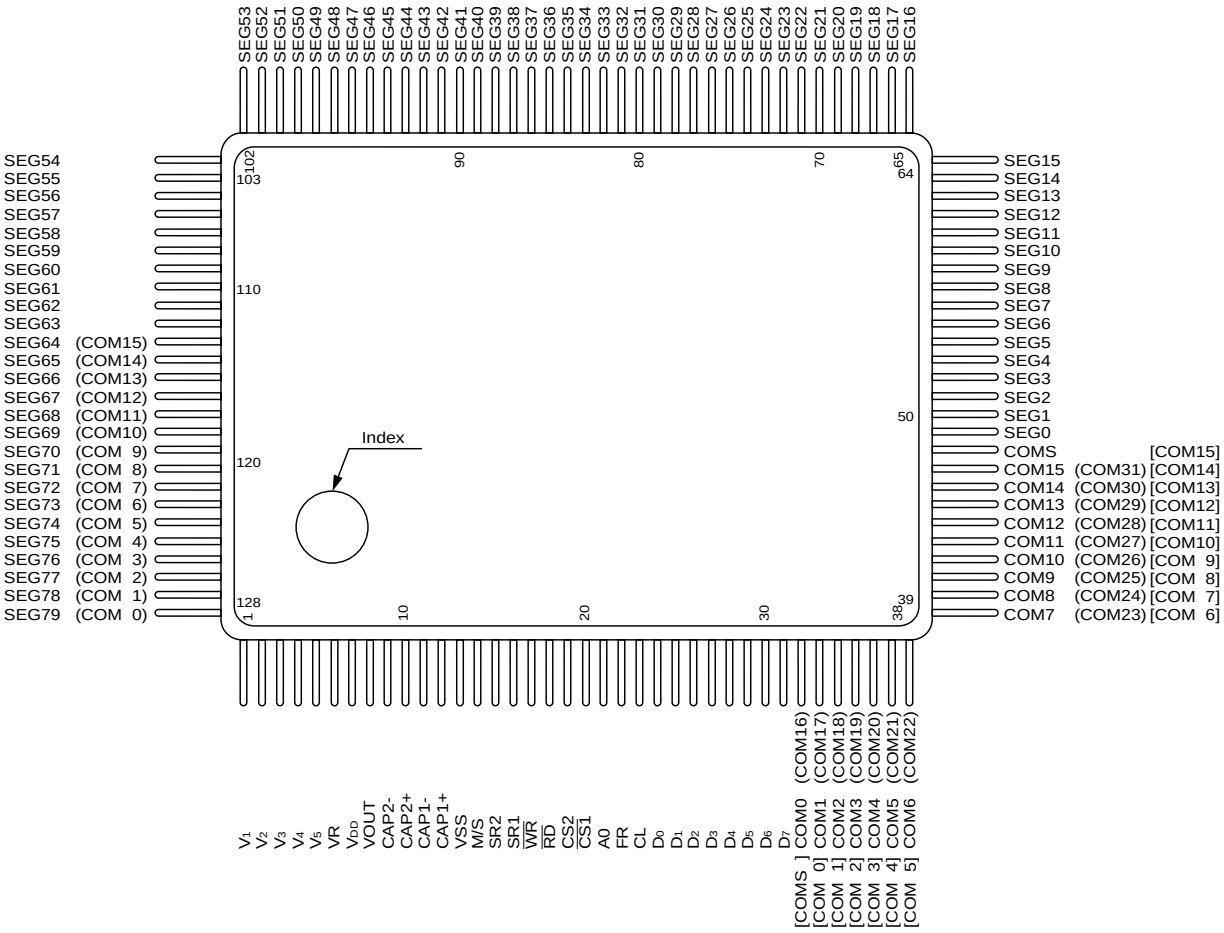
An S1D15206 series package has one of following subcodes according to its package type (an example of S1D15206):
S1D15206F****: 128-pin QFP5 flat package
S1D15206F**Y*: 128-pin QFP26 flat package
S1D15206D****: Bear chip
S1D15206D**A* :Al-pad chip
S1D15206D**B* :Au-bump chip
S1D15206T****: TCP

3. BLOCK DIAGRAM (S1D15206∗00∗∗)



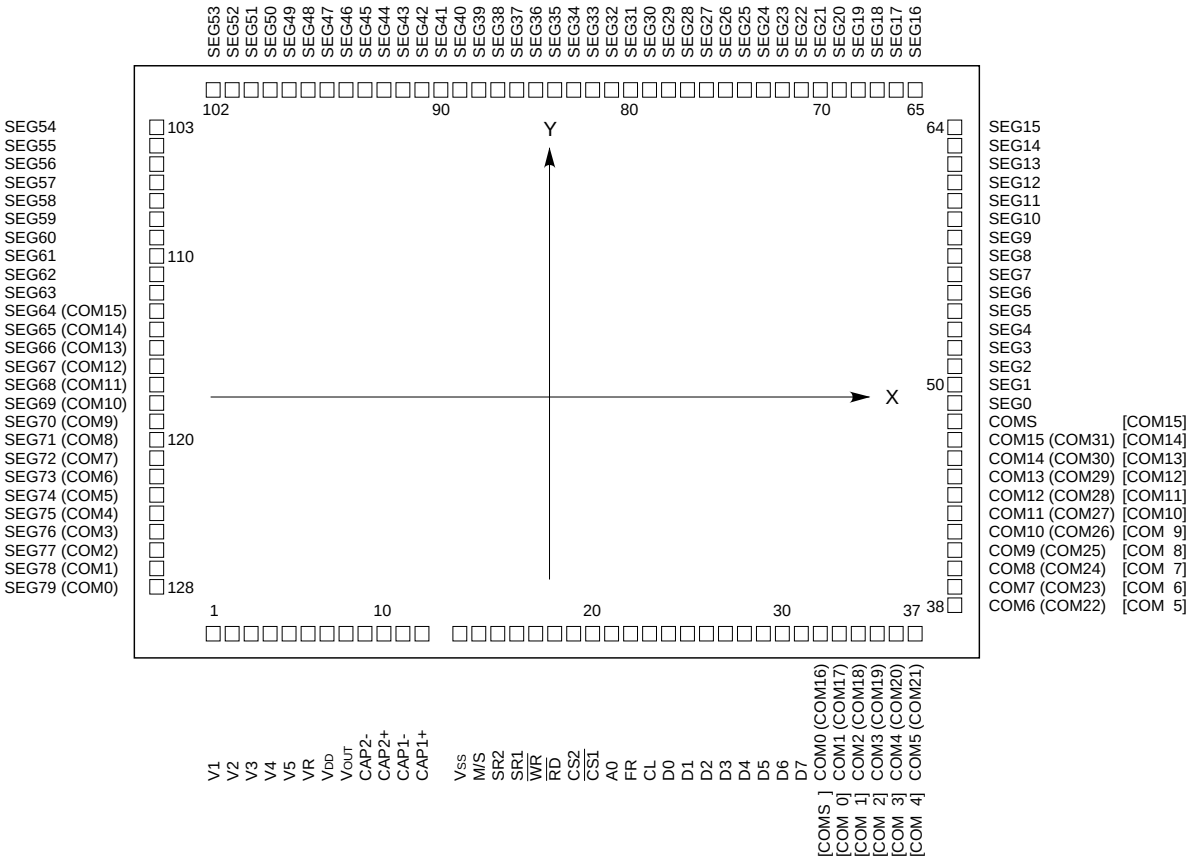
4. PIN LAYOUT

Package Pin Assignment



∗ Pin name in ( ) apply to S1D15208.
∗ Pin name in [ ] apply to S1D15206D10∗∗(CMOS Pin=Type B).

Pad Layout



* Pin names in ( ) apply to S1D15208.

* Pin names in [ ] apply to S1D15206D10** (CMOS pin = Type B).

Al- pad chip
- Chip size 5.92 mm × 4.68 mm
- Chip thickness 0.4 mm
- Pad opening 90.2 μm × 90.2 μm
- Pad pitch 130 μm (Min)

Au- bump chip (reference)
- Chip size 5.92 mm × 4.68 mm
- Chip thickness 0.4 mm
- Bump size 81.7 μm × 81.7 μm
- Bump height 22.5 μm

Pad Center Coordinates

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	V_1	–2767	–2106	65	SEG16	2516	2185
2	V_2	–2637	↓	66	SEG17	2367	↓
3	V_3	–2507		67	SEG18	2218	
4	V_4	–2377		68	SEG19	2088	
5	V_5	–2246	↓	69	SEG20	1957	
6	V_R	–2116	–2149	70	SEG21	1827	
7	V_{DD}	–1985	–2176	71	SEG22	1697	
8	V_{OUT}	–1857	↓	72	SEG23	1567	
9	CAP2–	–1727		73	SEG24	1437	
10	CAP2+	–1522		74	SEG25	1307	
11	CAP1–	–1318		75	SEG26	1177	
12	CAP1+	–1113	↓	76	SEG27	1046	
13	V_{SS}	–553	–2166	77	SEG28	916	
14	M/S	–356	–2185	78	SEG29	786	
15	SR2	–226	↓	79	SEG30	656	
16	SR1	–95		80	SEG31	526	
17	WR	35		81	SEG32	396	
18	RD	165		82	SEG33	266	
19	CS2	295		83	SEG34	135	
20	CS1	425		84	SEG35	5	
21	A0	555		85	SEG36	–125	
22	FR	719		86	SEG37	–255	
23	CL	849		87	SEG38	–385	
24	D0	979		88	SEG39	–515	
25	D1	1109		89	SEG40	–646	
26	D2	1239		90	SEG41	–776	
27	D3	1369		91	SEG42	–906	
28	D4	1500		92	SEG43	–1036	
29	D5	1630		93	SEG44	–1166	
30	D6	1760		94	SEG45	–1296	
31	D7	1890		95	SEG46	–1426	
32	COM0 (COM16) [CMOS]	2069		96	SEG47	–1557	
33	COM1 (COM17) [COM0]	2199		97	SEG48	–1687	
34	COM2 (COM18) [COM1]	2329		98	SEG49	–1817	
35	COM3 (COM19) [COM2]	2459		99	SEG50	–1947	
36	COM4 (COM20) [COM3]	2589		100	SEG51	–2077	
37	COM5 (COM21) [COM4]	2719	↓	101	SEG52	–2226	
38	COM6 (COM22) [COM5]	2802	–1654	102	SEG53	–2375	↓
39	COM7 (COM23) [COM6]	↓	–1524	103	SEG54	–2802	1932
40	COM8 (COM24) [COM7]		–1393	104	SEG55	↓	1802
41	COM9 (COM25) [COM8]		–1263	105	SEG56		1672
42	COM10 (COM26) [COM9]		–1133	106	SEG57		1541
43	COM11 (COM27) [COM10]		–1003	107	SEG58		1411
44	COM12 (COM28) [COM11]		–873	108	SEG59		1281
45	COM13 (COM29) [COM12]		–743	109	SEG60		1151
46	COM14 (COM30) [COM13]		–612	110	SEG61		1021
47	COM15 (COM31) [COM14]		–482	111	SEG62		891
48	COMS [COM15]		–352	112	SEG63		760
49	SEG0		–193	113	SEG64 (COM15)		599
50	SEG1		–63	114	SEG65 (COM14)		469
51	SEG2		67	115	SEG66 (COM13)		339
52	SEG3		197	116	SEG67 (COM12)		209
53	SEG4		327	117	SEG68 (COM11)		78
54	SEG5		457	118	SEG69 (COM10)		–52
55	SEG6		588	119	SEG70 (COM9)		–182
56	SEG7		718	120	SEG71 (COM8)		–312
57	SEG8		848	121	SEG72 (COM7)		–442
58	SEG9		978	122	SEG73 (COM6)		–572
59	SEG10		1108	123	SEG74 (COM5)		–703
60	SEG11		1238	124	SEG75 (COM4)		–833
61	SEG12		1368	125	SEG76 (COM3)		–963
62	SEG13		1499	126	SEG77 (COM2)		–1093
63	SEG14		1629	127	SEG78 (COM1)		–1223
64	SEG15	↓	1759	128	SEG79 (COM0)	↓	–1353

* Pin names in ( ) apply to S1D15208.

* Pin names in [ ] apply to S1D15206D10∗ (CMOS pin = Type B).

5. PIN DESCRIPTION

Power Supply

Name	I/O	Description	Number of pins
V_{DD}	Supply	+5VDC power supply. Common to microprocessor power supply pin V_{CC}.	1
V_{SS}	Supply	Ground	1
V_1, V_2 V_3, V_4 V_5	Supply	LCD driver supply voltages. The Set Power Control command can switch the on-chip and external power supply modes of these pins. When external mode selects, the voltage determined by LCD cell is impedance-converted by a resistive divider or an operational amplifier for application. Voltages should be the following relationship: $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ When master mode selects, these voltages are generated on the chip: S1D15206: V1 = 1/5 V_5, V2 = 2/5 V_5, V3 = 3/5 V_5, V4 = 4/5 V_5 S1D15208: V1 = 1/7 V_5, V2 = 2/7 V_5, V3 = 5/7 V_5, V4 = 6/7 V_5	5

LCD Driver Supplies

Name	I/O	Description	Number of pins
CAP1+	O	DC/DC voltage converter capacitor 1 positive connection	1
CAP1–	O	DC/DC voltage converter capacitor 1 negative connection	1
CAP2+	O	DC/DC voltage converter capacitor 2 positive connection	1
CAP2–	O	DC/DC voltage converter capacitor 2 negative connection	1
V_{OUT}	O	DC/DC voltage converter output	1
V_R	I	Voltage adjustment pin. Applies voltage between V_{DD} and V_5 using a resistive divider.	1

Microprocessor Interface

Name	I/O	Description	Number of pins
D0 to D7 (SI) (SCL)	I/O	Data input/outputs. The 8-bit bidirectional data buses to be connected to the standard 8-bit microprocessor data buses. When the serial interface selects, D7 is serial data input (SI) and D6 is serial clock input (SCL).	8
A0	I	Control/display data flag input. It is connected to the LSB of microprocessor address bus. When LOW, the data on D0 to D7 is control data. When HIGH, the data on D0 to D7 is display data.	1
$\overline{CS1}$ CS2	I	Chip select input. Data input/output is enabled when -CS1 is LOW and CS2 is HIGH.	2
$\overline{RD}$ (E)	I	• Read enable input. When interfacing to an 8080-series microprocessor and when its $\overline{RD}$ is LOW, the S1D15206 series data bus output is enabled. • When interfacing to an 6800-series microprocessor and when its R/$\overline{W}$ Enable (E) is HIGH, the S1D15206 series R/$\overline{W}$ input is enabled.	1
$\overline{WR}$ (R/$\overline{W}$)		• Write enable input. When interfacing to an 8080-series microprocessor, $\overline{WR}$ is active LOW. • When interfacing to an 6800-series microprocessor, it will be read mode when R/$\overline{W}$ is HIGH and it will be write mode when R/$\overline{W}$ is LOW. R/$\overline{W}$ = “1” : Read R/$\overline{W}$ = “0” : Write	1

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>SR1,
SR2</td><td>I</td><td>Microprocessor interface select, and parallel/serial data input select.
<table>
<tr><th>SR1</th><th>SR2</th><th>Type</th></tr>
<tr><td>0</td><td>1</td><td>8080 microprocessor bus (parallel input)</td></tr>
<tr><td>1</td><td>1</td><td>6800 microprocessor bus (parallel input)</td></tr>
<tr><td>1</td><td>0</td><td>Serial input</td></tr>
<tr><td>0</td><td>0</td><td>Reset</td></tr>
</table>
* In serial mode, no data can be read from RAM and D0 to D5 are HZ. $\overline{RD}$ and $\overline{WR}$ must be HIGH or LOW.
When set for the 68 family MPU, the SR1 and SR2 timing must match or SR1 must rise first.</td><td>2</td></tr>
</table>

LCD Driver Outputs

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>M/S</td><td>I</td><td>Normally “1”.</td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>Normally “1”.</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>Normally “1”.</td><td>1</td></tr>
<tr><td>SEGn</td><td>O</td><td>LCD segment driver output. V_{DD}, V_2, V_3, or V_5 can select according to the display RAM and FR signal.
<table>
<tr><th>RAM data</th><th>FR signal</th><th>Output voltage of SEGn</th></tr>
<tr><td rowspan="2">1</td><td>1</td><td>V_{DD}</td></tr>
<tr><td>0</td><td>V_5</td></tr>
<tr><td rowspan="2">0</td><td>1</td><td>V_2</td></tr>
<tr><td>0</td><td>V_3</td></tr>
<tr><td>Power save</td><td>–</td><td>V_{DD}</td></tr>
</table></td><td>80 (S1D15206)
or 64 (S1D15208)</td></tr>
<tr><td>COMn</td><td>O</td><td>LCD common driver output. V_{DD}, V_1, V_4, or V_5 can select according to IC internal scan signal and FR signal. The common scan sequence is reversed in slave mode.
<table>
<tr><th>Internal scan signal</th><th>FR signal</th><th>Output voltage of COMn</th></tr>
<tr><td rowspan="2">1</td><td>1</td><td>V_5</td></tr>
<tr><td>0</td><td>V_{DD}</td></tr>
<tr><td rowspan="2">0</td><td>1</td><td>V_1</td></tr>
<tr><td>0</td><td>V_4</td></tr>
<tr><td>Power save</td><td>–</td><td>V_{DD}</td></tr>
</table></td><td>16 (S1D15206)
or 32 (S1D15208)</td></tr>
<tr><td>COMS</td><td>O</td><td>Indicator COM output. COMS pin is equivalent to following COM output pin when Duty+1 command is running:
<table>
<tr><th rowspan="2"></th><th colspan="2">S1D15206</th><th>S1D15208</th></tr>
<tr><th>1/9 duty</th><th>1/17 duty</th><th>1/33 duty</th></tr>
<tr><td>Indicator COMS output</td><td>COM8</td><td>COM16</td><td>COM32</td></tr>
</table></td><td>1</td></tr>
</table>

6. FUNCTION DESCRIPTION

MPU Interface

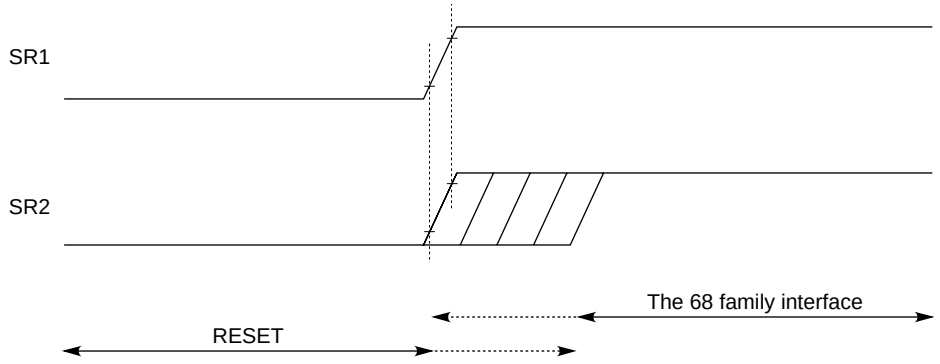
Parallel/Serial Interface

The S1D15206 series can transfer data via 8-bit bidirectional data buses D0 to D7 or via serial data input D7 (SI). The 8-bit parallel data input or serial data input, 8080/6800-series microprocessor, and reset status can select according to SR1 and SR2.
No data can be read from RAM and no status can be read during serial data input. Also, $\overline{RD}$ and $\overline{WR}$ are high or low, and D0 to D5 are open.

Table 1

SR1	SR2	Type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	Data (D0 to D7)
0	1	8080 microprocessor bus (parallel)	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
1	1	6800 microprocessor bus (parallel)	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D0 to D7
1	0	Serial input	$\overline{CS1}$	CS2	A0	0/1	0/1	D6 (SCL) and D7 (SI)
0	0	Reset	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	— — — — — — — —

* When set for the 68 family interface, the SR1 and SR2 timing must match or SR1 must rise first.



Data Bus Signals

The S1D15206 series identifies the data bus signal according to A0, $\overline{RD}$, and $\overline{WR}$ (E, R/$\overline{W}$) signals.

Table 2

Common	6800 processor	8080 processor		Function
A0	$\overline{WR}$ (R/$\overline{W}$)	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads display data.
1	0	1	0	Writes display data.
0	1	0	1	Reads status.
0	0	1	0	Writes control data in internal register. (commands)

Serial Interface (SR1 is high and SR2 is low)

The serial interface consists of an 8-bit shift register and a 3-bit counter. The serial data input and serial clock input are enabled when $\overline{CS1}$ is low and CS2 is high (in chip select status). When chip is not selected, the shift register and counter are reset.
When serial data input is enabled by SR1 and SR2, D7 (SI) receives serial data and D6 (SCL) receives serial clock. Serial data of D7, D6, ..., D0 is read at D7 in this sequence when serial clock goes high. They are converted into 8-bit parallel data and processed on rising edge of every eighth serial clock signal.
The serial data input is determined to be the display data when A0 is high, and it is control data when A0 is low. A0 is read on rising edge of every eighth clock signal.
Figure 1 shows a timing chart of serial interface signals. The serial clock signal must be terminated correctly against termination reflection and ambient noise. Operation checkout on the actual machine is recommended.

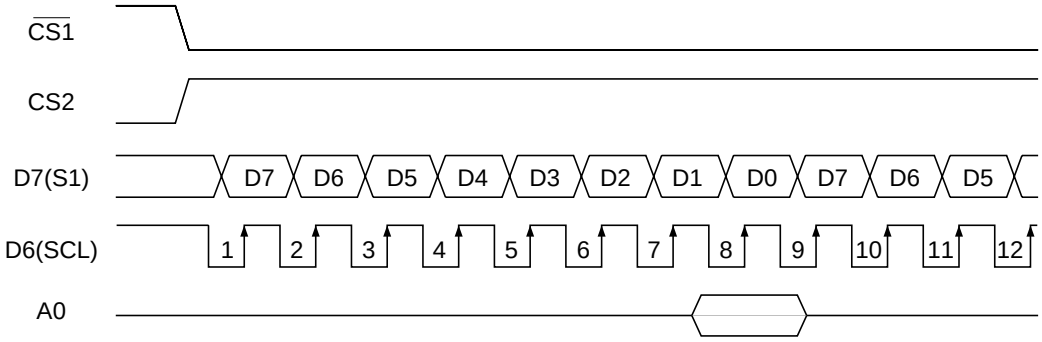


Figure 1

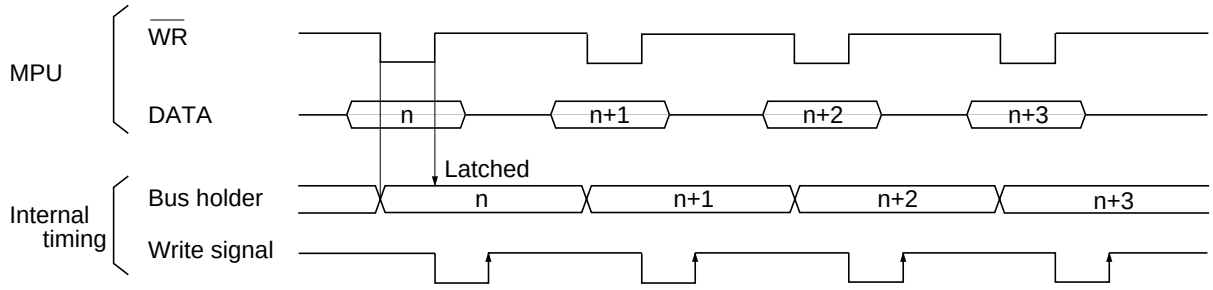
Chip Select Inputs

The S1D15206 series can interface to microprocessor when $\overline{CS1}$ is LOW and CS2 is HIGH.
When these pins are set to any other combination, D0 to D7 are high impedance. A0, $\overline{RD}$, and $\overline{WR}$ input are disabled. However, the reset signal is entered regardless of $\overline{CS1}$ and CS2 setup. The internal IC status including LCD driver circuit is held until a reset signal is entered.

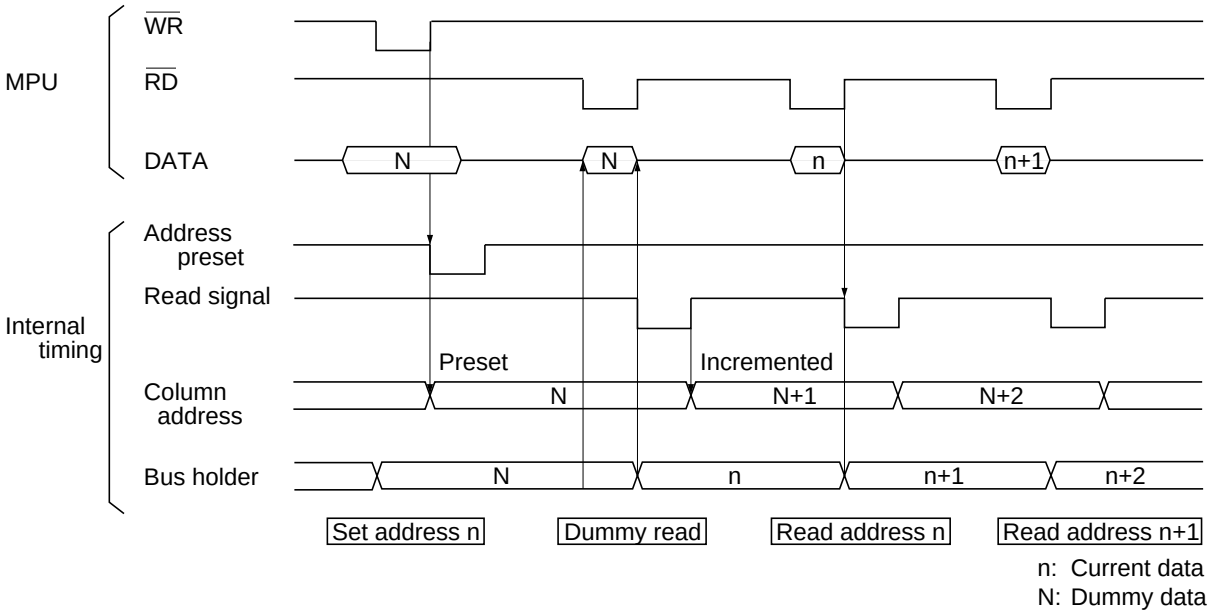
Access to Display Data RAM and Internal Registers

The S1D15206 series can perform a series of pipeline processing between LSI's using bus holder of internal data bus in order to match the operating frequency of display RAM and internal registers with the microprocessor. For example, the microprocessor reads data from display RAM in the first read (dummy) cycle, stores it in bus holder, and outputs it onto system bus in the next data read cycle. Also, the microprocessor temporarily stores display data in bus holder, and stores it in display RAM until the next data write cycle starts.
When viewed from the microprocessor, the S1D15206 series access speed greatly depends on the cycle time rather than access time to the display RAM (t_{ACC} and t_{DS}). It shows the data transfer speed to/from the microprocessor can increase. If the cycle time is inappropriate, the microprocessor can insert the NOP instruction that is equivalent to the wait cycle setup. However, there is a restriction in the display RAM read sequence. When an address is set, the specified address data is NOT output at the immediately following read instruction. The address data is output during second data read. A single dummy read must be inserted after address setup and after write cycle (refer to Figure 2).

•Write



•Read



n: Current data
N: Dummy data

Figure 2

Busy Flag

The Busy flag is set when the S1D15206 series starts to operate. During operating, it accepts Read Status instruction only. The busy flag signal is output at pin D7 when Read Status is issued. If the cycle time (t_{cyc}) is correct, the microprocessor needs not to check the flag before issuing a command. This can greatly improve the microprocessor performance.

Initial Display Line Register

When the display RAM data is read, the display line according to COM0 (usually, the top line of screen) is determined using register data. The register is also used for screen scrolling and page switching.

The Set Display Start Line command sets the 5-bit display start address in this register. The register data is preset on the line counter each time FR signal status changes. The line counter is incremented by oscillator circuit output (in master mode) or CL input (in slave mode), and it generates a line address to allow 80-bit sequential data output from display RAM to LCD driver circuit.

Column Address Counter

This is a 7-bit presettable counter that provides column address to the display RAM (refer to Figure 4). It is incremented by 1 when a Read/Write command is entered. However, the counter is not incremented but locked if a non-existing address above 50H is specified. It is unlocked when a column address is set again. The Column Address counter is independent of Page Address register.
When ADC Select command is issued to display inverse display, the column address decoder inverts the relationship between RAM column address and display segment output.

Page Address Register

This is a 4-bit page address register that provides page address to the display RAM (refer to Figure 4). The microprocessor issues Set Page Address command to change the page and access to another page. Page address 4 (D2 is high, but D0 and D1 are low) is RAM area dedicate to the indicator, and display data D0 is only valid.

Display Data RAM

The display data RAM stores pixel data for LCD. It is a 33-column by 80-row (4-page by 8+1 bit) addressable array. Each pixel can be selected when page and column addresses are specified.
The time required to transfer data is very short because the microprocessor enters D0 to D7 corresponding to LCD common lines as shown in Figure 3. Therefore, multiple S1D15206's can easily configure a large display having the high flexibility with very few data transmission restriction.
The microprocessor writes and reads data to/from the RAM through I/O buffer. As LCD controller operates independently, data can be written into RAM at the same time as data is being displayed, without causing the LCD to flicker.

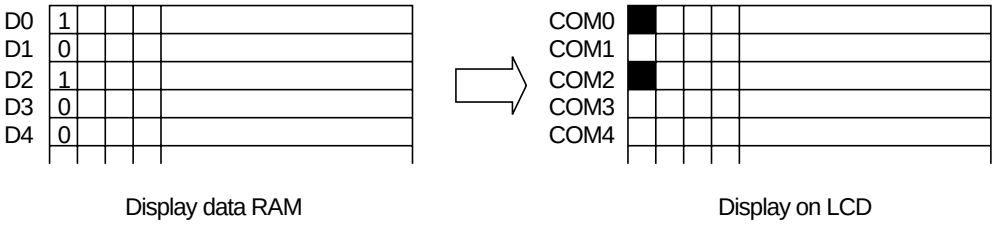


Figure 3

Relationship between display data RAM and addresses (if initial display line is 08):

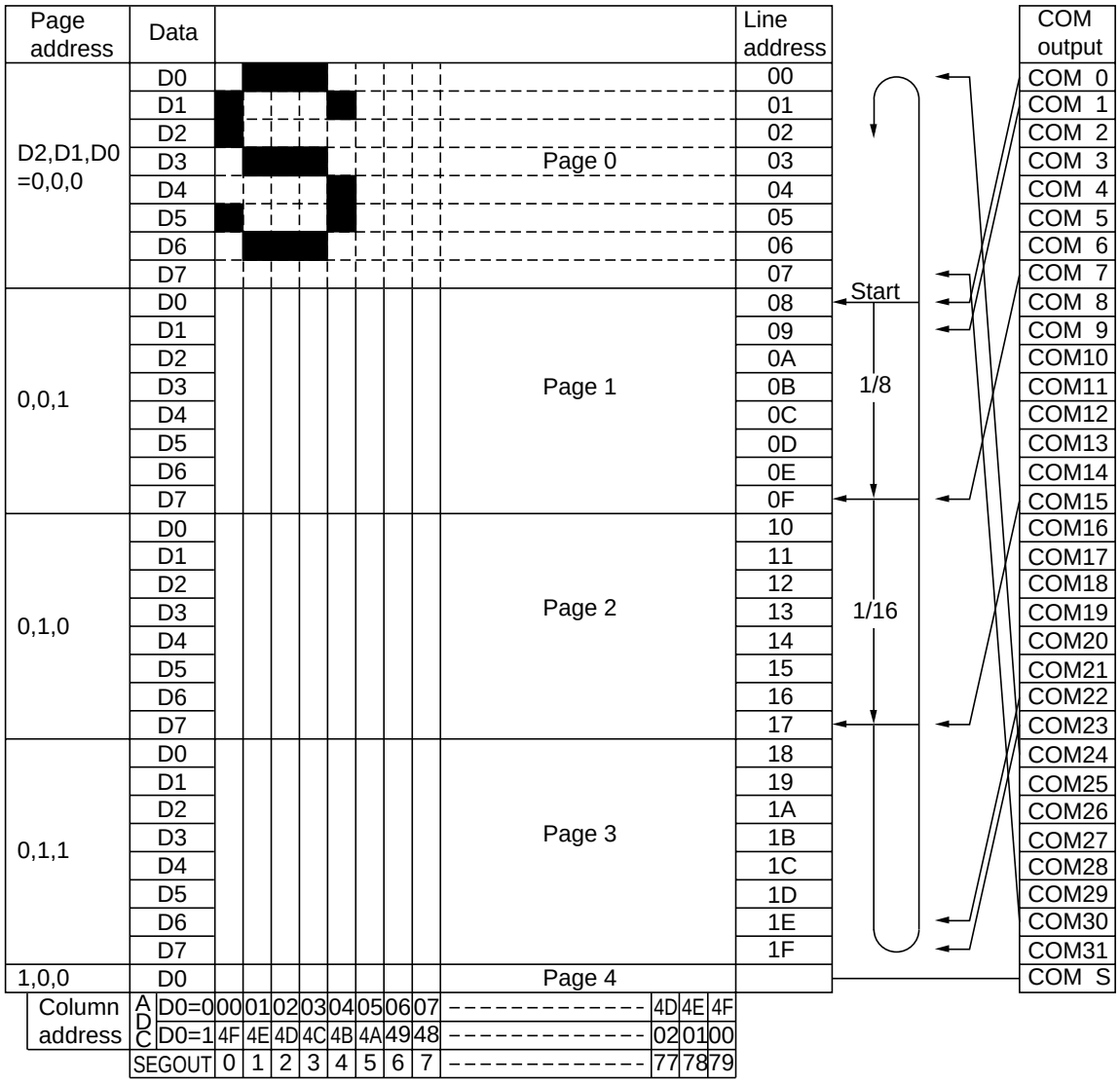


Figure 4

Display Timing Generator Circuit

This section explains how the display timing generator circuit operates.

Signal generation to line counter and display data latch circuit

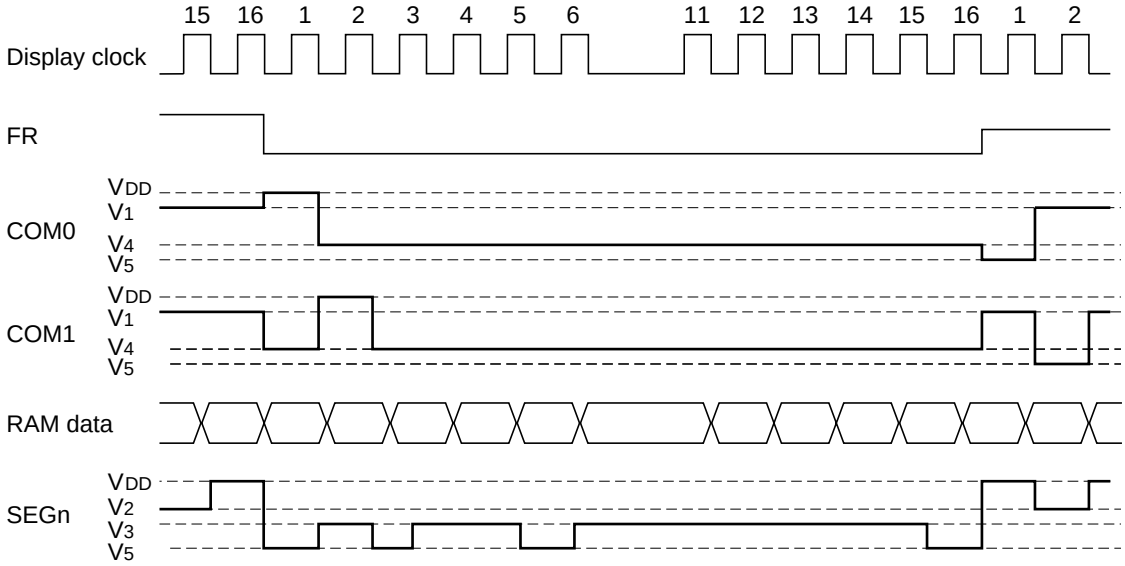
The line address counter, RAM, and latch circuit of the S1D15206 series operate synchronous to the display clock (the oscillator circuit outp).mm The LCD drive signal is sent to LCD panel driver output pin SEGn.

The timing of LCD panel driver outputs is independent of the timing of RAM data input from microprocessor.

LCD AC Signal (FR)

The LCD AC signal, FR, is generated from the display clock. The FR controller generates dual-frame AC driver waveforms for LCD panel driver circuit.

- **Dual-frame AC driver waveforms**
  (If S1D15206 is used in 1/16 duty)



Common timing Signals

The common timing generator circuit uses the display clock to generate common timing signal and FR frame signal. The Duty Select command can select 1/8 or 1/16 duty (S1D15206). A combination of Select Duty and Duty+1 commands can select 1/9 or 1/17 duty (S1D15206).

Display Data Latch Circuit

This circuit temporarily stores (or latches) display data (during a single common signal period) when it is output from display RAM to LCD panel driver circuit. This latch is controlled by Display ON/OFF and Static Drive ON/OFF commands. These commands do not alter the data.

LCD Driver

This is a multiplexer circuit consisting of 96 segment outputs to generate four-level LCD panel drive signals. The circuit also has a pair of COM outputs for indicator display.
The COMn output has a shift register to sequentially output COM scan signals. The LCD panel drive voltage is generated by a specific combination of display data, COM scan signal, and FR signal. Figure 6 gives an example of SEG and COM output waveforms.

Oscillation Circuit

This is a low power consumption CR oscillator having an oscillator resistor, and its output is used as the display timing signal source or as the clock for voltage boost circuit of LCD power supply.
The display clock output can be stopped by Clock Stop command to minimize the current consumption of LCD panel.

Power Supply Circuit

The power supply circuit produces voltage to drive LCD panel at low power consumption. The power circuit consists of three subcircuits: voltage tripler, voltage regulator, and voltage follower. The voltage tripler outputs V_{DD} -(V_{SS}×2) or -(V_{SS}×3) voltage at V_{OUT}. The regulator circuit generates V_5 voltage using external resistor. The voltage follower circuit changes the impedance of V_1 to V_4 that are generated from V_5 through division with internal resistors. (Details are explained later.)
S1D15206 series can drive LCD panel using on-chip power circuit. However, the on-chip power circuit is intended to use for a small LCD panel and it is inappropriate to a large panel requiring multiple driver chips. As the large LCD panel has the dropped display quality due to large load capacity, it must use an external power source.
The power circuit is controlled by Set Power Control command. This command sets a three-bit data in Power Control register to select one of eight power circuit functions. The external power supply and part of on-chip power circuit functions can be used simultaneously. The following explains how the Set Power Control command works.

[Control by Set Power Control command]

D2 turns on when triple booster control bit goes HIGH, and D2 turns off when this bit goes LOW.

D1 turns on when voltage regulator control bit goes HIGH, and D1 turns off when this bit goes LOW.

D0 turns on when voltage follower control bit goes HIGH, and D0 turns off when this bit goes LOW.

[Practical combination examples]

D2 D1 D0	Voltage booster	Voltage regulator	Voltage follower	External voltage input	Voltage booster terminal	Voltage regulator terminal
1 1 1	ON	ON	ON	—	Used	Used
1 0 0	ON	OFF	OFF	—	Used	OPEN
0 1 1	OFF	ON	ON	To V_{OUT}	OPEN	Used
0 0 0	OFF	OFF	OFF	To V_1 to V_5	OPEN	OPEN

To use the on-chip (internal) power supply only, set (D2,D1,D0)=(1,1,1).

To use the voltage booster circuit only, set (D2,D1,D0)=(1,0,0).

To use the voltage regulator and voltage follower, set (D2,D1,D0)=(0,1,1).

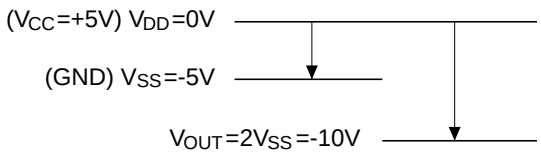
To use an external power supply only, set (D2,D1,D0)=(0,0,0).

Notes: 1. The voltage booster terminals are CAP1+, CAP1-, CAP2+, and CAP2-.
2. The above listed examples are the most practical use to control each circuit using control bits. Any other setup is unpractical and omitted in this manual.
3. The V/F circuit alone cannot be used. When this circuit is used, the V adjustment circuit must be set simultaneously.

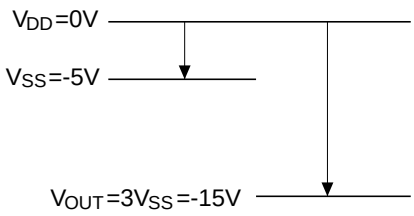
Voltage tripler

If capacitors C1 are inserted between CAP1+ and CAP1-, between CAP2+ and CAP2–, and between V_{SS} and V_{OUT}, the potential between V_{DD} and V_{SS} is boosted to triple toward negative side and it is output at V_{OUT}. For double boosting, remove only capacitor C1 between CAP2+ and CAP2-, open CAP2+, and jumper between CAP2- and V_{OUT}. The double boosted voltage appears at V_{OUT} (CAP2-).

The booster receives signals from oscillator circuit and, therefore, the oscillator must be active. The following shows the boosted potential.



Potential during double boosting

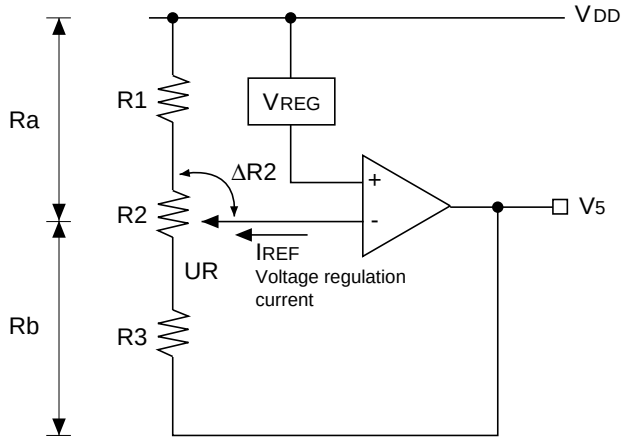


Potential during triple boosting

Voltage regulator

The boosting voltage occurring at V_{OUT} is sent to the voltage regulator and the V_5 liquid crystal display (LCD) drive voltage is output. This V_5 voltage can be determined by the following equation when resistors Ra and Rb (R1, R2 and R3) are adjusted within the range of $|V_5|<|V_{OUT}|$.

$$V_5=(1+\frac{Rb}{Ra})\cdot V_{REG}+I_{REF}\cdot Rb$$
$$=(1+\frac{R3+R2-\Delta R2}{R1+\Delta R2})\cdot V_{REG}$$
$$+I_{REF}\cdot(R3+R2-\Delta R2)$$



where, V_{REG} is the constant voltage source of the IC, and it is constant (V_{REG} ≒ –3.1 V). (V_{REG}=Type1) $V_{REG}=V_{SS}$(V_{DD} basis) (V_{REG}=Type2)
I_{REF} is the voltage regulation current of the Electronic Volume Control Function, and I_{REF} ≒ 2.4 µA if the electronic volume control register (32-state) has (D4,D3,D2,D1,D0)=(1,1,1,1,1).
To adjust the V_5 output voltage, insert a variable resistor between V_R, V_{DD} and V_5 as shown. A combination of R1 and R3 constant resistors and R2 variable resistor is recommended for fine-adjustment of V_5 voltage.

Setup example of resistors R1, R2 and R3:

When the Electronic Volume Control Function is OFF (electronic volume control register values are (D4,D3,D2,D1,D0) =(0,0,0,0,0)):

$$V_5 = (1 + \frac{R3 + R2 - \Delta R2}{R1 + \Delta R2}) \cdot V_{REG} \quad \cdots\cdots ①$$

(As I_{REF} = 0A)

- R1 + R2 + R3 = 6.0 MΩ ..... ②
  (Determined by the current passing between V_{DD} and V5)
- Variable voltage range by R2: –6.2 to –9.3 V
  (Determined by the LCD characteristics)
  ΔR2 = 0Ω, V_{REG} = –3.1 V
  To obtain V_5 = –9.3 V, from equation (1):
  R2 + R3 = 2 · R1 ..... ③
  ΔR2 = R2, V_{REG} = –3.1 V
  To obtain V_5 = –6.2 V, from equation (1):
  R1 + R2 = 1 · R1 ..... ④

From equations ②, ③ and ④: R1 = 2.0 MΩ
R2 = 1.0 MΩ
R3 = 3.0 MΩ

The voltage regulator circuit has a temperature gradient of approximately –0.17%/°C as the V_{REG} voltage. To obtain another temperature gradient, use the Electronic Volume Control Function for software processing using the MPU.
As the VR pin has a high input impedance, the shielded and short lines must be protected from a noise interference.
When the V_{REG} = Type 2, similarly preset R1, R2 and R3 on the basis of V_{REG} = V_{SS}.

Voltage regulator circuit using the Electronic Volume Control Function

The Electronic Volume Control Function can adjust the intensity (brightness level) of liquid crystal display (LCD) screen by command control of V_5 LCD driver voltage.
This function sets five-bit data in the electronic volume control register, and the V_5 LCD driver voltage can be one of 32-state voltages.

To use the Electronic Volume Control Function, issue the Set Power Control command to simultaneously operate both the voltage regulator circuit and voltage follower circuit.
Also, when the voltage tripler off, the voltage must be supplied from V_{OUT} terminal.

When the Electronic Volume Control Function is used, the V_5 voltage can be expressed as follows:

$$V_5 = (1 + \frac{Rb}{Ra}) \cdot V_{REG} + I_{REF} \cdot Rb \quad \cdots\cdots ⑤$$

(Variable voltage range)

The increased V_5 voltage is controlled by use of I_{REF} current source of the IC. (For 32 voltage levels, $\Delta I_{REF}=I_{REF}/31$)

The minimum setup voltage of the V_5 absolute value is determined by the ratio of external Ra and Rb, and the increased voltage by the Electronic Volume Control Function is determined by resistor Rb. Therefore, the resistors must be set as follows:

(1) Determine Rb resistor depending on the V_5 variable voltage range by use of the Electronic Volume Control.

$$Rb = \frac{V_5 \text{ variable voltage range}}{I_{REF}}$$

(2) To obtain the minimum voltage of the V_5 absolute value, determine Ra using the Rb of Step (1) above.

$$Ra = \frac{Rb}{\frac{V_5}{V_{REG}} - 1} \qquad [V_5 = (1 + Rb/Ra) \cdot V_{REG}]$$

The S1D15206 series have the built-in V_{REG} reference voltage and I_{REF} current source which are constant during voltage variation. However, they may change due to the variation occurring in IC manufacturing and due to the temperature change as shown below. Consider such variation and temperature change, and set the Ra and Rb appropriate to the LCD used.
V_{REG} =–3.1V±0.4V (Type1) V_{REG} =–0.17%/°C
V_{REG} =V_{SS} (V_{DD} basis) (Type2) V_{REG} =–0.00%/°C
I_{REF} = –1.2 µA ± 40% (For 16 levels) I_{REF} = 0.011 µA/°C
I_{REF} = –2.4 µA ± 40% (For 32 levels) I_{REF} = 0.022 µA/°C
Ra is a variable resistor that is used to correct the V5 voltage change due to V_{REG} and I_{REF} variation. Also, the contrast adjustment is recommended for each IC chip.
Before adjusting the LCD screen contrast, set the electronic volume control register values to (D4,D3,D2,D1,D0)=(1,0,0,0,0) or (0,1,1,1,1) first.
When not using the Electronic Volume Control Function, set the register values to (D4,D3,D2,D1,D0)=(0,0,0,0,0) by sending the $\overline{RES}$ signal or by issuing the Set Electronic Volume Control Register command.

Setup example of constants when Electronic Volume Control Function is used:

V_5 maximum voltage: V_5 = –6.2 V (Electronic volume control register values (D4,D3,D2,D1,D0)=(0,0,0,0,0))

V_5 minimum voltages: V_5 = –8.6 V (Electronic volume control register values (D4,D3,D2,D1,D0)=(1,1,1,1,1))

V_5 variable voltage range: 2.4 V

Variable voltage levels: 32 levels

(1) Determining the Rb:

$$Rb = \frac{V_5 \text{ variable voltage range}}{|I_{REF}|} = \frac{2.4\ V}{2.4\ \mu A} \qquad \underline{Rb = 1.0\ M\Omega}$$

(2) Determining the Ra:

$$Ra = \frac{Rb}{\frac{V_5\ max}{V_{REG}} - 1} = \frac{1.0\ M\Omega}{\frac{-6.2\ V}{-3.1\ V} - 1} \qquad \underline{Ra = 1.0\ M\Omega}$$

According to the V_5 voltage and temperature change, equation ⑤ can be as follows (if V_{DD} = 0 V reference):

If Ta = 25°C:

V_5 max = $(1 + Rb/Ra) \cdot V_{REG}$
= $(1 + 1\ M\Omega/1\ M\Omega) \times (-3.1\ V)$
= –6.2 V

V_5 min = V_5 max + $Rb \cdot I_{REF}$
= $-6.2\ V + 1\ M\Omega \times (-2.4\ \mu A)$
= –8.6 V

If Ta = –10°C:

V_5 max = $(1 + Rb/Ra) \cdot V_{REG}$
= $(1 + 1\ M\Omega/1M\Omega) \times (-3.1\ V) \times \{1 + (-0.17\%/°C) \times (-10°C - 25°C)\}$
= –6.57 V

V_5 min = V_5 max + $Rb \cdot I_{REF}$
= $-6.57\ V + 1M\Omega \times \{-2.4\ \mu A + (0.022\ \mu A/°C) \times (-10°C - 25°C)\}$
= –8.20 V

If Ta = 50°C:

V_5 max = $(1 + Rb/Ra) \cdot V_{REG}$
= $(1 + 1\ M\Omega/1\ M\Omega) \times (-3.1\ V) \times \{1 + (-0.17\%/°C) \times (50°C - 25°C)\}$
= –5.94 V

V_5 min = V_5 max + $Rb \cdot I_{REF}$
= $-5.94\ V + 1M\Omega \times \{-2.4\ \mu A + (0.022\ \mu A/°C) \times (-50°C - 25°C)\}$
= –8.89 V

The margin must also be determined in the same procedure given above by considering the V_{REG} and I_{REF} variation. This margin calculation results show that the V_5 center value is affected by the V_{REG} and I_{REF} variation. The voltage setup width of the Electronic Volume Control depends on the I_{REF} variation. When the typical value of 0.2 V/step is set, for example, the maximum variation range of 0.12 to 0.28 V must be considered.

When the V_{REG} = Type 2, it so becomes that $V_{REG} = V_{SS}$ and there is no temperature gradient. However, I_{REF} carries the same temperature characteristics as with V_{REG} = Type 1.

Voltage generator for LCD (Voltage fullower)

The V_5 potential is divided using resistance within IC and V_1, V_2, V_3 and V_4 potentials are generated for LCD panel drive. These potentials are then converted in impedance by voltage follower, and sent to LCD driver circuit.

Because the LCD drive voltage has been fixed to each model, the display quality may drop in specific duty selected by Select Duty command. If it occurs, use an external power supply.

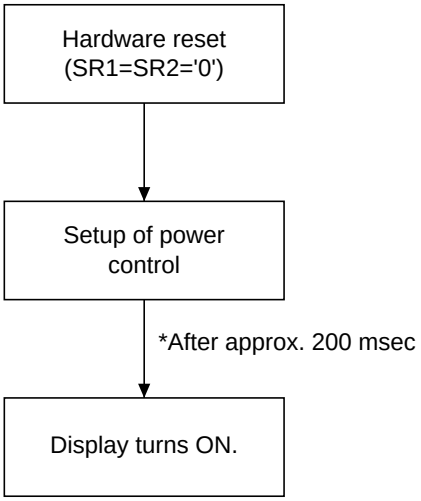
Model	LCD drive voltage
S1D15206 S1D15208	1/5 of bias voltage 1/7 of bias voltage

Subsection gives wiring examples and reference parts list when on-chip power supply is used and when not used.

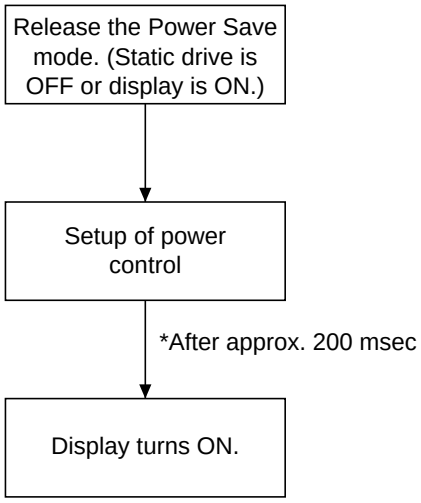
Command sequence for built-in power circuit startup

The built-in power circuit must follow the command sequence given below.

• To start the built-in power circuit when logic units are being powered:

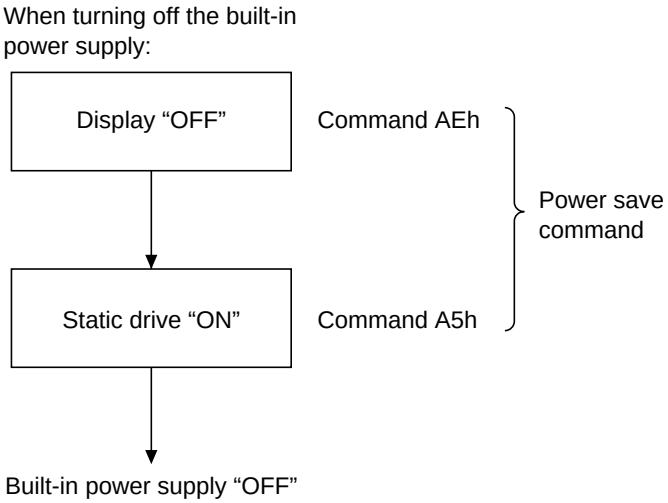


• To start the built-in power circuit after release of Power Save mode:



* When the Set Power Control command is issued, the V_{DD} level signal is output at both COM and SEG terminals for approximately 200 msec. Any other command can be entered during this period.

When turning off the built-in power circuit, observe the following command sequence to mainyain power save status.



* Precautions when installing the COG

When installing the COG, it is necessary to duly consider the fact that there exists a resistance of the ITO wiring occurring between the driver chip and the externally connected parts (such as capacitors and resistors). By the influence of this resistance, non-conformity may occur with the indications on the liquid crystal display.
Therefore, when installing the COG design the module paying sufficient considerations to the following three points.

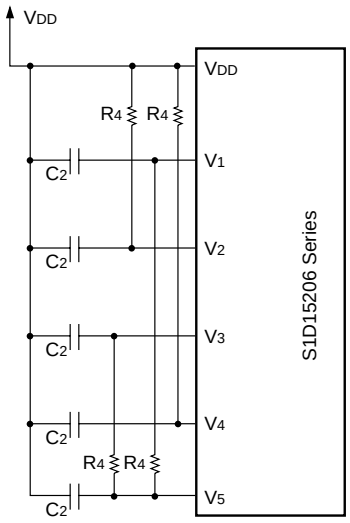
1. Suppress the resistance occurring between the driver chip pin to the externally connected parts as much as possible.
2. Suppress the resistance connecting to the power supply pin of the driver chip.
3. Make various COG module samples with different ITO sheet resistance to select the module with the sheet resistance with sufficient operation margin.

Also, as for this driver IC, pay sufficient attention to the following points when connecting to external parts for the characteristics of the circuit.

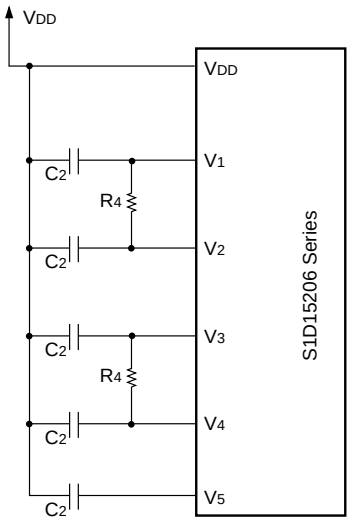
1. Connection to the boosting capacitors The boosting capacitors (the capacitors connecting to respective CAP pins and capacitor being inserted between V_{OUT} and V_{SS2}) of this IC are being switched over by use of the transistor with very low ON-resistance of about 10Ω. However, when installing the COG, the resistance of ITO wiring is being inserted in series with the switching transistor, thus dominating the boosting ability. Consequently, the boosting ability will be hindered as a result and pay sufficient attention to the wiring to respective boosting capacitors.
2. Connection of the smoothing capacitors for the liquid crystal drive
   The smoothing capacitors for the liquid crystal driving potentials (V_1. V_2, V_3 and V_4) are indispensable for liquid crystal drives not only for the purpose of mere stabilization of the voltage levels. If the ITO wiring resistance which occurs pursuant to installation of the COG is supplemented to these smoothing capacitors, the liquid crystal driving potentials become unstable to cause non-conformity with the indications of the liquid crystal display. Therefore, when using the COG module, we definitely recommend to connect reinforcing resistors externally. Reference value of the resistance is 100kΩ to 1MΩ.
   Meanwhile, because of the existence of these reinforcing resistors, current consumption will increase.

Indicated below is an exemplary connection diagram of external resistors.
Please make sufficient evaluation work for the display statuses with any connection tests.

Exemplary connection diagram 1.



Exemplary connection diagram 2.



Reset Circuit

The S1D15206 series chip parameters are initialized when both SR1 and SR2 are set to low.

○ **Initial parameter setup**

1. Display : Off
2. Duty cycle : 1/16 (S1D15206)
3. ADC select : Normal (D0 ADC command is high and ADC status flag is set)
4. Read-modify-write : Off
5. Power Control register : 0
6. Initial Display Line register : Line 1
7. Column Address counter : Address 0
8. Page Address register : Page 0
9. Register data of serial interface : Cleared
10. Electronic control register : 0
11. Static drive : Off
12. Clock : Output

As explained in Section 4-32, the microprocessor should also be reset when SR1 and SR2 are reset. The SR1 and SR2 go low only when logical low pulses are entered at least 10 microseconds (refer to Section for AC characteristics). The normal reset signal appears 1 microsecond after the rising edge of this signal.

If the on-board LCD power circuit of the S1D15206 series is not used, both SR1 and SR2 must be low when an external LCD power is supplied. If not low, the IC chip may be destroyed by surge current. When reset, each register is cleared but the present setup of oscillator circuit and output terminals (FR, CL, D0 to D7) is not cleared.

As the S1D15206 series does not have a Power-On Clear circuit, both SR1 and SR2 must go low when logic power applies. If not, any recovery may fail.

The Reset command can reset parameters 6 to 10 listed above.

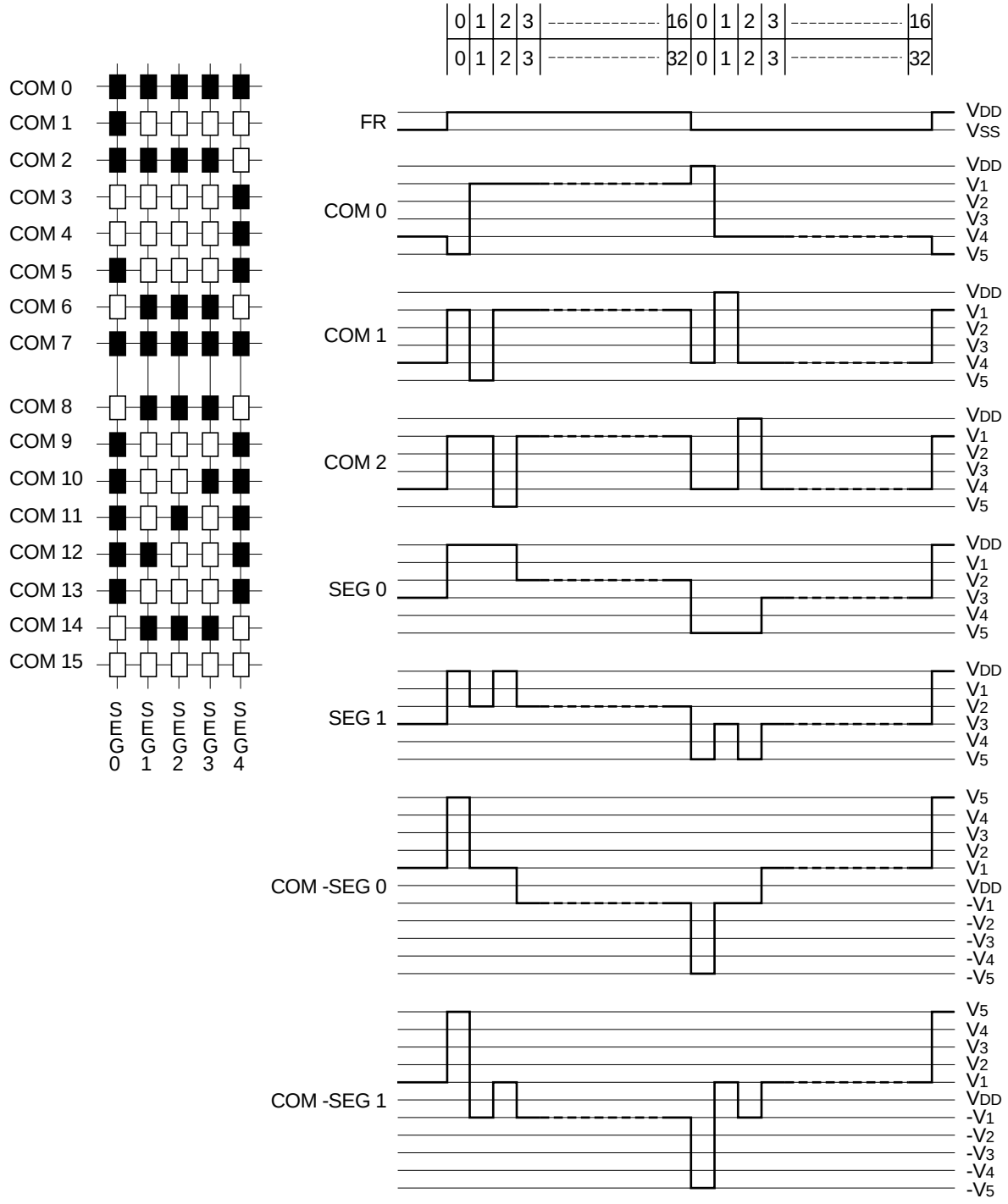


Figure 6

7. COMMANDS

Page 4–21 lists available commands. The S1D15206 series uses a combination of A0, $\overline{RD}$ and $\overline{WR}$ (or R/$\overline{W}$) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only (any external clock is required), its processing speed is very HIGH and its busy check is usually not required.

(1) Display ON/OFF
Alternatively turns the display on and off.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

The display turns off when D goes low, and it turns on when D goes HIGH.

(2) Initial Display Line
Specifies line address (refer to Figure 4) to determine the initial display line, or COM0. The RAM display data becomes the top line of LCD screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the line address, the smooth scrolling or page change takes place.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	1	0	A4	A3	A2	A1	A0

← HIGH-order bit

A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
		:			:
1	1	1	1	0	3 0
1	1	1	1	1	3 1

(3) Set Page Address
Specifies page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed. Page address 4 is the display RAM area dedicate to the indicator, and only D0 is valid for data change.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	1	1	A2	A1	A0

A2	A1	A0	Page Address
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4

(4) Set Column Address
Specifies column address of display RAM. When the microprocessor repeats to access to the display RAM, the column address counter is incremented by 1 during each access until address 80 is accessed. The page address is not changed during this time.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	0	A6	A5	A4	A3	A2	A1	A0

A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				:
1	0	0	1	1	1	1	7 9

(5) Read Status

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	PS	0	0	0

BUSY: When high, the S1D15206 series is busy due to internal operation or reset. Any command is rejected until BUSY goes LOW. The busy check is not required if enough time is provided for each cycle.

ADC: Indicates the relationship between RAM column address and segment drivers. When LOW, the display is normal and column address "79-n" corresponds to segment driver n. When HIGH, the display is reversed and column address n corresponds to segment driver n.

ON/OFF: Indicates whether the display is on or off. When goes low, the display turns on. When goes HIGH, the display turns off. This is the opposite of Display ON/OFF command.

RESET: Indicates the initialization is in progress by SR1 and SR2 to go LOW or by Reset command. When LOW, the display is on. When HIGH, the chip is being reset.

PS: When LOW, LCD panel is in Power Save mode.

(6) Write Display Data
Writes 8-bit data in display RAM. As the column address is incremented by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
1	1	0	Write data							

(7) Read Display Data
Reads 8-bit data from display RAM area specified by column address and page address. As the column address is incremented by 1 automatically after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
1	0	1	Read data							

(8) ADC Select
Changes the relationship between RAM column address and segment driver. The order of segment driver output pins can be reversed by software. This allows flexible IC layout during LCD module assembly. For details, refer to the column address section of Figure 4. When display data is written or read, the column address is incremented by 1 as shown in Figure 4.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

When D is low, the right rotation (normal direction). When D is HIGH, the left rotation (reverse direction).

(9) Static Drive ON/OFF

Forcibly turns the entire display ON and makes all common outputs selectable regardless of RAM data contents. The RAM data is held.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

When D goes LOW, the static drive turns off. When D goes HIGH, the static drive turns on.

The LCD panel enters Power Save mode if Static Drive ON command is issued when the display is off. Refer to the Power Save section for details.

(10) Select Duty

Selects the LCD driver duty. However, the bias of LCD driver voltage is fixed when on-chip power circuit is used (refer to Subsection).

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	D

Model	D	Duty
S1D15206	0	1/8
	1	1/16
S1D15208	0	1/32
	1	1/32

(11) Duty+1

Increments the duty by 1. If 1/8 duty is set for the S1D15206, for example, it is incremented to 1/9 duty. If 1/16 duty is set, it is incremented to 1/17 duty. The COMS terminal functions as COM8 or COM16. The display line of RAM area corresponding to page address 4, or D0, is always accessed.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	1	D

Model	D	Duty
S1D15206	0	1/8 or 1/16
	1	1/9 or 1/17
S1D15208	0	1/32
	1	1/33

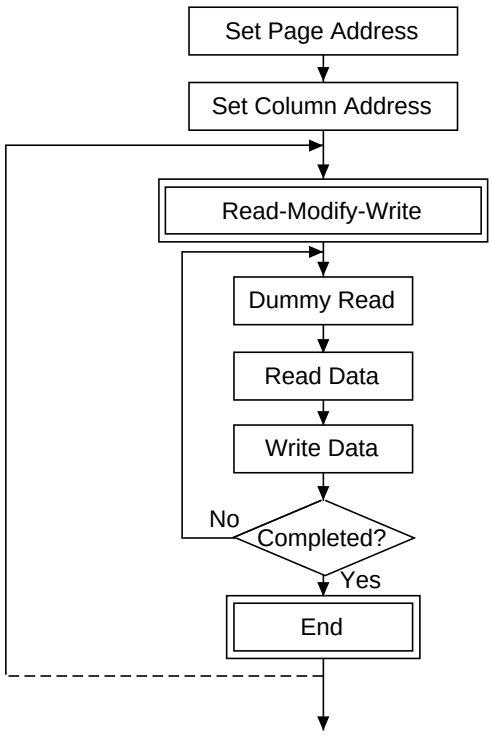
(12) Read-Modify-Write

A pair of Read-Modify-Write and End commands must always be used. Once Read-Modify-Write is issued, column address is not incremented by Read Display Data command but incremented by Write Display Data command only. It continues until End command is issued. When the End is issued, column address returns to the address when Read-Modify-Write was issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Note: Any command except Read/Write Display Data and Set Column Address can be issued during Read-Modify-Write mode.

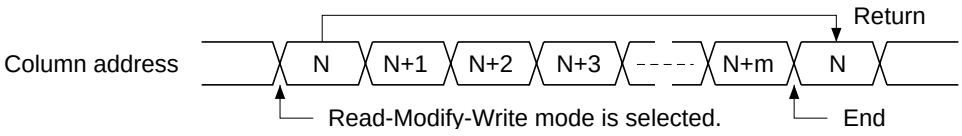
• Cursor display sequence



(13) End

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write was issued).

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



(14) Reset

Resets the Initial Display Line register, Column Address counter, Page Address register, register data of serial interface, and Electronic Control register to their initial status. The Reset command does not affect on the contents of display RAM. Refer to the Reset circuit section of FUNCTIONAL DESCRIPTION.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The Reset command cannot initialize LCD power supply. Only RES (that sets SR1 and SR2 to low) can initialize the supplies.

(15) Set Power Control

Selects one of eight power circuit functions using 3-bit register. An external power supply and part of on-chip power supply functions can be used simultaneously. Refer to Power Circuit section of FUNCTIONAL DESCRIPTION for details.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	1	0	D2	D1	D0

When D0 goes LOW, voltage follower turns off. When D0 goes HIGH, it turns on.
When D1 goes LOW, voltage regulator turns off. When D1 goes HIGH, it turns on.
When D2 goes LOW, voltage booster turns off. When D2 goes HIGH, it turns on.

(16) Set Electronic Control

Adjusts the contrast of LCD panel display by changing V_5 LCD drive voltage that is output by voltage regulator of on-chip power supply.

This command selects one of 32 V_5 LCD drive voltages by storing data in 5-bit register. The V_5 voltage adjusting range should be determined depending on the external resistance. Refer to the Voltage Regulator Circuit section of FUNCTIONAL DESCRIPTION for details.

This command is valid only when voltage regulator circuit is turned on by Set Power Control command.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	0	D4	D3	D2	D1	D0

D4	D3	D2	D1	D0	| V_5 |
0	0	0	0	0	Low
0	0	0	0	1	
0	0	0	1	0	
		↓			↓
1	1	1	0	1	
1	1	1	1	0	
1	1	1	1	1	High

Set register to (D4,D3,D2,D1,D0)=(0,0,0,0,0) to suppress electronic control function.

(17) Clock Stop

Stops clock output at CL to reduce current consumption.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	1	1	D

Clock outputs when D is low, but clock stops when D is high.

(18) Power Save (a combination with Static Drive command)

Sets LCD panel in power save mode if Static Drive ON is issued when the display is off. Power consumption drops power consumption level.

When LCD panel enters Power Save mode:

(a) Both oscillator and power supply stop.
(b) LCD driver stops, and segment and common driver have V_{DD} level output.
(c) External clock input is disabled, and clock output is set to low (at CL).
(d) Both display data and operation mode before issue of Power Save are held.
(As the power control register is cleared, the Set Power Control command must be issued again after the Power Save mode has been released.)
(e) All LCD driver voltages are fixed to V_{DD}.

The Power Save is released when the display is turned on or when Static Drive OFF is issued. If external voltage driver resistors are used to supply voltage to LCD panel, current passing through resistors must be cut off. An external power supply must be turned off if used; its voltage must be fixed to floating or V_{DD} level.

* When the S1D15206 series is operating, the internal status data set by commands is held. However, the internal status may change due to an excessive ambient noise. The package and system noise generation must be suppressed or a noise protection design must be considered.
We recommend to periodically refresh the internal status data to prevent a spike noise and other interference.

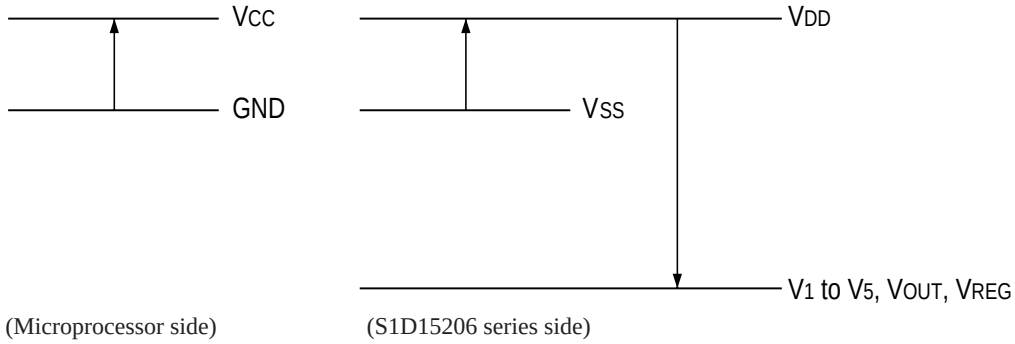
S1D15206 Series Command Table

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	Turns on LCD panel when goes HIGH, and turns off when goes LOW.
(2) Initial Display Line	0	1	0	1	1	0	Initial display address					Specifies RAM display line for COM0.
(3) Set Page Address	0	1	0	1	0	1	1	1	Page address			Sets the display RAM page in Page Address register.
(4) Set Column Address	0	1	0	0	Column address							Sets RAM column address in Column register.
(5) Read Status	0	0	1	Status					0	0	0	Reads the status information.
(6) Write Display Data	1	1	0	Write data								Writes data in display RAM.
(7) Read Display Data	1	0	1	Read data								Reads data from display RAM.
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Sets normal relationship between RAM column address and segment driver when low, but reverses the relationship when HIGH.
(9) Static Drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Normal indication when LOW, but full indication when HIGH.
(10) Duty Select	0	1	0	1	0	1	0	1	0	0	0 1	Selects LCD driver duty of 1/8 (1/16) when LOW and 1/16 (1/32) when HIGH.
(11) Duty+1	0	1	0	1	0	1	0	1	0	1	0 1	Selects normal LCD driver duty when LOW, and selects the duty added by 1 when HIGH.
(12) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Increments Column Address counter during each write when HIGH and during each read when LOW.
(13) End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read-Modify-Write.
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Resets internal functions.
(15) Set Power Control	0	1	0	1	0	1	1	0	Power control			Selects various power circuit functions.
(16) Set Electronic Control	0	1	0	1	0	0	Electronic control value					Sets V_5 output voltage to Electronic Control register.
(17) Clock Stop	0	1	0	1	1	1	0	0	1	1	0 1	Stops clock output at CL when LOW, and stops clock when HIGH.
(18) Power Save	–	–	–	–	–	–	–	–	–	–	–	A combination of Display OFF and Static Drive ON commands.

Note: Do not use any other command, or the system malfunction may result.

8. ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Supply voltage range		V_{DD}	–0.3 to +7.0	V
	Triple voltage conversion	V_{DD}	–0.3 to +6.0	
Driver supply voltage range (1)		V5	–18.0 to +0.3	V
Driver supply voltage range (2)		V1, V2, V3, V4	V5 to +0.3	V
Input voltage range		V_{IN}	–0.3 to V_{DD}+0.3	V
Output voltage range		VO	–0.3 to V_{DD}+0.3	V
Allowable loss		P_D	250	mW
Operating temperature range		T_{OPR}	–40 to +85	°C
Storage temperature range	QFP • TCP	T_{STG}	–65 to +150	°C
	Bear chip		–55 to +125	
Soldering temperature and time		T_{SOLDER}	260-10 (at leads)	°C•sec



Notes: 1. V_1 to V_5, V_{OUT}, and V_{REG} voltages are based on V_{DD}=0 V.
2. Voltages $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ $V_{SS} \geq V_{OUT}$ must always be satisfied.
3. If an LSI exceeds its absolute maximum rating, it may be damaged permanently. It is desirable to use it under electrical characteristics conditions during general operation. Otherwise, an LSI malfunction or reduced LSI reliability may result.
4. The moisture resistance of the flat package may drop during soldering. Take care not to excessively heat the package resin during chip mounting.

9. ELECTRICAL CHARACTERISTICS

DC Characteristics

V_{DD} = 5 V ±10%, V_{SS} = 0 V, Ta = –40 to +85°C unless otherwise noted.

Item			Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Power voltage (1)		Operational	V_{DD}		2.4		6.0	V	V_{DD} *1
Operating voltage (2)		Operational	V_5		–13.0		–4.0	V	V_5 *2
		Operational	V_1, V_2		$0.6 \times V_5$		V_{DD}	V	V_1, V_2
		Operational	V_3, V_4		V_5		$0.4 \times V_5$	V	V_3, V_4
CMOS	HIGH-level input voltage		V_{IHC}		$0.7 \times V_{DD}$		V_{DD}	V	*3
				V_{DD} = 2.7 V	$0.8 \times V_{DD}$		V_{DD}		
	LOW-level input voltage		V_{ILC}		V_{SS}		$0.3 \times V_{DD}$	V	*3
				V_{DD} = 2.7 V	V_{SS}		$0.2 \times V_{DD}$		
	HIGH-level output voltage		V_{OHC}	I_{OH} = –1 mA	$0.8 \times V_{DD}$		V_{DD}	V	*4
				V_{DD} = 2.7 V, I_{OH} = –0.5 mA	$0.8 \times V_{DD}$		V_{DD}		
	LOW-level output voltage		V_{OLC}	I_{OH} = 1 mA	V_{SS}		$0.2 \times V_{DD}$	V	*4
				V_{DD} = 2.7 V, I_{OL} = 0.5 mA	V_{SS}		$0.2 \times V_{DD}$		
Schmitt	HIGH-level input voltage		V_{IHS}		$0.4 \times V_{DD}$		$0.8 \times V_{DD}$	V	*5
				V_{DD} = 2.7 V	$0.4 \times V_{DD}$		$0.8 \times V_{DD}$		
	LOW-level input voltage		V_{ILS}		$0.2 \times V_{DD}$		$0.6 \times V_{DD}$	V	*5
				V_{DD} = 2.7 V	$0.2 \times V_{DD}$		$0.6 \times V_{DD}$		
Input leakage current			I_{LI}		–1.0		1.0	µA	*6
Output leakage current			I_{LO}		–3.0		3.0	µA	*7
LCD driver ON resistance			R_{ON}	Ta = 25°C V_5 = –0.5 V		15.0	30.0	KΩ	SEG0 to 79 COS0 to 15 COMS *9
Static current consumption			I_{DDQ}	$\overline{CS}$ = C_L = V_{DD}		0.05	3.0	µA	V_{DD}
Input pin capacity			C_{IN}	Ta = 25°C, f = 1 MHz		5.0	8.0	pF	Input pins
CL output frequency			f_{CL}	Ta = 25°C, V_{DD} = 2.7 to 5 V	2.4	2.9	3.7	kHz	*8 Applies to the S1D15206⁎10⁎⁎, S1D15208⁎10⁎⁎
					4.8	5.8	7.4		

Dynamic current consumption (1) when the built-in power supply is OFF

1.7 times of normal products apply to f_{CL} = 5.8 kHz products of S1D15206F11⁎⁎ and S1D15208F11⁎⁎ . Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
S1D15206	I_{DD} (1)	V_{DD} = 5.0V, V_5–V_{DD} = –6.0V	–	9.1	18	µA	*12
		V_{DD} = 3.0V, V_5–V_{DD} = –6.0V	–	12.0	24		
S1D15208		V_{DD} = 5.0V, V_5–V_{DD} = –8.0V	–	7.5	15		
		V_{DD} = 3.0V, V_5–V_{DD} = –8.0V	–	9.5	19		

Dynamic current consumption (2) when the built-in power supply is ON (Display all white)

1.7 times of normal products apply to f_{CL} = 5.8 kHz products of S1D15206F11** and S1D15208F11**. Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
S1D15206	I_{DD} (2)	V_{DD} = 5.0V, V_5–V_{DD} = –6.0V, dual boosting	–	31	62	µA	*13
		V_{DD} = 3.0V, V_5–V_{DD} = –6.0V, triple boosting	–	44	88		
S1D15208		V_{DD} = 5.0V, V_5–V_{DD} = –8.0V, dual boosting	–	37	74		
		V_{DD} = 3.0V, V_5–V_{DD} = –8.0V, triple boosting	–	55	110		

Dynamic current consumption (2) when the built-in power supply is ON (Display checker pattern)

1.7 times of normal products apply to f_{CL} = 5.8 kHz products of S1D15206F11** and S1D15208F11**. Ta = 25°C

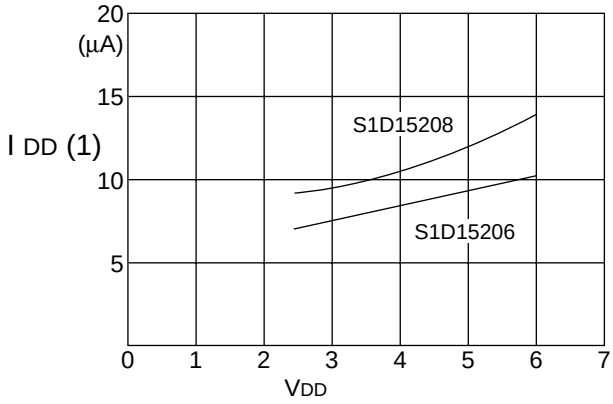
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
S1D15206	I_{DD} (2)	V_{DD} = 5.0V, V_5–V_{DD} = –6.0V, dual boosting	–	34	68	µA	*13
		V_{DD} = 3.0V, V_5–V_{DD} = –6.0V, triple boosting	–	46	92		
S1D15208		V_{DD} = 5.0V, V_5–V_{DD} = –8.0V, dual boosting	–	42	84		
		V_{DD} = 3.0V, V_5–V_{DD} = –8.0V, triple boosting	–	60	120		

Current consumption during Power Save mode V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Power save mode	I_{DDS1}	S1D15206, S1D15208	—	3	6	µA	—

Typical current consumption characteristics (reference data)

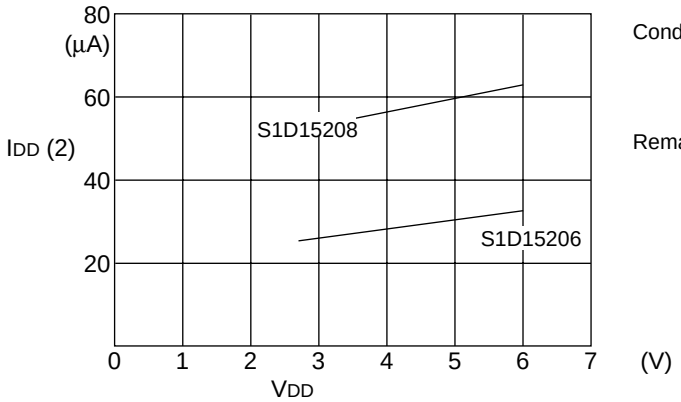
- Dynamic current consumption (1) when LCD external power mode lamp is ON



Conditions: The built-in power supply is OFF and an external power supply is used.
S1D15206 V_5-V_{DD}=–6.0V
S1D15208 V_5-V_{DD}=–8.0V
Ta=25°C

Remarks: *12
1.7 times of normal products apply to f_{CL} = 5.8 kHz products of S1D15206F11** and S1D15208F11**.

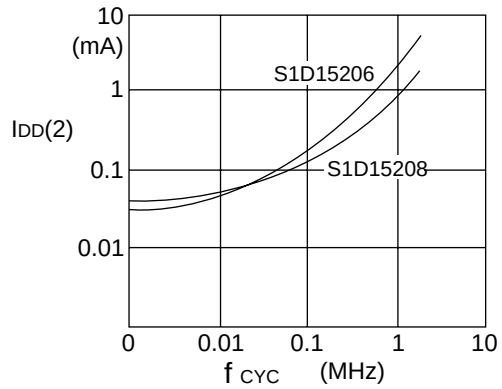
- Dynamic current consumption (2) when the LCD built-in power supply lamp is ON



Conditions: The built-in power supply is ON.
S1D15206 V_5-V_{DD}=–6.0V dual boosting
S1D15208 V_5-V_{DD}=–8.0V triple boosting
Ta=25°C

Remarks: *13
1.7 times of normal products apply to f_{CL} = 5.8 kHz products of S1D15206F11** and S1D15208F11**.

- Current consumption I_{DD} during access (2) during MPU access cycle



It shows the current consumption when a checker pattern is always written in fSYNC timing.
When not accessed, only the current consumption of IDD (2) occurs.

Conditions: S1D15206 $V_5 - V_{DD}$ = –6.0 V, dual boosting
S1D15208 $V_5 - V_{DD}$ = –8.0 V, triple boosting
Ta = 25°C

	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Pins used
Built-in power circuit	Input voltage	V_{DD}	—	2.4	—	6.0	V	*10
	Booster output voltage	V_{OUT}	V_{DD} reference (during triple boosting)	–16.5	—	—	V	V_{OUT}
	Voltage regulator circuit operating voltage	V_{OUT}	V_{DD} reference	–16.5	—	–4.0	V	V_{OUT}
	Voltage follower operating voltage	V_5	V_{DD} reference	–13.0	—	–4.0	V	*11
	Reference voltage	V_{REG}	V_{DD} reference Ta = 25°C	–3.5	–3.1	–2.7	V	V_R

* See notes below.

*1 Although the wide range of operating voltage is guaranteed, a spike voltage change during access to the MPU is not guaranteed.
*2 The operating voltage range of the V_{DD} and V_5 systems (See Figure 9.)
The operating voltage range is applied if an external power supply is used.
*3 Pins D0 to D5, A0, $\overline{CS1}$, CS2, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), M/S, CL, and FR
*4 Pins D0 to D7, FR, and CL
*5 Pins SI (D7), SCL (D6), SR1, and SR2
*6 Pins A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, M/S, SR1, and SR2
*7 Applied if pins D0 to D7, FR, and CL are high impedance.
*8 For the relationship between CL output frequency and frames, see Figure 7.
For the relationship between CL output frequency and power voltage, see Figure 8.
For the relationship between CL output frequency and temperature, see Figure 11.
*9 The resistance when the 0.1-volt voltage is applied between the SEG and COM output terminals and each power terminal (V_1, V_2, V_3 or V_4). It must be within operating voltage (2).
RON = 0.1 V/ΔI
where, ΔI is the current that flows between power supply and SEG or COM terminal when the 0.1-volt voltage is applied.
*10 If the triple voltage by the built-in power circuit are used the V_{DD} primary power must be used within the input voltage range.
*11 The V_5 voltage can be adjusted within the voltage follower operating range by use of voltage regulator.
*12 Applied if the built-in oscillation circuit is used and if not accessed by the MPU.
*13 Applied if the built-in oscillation circuit and the built-in power circuit are used, and if not accessed by the MPU.
The current flowing through the voltage regulator resistors (R1, R2 and R3) is not included.
When the built-in voltage booster is used, the current consumption for the V_{DD} power supply is shown.

- Relationship between CL output frequency and frames (S1D15206 series)

The relationship between CL output frequency (f_{CL}) and frame frequency (f_F) can be determined as follows:

	Duty	f_F
S1D15206	1/9 1/17	8 • FOSC/288 8 • fOSC/272
S1D15208	1/33	8 • fOSC/264

Figure 7

("f_F" indicates the LCD current alternating cycle, but not the cycle of f F signals.)

- Relationship between CL output frequency and power voltage

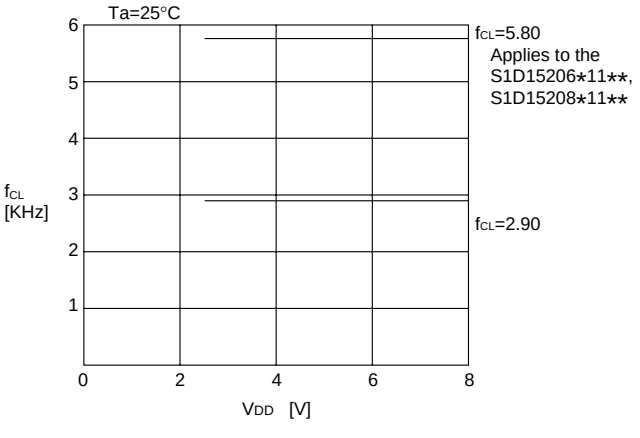
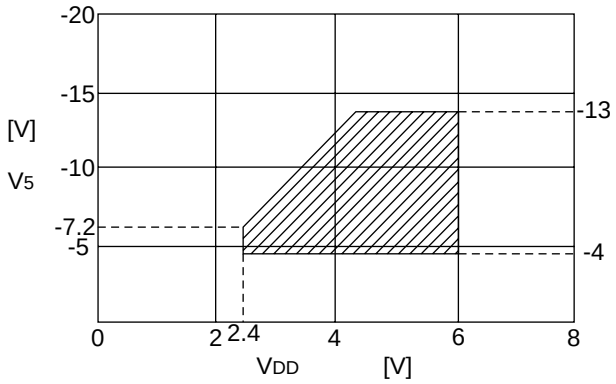
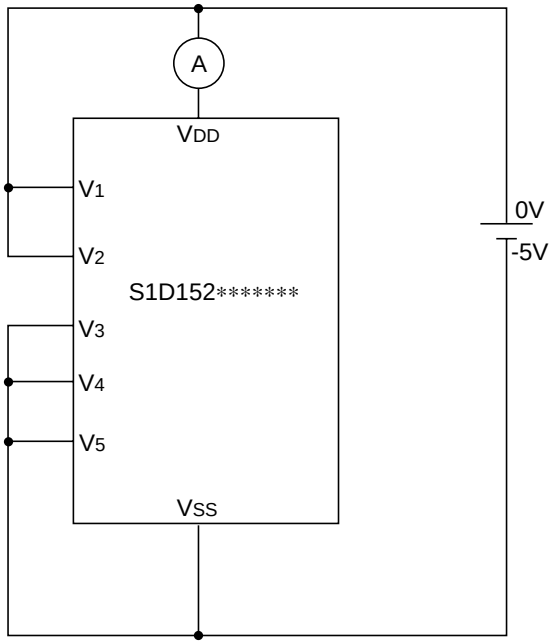


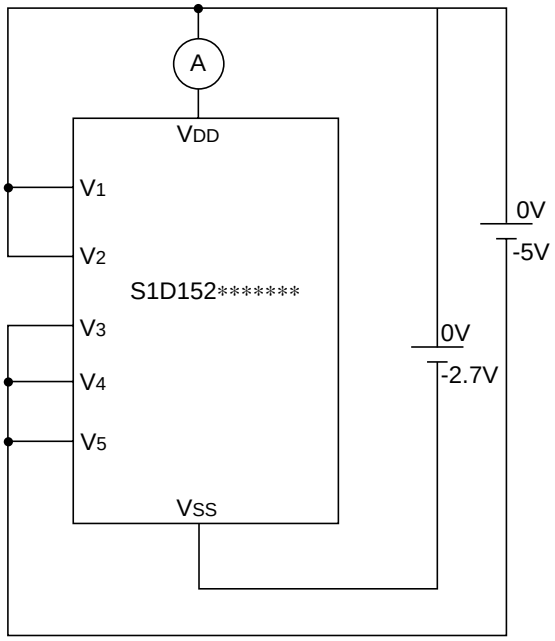
Figure 8

- Operating voltage range on V_{DD} and V_5

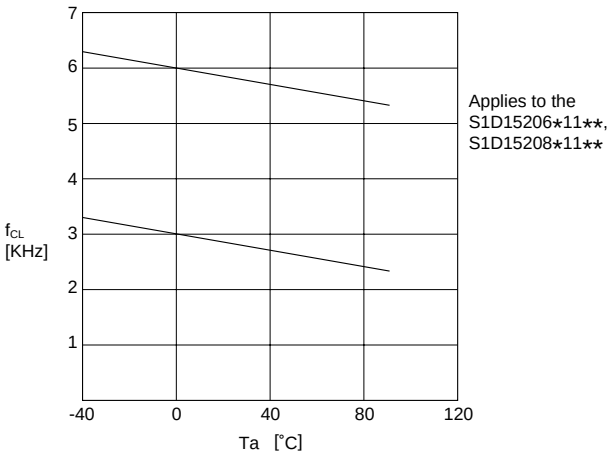


- I_{DD} measuring circuits





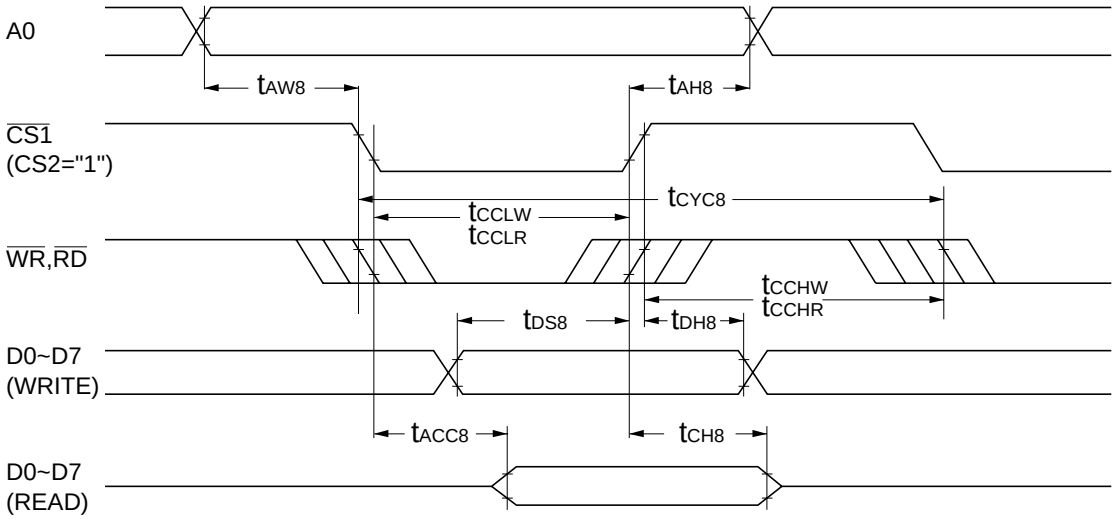
- Relationship between CL output frequency and temperature



AC Characteristics

(1) System buses

Read/write characteristics I (8080-series microprocessor)



V_{SS} = 0 V, V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time Address setup time	A0	t_{AH8} t_{AW8}		5 5		ns ns
System cycle time		t_{CYC8}		400		ns
Control LOW pulse width ($\overline{WR}$) Control LOW pulse width ($\overline{RD}$) Control HIGH pulse width ($\overline{WR}$) Control HIGH pulse width ($\overline{RD}$)	$\overline{WR}$ $\overline{RD}$ $\overline{WR}$ $\overline{RD}$	t_{CCLW} t_{CCLR} t_{CCHW} t_{CCHR}		100 75 145 145		
Data setup time Data hold time		t_{DS8} t_{DH8}		80 10		ns ns
$\overline{RD}$ access time Output disable time	D0 to D7	t_{ACC8} t_{CH8}	CL=100pF	 10	80 60	ns ns

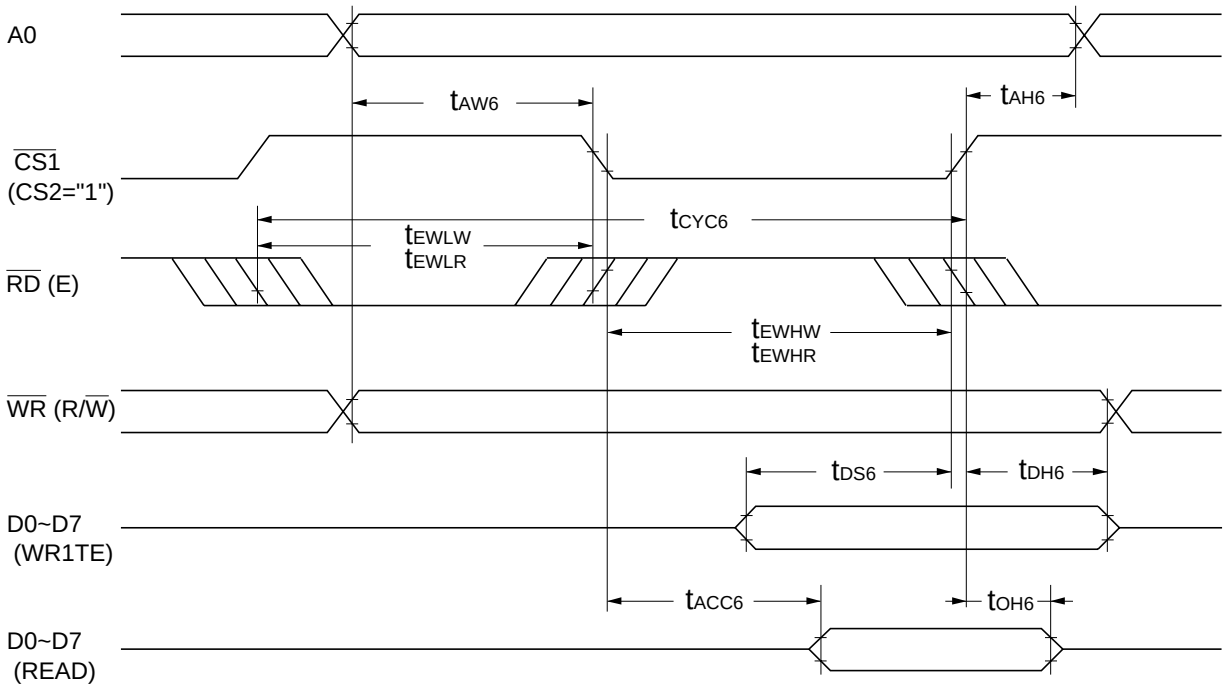
V_{SS} = 0 V, V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time Address setup time	A0	t_{AH8} t_{AW8}		10 10		ns ns
System cycle time		t_{CYC8}		800		ns
Control LOW pulse width ($\overline{WR}$) Control LOW pulse width ($\overline{RD}$) Control HIGH pulse width ($\overline{WR}$) Control HIGH pulse width ($\overline{RD}$)	$\overline{WR}$ $\overline{RD}$ $\overline{WR}$ $\overline{RD}$	t_{CCLW} t_{CCLR} t_{CCHW} t_{CCHR}		185 185 285 285		 ns ns
Data setup time Data hold time		t_{DS8} t_{DH8}		160 20		ns ns
$\overline{RD}$ access time Output disable time	D0 to D7	t_{ACC8} t_{CH8}	CL=100pF	 20	180 120	ns ns

Notes: 1. t_{CCLW} and t_{CCLR} are limited depending on the overlap time of $\overline{CS1}$ LOW (CS2 HIGH) and $\overline{WR}$ or $\overline{RD}$ LOW.
2. The input signal rise and fall times must be within 15 nanoseconds.
3. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

(2) System buses

Read/write characteristics II (6800-series microprocessor)



V_{SS} = 0 V, V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

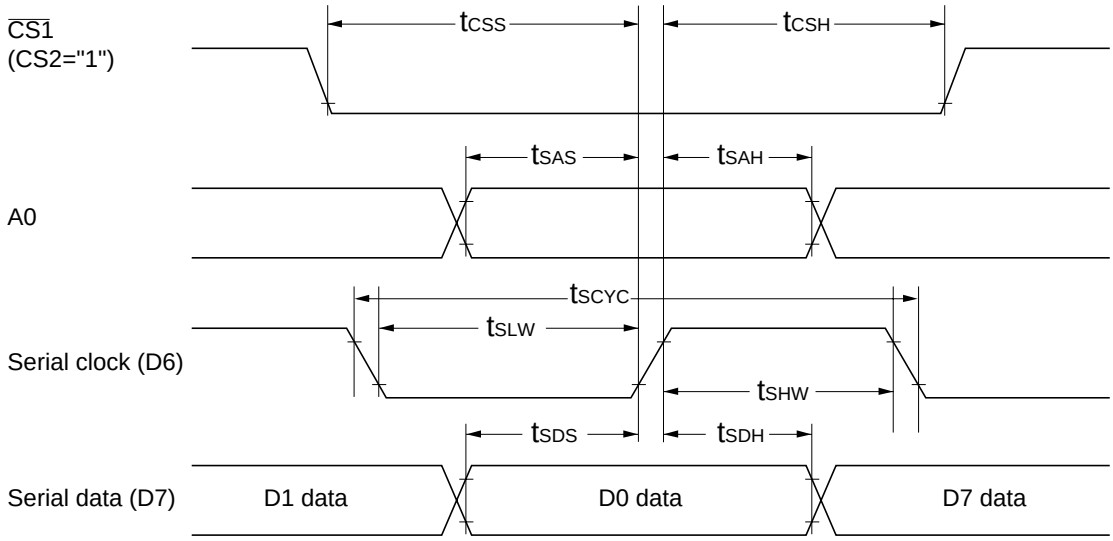
Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time			t_{CYC6}		400		ns
Address setup time Address hold time		$\overline{WR}$ (R/$\overline{W}$) A0	t_{AW6} t_{AH6}		20 10		ns ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		80 10		ns ns
Output disable time Access time			t_{OH6} t_{ACC6}	CL=100pF	10	60 90	ns ns
Enable	READ	$\overline{RD}$ (E)	t_{EWLR}		85		ns
LOW pulse width	WRITE		t_{EWLW}		75		ns
Enable	READ	$\overline{RD}$ (E)	t_{EWHR}		135		ns
HIGH pulse width	WRITE		t_{EWHW}		145		ns

V_{SS} = 0 V, V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C

Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time			t_{CYC6}		800		ns
Address setup time Address hold time		$\overline{WR}$ (R/$\overline{W}$) A0	t_{AW6} t_{AH6}		40 20		ns ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		160 20		ns ns
Output disable time Access time			t_{OH6} t_{ACC6}	CL=100pF	20	120 180	ns ns
Enable	READ	$\overline{RD}$ (E)	t_{EWLR}		185		ns
LOW pulse width	WRITE		t_{EWLW}		145		ns
Enable	READ	$\overline{RD}$ (E)	t_{EWHR}		285		ns
HIGH pulse width	WRITE		t_{EWHW}		325		ns

Notes: 1. t_{EWHR} and t_{EWHW} are limited depending on the overlap time of $\overline{CS1}$ LOW (CS2 high) and $\overline{RD}$ (E) HIGH.
2. The input signal rise and fall times must be within 15 nanoseconds.
3. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

(3) Serial interface



V_{SS} = 0 V, V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

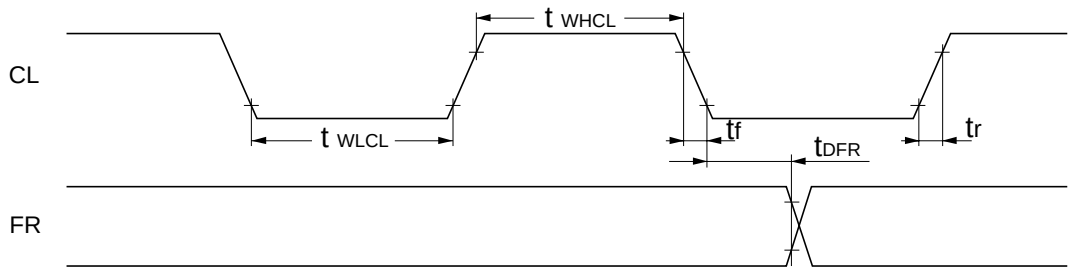
Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle	Serial clock	t_{SCYC}		500		ns
Serial clock HIGH pulse width		t_{SHW}		150		ns
Serial clock LOW pulse width		t_{SLW}		150		ns
Address setup time	A0	t_{SAS}		120		ns
Address hold time		t_{SAH}		200		ns
Data setup time	Serial data	t_{SDS}		120		ns
Data hold time		t_{SDH}		120		ns
$\overline{CS}$ serial clock time	$\overline{CS1}$ (CS2="1")	t_{CSS}		80		ns
		t_{CSH}		400		ns

V_{SS} = 0 V, V_{DD} = 2.7 to 4.5V, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle	Serial clock	t_{SCYC}		1000		ns
Serial clock HIGH pulse width		t_{SHW}		300		ns
Serial clock LOW pulse width		t_{SLW}		300		ns
Address setup time	A0	t_{SAS}		250		ns
Address hold time		t_{SAH}		400		ns
Data setup time	Serial data	t_{SDS}		250		ns
Data hold time		t_{SDH}		250		ns
$\overline{CS}$ serial clock time	$\overline{CS1}$ (CS2="1")	t_{CSS}		160		ns
		t_{CSH}		800		ns

Notes: 1. The input signal rise and fall times must be within 15 nanoseconds.
2. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

(4) Display control timing



V_{SS} = 0 V, V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
LOW level pulse width	CL	t_{WLCL}		35			µs
HIGH level pulse width		t_{WHCL}		35			µs
Rise time		tr			30	120	ns
Fall time		tf			30	120	ns
FR delay time	FR	t_{DFR}		–1.0	0.2	1.0	µs

V_{SS} = 0 V, V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
LOW level pulse width	CL	t_{WLCL}		70			µs
HIGH level pulse width		t_{WHCL}		70			µs
Rise time		tr			60	240	ns
Fall time		tf			60	240	ns
FR delay time	FR	t_{DFR}		–2.0	0.4	2.0	µs

Output timing

V_{SS} = 0 V, V_{DD} = 5.0 V ±10%,Ta = –40 to +85°C

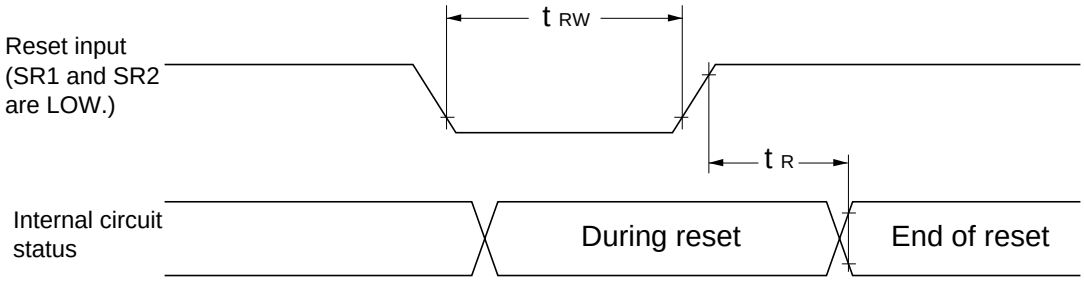
Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
FR delay time	FR	t_{DFR}	CL=100pF		0.2	0.4	µs

V_{SS} = 0 V, V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
FR delay time	FR	t_{DFR}	CL=100pF		0.4	0.8	µs

Notes: 1. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

(5) Reset timing



V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_R		1.0			µs
Reset LOW pulse width	Reset input	t_{RW}		10			µs

V_{DD} = 2.7 V ±10%, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_R		3.0			µs
Reset LOW pulse width	Reset input	t_{RW}		30			µs

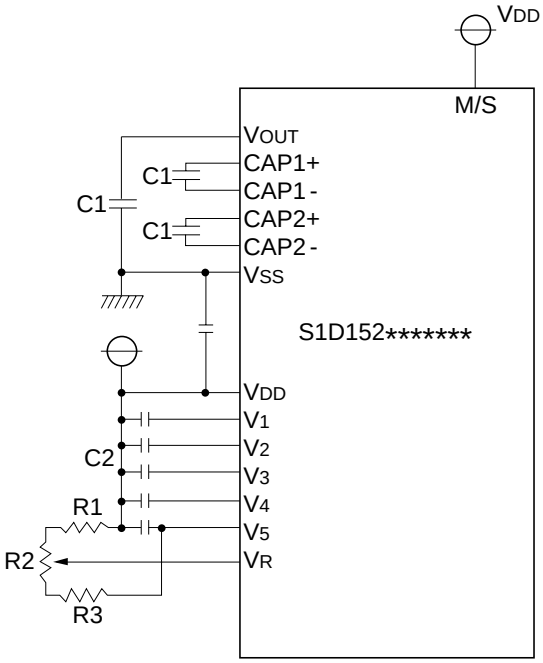
Notes: 1. t_R (reset time) represents the period from rising edge of reset input to end of internal circuit reset. The S1D15206 series can operate normally after t_R.
2. t_{RW} specifies the minimum pulse width of reset input. The low pulse exceeding t_{RW} is required for reset.
3. The input signal rise and fall times must be within 15 nanoseconds.
4. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

10. EXTERNAL WIRINGS

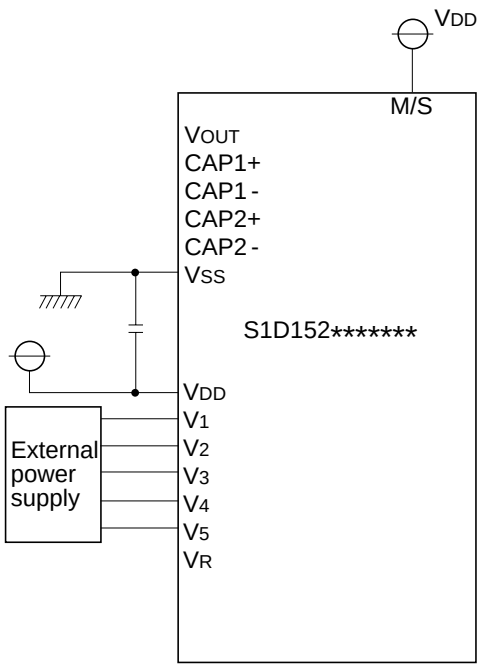
Power Supply and LCD Power Circuit

If a single S1D15206 series chip is used and if on-board power supply is used and not used

If on-chip power supply is used



If on-chip power supply is NOT used

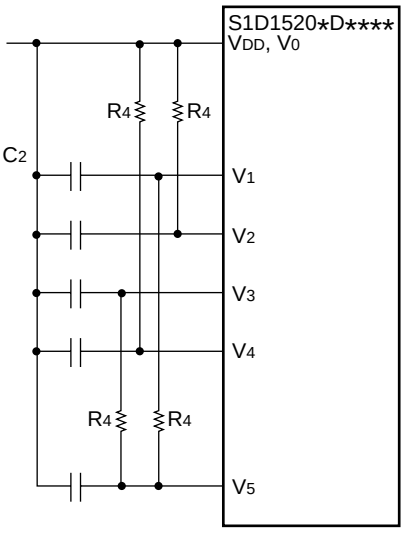


Parts list (Reference)

Variable V_5 ≒ –9.3 to –6.2 V

C 1	0.1 to 1 µF
C 2	0.1 to 1 µF
R 1	2.0 MΩ
R 1	1.0 MΩ
R 1	3.0 MΩ

Note: Use jumper and shielded wires as the input impedance of VR terminal is high.



Setting value for your reference: 100 kΩ to 1 MΩ.

In order to select an optimum value for resistor R4, you should reference the LCD and the drive waveform.

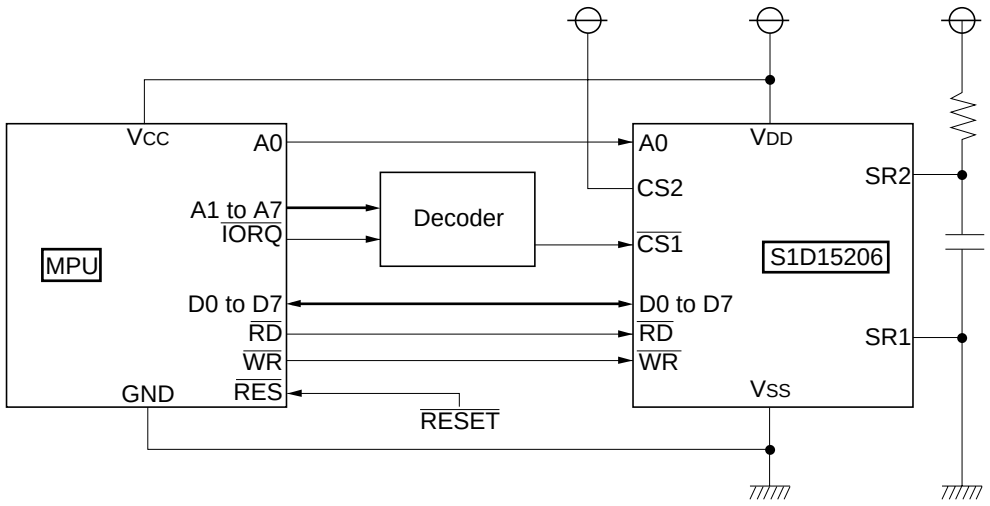
Notes:
1. Because of high input impedance on VR terminal, wiring should made as short as possible and shielded wire should be used for the wiring.
2. C1 and C2 depend on size of the liquid crystal panel to be driven. The value to be selected for C1 and C2 must be able to stabilize the liquid crystal drive voltage.
   [A setting example]
   Turn on the voltage regulator circuit and the voltage follower circuit to apply voltage to VOUT externally. Display the LCD heavy load patterns (horizontal stripe-shaped), then select the C2 value that can stabilize the liquid crystal drive voltages (V_1 to V_5). All C2 capacity values selected, however, must be the same. Then, turn on every built-in power supplies and select an appropriate C1 value.
3. In order to regulate the voltage, a capacitor must be connected between VDD and VSS (near to the IC).

Microprocessor Interface

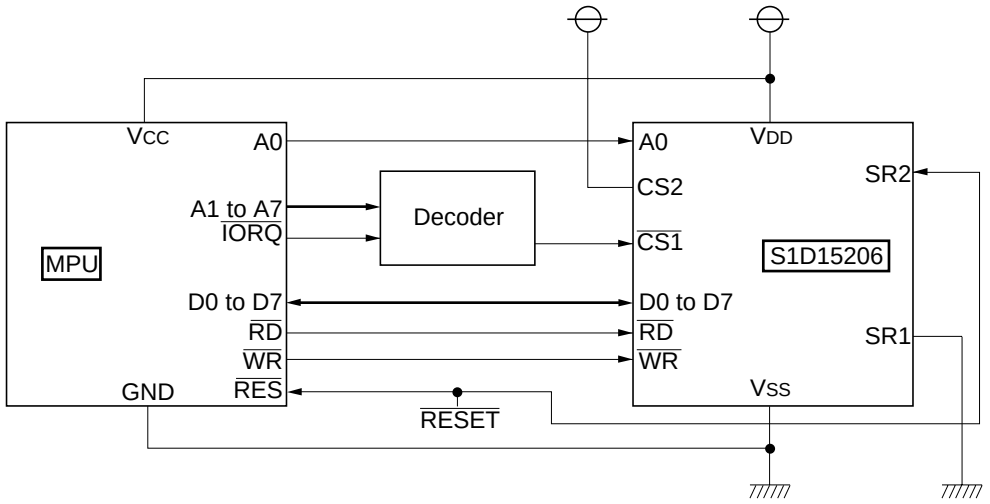
The S1D15206 series chips can directly connect to 8080 and 6800-series microprocessors. Also, serial interfacing requires less signal lines between them.

8080-series microprocessors

Wiring example 1:

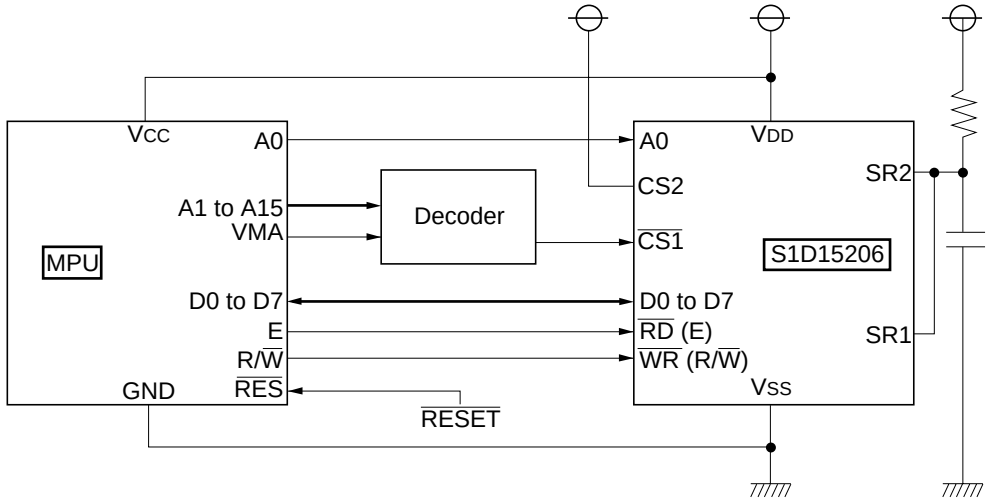


Wiring example 2:

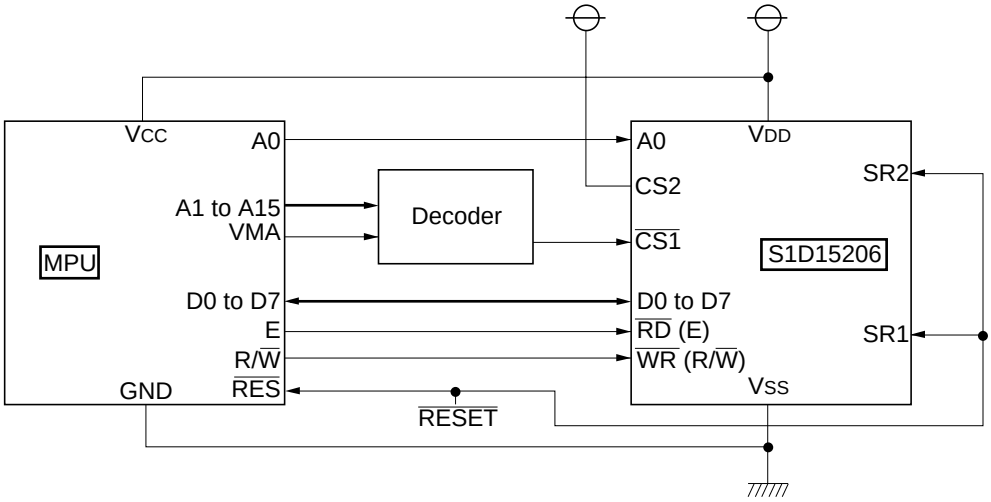


6800-series microprocessors

Wiring example 1:

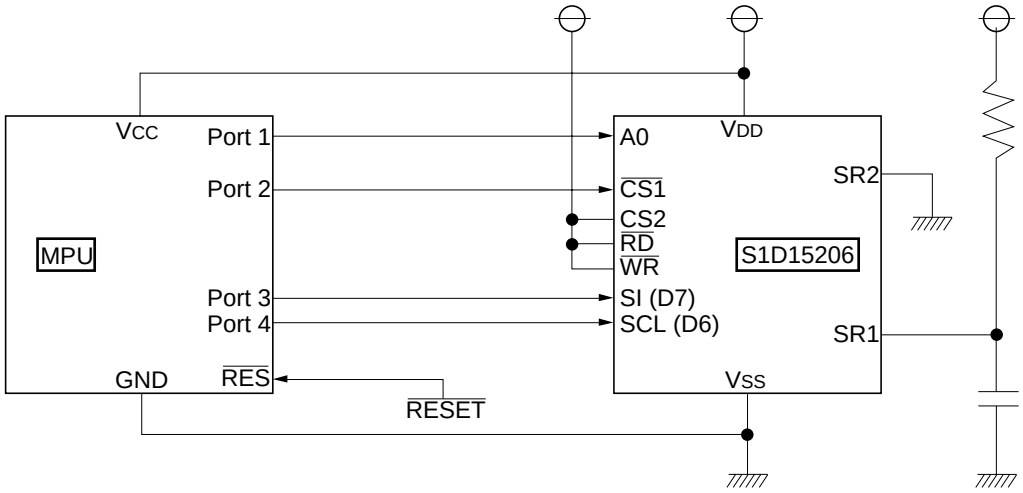


Wiring example 2:

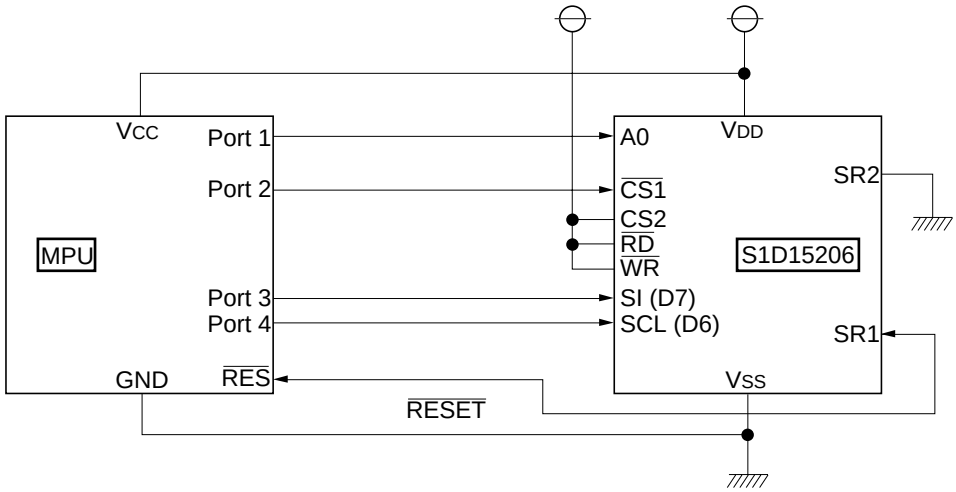


Serial interface

Wiring example 1:

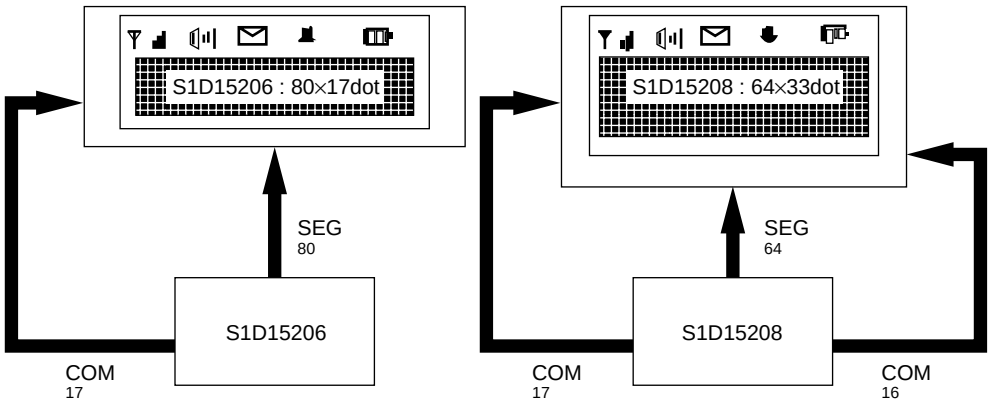


Wiring example 2:



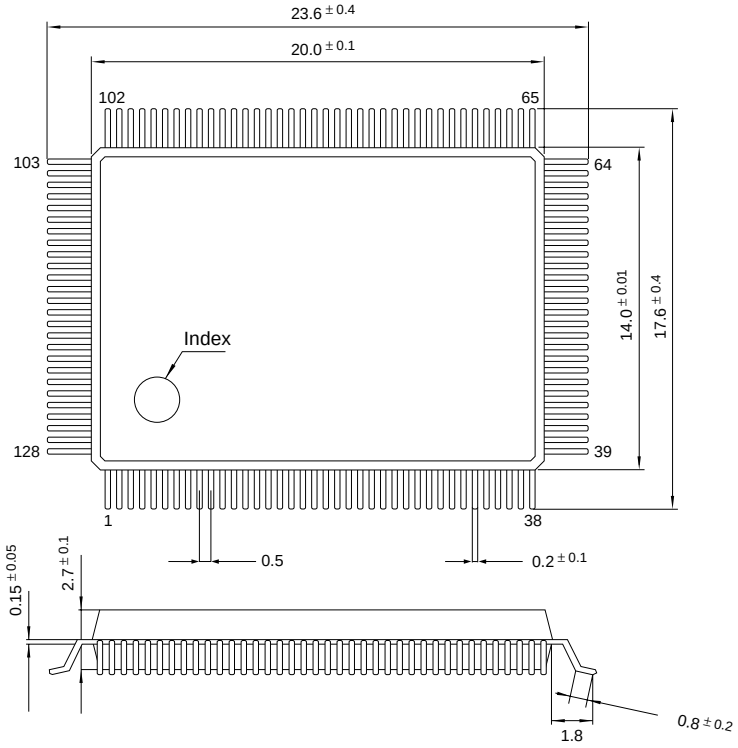
LCD Panel and Wiring Examples

Single-chip configuration



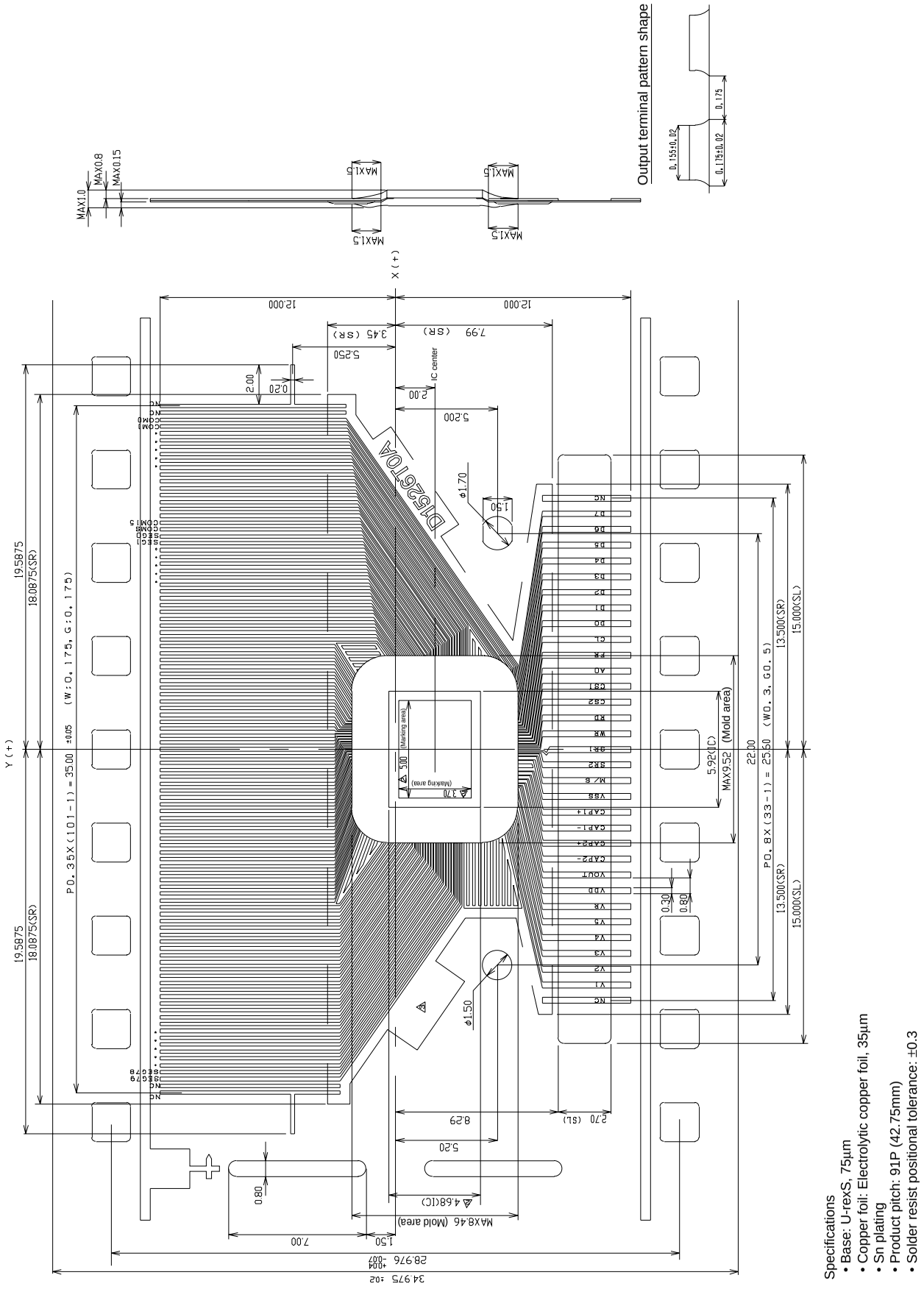
11. DIMENSIONS

Plastic 128-Pin QFP5 Package



The package dimensions are subject to change without notice.

TPC shape S1D15206T00A* (Reference drawing)



Specifications
- Base: U-rexS, 75µm
- Copper foil: Electrolytic copper foil, 35µm
- Sn plating
- Product pitch: 91P (42.75mm)
- Solder resist positional tolerance: ±0.3

This dimensional outline drawing is subject to change for improvements without prior notice

5. S1D15300 Series

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1. DESCRIPTION

The S1D15300 series is a single-chip LCD driver for dot-matrix liquid crystal displays (LCD's) which is directly connectable to a microcomputer bus. It accepts 8-bit serial or parallel display data directly sent from a microcomputer and stores it in an on-chip display RAM. It generates an LCD drive signal independent of microprocessor clock.

The use of the on-chip display RAM of 65 × 132 bits and a one-to-one correspondence between LCD panel pixel dots and on-chip RAM bits permits implementation of displays with a high degree of freedom.

As a total of 133 circuits of common and segment outputs are incorporated, a single chip of S1D15300 can make 33 × 100-dot (16 × 16-dot kanji font: 6 columns × 2 lines) displays, and a single chip of S1D15301 can make 65 × 132-dot (kanji font: 8 columns x 4 lines) displays when the S1D15301 is combined with the common driver S1D16700.

The S1D15302 can display the 65 × 200-dot (or 12-column by 4-line Kanji font) area using two ICs in master and slave modes. As an independent static indicator display is provided for time-division driving, the low-power display is realized during system standby and others.

No external operation clock is required for RAM read/write operations. Accordingly, this driver can be operated with a minimum current consumption and its on-board low-current-consumption liquid crystal power supply can implement a high-performance handy display system with a minimum current consumption and a smallest LSI configuration.

Two types of S1D15300 series are available: one in which common outputs are arranged on a single side and the other in which common outputs are arranged on both sides.

2. FEATURES

- Direct RAM data display using the display RAM. When RAM data bit is 0, it is not displayed. When RAM data bit is 1, it is displayed. (At normal display)
- RAM capacity: 65 × 132 = 8580 bits
- High-speed 8-bit microprocessor interface allowing direct connection to both the 8080 and 6800.
- Serial interface
- Many command functions: Read/Write Display Data, Display ON/OFF, Normal/Reverse Display, Page Address Set, Set Display Start Line, Set Column Address, Read Status, All Display ON/OFF, Set LCD Bias, Electronic contrast Controls, Read Modify Write, Select Segment Driver Direction, Power Save

• Series specifications (in cases of chip shipments)

Type 1 [V_{REG} (Built-in power supply regulating voltage)
Temperature gradient: -0.2% / °C]

Name	Duty	LCD bias	Segment driver	COM driver	Display area	Remarks
S1D15300D00**	1/33	1/5, 1/6	100	33	33 × 100	COM single-side layout
S1D15300D10**	1/33	1/5, 1/6	100	33	33 × 100	COM dual-side layout
S1D15301D00**	1/65	1/6, 1/8	132	0	65 × 132	S1D16700 is used as the COM.
S1D15302D00**	1/65	1/6, 1/8	100	33	65 × 200	COM single-side, right-hand layout
S1D15302D11**	1/65	1/6, 1/8	100	33	65 × 200	COM single-side, left-hand layout
S1D15305D10**	1/35	1/5, 1/6	98	35	35 × 98	COM both-side layout

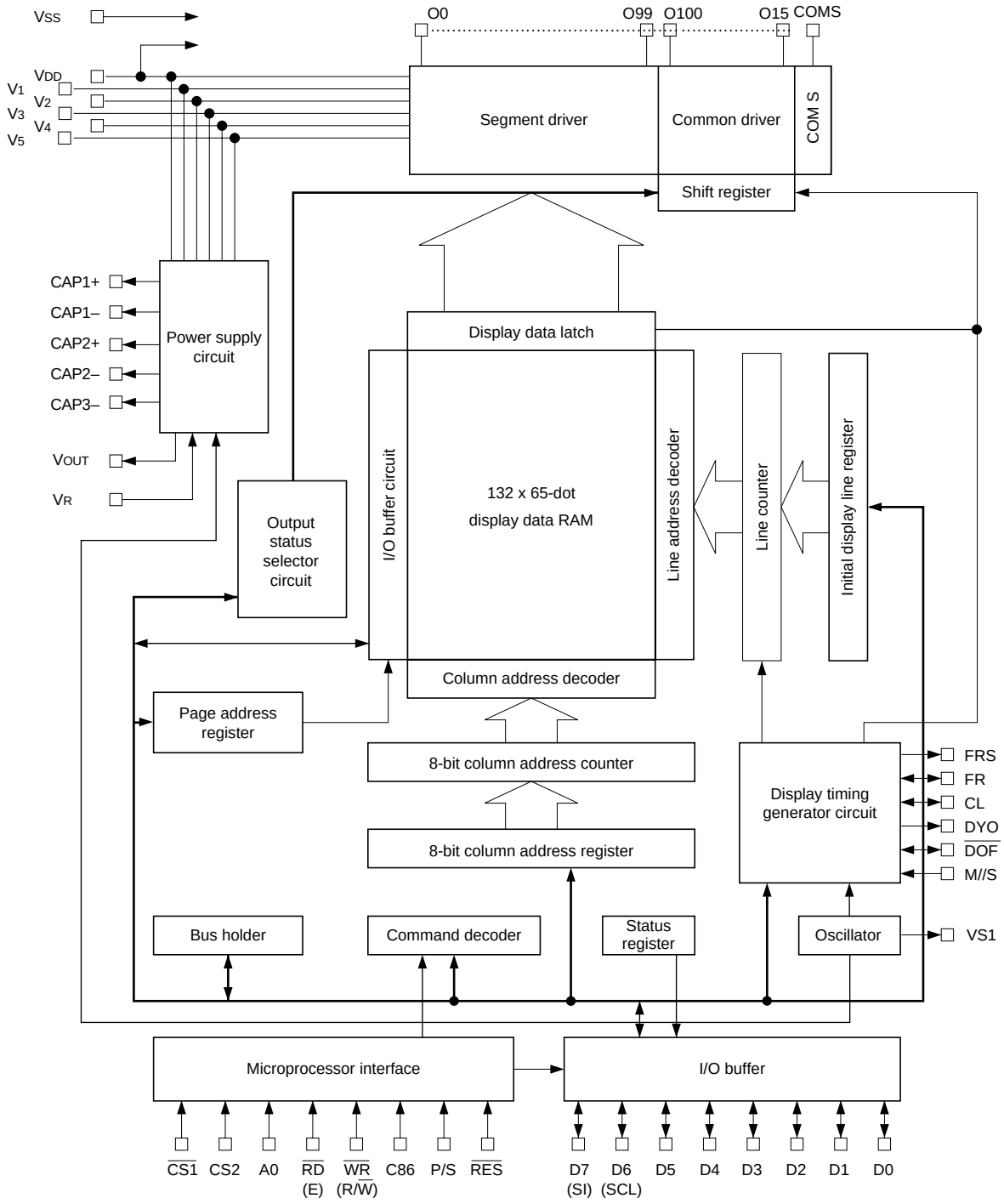
Type 2 [V_{REG} Temperature gradient: 0.00% / °C]

Name	Duty	LCD bias	Segment driver	COM driver	Display area	Remarks
S1D15300D15**	1/33	1/5, 1/6	100	33	33 × 100	COM both-side layout
S1D15302D14**	1/65	1/6, 1/8	100	33	65 × 200	COM single-side, right-hand layout
S1D15303D15**	1/17	1/5	116	17	17 × 116	COM both-side layout
S1D15304D14**	1/9	1/5	124	9	9 × 124	COM single-side layout

Note: The S1D15300 series has the following subcodes depending on their shapes. (The S1D15300 examples are given.)
S1D15300T**** : TCP (The TCP subcode differs from the inherent chip subcode.)
S1D15300D**** : Bear chips — S1D15300D**A* : Al-pad chip
S1D15300D**B* : Au-bump chip

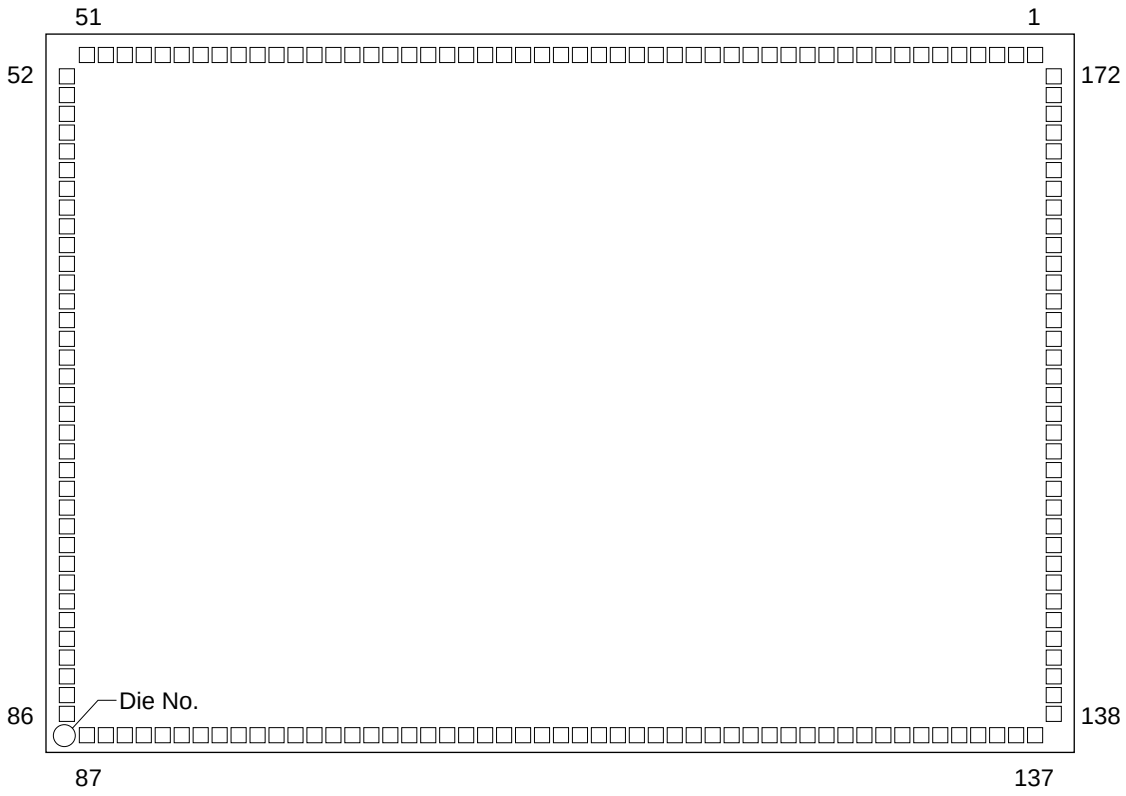
- On-chip LCD power circuit: Voltage booster, voltage regulator, voltage follower × 4.
- On-chip electronic contrast control functions
- Ultra low power consumption
- Power supply voltages: V_{DD} - V_{SS} -2.4 V to -6.0 V
  V_{DD} - V5 -4.5 V to -16.0 V
- Wide operating temperature range: Ta = -40 to 85°C
- CMOS process
- Package: TCP and bare chip
- Non-radiation-resistant design

3. BLOCK DIAGRAM (S1D15300D00B*)



4. PAD LAYOUT

S1D15300 series chips



Chip Size:	6.65x4.57 mm
Pad Pitch:	118 µm (Min.)
S1D1530∗D∗∗A∗	(Al-pad chip)
Pad Center Size:	90x90 µm
Chip Thickness:	300 µm
S1D1530∗D∗∗B∗	(Al-bump chip)
Bump Size:	76x76 µm
Bump Height:	23µm (Typ.)
Chip Thickness:	625 µm

Pad Center Coordinates

Unit: μm

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	O127	2986	2142	51	O5	-2986	2142	101	O55	-1298	-2142	151	O105	3178	-472
2	O128	2862		52	O6	-3178	2006	102	O56	-1180		152	O106		-354
3	O129	2738		53	O7		1888	103	O57	-1062		153	O107		-236
4	O130	2614		54	O8		1770	104	O58	-944		154	O108		-118
5	O131	2490		55	O9		1652	105	O59	-826		155	O109		0
6	COMS	2366		56	O10		1534	106	O60	-708		156	O110		118
7	FRS	2242		57	O11		1416	107	O61	-590		157	O111		236
8	FR	2124		58	O12		1298	108	O62	-472		158	O112		354
9	DYO	2006		59	O13		1180	109	O63	-354		159	O113		472
10	CL	1888		60	O14		1062	110	O64	-236		160	O114		590
11	$\overline{DOF}$	1770		61	O15		944	111	O65	-118		161	O115		708
12	VS1	1652		62	O16		826	112	O66	0		162	O116		826
13	M/S	1534		63	O17		708	113	O67	118		163	O117		944
14	$\overline{RES}$	1416		64	O18		590	114	O68	236		164	O118		1062
15	P/S	1298		65	O19		472	115	O69	354		165	O119		1180
16	$\overline{CS1}$	1180		66	O20		354	116	O70	472		166	O120		1298
17	CS2	1062		67	O21		236	117	O71	590		167	O121		1416
18	C86	944		68	O22		118	118	O72	708		168	O122		1534
19	A0	826		69	O23		0	119	O73	826		169	O123		1652
20	$\overline{WR}$(W/$\overline{R}$)	708		70	O24		-118	120	O74	944		170	O124		1770
21	$\overline{RD}$(E)	590		71	O25		-236	121	O75	1062		171	O125		1888
22	V_{DD}	472		72	O26		-354	122	O76	1180		172	O126		2006
23	D0	354		73	O27		-472	123	O77	1298					
24	D1	236		74	O28		-590	124	O78	1416					
25	D2	118		75	O29		-708	125	O79	1534					
26	D3	0		76	O30		-826	126	O80	1652					
27	D4	-118		77	O31		-944	127	O81	1770					
28	D5	-236		78	O32		-1062	128	O82	1888					
29	D6(SCL)	-354		79	O33		-1180	129	O83	2006					
30	D7(SI)	-472		80	O34		-1298	130	O84	2124					
31	V_{SS}	-590		81	O35		-1416	131	O85	2242					
32	V_{OUT}	-708		82	O36		-1534	132	O86	2366					
33	CAP3-	-826		83	O37		-1652	133	O87	2490					
34	CAP1+	-944		84	O38		-1770	134	O88	2614					
35	CAP1-	-1062		85	O39		-1888	135	O89	2738					
36	CAP2+	-1180		86	O40		-2006	136	O90	2862					
37	CAP2-	-1298		87	O41	-2986	-2142	137	O91	2986					
38	V_5	-1416		88	O42	-2862		138	O92	3178	-2006				
39	V_R	-1534		89	O43	-2738		139	O93		-1888				
40	V_{DD}	-1652		90	O44	-2614		140	O94		-1770				
41	V_1	-1770		91	O45	-2490		141	O95		-1652				
42	V_2	-1888		92	O46	-2366		142	O96		-1534				
43	V_3	-2006		93	O47	-2242		143	O97		-1416				
44	V_4	-2124		94	O48	-2124		144	O98		-1298				
45	V_5	-2242		95	O49	-2006		145	O99		-1180				
46	O0	-2366		96	O50	-1888		146	O100		-1062				
47	O1	-2490		97	O51	-1770		147	O101		-944				
48	O2	-2614		98	O52	-1652		148	O102		-826				
49	O3	-2738		99	O53	-1534		149	O103		-708				
50	O4	-2862		100	O54	-1416		150	O104		-590				

5. PIN DESCRIPTION

Power Supply

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>V_{DD}</td><td>Supply</td><td>+5V power supply. Connect to microprocessor power supply pin V_{CC}.</td><td>2</td></tr>
<tr><td>V_{SS}</td><td>Supply</td><td>Ground</td><td>1</td></tr>
<tr><td>V_1, V_2
V_3, V_4
V_5</td><td>Supply</td><td>LCD driver supply voltages. The voltage determined by LCD cell is impedance-converted by a resistive driver or an operational amplifier for application. Voltages should be the following relationship:
$V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$
When the on-chip operating power circuit is on, the following voltages are given to V_1 to V_4 by the on-chip power circuit. Voltage selection is performed by the Set LCD Bias command. (The S1D15303 and S1D15304 are fixed to 1/5 bias.)
<table>
<tr><th></th><th colspan="2">S1D15300/S1D15305</th><th colspan="2">S1D15301</th><th colspan="2">S1D15302</th></tr>
<tr><td>V_1</td><td>1/5•V_5</td><td>1/6•V_5</td><td>1/6•V_5</td><td>1/8•V_5</td><td>1/6•V_5</td><td>1/8•V_5</td></tr>
<tr><td>V_2</td><td>2/5•V_5</td><td>2/6•V_5</td><td>2/6•V_5</td><td>2/8•V_5</td><td>2/6•V_5</td><td>2/8•V_5</td></tr>
<tr><td>V_3</td><td>3/5•V_5</td><td>4/6•V_5</td><td>4/6•V_5</td><td>6/8•V_5</td><td>4/6•V_5</td><td>6/8•V_5</td></tr>
<tr><td>V_4</td><td>4/5•V_5</td><td>5/6•V_5</td><td>5/6•V_5</td><td>7/8•V_5</td><td>5/6•V_5</td><td>7/8•V_5</td></tr>
</table>
<table>
<tr><th></th><th>S1D15303</th><th>S1D15304</th></tr>
<tr><td>V_1</td><td>1/5•V_5</td><td>1/5•V_5</td></tr>
<tr><td>V_2</td><td>2/5•V_5</td><td>2/5•V_5</td></tr>
<tr><td>V_3</td><td>3/5•V_5</td><td>3/5•V_5</td></tr>
<tr><td>V_4</td><td>4/5•V_5</td><td>4/5•V_5</td></tr>
</table>
</td><td>6</td></tr>
</table>

LCD Driver Supplies

Name	I/O	Description	Number of pins
CAP1+	O	DC/DC voltage converter capacitor 1 positive connection	1
CAP1–	O	DC/DC voltage converter capacitor 1 negative connection	1
CAP2+	O	DC/DC voltage converter capacitor 2 positive connection	1
CAP2–	O	DC/DC voltage converter capacitor 2 negative connection	1
CAP3–	O	DC/DC voltage converter capacitor 1 negative connection	1
V_{OUT}	I/O	DC/DC voltage converter output	1
VR	I	Voltage adjustment pin. Applies voltage between V_{DD} and V5 using a resistive divider.	1

Microprocessor Interface

Name	I/O	Description	Number of pins
D0 to D7 (SI) (SCL)	I/O	8-bit bi-directional data bus to be connected to the standard 8-bit or 16-bit microprocessor data bus. When the serial interface selects; D7: Serial data input (SI) D6: Serial clock input (SCL)	8
A0	I	Control/display data flag input. It is connected to the LSB of micro-processor address bus. When LOW, the data on D0 to D7 is control data. When HIGH, the data on D0 to D7 is display data.	1
$\overline{RES}$		When $\overline{RES}$ is caused to go LOW, initialization is executed. A reset operation is performed at the $\overline{RES}$ signal level.	1
$\overline{CS1}$ CS2	I	Chip select input. Data input/output is enabled when -CS1 is LOW and CS2 is HIGH. When chip select is non-active, D0 to D7 will be "HZ".	2
RD (E)	I	• When interfacing to an 8080 series microprocessor: Active LOW. This input connects the RD signal of the 8080 series microprocessor. While this signal is LOW, the S1D15300 series data bus output is enabled. • When interfacing to a 6800 series microprocessor: Active HIGH. This is used as an enable clock input pin of the 6800 series microprocessor.	1

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>$\overline{WR}$
(R/$\overline{W}$)</td><td>I</td><td>• Write enable input. When interfacing to an 8080-series microprocessor, $\overline{WR}$ is active LOW.
• When interfacing to an 6800-series microprocessor, it will be read mode when R/$\overline{W}$ is HIGH and it will be write mode when R/$\overline{W}$ is LOW.
R/$\overline{W}$ = “1”:Read
R/$\overline{W}$ = “0”:Write</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>Microprocessor interface select terminal.
C86 = HIGH: 6800 series microprocessor interface
C86 = LOW: 8080 series microprocessor interface</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>Serial data input/parallel data input select pin.
<table>
<tr><th>P/S</th><th>Chip select</th><th>Data/command</th><th>Data</th><th>Read/write</th><th>Serial clock</th></tr>
<tr><td>HIGH</td><td>$\overline{CS1}$, CS2</td><td>A0</td><td>D0-D7</td><td>$\overline{RD}$, $\overline{WR}$</td><td>—</td></tr>
<tr><td>LOW</td><td>$\overline{CS1}$, CS2</td><td>A0</td><td>SI(D7)</td><td>Write only</td><td>SCL(D6)</td></tr>
</table>
* In serial mode, no data can be read from RAM.
When P/S = LOW, D0 to D5 are HZ and $\overline{RD}$ and $\overline{WR}$ must be fixed HIGH or LOW.</td><td>1</td></tr>
</table>

LCD Driver Outputs

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>M/S</td><td>I</td><td>S1D15300 series master/slave mode select input. When a necessary signal is output to the LCD, the master operation is synchronized with the LCD system, while when a necessary signal is input to the LCD, the slave operation is synchronized with the LCD system.
M/S = HIGH: Master operation
M/S = LOW : Slave operation
The folLOWing is provided depending on the M/S status.
<table>
<tr><th>Model</th><th>Status</th><th>OSC circuit</th><th>Power supply circuit</th><th>CL</th><th>FR</th><th>DYO</th><th>FRS</th><th>DOF</th></tr>
<tr><td rowspan="2">S1D1530*D****</td><td>Master</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>Slave</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>HZ</td><td>HZ</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input/output. When the S1D15300 series selects master/slave mode, each CL pin is connected. When it is used in combination with the common driver, this input/output is connected to common driver YSCL pin.
M/S = HIGH: Output
M/S = LOW: Input</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>LCD AC signal input/output. When the S1D15300 series selects master/slave mode, each FR pin is connected.
When the S1D15300 series selects master mode this input/output is connected to the common driver FR pin.
M/S = HIGH: Output
M/S = LOW: Input</td><td>1</td></tr>
<tr><td>DYO</td><td>I/O</td><td>Common drive signal output. This output is enabled for only at master operation and connects to the common driver DIO pin. It becomes HZ at slave operation.</td><td>1</td></tr>
<tr><td>VS1</td><td>O</td><td>Test pin. Don’t connect.</td><td>1</td></tr>
<tr><td>$\overline{DOF}$</td><td>I/O</td><td>LCD blanking control input/output. When the S1D15300 series selects master/slave mode, the respective $\overline{DOF}$ pin is connected. When it is used in combination with the common driver (S1D16305), this output/input is connected to the common driver $\overline{DOFF}$ pin.
M/S = HIGH: Output
M/S = LOW: Input</td><td>1</td></tr>
<tr><td>FRS</td><td>O</td><td>Static drive output.
This is enabled only at master operation and used together with the FR pin. This output becomes HZ at slave operation.</td><td>1</td></tr>
</table>

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>On
(SEG n)
(Com n)</td><td>O</td><td>LCD drive output. The following assignment is made depending on the model.
<table>
<tr><th></th><th>SEG</th><th>COM</th></tr>
<tr><td>S1D15300D00**</td><td>O0~O99</td><td>O100~O131</td></tr>
<tr><td>S1D15300D10**
S1D15300D15**</td><td>O16~O115</td><td>O0~O15, O116~O131</td></tr>
<tr><td>S1D15301D00**</td><td>O0~O131</td><td></td></tr>
<tr><td>S1D15302D00**
S1D15302D14**</td><td>O0~O99</td><td>O100~O131</td></tr>
<tr><td>S1D15302D11**</td><td>O32~O131</td><td>O0~O31</td></tr>
<tr><td>S1D15303D15**</td><td>O8~O123</td><td>O0~O7, O124~O131</td></tr>
<tr><td>S1D15304D14**</td><td>O0~O123</td><td>O124~O131</td></tr>
<tr><td>S1D15305D10**</td><td>O18~O115</td><td>O0~O17, O116~O131</td></tr>
</table>
SEG output. LCD segment drive output. One of V_{DD}, V_2, V_3 and V_5 levels is selected by combination of the contents of display RAM and FR signal.
<table>
<tr><th rowspan="2">RAM data</th><th rowspan="2">FR</th><th colspan="2">On output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td rowspan="2">HIGH</td><td>HIGH</td><td>V_{DD}</td><td>V_2</td></tr>
<tr><td>LOW</td><td>V_5</td><td>V_3</td></tr>
<tr><td rowspan="2">0</td><td>HIGH</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td>LOW</td><td>V_3</td><td>V_5</td></tr>
<tr><td>Power save</td><td>–</td><td colspan="2">V_{DD}</td></tr>
</table>
COM output. LCD common drive output. One of V_{DD}, V_1, V_4 and V_5 levels is selected by combination of scan data and FR signal.
<table>
<tr><th>Scan data</th><th>FR</th><th>On output voltage</th></tr>
<tr><td rowspan="2">HIGH</td><td>HIGH</td><td>V_5</td></tr>
<tr><td>LOW</td><td>V_{DD}</td></tr>
<tr><td rowspan="2">LOW</td><td>HIGH</td><td>V_1</td></tr>
<tr><td>LOW</td><td>V_4</td></tr>
<tr><td>Power save</td><td>–</td><td>V_{DD}</td></tr>
</table></td><td>132</td></tr>
<tr><td>COMS</td><td>O</td><td>Indicator COM output. When it is not used, it is made open.
Effective only with the S1D15300, S1D15302, S1D15303 and S1D15304, S1D15305 and “HZ” with the S1D15301.
When multiple numbers of the S1D15300, S1D15302, S1D15303 and S1D15304, S1D15305 are used, the same COMS signal is output to both master and slave units.</td><td>1</td></tr>
<tr><td></td><td></td><td>Total</td><td>172</td></tr>
</table>

6. FUNCTIONAL DESCRIPTION

Microprocessor Interface

Interface type selection

The S1D15300 series can transfer data via 8-bit bi-directional data buses (D7 to D0) or via serial data input (SI). When HIGH or LOW is selected for the polarity of P/S pin, either 8-bit parallel data input or serial data input can be selected as shown in Table 1. When serial data input is selected, RAM data cannot be read out.

Table 1

P/S	Type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D0 to D5
HIGH	Parallel input	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D0 to D5
LOW	Serial input	$\overline{CS1}$	CS2	A0	–	–	–	SI	SCL	(HZ)

"–" must always be HIGH or LOW.

Parallel input

When the S1D15300 series selects parallel input (P/S = HIGH), the 8080 series microprocessor or 6800 series microprocessor can be selected by causing the C86 pin to go HIGH or LOW as shown in Table 2.

Table 2

C86	Type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	WR	D0 to D7
HIGH	6800 micro-processor bus	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D0 to D7
LOW	8080 micro-processor bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{RW}$	D0 to D7

Data Bus Signals

The S1D15300 series identifies the data bus signal according to A0, E, R/$\overline{W}$, ($\overline{RD}$, $\overline{WR}$) signals.

Table 3

Common	6800 processor	8080 processor		Function
A0	(R/$\overline{W}$)	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads display data.
1	0	1	0	Writes display data.
0	1	0	1	Reads status.
0	0	1	0	Writes control data in internal register. (Command)

Serial Interface (P/S is low)

The serial interface consists of an 8-bit shift register and a 3-bit counter. The serial data input and serial clock input are enabled when $\overline{CS1}$ is low and CS2 is high (in chip select status). When chip is not selected, the shift register and counter are reset.

Serial data of D7, D6, ..., D0 is read at D7 in this sequence when serial clock (SCL) goes high. They are converted into 8-bit parallel data and processed on rising edge of every eighth serial clock signal.

The serial data input (S1) is determined to be the display data when A0 is high, and it is control data when A0 is low. A0 is read on rising edge of every eighth clock signal.

Figure 1 shows a timing chart of serial interface signals. The serial clock signal must be terminated correctly against termination reflection and ambient noise. Operation checkout on the actual machine is recommended.

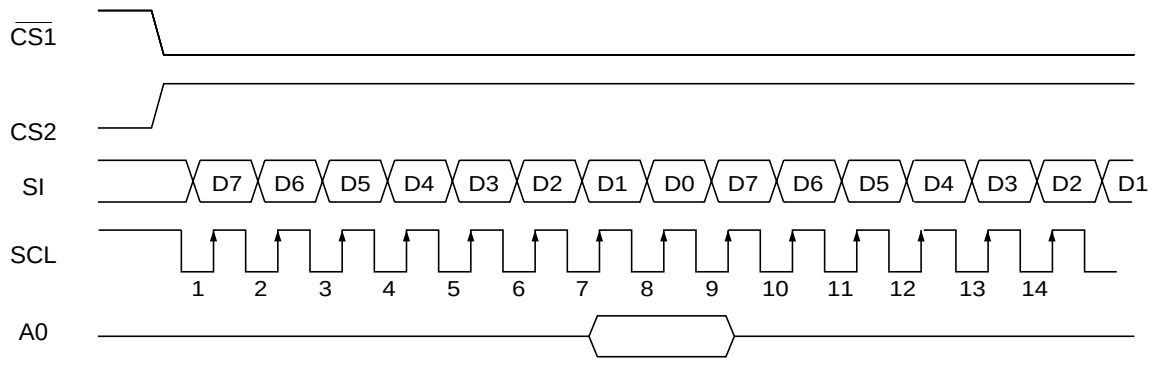


Figure 1

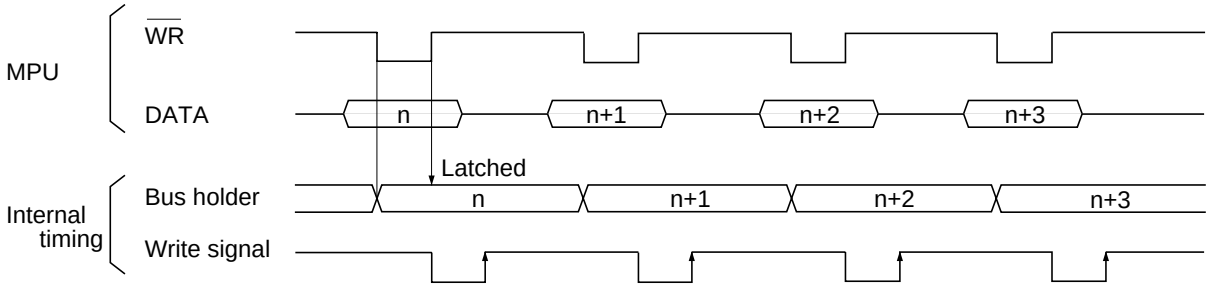
Chip Select Inputs

The S1D15300 series has two chip select pins, $\overline{CS1}$ and CS2 and can interface to a microprocessor when $\overline{CS1}$ is low and CS2 is high. When these pins are set to any other combination, D0 to D7 are high impedance and A0, $\overline{RD}$ and $\overline{WR}$ inputs are disabled.
When serial input interface is selected, the shift register and counter are reset.

Access to Display Data RAM and Internal Registers

The S1D15300 series can perform a series of pipeline processing between LSI's using bus holder of internal data bus in order to match the operating frequency of display RAM and internal registers with the microprocessor. For example, the microprocessor reads data from display RAM in the first read (dummy) cycle, stores it in bus holder, and outputs it onto system bus in the next data read cycle. Also, the microprocessor temporarily stores display data in bus holder, and stores it in display RAM until the next data write cycle starts.
When viewed from the microprocessor, the S1D15300 series access speed greatly depends on the cycle time rather than access time to the display RAM (t_{ACC}). It shows the data transfer speed to/from the microprocessor can increase. If the cycle time is inappropriate, the microprocessor can insert the NOP instruction that is equivalent to the wait cycle setup. However, there is a restriction in the display RAM read sequence. When an address is set, the specified address data is NOT output at the immediately following read instruction. The address data is output during second data read. A single dummy read must be inserted after address setup and after write cycle (refer to Figure 2).

•Write



•Read

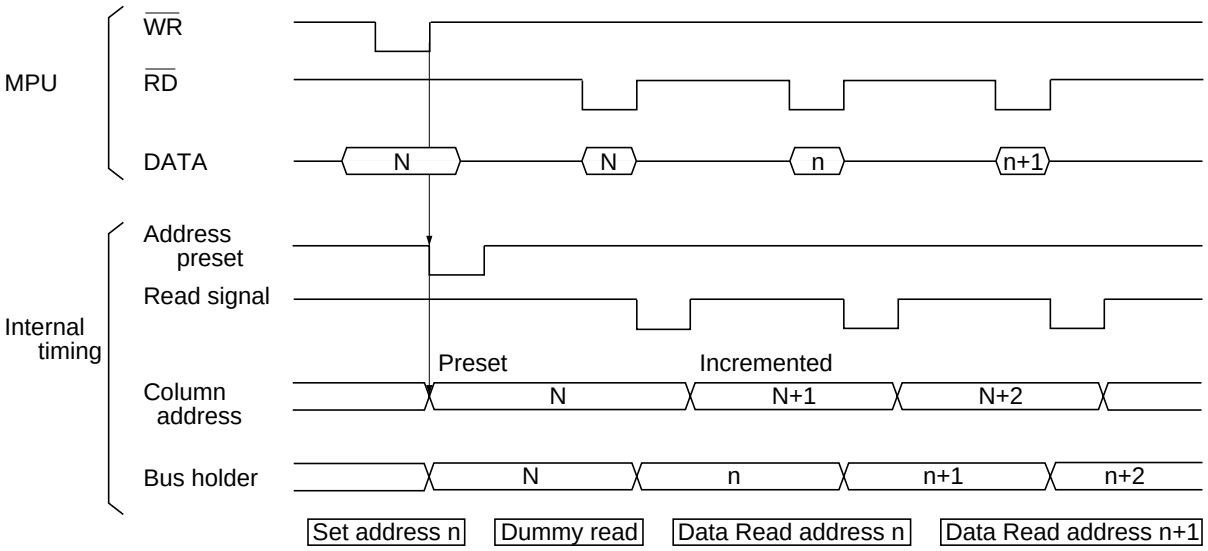


Figure 2

Busy Flag

The Busy flag is set when the S1D15300 series starts to operate. During operating, it accepts Read Status instruction only. The busy flag signal is output at pin D7 when Read Status is issued. If the cycle time (t_{cyc}) is correct, the microprocessor needs not to check the flag before issuing a command. This can greatly improve the microprocessor performance.

Initial Display Line Register

When the display RAM data is read, the display line according to COM0 (usually, the top line of screen) is determined using register data. The register is also used for screen scrolling and page switching.

The Set Display Start Line command sets the 6-bit display start address in this register. The register data is preset on the line counter each time FR signal status changes. The line counter is incremented by CL signal and it generates a line address to allow 132-bit

Column Address Counter

This is a 8 bit presettable counter that provides column address to the display RAM (refer to Figure 4). It is incremented by 1 when a Read/ Write command is entered. However, the counter is not incremented but locked if a non-existing address above 84H is specified. It is unlocked when a column address is set again. The Column Address counter is independent of Page Address register.
When ADC Select command is issued to display inverse display, the column address decoder inverts the relationship between RAM column address and display segment output.

Page Address Register

This is a 4-bit page address register that provides page address to the display RAM (refer to Figure 4). The microprocessor issues Set Page Address command to change the page and access to another page. Page address 8 (D3 is high, but D2, D1 and D0 are low) is RAM area dedicate to the indicator, and display data D0 is only valid.

Display Data RAM

The display data RAM stores pixel data for LCD. It is a 65-column by 132-row (8-page by 8 bit+1) addressable array. Each pixel can be selected when page and column addresses are specified.
The time required to transfer data is very short because the microprocessor enters D0 to D7 corresponding to LCD common lines as shown in Figure 3. Therefore, multiple S1D15300 can easily configure a large display having the high flexibility with very few data transmission restriction.
The microprocessor writes and reads data to/from the RAM through I/O buffer. As LCD controller operates independently, data can be written into RAM at the same time as data is being displayed, without causing the LCD to flicker.

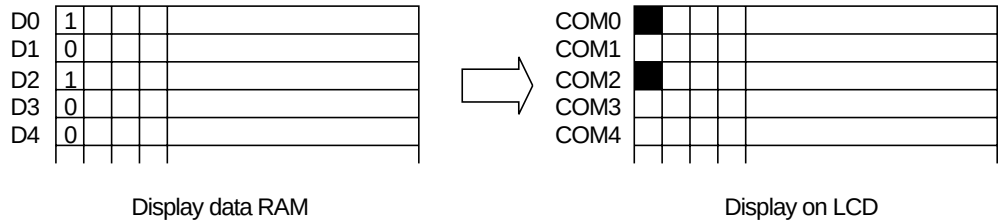


Figure 3

Relationship between display data RAM and addresses (if initial display line is 1CH):

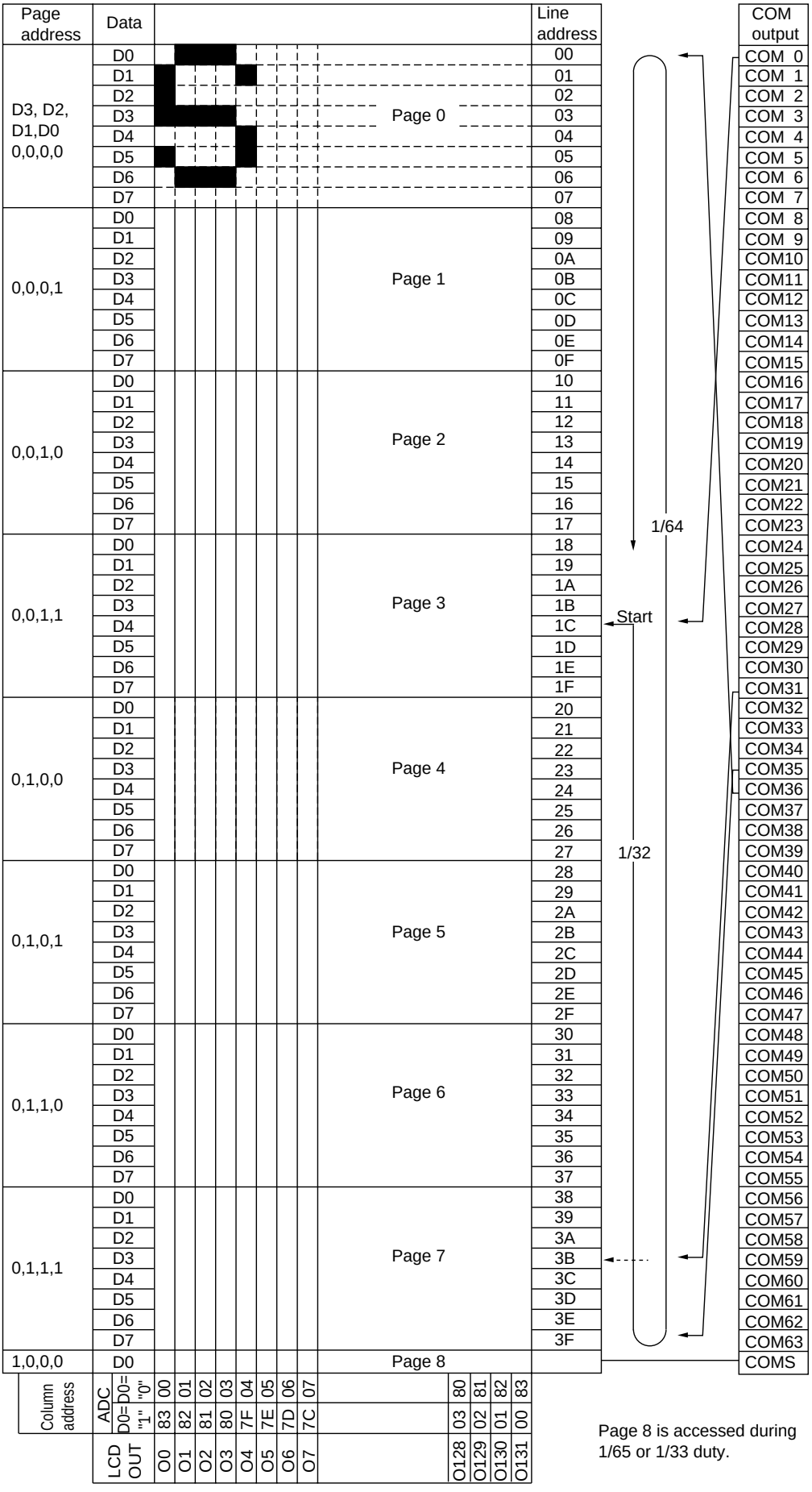


Figure 4

Output Status Selector

The S1D15300 series except S1D15301 can set a COM output scan direction to reduce restrictions at LCD module assembly. This scan direction is set by setting "1" or "0" in the output status register D3. Fig.5 shows the status.

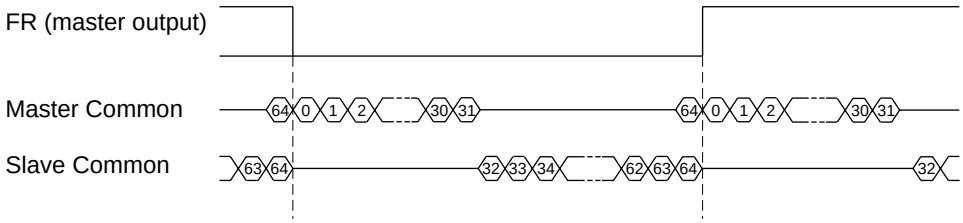
Fig. 5 shows the status.

LCD output		O0		O131
ADC (D0)	"0"	0 (H) →	Column address	→ 83 (H)
	"1"	83 (H) ←		← 0 (H)
		Display data RAM		

	D3			
S1D15300D00**	0	SEG100		COM0 ---------- COM31
	1	SEG100		COM31---------- COM0
S1D15300D10**	0	COM15--0	SEG100	COM16--31
S1D15300D15**	1	COM16--31	SEG100	COM15--0
S1D15301D00**	–	SEG132		
S1D15302D00**	0	SEG100		COM0 ---------- COM31
S1D15302D14**	1	SEG100		COM31---------- COM0
S1D15302D11**	0	COM31---------- 0	SEG100	
	1	COM0 ---------- 31	SEG100	
S1D15303D15**	0	COM7 --0	SEG116	COM8 --15
	1	COM8 --15	SEG116	COM7 --0
S1D15304D14**	0	SEG124		COM0 --7
	1	SEG124		COM7 --0
S1D15305D10**	0	COM17--0	SEG98	COM18--33
	1	COM16--33	SEG98	COM17--0

The COMS pin is assigned to COM32 on S1D15300 and it is assigned to COM64 on S1D15302 independent from their output status. The COMS pin of the S1D15303 is assigned to COM16 the COMS pin of the S1D15304 is assigned to COM8 and the COMS pin of the S1D15305 is assigned to COM34.

Figure 5 shows the COM output pin numbers of S1D15302D00** and S1D15302D11** in the master mode. In the slave mode, COM0 to COM31 must be replaced by COM32 to COM63.



Display Timing Generator

This section explains how the display timing generator circuit operates.

Signal generation to line counter and display data latch circuit

The display clock (CL) generates a clock to the line counter and a latch signal to the display data latch circuit.
The line address of the display RAM is generated in synchronization with the display clock. 132-bit display data is latched by the display data latch circuit in synchronization with the display clock and output to the segment LCD drive output pin.
The display data is read to the LCD drive circuit completely independent of access to the display data RAM from the microprocessor.

LCD AC signal (FR) generation

The display clock generates an LCD AC signal (FR). The FR causes the LCD drive circuit to generate a AC drive waveform.
It generates a 2-frame AC drive waveform.

When the S1D15300 is operated in slave mode on the assumption of multi-chip, the FR pin and CL pin become input pins.

Common timing signal generation

The display clock generates an internal common timing signal and a start signal (DYO) to the common driver. A display clock resulting from frequency division of an oscillation clock is output from the CL pin.
When an AC signal (FR) is switched, a high pulse is output as a DYO output at the training edge of the previous display clock.
Refer to Fig. 6. The DYO output is output only in master mode.
When the S1D15300 series is used for multi-chip, the slave requires to receive the FR, CL, $\overline{DOF}$ signals from the master.
Table 4 shows the FR, CL, DYO and $\overline{DOF}$ status.

Table 4

Model	Operation mode	FR	CL	DYO	$\overline{DOF}$
S1D1530*D****	Master	Output	Output	Output	Output
	Slave	Input	Input	Hz	Input

HZ denotes a high-impedance status.

Example of S1D15300D00B* 1/33 duty

- **Dual-frame AC driver waveforms**

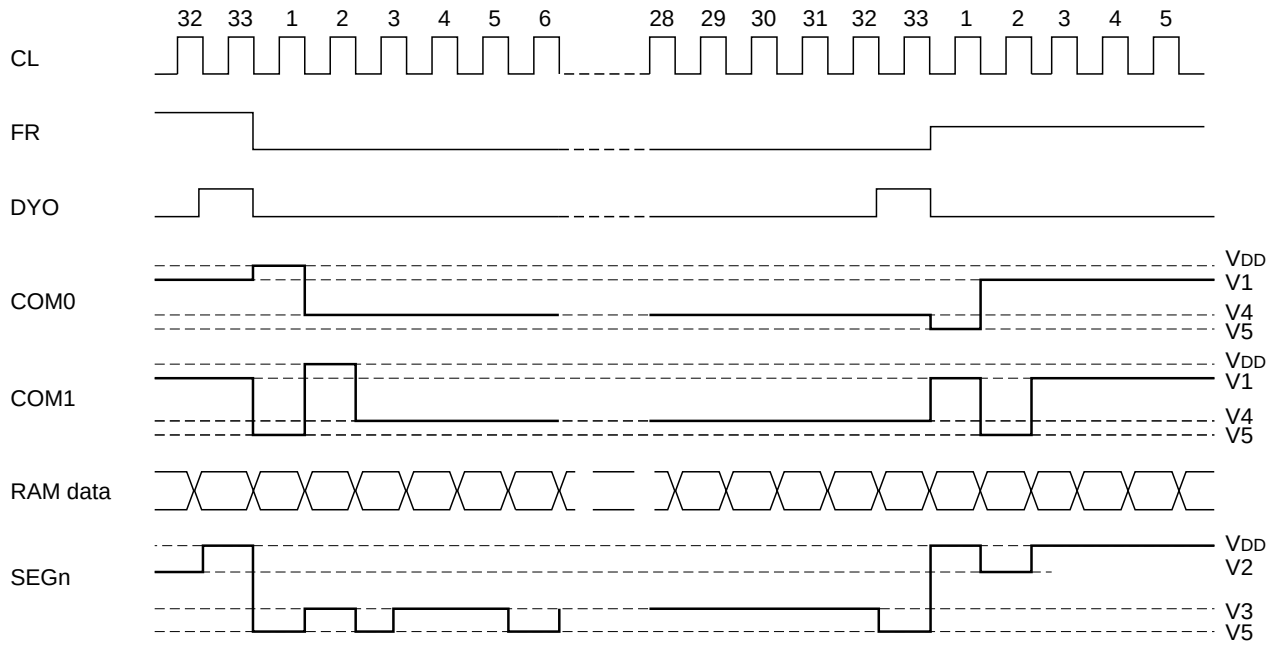


Fig. 6

Display Data Latch Circuit.

This circuit temporarily stores (or latches) display data (during a single common signal period) when it is output from display RAM to LCD panel driver circuit. This latch is controlled by Display in normal/in reverse Display ON/OFF and Static All-display on commands. These commands do not alter the data.

LCD Driver

This is a multiplexer circuit consisting of 133 segment outputs to generate four-level LCD panel drive signals. The LCD panel drive voltage is generated by a specific combination of display data, COM scan signal, and FR signal. Figure 8 gives an example of SEG and COM output waveforms.

Oscillator Circuit

This is an oscillator having a complete built-in type CR, and its output is used as the display timing signal source or as the clock for voltage booster circuit of the LCD power supply.
The oscillator circuit is available in master mode only.
The oscillator signal is divided and output as display clock at CL pin.

Power Supply Circuit

The power supply circuit generates voltage to drive the LCD panel at low power consumption, and is available in S1D15300 master mode only. The power supply circuit consists of a voltage booster voltage regulator, and LCD drive voltage follower.
The power supply circuit built in the S1D15300 series is set for a small-scale LCD panel and is inappropriate to a large-pixel panel and a large-display-capacity LCD panel using multiple chips. As the large LCD panel has the dropped display quality due to a large load capacity, it must use an external power source.

The power circuit is controlled by Set Power Control command. This command sets a three-bit data in Power Control register to select one of eight power circuit functions. The external power supply and part of internal power circuit functions can be used simultaneously. The following explains how the Set Power Control command works.

[Control by Set Power Control command]

D2 turns on when triple booster control bit goes high, and D2 turns off when this bit goes low.

D1 turns on when voltage regulator control bit goes high, and D1 turns off when this bit goes low.

D0 turns on when voltage follower control bit goes high, and D0 turns off when this bit goes low.

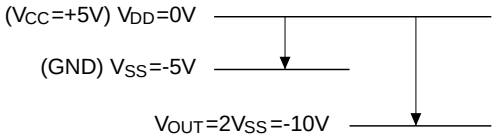
[Practical combination examples]
Status 1: To use only the internal power supply.
Status 2: To use only the voltage regulator and voltage follower.
Status 3: To use only the voltage follower. input the external voltage as V_5=Vout.
Status 4: To use only an external power supply because the internal power supply does not operate.

* The voltage booster terminals are CAP1+, CAP1-, CAP2+, CAP2- and CAP3-.
* Combinations other than those shown in the above table are possible but impractical.

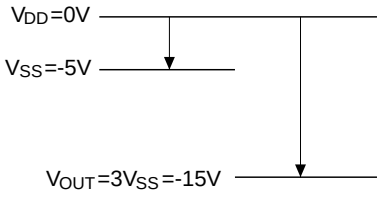
	D2 D1 D0	Voltage booster	Voltage regulator	Voltage follower	External voltage input	Voltage booster terminal	Voltage regulator terminal
①	1 1 1	ON	ON	ON	—	Used	Used
②	0 1 1	OFF	ON	ON	V_{OUT}	OPEN	Used
③	0 0 1	OFF	OFF	ON	V_5	OPEN	OPEN
④	0 0 0	OFF	OFF	OFF	V_1 to V_5	OPEN	OPEN

Booster circuit

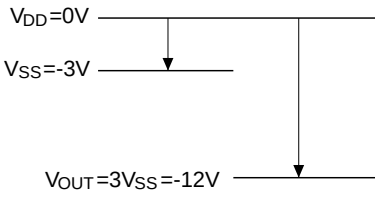
If capacitors C1 are inserted between CAP1+ and CAP1-, between CAP2+ and CAP2-, CAP1+ and CAP3- and VSS and VOUT, the potential between VDD and VSS is boosted to quadruple toward the negative side and it is output at VOUT.
For triple boosting, remove only capacitor C1 between CAP+1 and CAP3- from the connection of quadruple boosting operation and jumper between CAP3- and VOUT. The triple boosted voltage appears at VOUT (CAP3-).
For double boosting, remove only capacitor C1 between CAP2+ and CAP2- from the connection of triple boosting operation, open CAP+2 and jumper between CAP2- and VOUT (CAP3-). The double boosted voltage appears at VOUT (CAP3-, CAP2-).
For quadruple boosting, set a VSS voltage range so that the voltage at VOUT may not exceed the absolute maximum rating.
As the booster circuit uses signals from the oscillator circuit, the oscillator circuit must operate.
Subsection 10.1.1 gives an external wiring example to use master and slave chips when on-board power supply is active.



Potential during double boosting



Potential during triple boosting



Potential during quadruple boosting

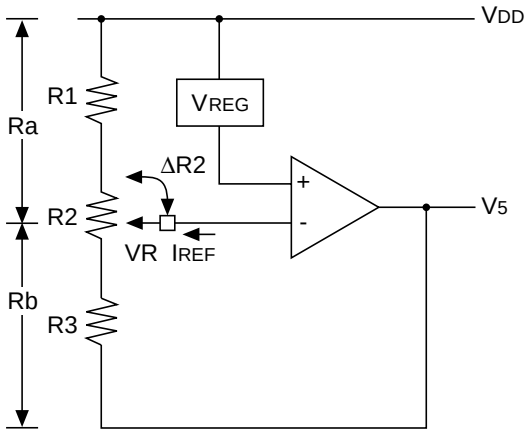
Voltage regulator circuit

The boosting voltage occurring at V_{OUT} is sent to the voltage regulator and the V_5 liquid crystal display (LCD) driver voltage is output. This V_5 voltage can be determined by the following equation when resistors Ra and Rb (R1, R2 and R3) are adjusted within the range of $|V5| < |V_{OUT}|$.

$$V5=(1+\frac{Rb}{Ra})\ V_{REG}+I_{REF}\cdot Rb$$

$$=(1+\frac{R3+R2-\Delta R2}{R1+\Delta R2})\ V_{REG}$$

$$+I_{REF}\cdot(R3+R2-\Delta R2)$$



V_{REG} is the constant voltage source of the IC, and in case of Type 1, it is constant and $V_{REG} \fallingdotseq -2.55$ V (if V_{DD} is 0 V), In case of Type 2, $V_{REG}=V_{SS}$ (V_{DD} basis). To adjust the V_5 output voltage, insert a variable resistor between V_R, V_{DD} and V_5 as shown. A combination of R1 and R3 constant resistors and R2 variable resistor is recommended for fine-adjustment of V_5 voltage.

Setup example of resistors R1, R2 and R3:

When the Electronic Volume Control Function is OFF (electronic volume control register values are (D4,D3,D2,D1,D0)=(0,0,0,0,0)):

$$V_5 = \frac{(1 + R3 + R2 - \Delta R2)}{R1 + \Delta R2} V_{REG} \quad \cdots\cdots\cdots\cdots \textcircled{1}$$

(As $I_{REF} = 0$ A)

- R1 + R2 + R3 = 5MΩ ..... ②
  (Determined by the current passing between V_{DD} and V_5)
- Variable voltage range by R2 V_5 = –6 to –10 V
  (Determined by the LCD characteristics)
  ΔR2 = OΩ, V_{REG} = –2.55V
  To obtain V_5 = -10 V, from equation ①:
  R2 + R3 = 2.92 × R1 ..... ③
  ΔR2 = R2, V_{REG} = –2.55V
  To obtain V_5 = -6 V, from equation ①:
  1.35 × (R1 + R2) = R3 ..... ④

From equations ②, ③ and ④:
R1=1.27MΩ
R2=0.85MΩ
R3=2.88MΩ

The voltage regulator circuit has a temperature gradient of approximately -0.2%/°C as the V_{REG} voltage. To obtain another temperature gradient, use the Electronic Volume Control Function for software processing using the MPU.

As the V_R pin has a high input impedance, the shielded and short lines must be protected from a noise interference.

Voltage regulator using the Electronic Volume Control Function

The Electronic Volume Control Function can adjust the intensity (brightness level) of liquid crystal display (LCD) screen by command control of V_5 LCD driver voltage.
This function sets five-bit data in the electronic volume control register, and the V_5 LCD driver voltage can be one of 32-state voltages.
To use the Electronic Volume Control Function, issue the Set Power Control command to simultaneously operate both the voltage regulator circuit and voltage follower circuit.
Also, when the boosting circuit is off, the voltage must be supplied from V_{OUT} terminal.
When the Electronic Volume Control Function is used, the V_5 voltage can be expressed as follows:

$$V_5 = (1 + \frac{Rb}{Ra})\ V_{REG} + Rb \times \Delta I_{REF} \quad \cdots\cdots\cdots\cdots \textcircled{5}$$

Variable voltage range

The increased V_5 voltage is controlled by use of I_{REF} current source of the IC. (For 32 voltage levels, $\Delta I_{REF} = I_{REF}/31$)

The minimum setup voltage of the V_5 absolute value is determined by the ratio of external Ra and Rb, and the increased voltage by the Electronic Volume Control Function is determined by resistor Rb. Therefore, the resistors must be set as follows:

1) Determine Rb resistor depending on the V_5 variable voltage range by use of the Electronic Volume Control.

$$Rb = \frac{V_5 \text{ variable voltage range}}{I_{REF}}$$

2) To obtain the minimum voltage of the V_5 absolute value, determine Ra using the Rb of Step 1) above.

$$Ra = \frac{Rb}{\frac{V_5}{V_{REG}} - 1} \qquad \{V_5 = (1 + Rb/Ra) \times V_{REG}\}$$

The S1D15300 series have the built-in V_{REG} reference voltage and I_{REF} current source which are constant during voltage variation. However, they may change due to the variation occurring in IC manufacturing and due to the temperature change as shown below. Consider such variation and temperature change, and set the Ra and Rb appropriate to the LCD used.

V_{REG} = –2.55V±0.20V (Type1)	V_{REG} = –0.2%/˚C
V_{REG} = V_{SS} (V_{DD} basis) (Type2)	V_{REG} = –0.00%/˚C
I_{REF} = –3.2µA±40% (For 16 levels)	I_{REF} = 0.023µA/°C
–6.5µA±40% (For 32 levels)	0.052µA/°C

Ra is a variable resistor that is used to correct the V_5 voltage change due to V_{REG} and I_{REF} variation. Also, the contrast adjustment is recommended for each IC chip.
Before adjusting the LCD screen contrast, set the electronic volume control register values to (D4,D3,D2,D1,D0)=(1,0,0,0,0) or (0,1,1,1,1) first.
When not using the Electronic Volume Control Function, set the register values to (D4,D3,D2,D1,D0)=(0,0,0,0,0) by sending the $\overline{RES}$ signal or the Set Electronic Volume Control Register command.

Setup example of constants when Electronic Volume Control Function is used:

V_5 maximum voltage:	V_5 = –6 V (Electronic volume control register values (D4,D3,D2,D1,D0) = (0,0,0,0,0))
V_5 minimum voltages:	V_5 = –10 V (Electronic volume control register values (D4,D3,D2,D1,D0) = (1,1,1,1,1))
V_5 variable voltage range:	4 V
Variable voltage levels:	32 levels

1) Determining the Rb:

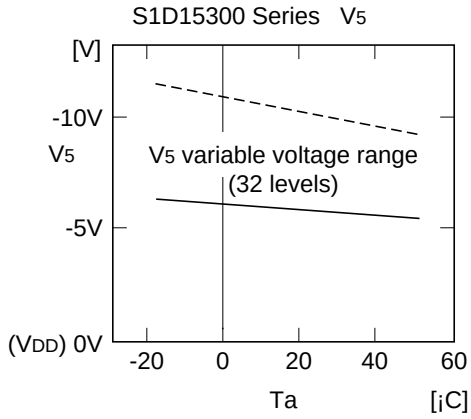
$$R3 = \frac{V_5 \text{ variable voltage range}}{|I_{REF}|} = \frac{4V}{6.5\mu A} \quad \underline{Rb = 625K\Omega}$$

2) Determining the Ra:

$$Ra = \frac{Rb}{\frac{V_5max}{V_{REG}} - 1} = \frac{625k\Omega}{\frac{-6V}{-2.55V} - 1} \qquad \underline{Ra = 462K\Omega}$$

Ta=25°C

$V_5max = (1+Rb/Ra) \times V_{REG}$
$= (1+625k/442k) \times (–2.55V)$
$= –6.0V$
$V_5min = V_5 max + Rb \times I_{REF}$
$= –6V + 625k \times (–6.5\mu A)$
$= –10.0V$



According to the V_5 voltage and temperature change, equation ⑤ can be as follows (if V_{DD} = 0 V reference):

Ta=–10°C

$V_5max = (1+Rb/Ra) \times V_{REG}$ (Ta=–10°C)
$= (1+625k/462k) \times (–2.55V)$
$\times \{1+(–0.2\%/°C) \times (–10°C–25°C)\}$
$= –6.42V$
$V_5min = V_5max + Rb \times I_{REF}$ (Ta=–10°C)
$= –6.42V + 625k$
$\times \{–6.5\mu A+(0.052\mu A/°C) \times (–10°C–25°C)\}$
$= –11.63V$

Ta=–50°C

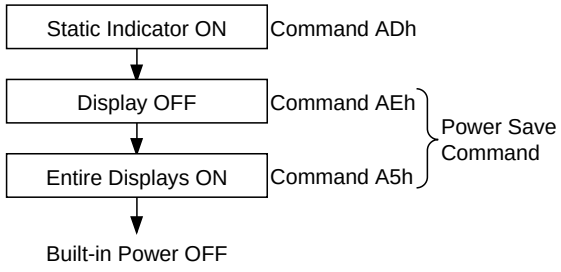
$V_5max = (1+Rb/Ra) \times V_{REG}$ (Ta=50°C)
$= (1+625k/462k) \times (–2.55V)$
$\times \{1+(–0.2\%/°C) \times (50°C–25°C)\}$
$= –5.7V$
$V_5min = V_5max + Rb \times I_{REF}$ (Ta=50°C)
$= –5.7V + 625k$
$\times \{–6.5\mu A+(0.052\mu A/°C) \times (50°C–25°C)\}$
$= –8.95V$

The margin must also be determined in the same procedure given above by considering the V_{REG} and I_{REF} variation. This margin calculation results show that the V_5 center value is affected by the V_{REG} and I_{REF} variation. The voltage setup width of the Electronic Volume Control depends on the I_{REF} variation. When the typical value of 0.2 V/step is set, for example, the maximum variation range of 0.12 to 0.28 V must be considered.

In case of Type 2, it so becomes that V_{REG} = V_{SS} (V_{DD} basis) and there is no temperature gradient. However, I_{REF} carries the same temperature characteristics as with Type 1.

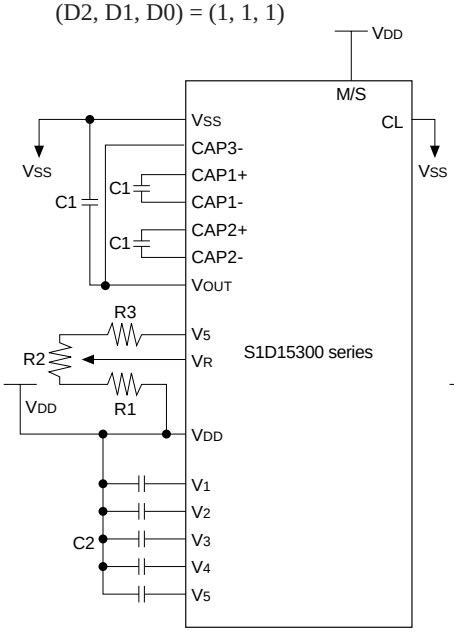
Command Sequence when Built-in Power Supply is Turned OFF

To turn off the built-in power supply, follow the command sequence as shown below to turn it off after making the system into the standby mode.

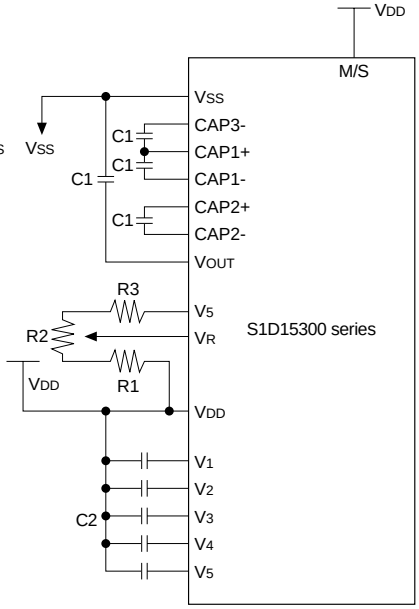


Voltage generator circuit

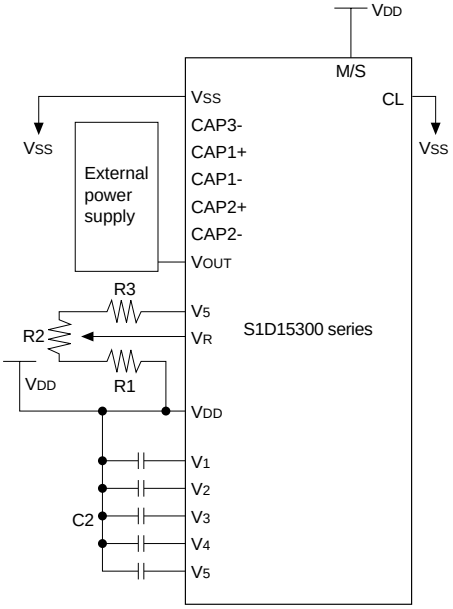
①–1 Power set command when the built-in power supply is used (triple boosting) (D2, D1, D0) = (1, 1, 1)



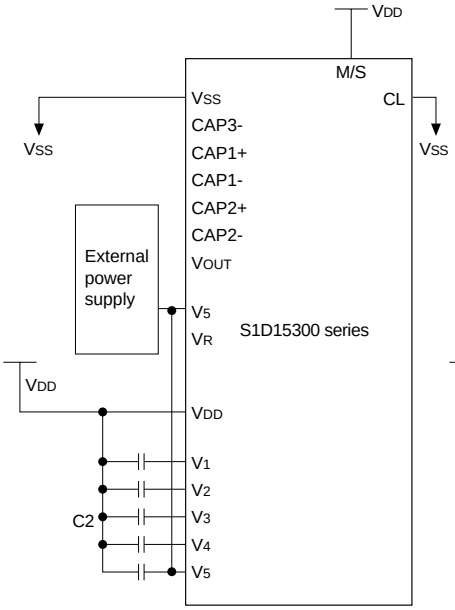
①–2 when the on-chip power circuit is used



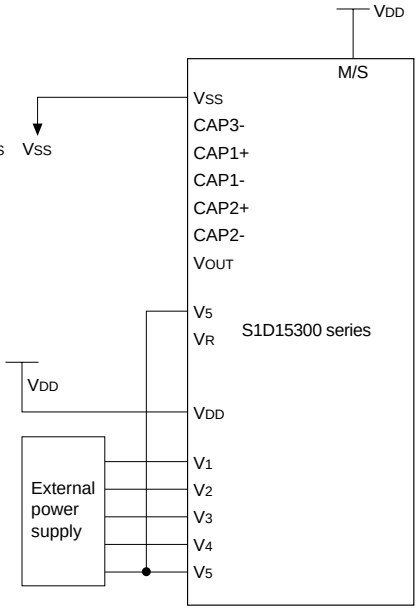
② when VOUT is input from the outside (D2, D1, D0) = (0, 1, 1)



③ when V5 is input from the outside (D2, D1, D0) = (0, 0, 1)



④ when the on-chip power circuit is used



Reference setup value: S1D15300 $V_5 \fallingdotseq$ -7 to -9 V
S1D15301 $V_5 \fallingdotseq$ -11 to -13 V (variable)
S1D15302 $V_5 \fallingdotseq$ -11 to -13 V (variable)

	SED1530	SED1531	SED1532
C1	1.0~4.7 uF	1.0~4.7 uF	1.0~4.7 uF
C2	0.22~0.47 uF	0.47~1.0 uF	0.47~1.0 uF
R1	700 KΩ	1 MΩ	1 MΩ
R2	200 KΩ	200 KΩ	200 KΩ
R3	1.6 MΩ	4 MΩ	4 MΩ
LCD SIZE	16 × 50 mm	32 × 64 mm	32 × 100 mm
DOT CONFIGURATION	32 × 100	64 × 128	64 × 200

1: As the input impedance of V_R is high, a noise protection using short wire and cable shield is required.

*2: C1 and C2 depend on the capacity of the LCD panel to be driven. Set a value so that the LCD drive voltage may be stable.

[Setup example]
Turn on the voltage regulator and voltage follower and give an external voltage to V_{OUT}. Display a horizontal-stripe LCD heavy load pattern and determine C2 so that the LCD drive voltage (V_1 to V_5) may be stable. However, the capacity value of C2 must be all equal. Next, turn on all the on-board power supplies and determine C1.

*3: LCD SIZE means the length and breadth of the display portion of the LCD panel.

Model	LCD drive voltage
S1D15300	1/5 or 1/6 bias
S1D15301 S1D15302	1/6 or 1/8 bias

Reset Circuit

When the RES input goes low, this LSI is initialized.

Initialized status

1. Display OFF
2. Normal display
3. ADC select: Normal display (ADC command D0 = low)
4. Read modify write OFF
5. Power control register (D2, D1, D0) = (0, 0, 0)
6. Register data clear in serial interface
7. LCD power supply bias ratio 1/6 (S1D15300), 1/8 (S1D15301, SE1D15302)
8. Static indicator: OFF
9. Display start line register set at line 1
10. Column address counter set at address 0
11. Page address register set at page 0
12. Output status register (D3) = (0)
13. Electronic control register set at 0
14. Test command OFF

As seen in 11. Microprocessor Interface (Reference Example), connect the $\overline{RES}$ pin to the reset pin of the microprocessor and initialize the microprocessor at the same time.

In case the S1D15300 series does not use the internal LCD power supply circuit, the $\overline{RES}$ must be low when the external LCD power supply is turned on.

When $\overline{RES}$ goes low, each register is cleared and set to the above initialized status. However, it has no effect on the oscillator circuit and output pins (FR, CL, DYO, D0 to D7).
The initialization by $\overline{RES}$ pin signal is always required during power-on. If the control signal from the MPU is HZ, an overcurrent may flow through the IC. A protection is required to prevent the HZ signal at the input pin during power-on.

Be sure to initialize it by $\overline{RES}$ pin when turning on the power supply. When the reset command is used, only parameters 8 to 14 in the above initialization are executed.

* Precautions when installing the COG

When installing the COG, it is necessary to duly consider the fact that there exists a resistance of the ITO wiring occurring between the driver chip and the externally connected parts (such as capacitors and resistors). By the influence of this resistance, non-conformity may occur with the indications on the liquid crystal display.
Therefore, when installing the COG design the module paying sufficient considerations to the following three points.

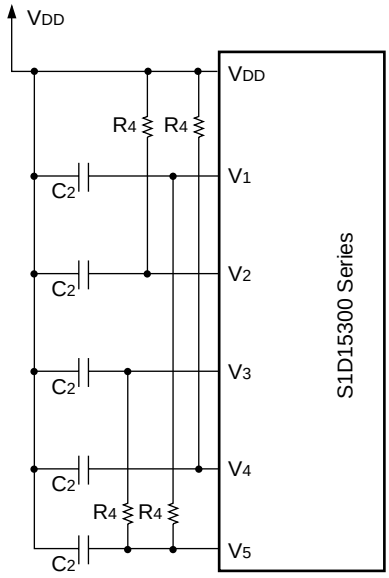
1. Suppress the resistance occurring between the driver chip pin to the externally connected parts as much as possible.
2. Suppress the resistance connecting to the power supply pin of the driver chip.
3. Make various COG module samples with different ITO sheet resistance to select the module with the sheet resistance with sufficient operation margin.

Also, as for this driver IC, pay sufficient attention to the following points when connecting to external parts for the characteristics of the circuit.

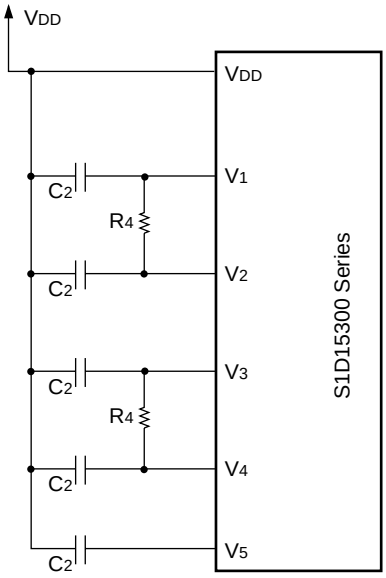
1. Connection to the boosting capacitors The boosting capacitors (the capacitors connecting to respective CAP pins and capacitor being inserted between V_{OUT} and V_{SS2}) of this IC are being switched over by use of the transistor with very low ON-resistance of about 10Ω. However, when installing the COG, the resistance of ITO wiring is being inserted in series with the switching transistor, thus dominating the boosting ability. Consequently, the boosting ability will be hindered as a result and pay sufficient attention to the wiring to respective boosting capacitors.
2. Connection of the smoothing capacitors for the liquid crystal drive
   The smoothing capacitors for the liquid crystal driving potentials (V_1. V_2, V_3 and V_4) are indispensable for liquid crystal drives not only for the purpose of mere stabilization of the voltage levels. If the ITO wiring resistance which occurs pursuant to installation of the COG is supplemented to these smoothing capacitors, the liquid crystal driving potentials become unstable to cause non-conformity with the indications of the liquid crystal display. Therefore, when using the COG module, we definitely recommend to connect reinforcing resistors externally. Reference value of the resistance is 100kΩ to 1MΩ.
   Meanwhile, because of the existence of these reinforcing resistors, current consumption will increase.

Indicated below is an exemplary connection diagram of external resistors.
Please make sufficient evaluation work for the display statuses with any connection tests.

Exemplary connection diagram 1.



Exemplary connection diagram 2.



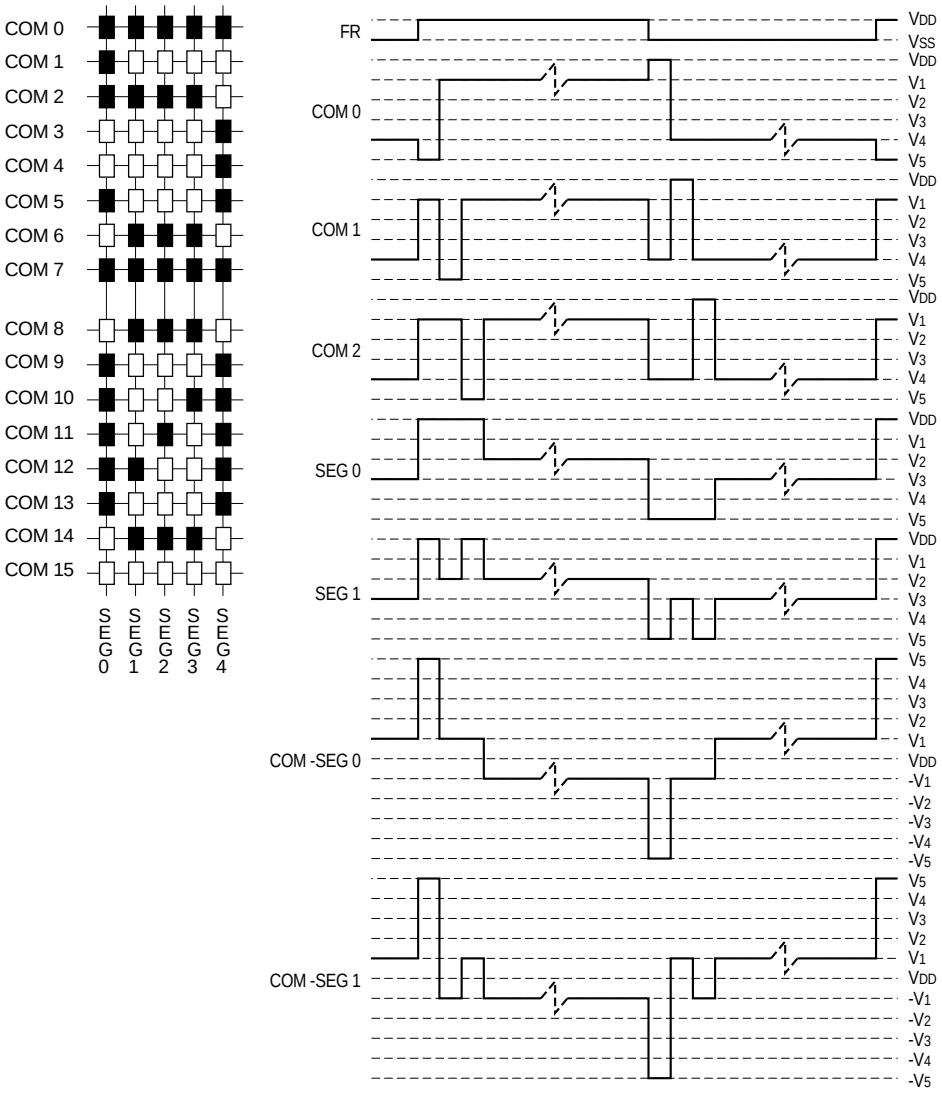


Figure 8

7. COMMANDS

The S1D15300 series uses a combination of A0, $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the $\overline{RD}$ pin and a write status when a low pulse is input to the $\overline{WR}$ pin. The 6800 series microprocessor interface enters a read status when a high pulse is input to the R/$\overline{W}$ pin and a write status when a low pulse is input to this pin. When a high pulse is input to the E pin, the command is activated. (For timing, see Timing Characteristics.) Accordingly, in the command explanation and command table, $\overline{RD}$ (E) becomes 1 (high) when the 6800 series microprocessor interface reads status or display data. This is an only different point from the 8080 series microprocessor interface.

Taking the 8080 series microprocessor interface as an example, commands will be explained below.
When the serial interface is selected, input data starting from D7 in sequence.

(1) Display ON/OFF
Alternatively turns the display on and off.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

The display turns off when D goes low, and it turns on when D goes high.

(2) Start Display Line
Specifies line address (refer to Figure 4) to determine the initial display line, or COM0. The RAM display data becomes the top line of LCD screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the line address, the smooth scrolling or page change takes place.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

← High-order bit

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
			:			:
1	1	1	1	1	0	6 2
1	1	1	1	1	1	6 3

(3) Set Page Address
Specifies page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed. Page address 8 is the display RAM area dedicate to the indicator, and only D0 is valid for data change.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Page Address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

(4) Set Column Address
Specifies column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them succession. When the microprocessor repeats to access to the display RAM, the column address counter is incremented by 1 during each access until address 132 is accessed. The page address is not changed during this time.

	A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Higher bits	0	1	0	0	0	0	1	A7	A6	A5	A4
Lower bits	0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				:				:
1	0	0	0	0	0	1	1	1 3 1

(5) Read Status

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY: When high, the S1D15206 series is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

ADC: Indicates the relationship between RAM column address and segment drivers. When low, the display is normal and column address "131-n" corresponds to segment driver n. When high, the display is reversed and column address n corresponds to segment driver n.

ON/OFF: Indicates whether the display is on or off. When goes low, the display turns on. When goes high, the display turns off. This is the opposite of Display ON/OFF command.

RESET: Indicates the initialization is in progress by $\overline{RES}$ signal or by Reset command. When low, the display is on. When high, the chip is being reset.

(6) Write Display Data
Writes 8-bit data in display RAM. As the column address is incremented by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

(7) Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address is incremented by 1 automatically after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

(8) ADC Select

Changes the relationship between RAM column address and segment driver. The order of segment driver output pins can be reversed by software. This allows flexible IC layout during LCD module assembly. For details, refer to the column address section of Figure 4. When display data is written or read, the column address is incremented by 1 as shown in Figure 4.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

When D is low, the right rotation (normal direction). When D is high, the left rotation (reverse direction).

(9) Normal/Reverse Display

Reverses the Display ON/OFF status without rewriting the contents of the display data RAM.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D is low, the RAM data is high, being LCD ON potential (normal display).
When D is high, the RAM data is low, being LCD ON potential (reverse display).

(10) Entire Display ON

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.
This command has priority over the Normal/Reverse Display command. When D is low, the normal display status is provided.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D is high, the entire display ON status is provided.
If the Entire Display ON command is executed in the display OFF status, the LCD panel enters Power Save mode. Refer to the Power Save section for details.

(11) Set LCD Bias

Selects a bias ratio of the voltage required for driving the LCD. This command is enabled when the voltage follower in the power supply circuit operates.
(The LCD bias setting command is invalid for the S1D15303 and S1D15304. They are being fixed to the 1/5 bias.)

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	1	D

The potential V_5 is resistively divided inside the IC to produce potentials V_1, V_2, V_3 and V_4 which are necessary to drive the LCD. The bias ratio can be selected using the LCD bias setting command. (The S1D15303 and S1D15304 are fixed to 1/5 bias.)
Moreover, the potentials V_1, V_2, V_3 and V_4 are converted in the impedance and supplied to the LCD drive circuit.

Model	Bias ratio of LCD power supply
S1D15300	1/5 bias or 1/6 bias
S1D15301 S1D15302	1/6 bias or 1/8 bias
S1D15303 S1D15304	1/5 bias

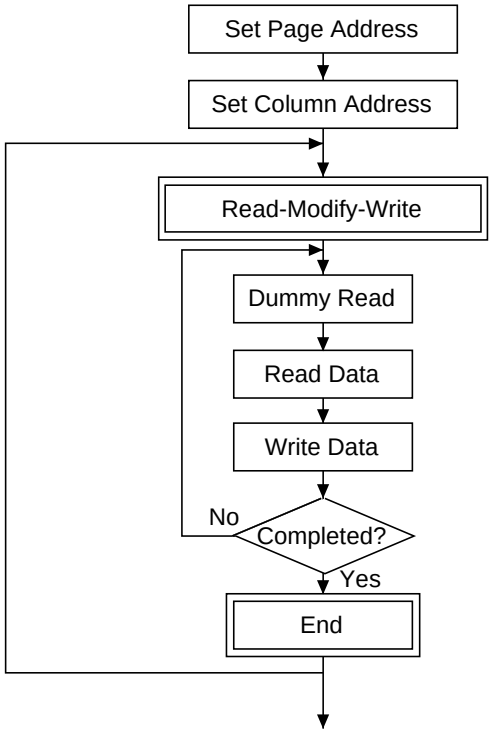
(12) Read-Modify-Write

A pair of Read-Modify-Write and End commands must always be used. Once Read-Modify-Write is issued, column address is not incremented by Read Display Data command but incremented by Write Display Data command only. It continues until End command is issued. When the End is issued, column address returns to the address when Read-Modify-Write was issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Note: Any command except Read/Write Display Data and Set Column Address can be issued during Read-Modify-Write mode.

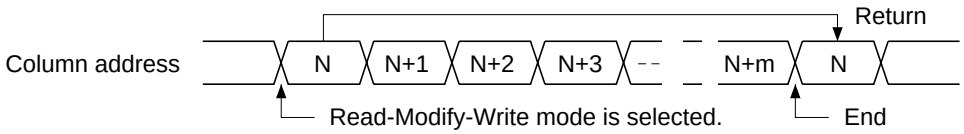
• Cursor display sequence



(13) End

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write was issued).

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



(14) Reset

Resets the Initial Display Line register, Column Address counter, Page Address register, and output status selector circuit to their initial status. The Reset command does not affect on the contents of display RAM. Refer to the Reset circuit section of FUNCTIONAL DESCRIPTION.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The Reset command cannot initialize LCD power supply. Only the Reset siganl to the $\overline{RES}$ pin can initialize the supplies.

(15) Output Status Select Register

Applicable to the S1D15300 and S1D15302. When D is high or low, the scan direction of the COM output pin is selectable. Refer to Output Status Selector Circuit in Functional Description for details.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	D	*	*	*

D: Selects the scan direction of COM output pin
* : Invalid bit

(16) Set Power Control

Selects one of eight power circuit functions using 3-bit register. An external power supply and part of on-chip power circuit can be used simultaneously. Refer to Power Supply Circuit section of FUNCTIONAL DESCRIPTION for details.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	A2	A1	A0

When A0 goes low, voltage follower turns off. When A0 goes high, it turns on.
When A1 goes low, voltage regulator turns off. When A1 goes high, it turns on.
When A2 goes low, voltage booster turns off. When A2 goes high, it turns on.

(17) Set Electronic Control

Adjusts the contrast of LCD panel display by changing V5 LCD drive voltage that is output by voltage regulator of on-board power supply.
This command selects one of 32 V_5 LCD drive voltages by storing data in 5-bit register. The V_5 voltage adjusting range should be determined depending on the external resistance. Refer to the Voltage Regulator section of FUNCTIONAL DESCRIPTION for details.

A0	RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	A4	A3	A2	A1	A0

D4	D3	D2	D1	D0	| V5 |
0	0	0	0	0	LOW
0	0	0	0	1	
0	0	0	1	0	
		:			↓
1	1	1	0	1	
1	1	1	1	0	
1	1	1	1	1	HIGH

Set register to (D4,D3,D2,D1,D0)=(0,0,0,0,0) to suppress electronic control function.

(18) Static Indicator

This command turns on or off static drive indicators. The indicator display is controlled by this command only, and it is not affected by the other display control commands.
Either FR or FRS terminal is connected to either of static indicator LCD drive electrodes, and the remaining terminal is connected to another electrode. When the indicator is turned on, the static drive operates and the indicator blinks at an interval of approximately one second. The pattern separation between indicator electrodes are dynamic drive electrodes is recommended. A closer pattern may cause an LCD and electrode deterioration.

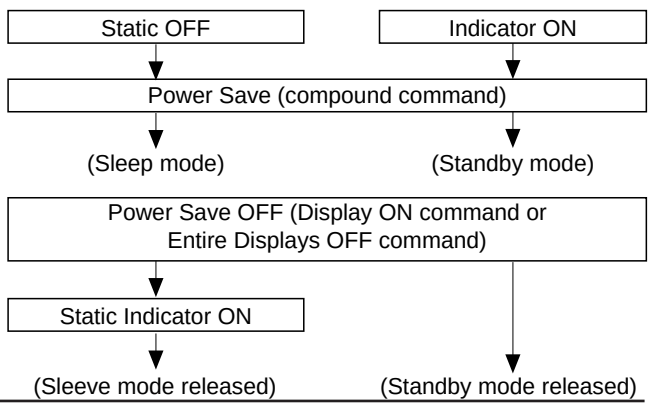
A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	D

D 0: Static indicator OFF
1: Static indicator ON

(19) Power Save (Compound Command)

When all displays are turned on during indicator off, the Power Save command is issued to greatly reduce the current consumption.
If the static indicators are off, the Power Save command sleeps the system. If on, this command stands by the system.

Release the Sleep mode using the both Power Save OFF command (Indicator ON command or All Indicator Displays OFF command) and Static Indictor ON command.
Release the Standby mode using the Power Save OFF command (Indicator ON command or All Indicator Displays OFF command).



Sleep mode
This mode stops every operation of the LCD display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

(1) Stops the oscillator circuit and LCD power supply circuit.
(2) Stops the LCD drive and outputs the VDD level as the segment/common driver output.
(3) Holds the display data and operation mode provided before the start of the sleep mode.
(4) The MPU can access to the built-in display RAM.

Standby mode
Stops the operation of the duty LCD display system and turns on only the static drive system to reduce current consumption to the minimum level required for static drive.
The ON operation of the static drive system indicates that the S1D15300 series is in the standby mode. The internal status in the standby mode is as follows:

(1) Stops the LCD power supply circuit.
(2) Stops the LCD drive and outputs the VDD level as the segment/common driver output. However, the static drive system operates.
(3) Holds the display data and operation mode provided before the start of the standby mode.
(4) The MPU can access to the built-in display RAM.
When the RESET command is issued in the standby mode, the sleep mode is set.

When the LCD drive voltage level is given by an external resistive driver, the current of this resistor must be cut so that it may be fixed to floating or VDD level, prior to or concurrently with causing the S1D15300 series to go to the sleep mode or standby mode.

When an external power supply is used, likewise, the function of this external power supply must be stopped so that it may be fixed to floating or VDD level, prior to or concurrently with causing the S1D15300 series to go to the sleep mode or standby mode.

When the common driver S1D16305 or S1D16501 is combined with the S1D15301 in the configuration, the DOF pin of the S1D15301 must be connected to the DOFF pin of the S1D16305 or S1D16501.

(20) Test Command
This is the dedicate IC chip test command. It must not be used for normal operation. If the Test command is issued erroneously, set the -RES input to low or issue the Reset command to release the test mode.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

* : Invalid bit

Cautions: The S1D15300 Series holds an operation status specified by each command. However, the internal operation status may be changed by a high level of ambient noise. It must be considered to suppress the noise on the its package and system or to prevent an ambient noise insertion. To prevent a spike noise, a built-in software for periodical status refreshment is recommended to use.
The test command can be inserted in an unexpected place. Therefore, it is recommended to enter the test mode reset command F0h during the refresh sequence.

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	Turns on LCD panel when goes high, and turns off when goes low.
(2) Initial Display Line	0	1	0	0	1	Start display address						Specifies RAM display line for COM0.
(3) Set Page Address	0	1	0	1	0	1	1	Page address				Sets the display RAM page in Page Address register.
(4) Set Column Address 4 higher bits	0	1	0	0	0	0	1	Higher column address				Sets 4 higher bits of column address of display RAM in register
(4) Set Column Address 4 lower bits	0	1	0	0	0	0	0	Lower column address				Sets 4 lower bits of column address of display RAM in register
(5) Read Status	0	0	1	Status				0	0	0	0	Reads the status information.
(6) Write Display Data	1	1	0	Write data								Writes data in display RAM.
(7) Read Display Data	1	0	1	Read data								Reads data from display RAM.
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Sets normal relationship between RAM column address and segment driver when low, but reverses the relationship when high.
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0 1	Normal indication when low, but full indication when high.
(10) Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Selects normal display (0) or Entire Display ON (1).
(11) Set LCD Bias	0	1	0	1	0	1	0	0	0	1	0 1	Sets LCD drive voltage bias ratio.
(12) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Increments Column Address counter during each write when high and during each read when low.
(13) End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read-Modify-Write.
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Resets internal functions.
(15) Set Output Status Register	0	1	0	1	1	0	0	0 1	*	*	*	Selects COM output scan direction. * Invalid data
(16) Set Power Control	0	1	0	0	0	1	0	1	Operation status			Selects the power circuit operation mode.
(17) Set Electronic Control Register	0	1	0	1	0	0	Electronic control value					Sets V5 output voltage to Electronic Control register.
(18) Set Standby	0	1	0	1	0	1	0	1	1	0	0 1	Selects standby status. 0: OFF 1: ON
(19) Power Save	–	–	–	–	–	–	–	–	–	–	–	Compound command of display OFF and entire display ON
(20) Test Command	0	1	0	1	1	1	1	*	*	*	*	IC Test command. Do not use!
(21) Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	Command of test mode reset

Note: Do not use any other command, or the system malfunction may result.

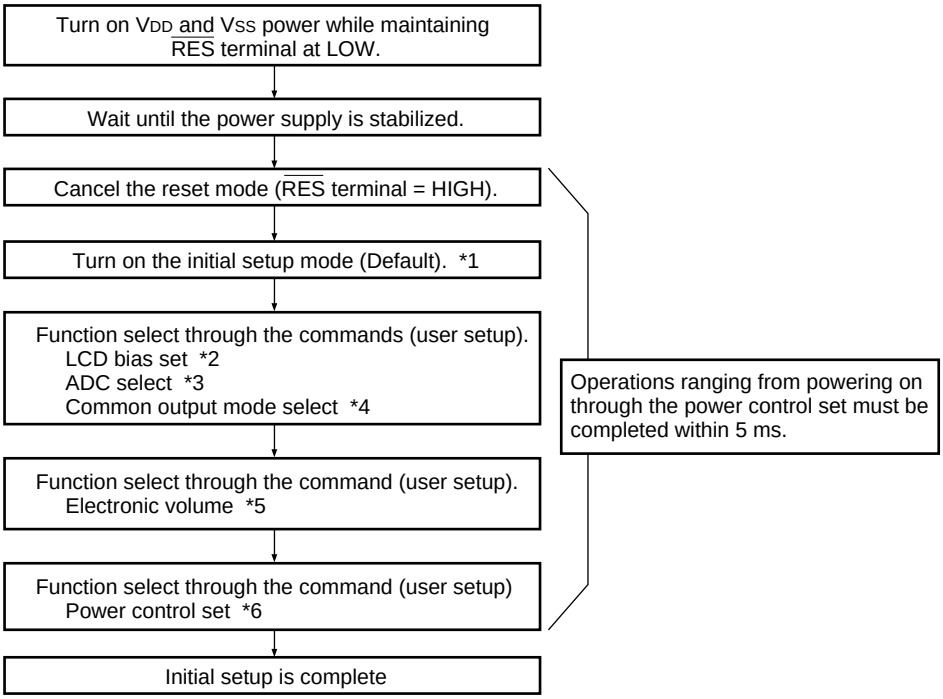
8. COMMAND SETTING (For Refrence)

Instruction Setup Examples

Initial setup

Note: As power is turned on, this IC outputs non-LCD-drive potentials V_2 – V_6 from SEG terminal (generates output for driving the LCD) and V_1 – V_4 from COM terminal (also used for generating the LCD drive output). If charge remains on the smoothing capacitor being inserted between the above LCD driving terminals, the display screen can be blacked out momentarily. In order to avoid this trouble, it is recommended to employ the following powering on procedure.

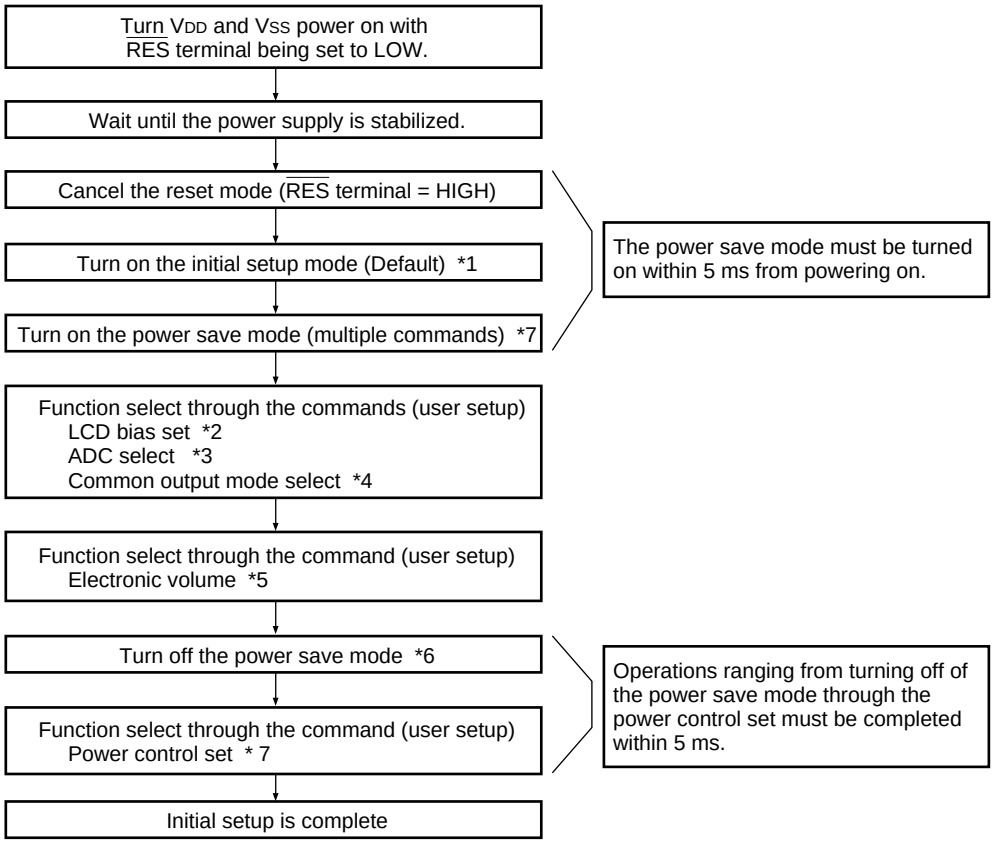
- **When the built-in power is used immediately after the main power is turned on:**



* This duration of 5 ms depends on the panel characteristics as well as capacity of the capacitor concerned.

Notes: *1: Refer to the “Reset Circuit” in the Function Description.
*2: Refer to the “LCD Bias Set” in the Command Description (11).
*3: Refer to the “ADC Select” in the Command Description (8).
*4: Refer to the “Output State Register Set” in the Command Description (15)
*5: Refer to the “Supply Circuit” in the Function Description and the “Electronic Volume Register Set” in the Command Description (17).
*6: Refer to the “Supply Circuit” in the Function Description and the “Power Control Set” in the Command Description (16).

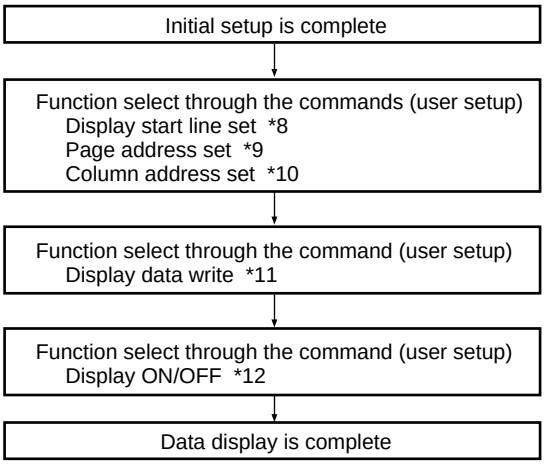
- **When the built-in power supply is not used immediately after the main power is turned on:**



* This duration of 5 ms depends on the panel characteristics as well as capacity of the capacitor concerned. Check them on the actual system.

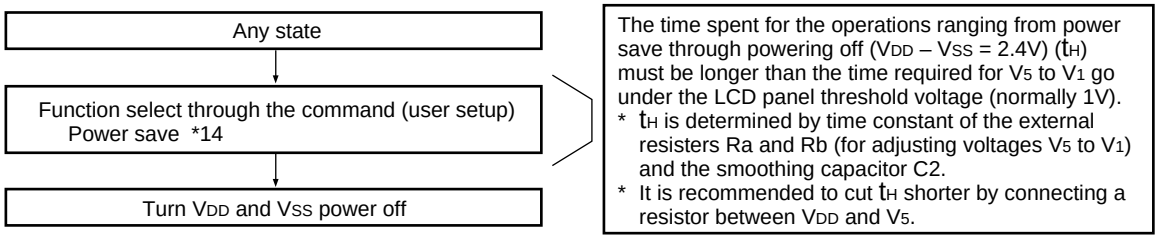
Notes: *1: Refer to the “Reset Circuit” in the Function Description.
*2: Refer to the “LCD Bias Set” in the Command Description (11).
*3: Refer to the “ADC Select” in the Command Description (8).
*4: Refer to the “Output State Register Set” in the Command Description (15)
*5: Refer to the “Supply Circuit” in the Function Description and the “Electronic Volume Register Set” in the Command Description (17).
*6: Refer to the “Supply Circuit” in the Function Description and the “Power Control Set” in the Command Description (16).
*7: You can select either the sleep mode or standby mode for the power save mode. Refer to the “Power Save (Multiple Commands)” in the Command Description (19).

- **Data Display**



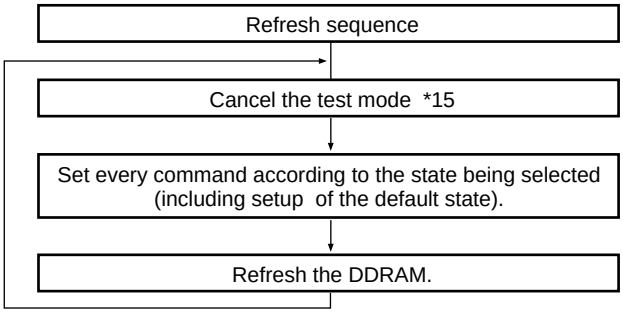
Notes: *8: Refer to the "Display Line Set" in the Command Description (2).
*9: Refer to the "Page Address Set" in the Command Description (3).
*10: Refer to the "Column Address Set" in the Command Description (4).
*11: Refer to the "Display Data Write" in the Command Description (6).
*12: Refer to the "Display ON/OFF" in the Command Description (1). It is recommended to avoid the all-white-display of the display start data.

- **Powering Off** *13



Notes: *13: This IC functions as the logic circuit of the power supplies $V_{DD} - V_{SS}$, and used for controlling the driver of LCD power supplies $V_{DD} - V_5$. Thus, if power supplies $V_{DD} - V_{SS}$ are turned off while voltage is still present on LCD power supplies $V_{DD} - V_5$, drivers (COM and SEG) may output uncontrolled voltage. Therefore, you are required to observe the following powering off procedure: Turn the built-in power supply off, then turn off the IC power supplies ($V_{DD} - V_{SS}$) only after making sure that potential of $V_5 - V_1$ is below the LCD panel threshold voltage level. Refer to the "Supply Circuit" in the Function Description.
*14: When the power save command is entered, you must not implement reset from $\overline{RES}$ terminal until $V_{DD} - V_{SS}$ power are turned off. Refer to the "Power Save" in the Command Description.

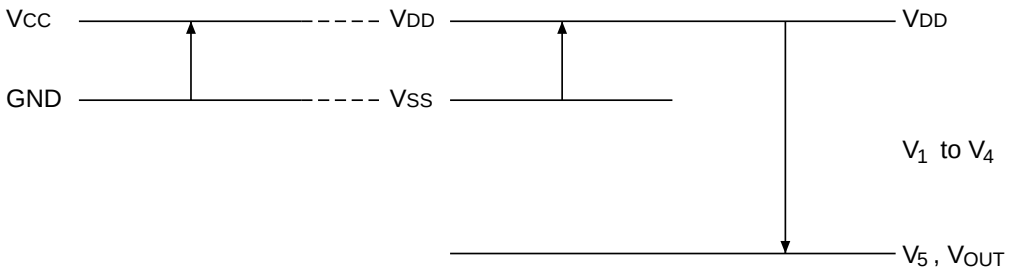
- **Refresh**
  It is recommended that the operating modes and display contents be refreshed periodically to prevent the effect of unexpected noise.



Notes: *15: Refer to the "Test Mode Cancellation" in the Command Description (21).

9. ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Supply voltage range		V_{DD}	–0.3 to +7.0	V
	Triple boosting		–0.3 to +6.0	
	Quadruple boosting		–0.3 to +4.5	
Supply voltage range (1) (V_{DD} Level)		V_5, V_{OUT}	–18.0 to +0.3	V
Supply voltage range (2) (V_{DD} Level)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage range		V_{IN}	–0.3 to V_{DD}+0.3	V
Output voltage range		V_O	–0.3 to V_{DD}+0.3	V
Operating temperature range		T_{OPR}	–40 to +85	°C
Storage temperature range	TCP	T_{STR}	–55 to +100	°C
	Bear chip		–55 to +125	



Notes: 1. V_1 to V_5, V_{OUT}, voltages are based on V_{DD}=0 V.
2. Voltages $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ must always be satisfied.
3. If an LSI exceeds its absolute maximum rating, it may be damaged permanently. It is desirable to use it under electrical characteristics conditions during general operation. Otherwise, an LSI malfunction or reduced LSI reliability may result.

10. ELECTRICAL CHARACTERISTICS

DC Characteristics

V_{SS} = 0 V, V_{DD} = 5 V ±10%, Ta = –40 to +85°C unless otherwise noted.

Item			Symbol	Condition		Min.	Typ.	Max.	Unit	Pin used
Power voltage (1)		Recommended Operation	V_{DD}			4.5	5.0	5.5	V	V_{SS} *1
		Operational				2.4	–	6.0		
Operating voltage (2)		Operational	V_5	V_{DD} level (V_{DD} = 0 V)		–16.0	–	–4.5	V	V_5 *2
		Operational	V_1, V_2	V_{DD} level (V_{DD} = 0 V)		0.4 × V_5	–	V_{DD}	V	V_1, V_2
		Operational	V_3, V_4	V_{DD} level (V_{DD} = 0 V)		V_5	–	0.6 × V_5	V	V_3, V_4
CMOS	HIGH-level input voltage		V_{IHC}			0.7 × V_{DD}	–	V_{DD}	V	*3
				V_{DD} = 2.7 V		0.8 × V_{DD}	–	V_{DD}		*3
	LOW-level input voltage		V_{ILC}			V_{SS}	–	0.3 × V_{DD}	V	*3
				V_{DD} = 2.7 V		V_{SS}	–	0.2 × V_{DD}		*3
	HIGH-level output voltage		V_{OHC}	I_{OH} = –1 mA		0.8 × V_{DD}	–	V_{DD}	V	*5
				V_{DD} = 2.7 V, I_{OH} = –0.5 mA		0.8 × V_{DD}	–	V_{DD}		*5
	LOW-level output voltage		V_{OLC}	I_{OL} = 1 mA		V_{SS}	–	0.2 × V_{DD}	V	*5
				V_{DD} = 2.7 V, I_{OL} = 0.5 mA		V_{SS}	–	0.2 × V_{DD}		*5
Schmitt	HIGH-level input voltage		V_{IHS}			0.85 × V_{DD}	–	V_{DD}		*4
				V_{DD} = 2.7 V		0.8 × V_{DD}	–	V_{DD}		*4
	LOW-level input voltage		V_{ILS}			V_{SS}	–	0.15 × V_{DD}		*4
				V_{DD} = 2.7 V		V_{SS}	–	0.2 × V_{DD}		*4
Input leakage current			I_{LI}	V_{IN} = V_{DD} or V_{SS}		–1.0	–	1.0	µA	*6
Output leakage current			I_{LO}			–3.0	–	3.0	µA	*7
LCD driver ON resistance			R_{ON}	Ta = 25°C	V_5 = –14.0 V	–	2.0	3.0	kΩ	SEG n COM n *8
				V_{DD} level	V_5 = –8.0 V	–	3.0	4.5		
Static current consumption			I_{SSQ}	V_{IN} = V_{DD} or V_{SS}		–	0.01	5.0	µA	V_{SS}
			I_{5Q}	V_5 = –18.0 V (V_{DD} level)		–	0.01	15.0	µA	V_5
Input pin capacity			C_{IN}	Ta = 25°C, f = 1 MHz		–	5.0	8.0	pF	*3 *4
Oscillation frequency			f_{OSC}	Ta = 25°C	V_{DD} = 5 V	18	22	26	kHz	*9
					V_{DD} = 2.7 V	18	22	26		

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Built-in power circuit	Input voltage	V_{DD}	Triple boosting	2.4	–	6.0	V	*10
			Quadruple boosting	2.4	–	4.5		
	Booster output voltage	V_{OUT}	Triple voltage conversion (V_{DD} level)	–18.0	–	–	V	V_{OUT}
	Voltage regulator operation voltage	V_{OUT}	(V_{DD} level)	–18.0	–	–6.0	V	V_{OUT}
	Voltage follower operation voltage	V5	(V_{DD} level)	–18.0	–	–6.0	V	*11
				–16.0	–	–4.5	V	
	Reference voltage	V_{REG}	Ta = 25°C (V_{DD} level)	–2.75	–2.55	–2.35	V	

For the mark *, refer to P. 1–25

Dynamic current consumption (1) when the built-in power supply is OFF

Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
S1D15300/ S1D15305	I_{DD} (1)	V_{DD} = 5.0V, $V_5 - V_{DD}$ = –8.0 V	—	24	40	µA	*12
		V_{DD} = 3.0V, $V_5 - V_{DD}$ = –8.0 V	—	22	35		
S1D15301		V_{DD} = 5.0V, $V_5 - V_{DD}$ = –11.0 V	—	40	65		
		V_{DD} = 3.0V, $V_5 - V_{DD}$ = –11.0 V	—	36	60		
S1D15302		V_{DD} = 5.0V, $V_5 - V_{DD}$ = –11.0 V	—	39	65		
		V_{DD} = 3.0V, $V_5 - V_{DD}$ = –11.0 V	—	32	55		
S1D15303		V_{DD} = 3.0V, $V_5 - V_{DD}$ = –5.0 V	—	20	35		
S1D15304		V_{DD} = 3.0V, $V_5 - V_{DD}$ = –5.0 V	—	20	35		

Dynamic current consumption (2) when the built-in power supply is ON

Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
S1D15300/ S1D15305	I_{DD} (1)	V_{DD} = 5.0V, $V_5 - V_{DD}$ = –8.0 V, dual boosting	—	41	70	µA	*13
		V_{DD} = 3.0V, $V_5 - V_{DD}$ = –8.0 V, triple boosting	—	48	80		
S1D15301		V_{DD} = 5.0V, $V_5 - V_{DD}$ = –11.0 V, triple boosting	—	96	160		
		V_{DD} = 3.0V, $V_5 - V_{DD}$ = –11.0 V, quadruple boosting	—	118	190		
S1D15302		V_{DD} = 5.0V, $V_5 - V_{DD}$ = –11.0 V, triple boosting	—	95	160		
		V_{DD} = 3.0V, $V_5 - V_{DD}$ = –11.0 V, quadruple boosting	—	114	190		
S1D15303		V_{DD} = 3.0V, $V_5 - V_{DD}$ = –5.0 V, dual boosting	—	30	50		
S1D15304		V_{DD} = 3.0V, $V_5 - V_{DD}$ = –5.0 V, dual boosting	—	32	55		

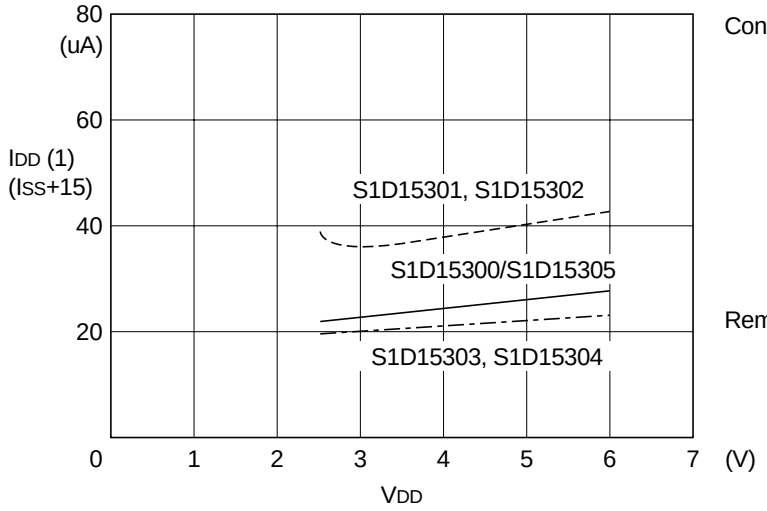
Current consumption during Power Save mode

V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
During sleep	I_{DDS1}	S1D15300, S1D15301, S1D15302	—	0.01	1	µA	
During standby	I_{DDS2}	S1D15300, S1D15301, S1D15302	—	10	20		

Typical current consumption characteristics (reference data)

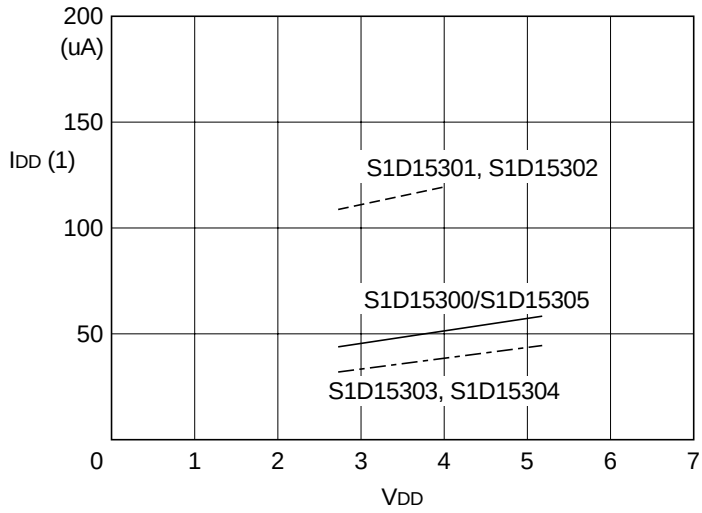
- Dynamic current consumption (1) when LCD external power mode lamp is ON



Condition: The built-in power supply is OFF and an external power supply is used.
S1D15300/S1D15305 V_5-V_{DD}=–8.0V
S1D15301 V_5-V_{DD}=–11.0V
S1D15302 V_5-V_{DD}=–11.0V
S1D15303 V_5-V_{DD}=–6.0V
S1D15304 V_5-V_{DD}=–6.0V
Ta=25°C

Remarks: ✻12

- Dynamic current consumption (2) when the LCD built-in power circuit lamp is ON



Condition: The built-in power circuit is ON.
S1D15300/S1D15305: V5-VDD=–8.0 V, triple boosting
S1D15301: V5-VDD=–11.0 V, quadruple boosting
S1D15302: V5-VDD=–11.0 V, quadruple boosting
S1D15303: V5-VDD=–5.0 V, dual boosting
S1D15304: V5-VDD=–5.0 V, dual boosting
Ta=25°C

Remarks: ✻13

*1 Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the microprocessor.
*2 V_{DD} and V_5 operating voltage range. (Refer to Fig. 10.)
The operating voltage range applies if an external power supply is used.
*3 A0, D0 - D5, D6, D7 (SI), $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, FR, M/S, C86, P/S and $\overline{DOF}$ pins
*4 CL, SCL (D6) and $\overline{RES}$ pins
*5 D0 - D5, D6, D7 (SI), FR, FRS, DYO, $\overline{DOF}$ and CL pins
*6 A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, M/S, $\overline{RES}$, C86 and P/S pins
*7 Applies when the D0 - D7, FR, CL, DYO and $\overline{DOF}$ pins are in high impedance,
*8 Resistance value when 0.1 V is applied between the output pin SEGn or COMn and each power supply pin (V1, V2, V3, V4). This is specified in the operating voltage (2) range.
R ON = 0.1 V/ΔI (ΔI: Current flowing when 0.1 V is applied in the ON status.)
*9 For the relationship between oscillation frequency and frame frequency, refer to Fig. 9.
*10 For triple or quadruple boosting using the on-chip power useing the primary-side power supply V_{DD} must be used within the input voltage range.
*11 The voltage regulator adjusts V_5 within the voltage follower operating voltage range.
*12, *13 Current that each IC unit consumes. It does not include the current of the LCD panel capacity, wiring capacity, etc.
This is current consumption under the conditions of display data = checker, display ON, S1D15300 = 1/33 duty (1/6 Bias), and S1D15301 and S1D15302 = 1/65 duty. (1/8 Bias)
*12 Applies to the case where the on-chip oscillator circuit is used and no access is made from the microprocessor.
*13 Applies to the case where the on-chip oscillator circuit and the on-chip power circuit are used and no access is made from the microprocessor.
The current flowing through voltage regulation resistors (R1, R2 and R3) is not included.
The current consumption, when the on-chip voltage booster is used, is for the power supply V_{DD}.

- Relationship between oscillation frequency and frame frequency

The relationship between oscillation frequency f_{OSC} and LCD frame frequency, f_F can be obtained by the following expression.

	Duty	f CL	f F
S1D15300	1/33	f OSC/8	f OSC/(8*33)
S1D15301 S1D15302	1/65	f OSC/4	f OSC/(4*65)
S1D15303	1/17	f OSC/8	f OSC/(8*17)
S1D15304	1/9	f OSC/8	f OSC/(8*9)
S1D15305	1/35	f OSC/8	f OSC/(8*35)

(f_F does not indicate the FR signal cycle but the AC cycle.)

Fig. 9

Relationship between clock (f_{CL}) and frame frequency f_F

- V_{SS} and V_5 operating voltage range

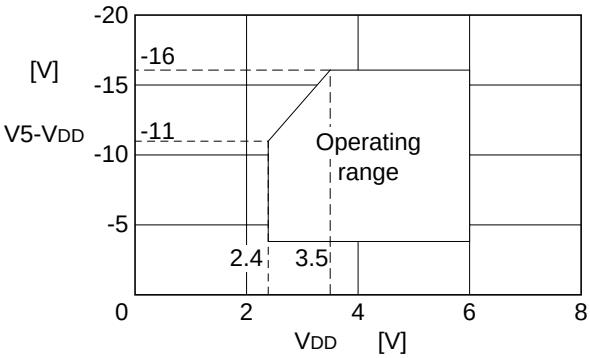
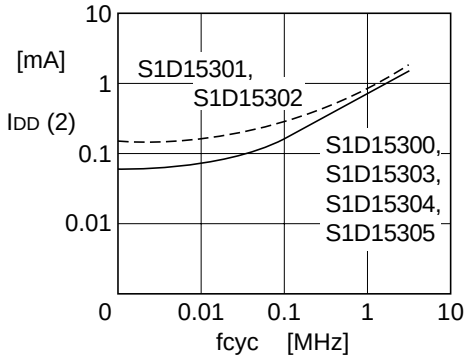


Fig 10

- Current consumption at access IDD (2) - Microprocessor access cycle



This indicates current consumption when data is always written on the checker pattern at fcyc. When no access is made, only IDD (1) occurs.

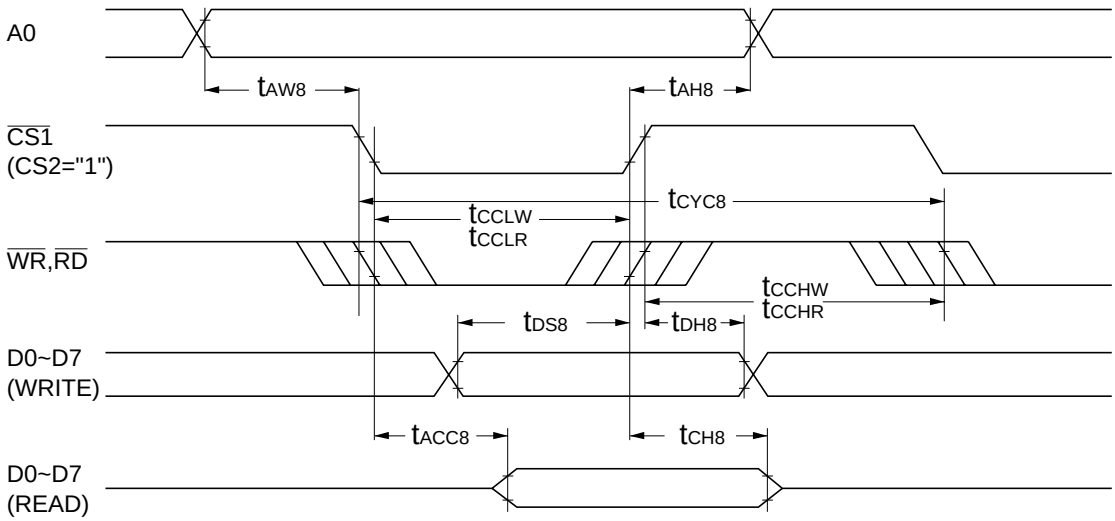
Condition: S1D15300/S1D15305 V_5-V_{DD}=-8.0V, triple boosting
S1D15301 V_5-V_{DD}=-11.0V, quadruple boosting
S1D15302 V_5-V_{DD}=-11.0V, quadruple boosting
S1D15303 V_5-V_{DD}=-6.0V, dual boosting
S1D15304 V_5-V_{DD}=-6.0V, dual boosting
Ta = 25¡C

Fig. 11

AC Characteristics

(1) System buses

Read/write characteristics I (8080-series microprocessor)



V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time	A0	t_{AHIGH8}		10	–	ns
Address setup time		t_{AW8}		10	–	ns
System cycle time		t_{CYC8}		166	–	ns
Control LOW pulse width(WR)	$\overline{WR}$	t_{CCLOWW}		30	–	ns
Control LOW pulse width(RD)	$\overline{RD}$	t_{CCLOWR}		70	–	ns
Control HIGH pulse width (WR)	$\overline{WR}$	$t_{CCHIGHW}$		100	–	ns
Control HIGH pulse width (RD)	$\overline{RD}$	$t_{CCHIGHR}$		70	–	ns
Data setup time		t_{DS8}		20	–	ns
Data hold time		t_{DHIGH8}		10	–	ns
$\overline{RD}$ access time	D0 to D7	t_{ACC8}	CL=100pF	–	70	ns
Output disable time		t_{CHIGH8}		10	50	ns

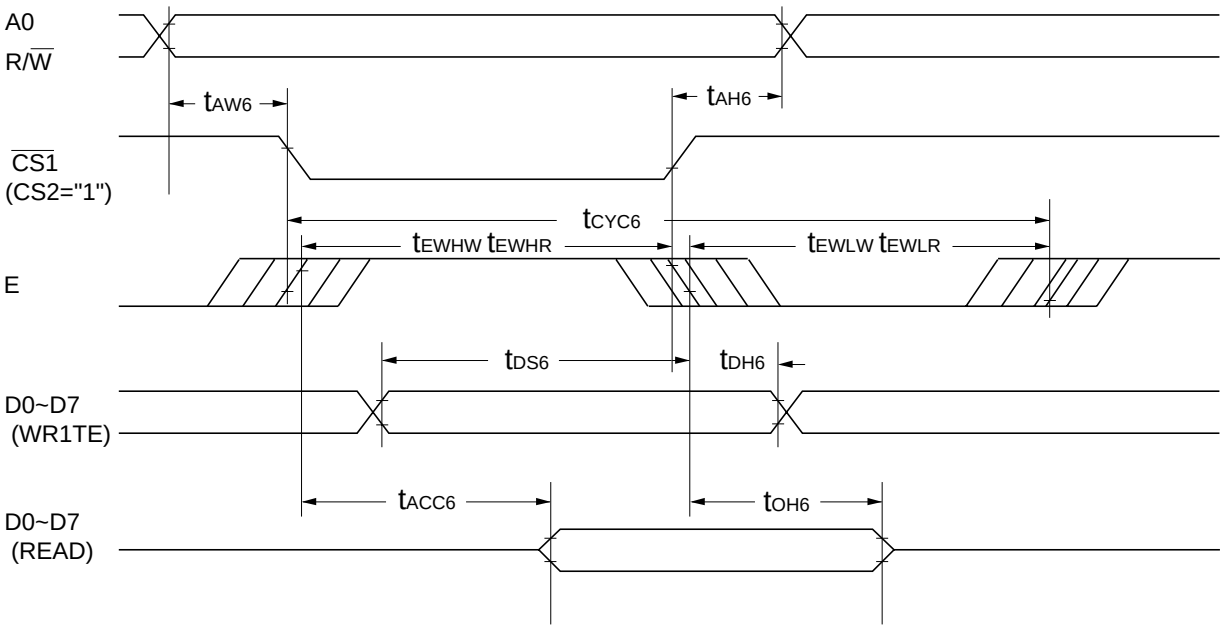
V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time	A0	t_{AH8}		19	–	ns
Address setup time		t_{AW8}		15	–	ns
System cycle time		t_{CYC8}		450	–	ns
Control LOW pulse width (WR)	$\overline{WR}$	t_{CCLW}		60	–	ns
Control LOW pulse width (RD)	$\overline{RD}$	t_{CCLR}		140	–	ns
Control HIGH pulse width (WR)	$\overline{WR}$	t_{CCHW}		200	–	ns
Control HIGH pulse width (RD)	$\overline{RD}$	t_{CCHR}		140	–	ns
Data setup time		t_{DS8}		40	–	ns
Data hold time		t_{DH8}		15	–	ns
$\overline{RD}$ access time	D0 to D7	t_{ACC8}	CL=100pF	–	140	ns
Output disable time		t_{CH8}		10	100	ns

Notes: 1. The input signal rise/fall time (t_r, t_f) is specified at 15 ns or less.
When system cycle time is used at a high speed, it is specified by $t_r + t_f \leq (t_{CYC8} - t_{CCLW})$ or
$t_r + t_f \leq (t_{CYC8} - t_{CCLR} - t_{CCHR})$.
2. Every timing is specified on the basis of 20% and 80% of V_{DD}.
3. t_{EWHR} and t_{EWHW} are specified by the overlap period in which $\overline{CS1}$ is "0" (CS2 = "1") and $\overline{WR}$ and $\overline{RD}$ are "0".
4. When it is expected that Vss ranges from -2.4 V to -4.5 V during the operation, increase all the above specifications from -2.7 V to -4.5 V by 30% before the operation.

(2) System buses

Read/write characteristics II (6800-series microprocessor)



V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

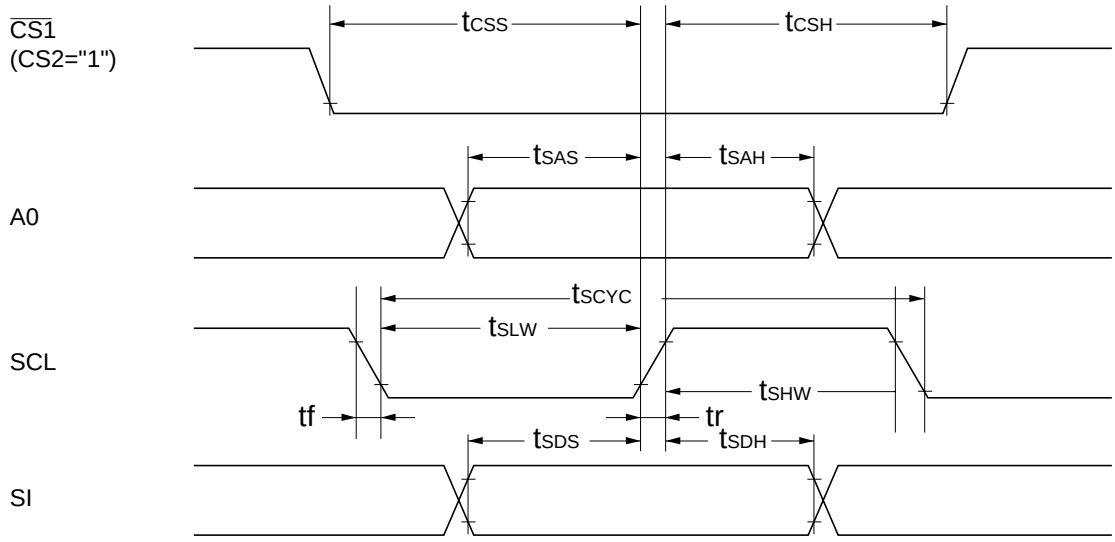
Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time			t_{CYC6}		166	–	ns
Address setup time Address hold time		A0 W/R	t_{AW6} t_{AH6}		10 10	– –	ns ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		20 10	– –	ns ns
Output disable time Access time			t_{OH6} t_{ACC6}	CL=100pF	10 –	50 70	ns ns
Enable	READ	E	t_{EWHR}		70	–	ns
LOW pulse width	WRITE		t_{EWHW}		30	–	ns
Enable	READ	E	t_{EWLR}		70	–	ns
HIGH pulse width	WRITE		t_{EWLW}		100	–	ns

V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C

Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time			t_{CYC6}		450	–	ns
Address setup time Address hold time		A0 R/W	t_{AW6} t_{AH6}		15 19	– –	ns ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		40 15	– –	ns ns
Output disable time Access time			t_{OH6} t_{ACC6}	CL=100pF	10 –	100 140	ns ns
Enable	READ	E	t_{EWHR}		140	–	ns
LOW pulse width	WRITE		t_{EWHW}		60	–	ns
Enable	READ	E	t_{EWLR}		140	–	ns
HIGH pulse width	WRITE		t_{EWLW}		200	–	ns

Notes: 1. The input rise/fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is used at a high speed, it is specified by $t_r + t_f \leq (t_{CYC6} - t_{EWLW} - t_{EWHW})$ or $tr + tf \leq (t_{CYC6} - t_{EWLR} - t_{EWHR})$.
2. Every timing is specified on the basis of 20% and 80% of V_{DD}.
3. t_{EWHR} and t_{EWHW} are specified by the overlap period in which CS1 is "0" (CS2 = "1") and E is "1".
4. When it is expected that Vss ranges from -2.4 V to -4.5 V during the operation, increase all the above specifications from -2.7 V to -4.5 V by 30% before the operation.

(3) Serial interface



V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

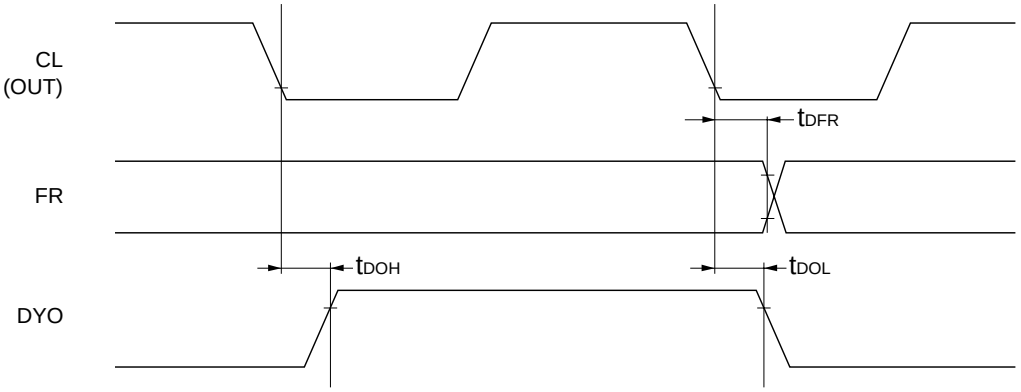
Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle	SCL	t_{SCYC}		250	–	ns
Serial clock HIGH pulse width		t_{SHW}		100	–	ns
Serial clock LOW pulse width		t_{SLW}		75	–	ns
Address setup time	A0	t_{SAS}		50	–	ns
Address hold time		t_{SAH}		200	–	ns
Data setup time	SI	t_{SDS}		50	–	ns
Data hold time		t_{SDH}		50	–	ns
$\overline{CS}$ serial clock time	CS	t_{CSS}		30	–	ns
		t_{CSH}		100	–	

V_{DD} = 2.7 to 4.5V, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle	SCL	t_{SCYC}		500	–	ns
Serial clock HIGH pulse width		t_{SHW}		200	–	ns
Serial clock LOW pulse width		t_{SLW}		150	–	ns
Address setup time	A0	t_{SAS}		100	–	ns
Address hold time		t_{SAH}		400	–	ns
Data setup time	SI	t_{SDS}		100	–	ns
Data hold time		t_{SDH}		100	–	ns
$\overline{CS}$ serial clock time	CS	t_{CSS}		60	–	ns
		t_{CSH}		200	–	

Notes: 1. The input signal rise and fall times must be within 15 nanoseconds.
2. All signal timings are limited based on 20% and 80% of V_{DD} voltage.
3. When it is expected that Vss ranges from -2.4 V to -4.5 V during the operation, increase all the above specifications from -2.7 V to -4.5 V by 30% before the operation.

(4) Display control timing



Output timing V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

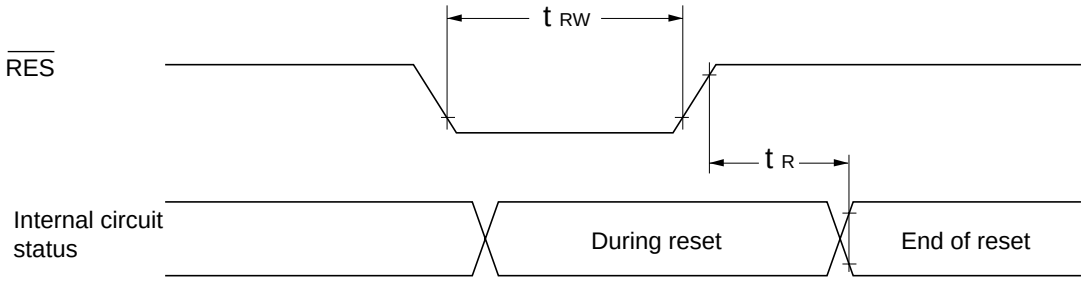
Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
FR delay time	FR	t_{DFR}	CL = 50 pF	–	10	40	ns
DYO HIGH delay time	DYO	t_{DOH}		–	40	100	ns
DYO LOW delay time		t_{DOL}		–	40	100	ns

Output timing V_{SS} = 0 V, V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
FR delay time	FR	t_{DFR}	CL = 50 pF	–	15	80	ns
DYO HIGH delay time	DYO	t_{DOH}		–	70	200	ns
DYO LOW delay time		t_{DOL}		–	70	200	ns

Notes: 1. The otput timing is valid in master mode.
2. Every timing is specified on the basis of 20% and 80% of V_{DD}.

(5) Reset timing



V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_R		0.5	–	–	µs
Reset LOW pulse width	$\overline{RES}$	t_{RW}		0.5	–	–	µs

V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C

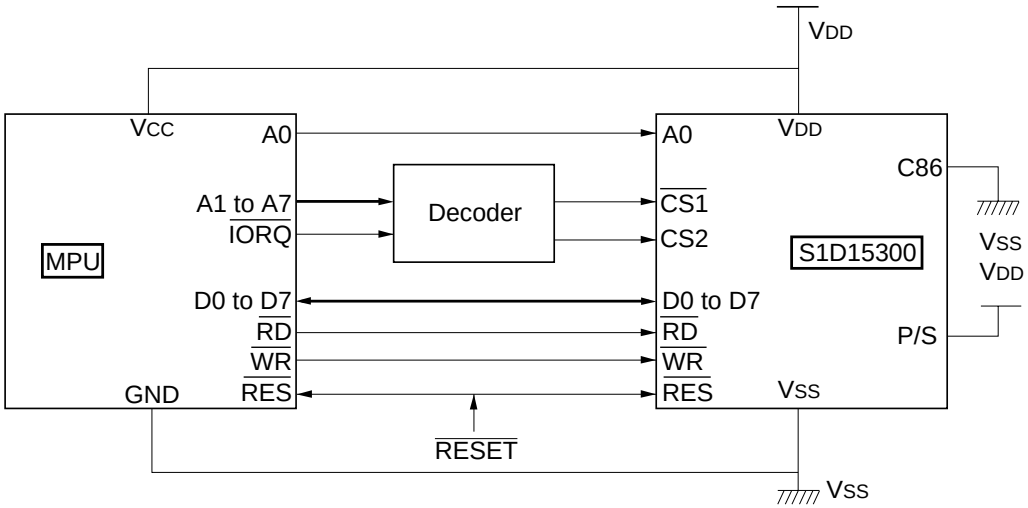
Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_R		1.0	–	–	µs
Reset LOW pulse width	$\overline{RES}$	t_{RW}		1.0	–	–	µs

Note: The reset timing is specified on the basis of 20% and 80% of V_{DD}.

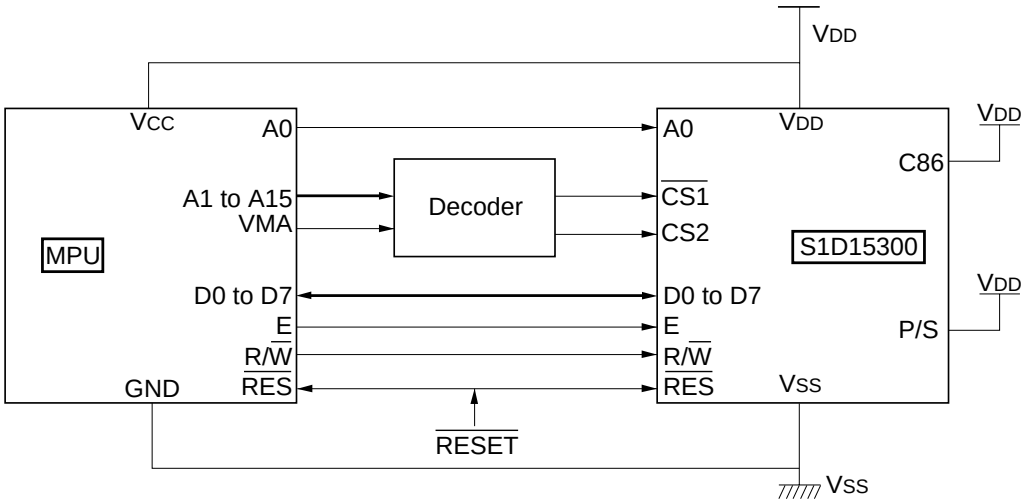
11. MPU INTERFACE (For Reference)

The S1D15300 series chips can directly connect to 8080 and 6800-series microprocessors. Also, serial interfacing requires less signal lines between them. When multiple chips are used in the S1D15300 series they can be connected to the microprocessor and one of them can be selected by Chip Select.

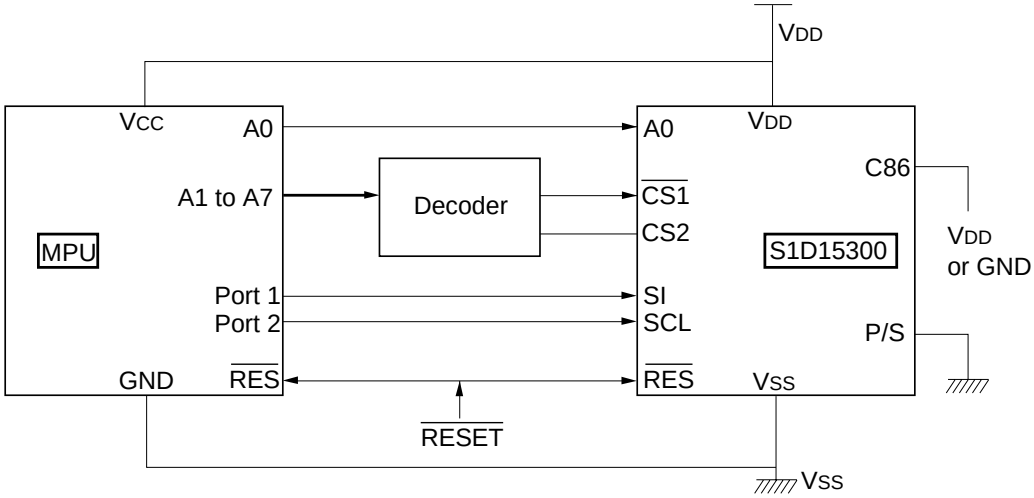
8080-series microprocessors



6800-series microprocessors



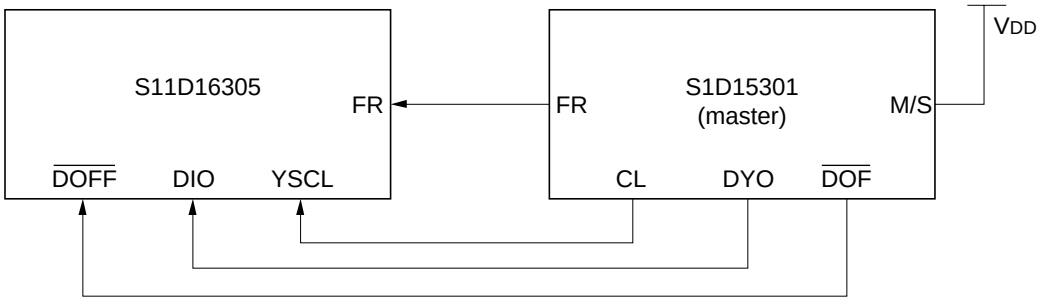
Serial interface



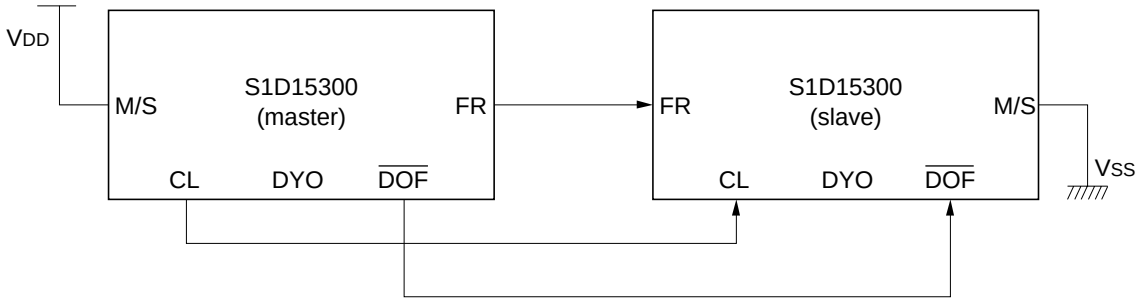
12. CONNECTION BETWEEN LCD DRIVERS

The LCD panel display area can easily be expanded by use of multiple S1D15300 series chips. The S1D15300 series can also be connected to the common driver (S1D16305).

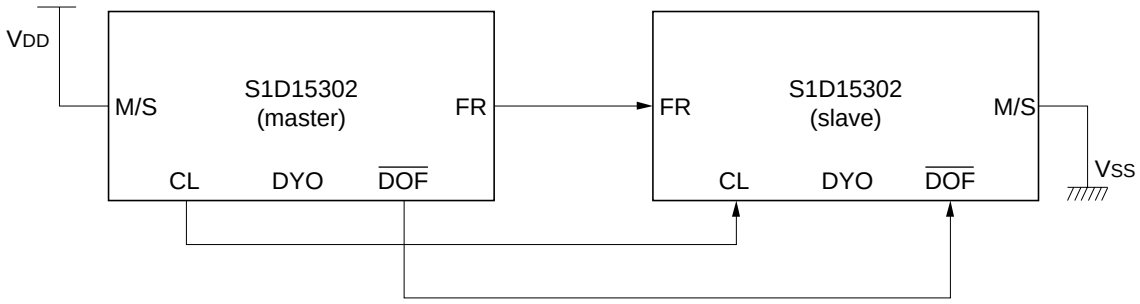
S1D15301 to S1D16305 (S1D16305)

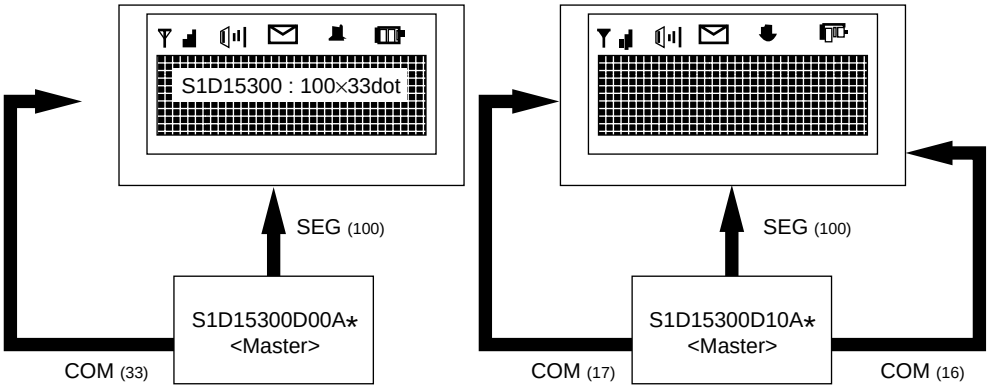


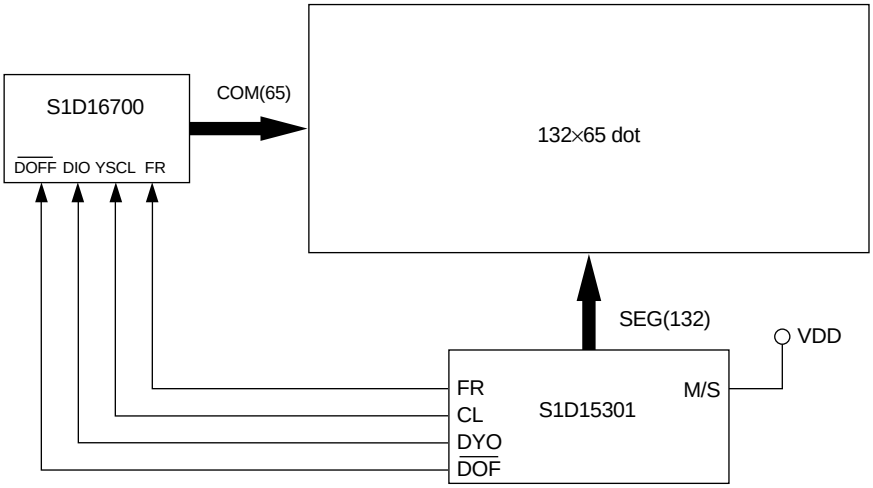
S1D15300 to S1D15301

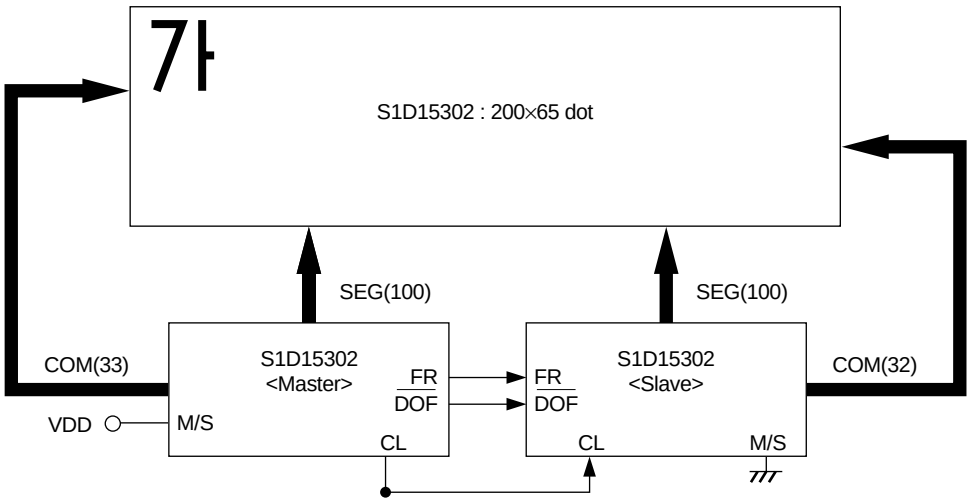


S1D15302 to S1D15302



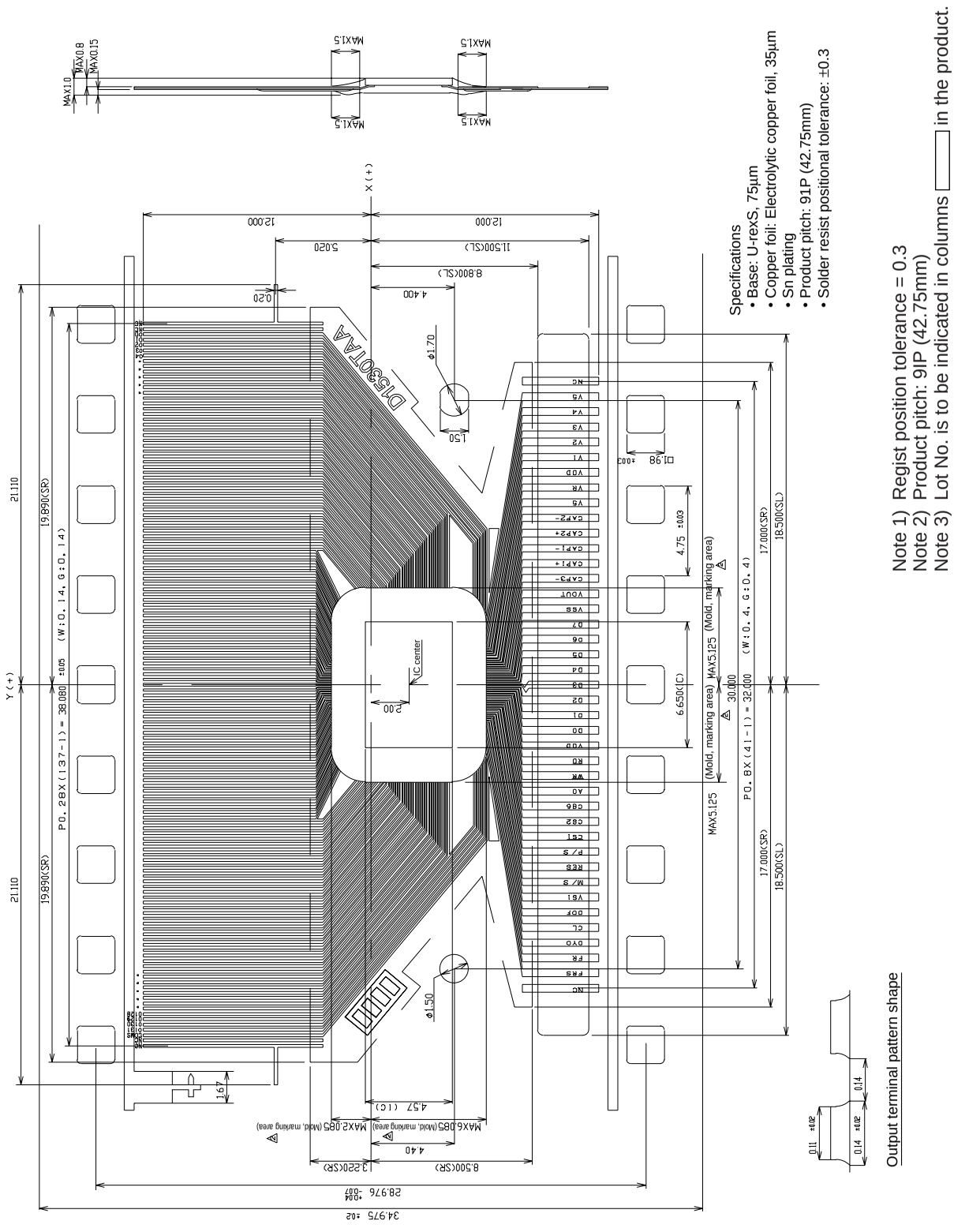

S1D15300 : 100×33dot
SEG (100)
S1D15300D00A*
<Master>
COM (33)
SEG (100)
S1D15300D10A*
<Master>
COM (17)
COM (16)


S1D16700
DOFF DIO YSCL FR
COM(65)
132×65 dot
SEG(132)
VDD
FR
CL
DYO
DOF
S1D15301
M/S


S1D15302 : 200×65 dot
SEG(100)
SEG(100)
COM(33)
VDD
S1D15302
<Master>
FR
DOF
M/S
CL
FR
DOF
CL
S1D15302
<Slave>
M/S
COM(32)

Dimensional outline drawing of the flexible substrate

(an example) The dimensions are subject to change without prior notice.



6. S1D15400 Series

Contents

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1. DESCRIPTION

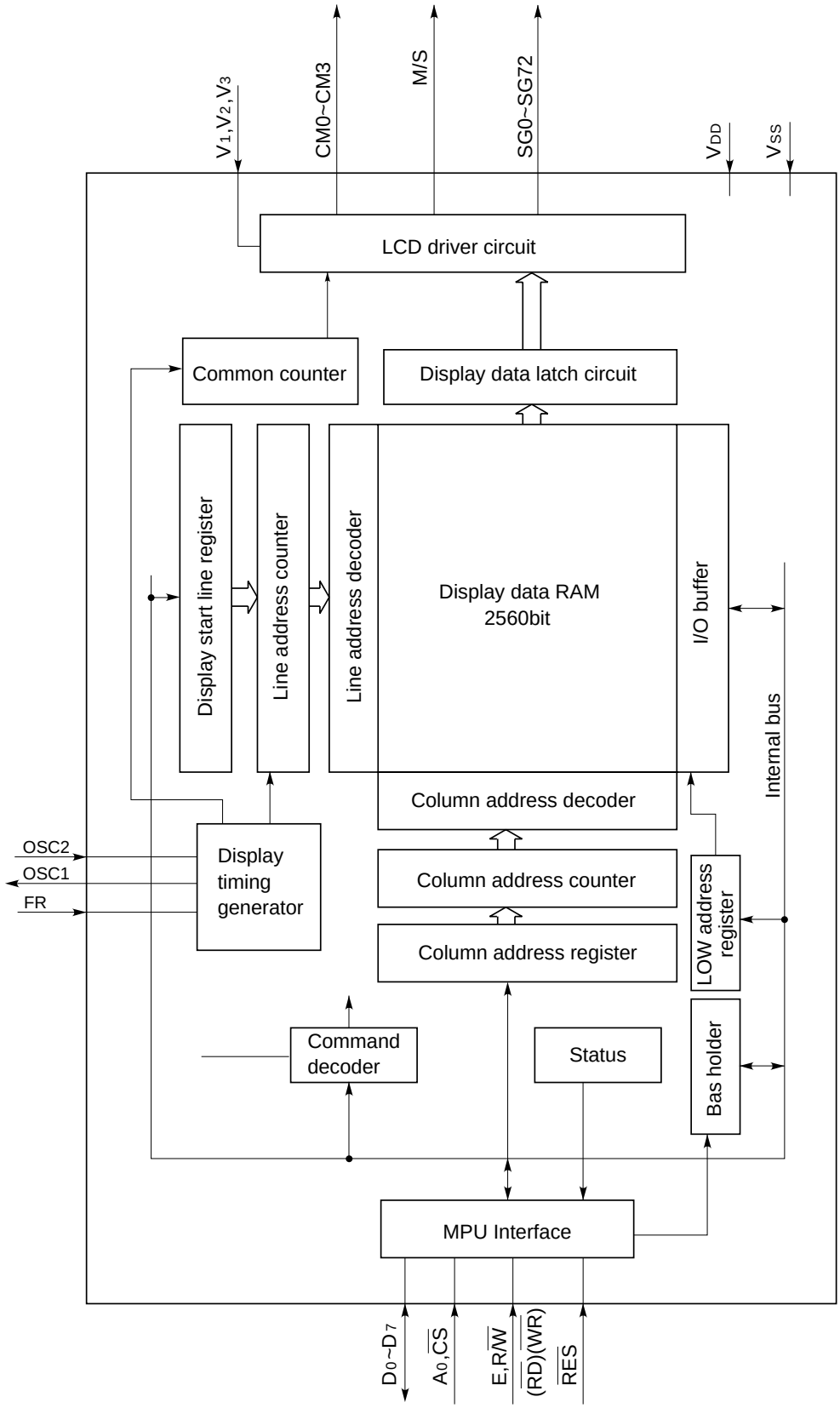
The S1D15400 is a segment LCD driver intended for use with medium size LCD panels.
The driver generates LCD drive signals from data supplied by an MPU over a high speed, 8-bit bus, 4-bit bus and stored in its internal display RAM.
The S1D15400 incorporates innovative circuit design strategies, to achieve very low power consumption at a wide range of operating voltages, and a rich command set. These features give the designer a flexible means of implementing small to medium size LCD displays for compact, low power systems.

2. FEATURES

- Fast 8-bit MPU interface compatible with 80- and 68-family microcomputers
- Rich command set
- 73 segment drive outputs
- 4 common drive outputs
- Selectable 1/3 or 1/4 duty cycle
- Low power consumption -70 μW maximum
- Wide range of supply voltages, V_{SS} –2.4 V to –7.0 V
- Implemented in CMOS
- Choice of packages
  —S1D15400F00A∗ : 100-pin QFP
  —S1D15400D00A∗ : Al-pad chip
  —S1D15400D00B∗ : Au-bump chip

Clock Source	f_{CL}	Frame Frequency
External clock	4 kHz	85/64 Hz
Internal osc.	18 kHz	375/281 Hz

3. BLOCK DIAGRAM



4. PIN LAYOUT

For chip pad locations see section 4.3, Mechanical Specifications.

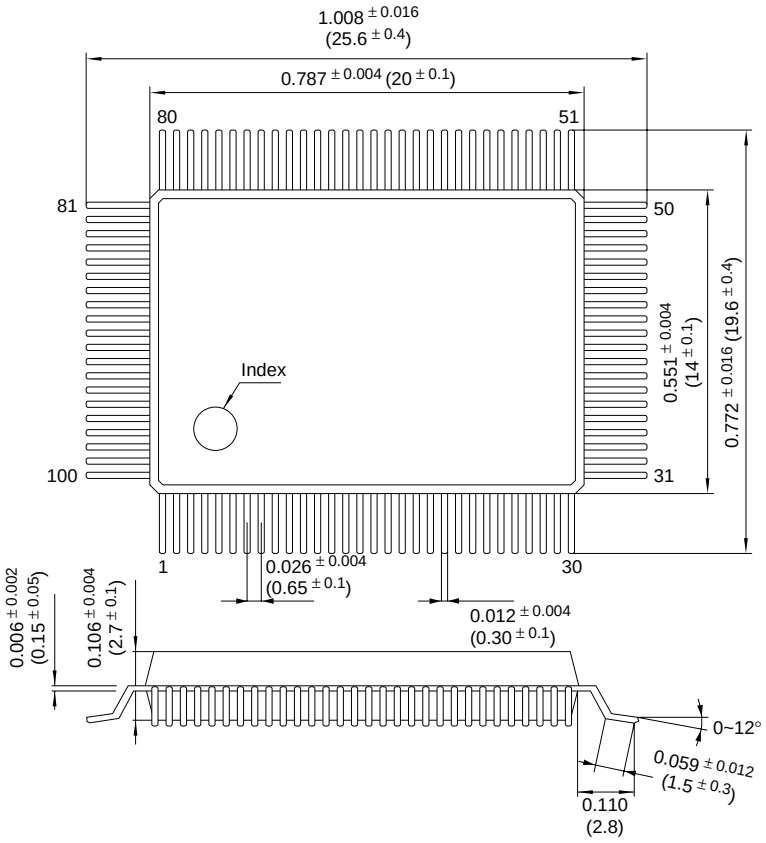
Number	Name	Number	Name	Number	Name	Number	Name
1	SEG71	26	SEG46	51	SEG21	76	E ($\overline{RD}$)
2	SEG70	27	SEG45	52	SEG20	77	R/$\overline{W}$ ($\overline{WR}$)
3	SEG69	28	SEG44	53	SEG19	78	V_{SS}
4	SEG68	29	SEG43	54	SEG18	79	DB0
5	SEG67	30	SEG42	55	SEG17	80	DB1
6	SEG66	31	SEG41	56	SEG16	81	DB2
7	SEG65	32	SEG40	57	SEG15	82	DB3
8	SEG64	33	SEG39	58	SEG14	83	DB4
9	SEG63	34	SEG38	59	SEG13	84	DB5
10	SEG62	35	SEG37	60	SEG12	85	DB6
11	SEG61	36	SEG36	61	SEG11	86	DB7
12	SEG60	37	SEG35	62	SEG10	87	V_{DD}
13	SEG59	38	SEG34	63	SEG9	88	$\overline{RES}$
14	SEG58	39	SEG33	64	SEG8	89	FR
15	SEG57	40	SEG32	65	SEG7	90	V3
16	SEG56	41	SEG31	66	SEG6	91	$\overline{CS}$
17	SEG55	42	SEG30	67	SEG5	92	NC
18	SEG54	43	SEG29	68	SEG4	93	M/$\overline{S}$
19	SEG53	44	SEG28	69	SEG3	94	V2
20	SEG52	45	SEG27	70	SEG2	95	V1
21	SEG51	46	SEG26	71	SEG1	96	COM0
22	SEG50	47	SEG25	72	SEG0	97	COM1
23	SEG49	48	SEG24	73	A0	98	COM2
24	SEG48	49	SEG23	74	OSC1	99	COM3
25	SEG47	50	SEG22	75	OSC2	100	SEG72

Duty	Pin	
	98	99
1/4	COM2	COM3
1/3	NC	COM2

Mechanical Specifications

S1D15400F00A* Flat Pack

Dimensions: inches (mm)

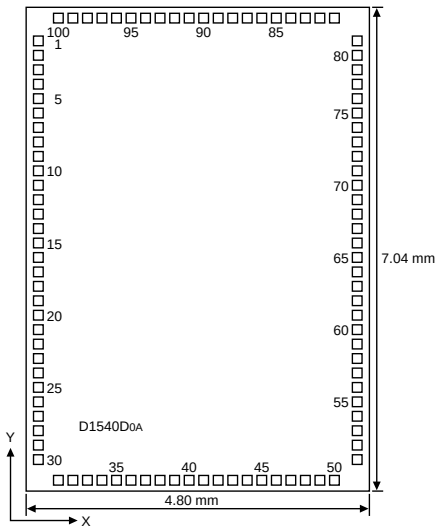


5. PAD

S1D15400D Pad Layout

Al-pad chip
- Die size: 4.80 mm × 7.04 mm × 0.525 mm
- Pad size: 100 × 100 μm

Au-bump chip
- Minimum bump pitch: 199 μm
- Bump height: 20 μm +10/–5 μm
- Bump size: 132 × 111 μm ±20 μm



Pad Center Coordinates

Pad		X	Y
Number	Name		
1	SEG71	159	6507
2	SEG70	159	6308
3	SEG69	159	6108
4	SEG68	159	5909
5	SEG67	159	5709
6	SEG66	159	5510
7	SEG65	159	5310
8	SEG64	159	5111
9	SEG63	159	4911
10	SEG62	159	4712
11	SEG61	159	4512
12	SEG60	159	4169
13	SEG59	159	3969
14	SEG58	159	3770
15	SEG57	159	3570
16	SEG56	159	3371
17	SEG55	159	3075
18	SEG54	159	2876
19	SEG53	159	2676
20	SEG52	159	2477
21	SEG51	159	2277
22	SEG50	159	2078
23	SEG49	159	1878
24	SEG48	159	1679
25	SEG47	159	1479
26	SEG46	159	1280
27	SEG45	159	1080
28	SEG44	159	881
29	SEG43	159	681
30	SEG42	159	482
31	SEG41	504	159
32	SEG40	704	159
33	SEG39	903	159
34	SEG38	1103	159

Pad		X	Y
Number	Name		
35	SEG37	1302	159
36	SEG36	1502	159
37	SEG35	1701	159
38	SEG34	1901	159
39	SEG33	2100	159
40	SEG32	2300	159
41	SEG31	2499	159
42	SEG30	2699	159
43	SEG29	2898	159
44	SEG28	3098	159
45	SEG27	3297	159
46	SEG26	3497	159
47	SEG25	3696	159
48	SEG24	3896	159
49	SEG23	4095	159
50	SEG22	4295	159
51	SEG21	4641	482
52	SEG20	4641	681
53	SEG19	4641	881
54	SEG18	4641	1080
55	SEG17	4641	1280
56	SEG16	4641	1479
57	SEG15	4641	1679
58	SEG14	4641	1878
59	SEG13	4641	2078
60	SEG12	4641	2277
61	SEG11	4641	2477
62	SEG10	4641	2676
63	SEG9	4641	2876
64	SEG8	4641	3075
65	SEG7	4641	3275
66	SEG6	4641	3474
67	SEG5	4641	3674
68	SEG4	4641	3948

Pad		X	Y
Number	Name		
69	SEG3	4641	4148
70	SEG2	4641	4347
71	SEG1	4641	4547
72	SEG0	4641	4789
73	A0	4641	5048
74	OSC1	4641	5247
75	OSC2	4641	5447
76	E ($\overline{RD}$)	4641	5646
77	R/$\overline{W}$ ($\overline{WR}$)	4641	5846
78	VSS	4641	6107
79	DB0	4641	6307
80	DB1	4641	6506
81	DB2	4295	6884
82	DB3	4095	6884
83	DB4	3896	6884
84	DB5	3696	6884
85	DB6	3497	6884
86	DB7	3297	6884
87	V_{DD}	3098	6884
88	$\overline{RES}$	2898	6884
89	FR	2699	6884
90	V3	2499	6884
91	$\overline{CS}$	2300	6884
92	NC	2100	6884
93	M/$\overline{S}$	1901	6884
94	V2	1701	6884
95	V1	1502	6884
96	COM0	1302	6884
97	COM1	1103	6884
98	COM2	903	6884
99	COM3	704	6884
100	SEG72	504	6884
—	—	—	—
—	—	—	—

6. PIN DESCRIPTION

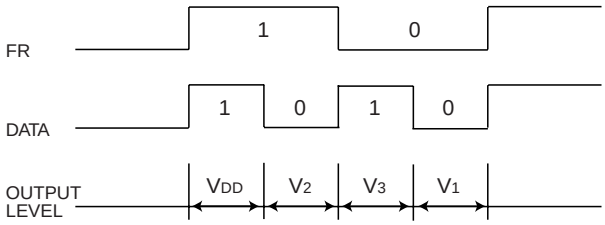
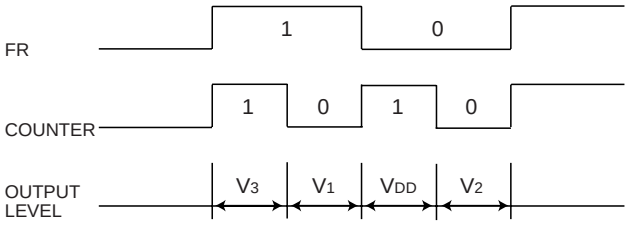
Power Terminals

Terminal name	Description
V_{DD}	Connects to a +5-V power supply. Used in common with the MPU power terminal.
V_{SS}	A 0-V terminal connected to the system GND.
V_1,V_2,V_3	Multi-level power supply terminals for driving the LCD panel. Through divisions by resistors or impedance conversion with an operational amplifier, they apply a voltage determined by the LCD cells.Electric potential is determined depending on VDD. The following relationship must be observed. $V_{DD} \geq V_1 \geq V_2 \geq V_3$

System Bus Connection Terminals

D_7-D_0	Three-state I/O terminals They comprise an 8-bit bi-directional data bus, and connected to an 8- or a 16-bit standard MPU data bus.
A_0	Input terminal Typically, the least significant bit of an MPU address bus is connected to discriminate between data and commands. 0: Represents that D_0-D_7 output display control commands. 1: Represents that D_0-D_7 output data to be displayed.
$\overline{RES}$	Input By setting $\overline{RES}$ to “ ⎍ ,” series 68 and 80 MPUs are initialized respectively. MPUs are reset when a RES signal edge is detected. After initialization, the type of an interface to the 68/80 MPUs is selected depending on the input level. HIGH: Interface to series 68 MPU is selected. LOW : Interface to series 80 MPU is selected.
$\overline{CS}$	Input activated at the LOW level A terminal for chip selection signals. Typically, signals that result from decoding of address bus signals are input.
E($\overline{RD}$)	<When series 68 MPU is connected> Input activated at the HIGH level An enable clock input terminal for the MPU. <When series 80 MPU is connected> Input activated at the LOW level A terminal for $\overline{RD}$ signal from the MPU. The data bus on the S1D15400 outputs signals while the $\overline{RD}$ signal is at the LOW level.
R/$\overline{W}$($\overline{WR}$)	<When series 68 MPU is connected> Input An input terminal for read/write control signals. R/$\overline{W}$ = HIGH: Read R/$\overline{W}$ = LOW: Write <When series 80 MPU is connected> Input activated at the LOW level A terminal for WR signal from the MPU. The signals on the data bus are fetched at a rising edge of the $\overline{WR}$ signal.

LCD Panel Driving Circuit Terminals

<table>
<tr><th>Terminal name</th><th>Description</th></tr>
<tr><td>OSC1</td><td>A terminal for connecting a resistor for internal oscillation.</td></tr>
<tr><td>OSC2</td><td>When M/S = 0, internal oscillation is prohibited, making OCS2 serve as a clock input terminal in the opposite phase to OCS1. During the power-saving mode, oscillation and clock input are prohibited, making OCS2 work as a high-impedance terminal. (See the explanation of functions.)</td></tr>
<tr><td>FR</td><td>Input/output terminal
An input/output terminal for AC control signals for the LCD panel.
M/S = 1: Output
M/S = 0: Input</td></tr>
<tr><td>SEG0-SEG72</td><td>Output terminal
Output for driving the LCD segments. Depending on the combination of the FR signal and the contents of the display RAM, one of the V_{DD}, V_1, V_2, and V_3 levels is selected.
 
</td></tr>
<tr><td>COM0-COM3</td><td>Output terminals (The function of the COM2 and COM3 output terminals changes depending on the duty select command.)
They are common (LOW) output terminals for driving the LCD panel. Depending on the combination of the FR signal and the output from the common counter, one of the V_{DD}, V_1, V_2, and V_3 levels is selected.
 
</td></tr>
<tr><td>MS</td><td>Counter output
Output level
Input
A terminal that selects whether the MPU operates as a master or slave of the S1D15400. It connects to V_{DD} or V_{SS}. This terminal determines the function of the FR, OSC1, and OSC2 terminals.
M/S = V_{DD}: Master
= V_{SS}: Slave
<table>
<tr><th>M/S</th><th>FR</th><th>OSC1</th><th>OSC2</th><th>COMOutput</th></tr>
<tr><td>VDD</td><td>output</td><td>Input</td><td>output</td><td>Enabled</td></tr>
<tr><td>VDD</td><td>output</td><td>Input</td><td>output</td><td>Enabled</td></tr>
</table>
* When the FR signal is used to establish synchronization between the master and slave ICs, both of them will output the same waveforms from the COM terminal.</td></tr>
</table>

7. BLOCK DESCRIPTION

System Bus

Data transfer

The S1D15400 driver uses the A0, E (or $\overline{RD}$) and R/W (or $\overline{WR}$) signals to transfer data between the system MPU and internal registers. The combinations used are given in the table below.

In order to match the timing requirements of the MPU with those of the display data RAM and control registers, all data is latched into and out of the driver. This introduces a one cycle delay between a read request for data and the data arriving. For example, when the MPU executes a read cycle to access display RAM, the current contents of the latch are placed on the system data bus while the desired contents of the display RAM are moved into the latch.

By using an MPU data bus I/O latch the display data RAM access timing is determined by the driver cycle time, t_{cyc}, not by the RAM access time. In general this strategy leads to faster data transfers between the driver and the MPU.

If the MPU access frequency is likely to exceed $1/t_{cyc}$, then the designer has the choice of inserting NOPs into the access loop or polling the driver, by reading the busy flag, to see if it will accept new data or instructions.

This means that a dummy read cycle has to be executed at the start of every series of reads.

No dummy cycle is required at the start of a series of writes as data is transferred automatically from the input latch to its destination.

Common	68 MPU	80 MPU		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read display data
1	0	1	0	Write display data
0	1	0	1	Read status
0	0	1	0	Write to internal register (command)

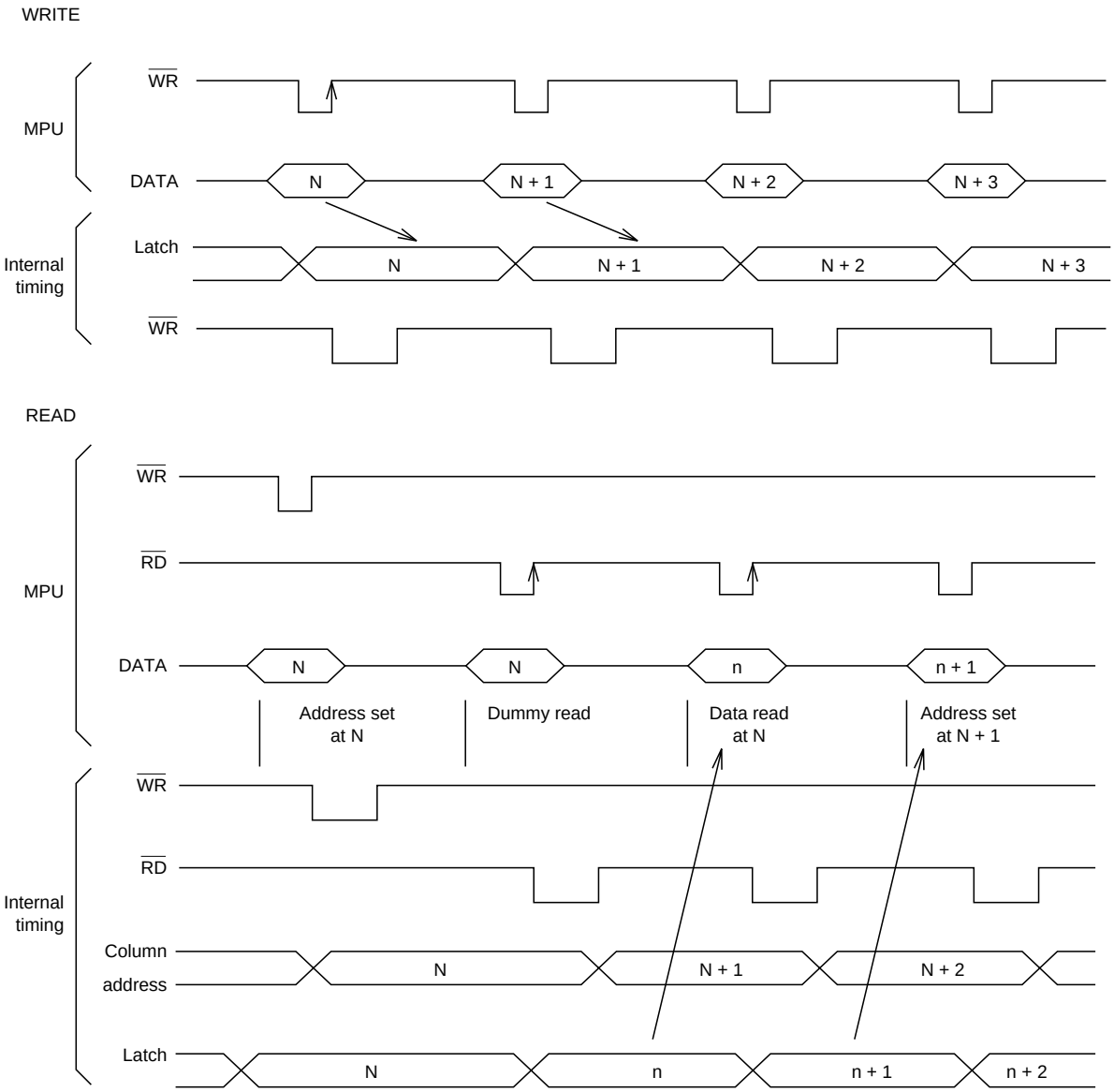


Figure 1 Bus Buffer Delay

Busy flag

When the Busy flag is logical 1, the S1D15400 is executing its internal operations. Any command other than Status Read is rejected during this time. The Busy flag is output at pin D7 by the Status Read command. If an appropriate cycle time (tcyc) is given, this flag needs not be checked at the beginning of each command and, therefore, the MPU processing capacity can greatly be

Display Start Line and Line Count Registers

The contents of this register form a pointer to a line of data in display data RAM corresponding to the first line of the display (COM0), and are set by the "Set Display Start Line" command (see section 3).
The contents of the display start-line register are copied into the line count register at the start of every frame, that is on each edge of FR. The line count register is incremented by the CL clock once for every display line, thus generating a pointer to the current line of data in display data RAM being transferred to the segment driver ciruits.

Column Address Counter

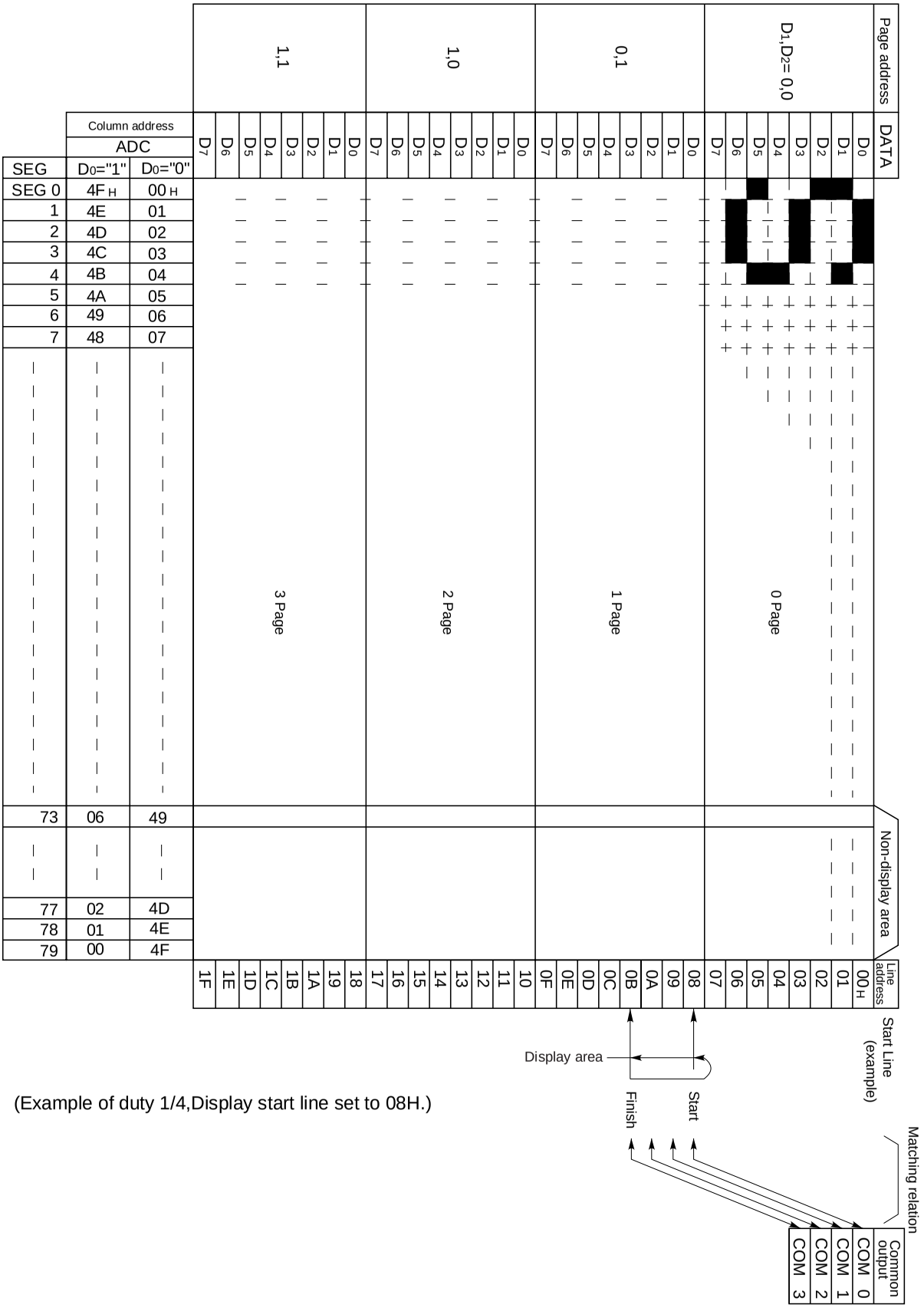
The column address counter is a 7-bit presettable counter which supplies the column address (see figure 2) for MPU accesses to the display data RAM. The counter is incremented by one every time the driver receives a Read or Write Display Data Command.
Addresses above 50 H are invalid, and the counter will not increment past this valu. The contents of the column address conter are set with the Set Column Address command.

Page Register

The page register is a 2-bit register which supplies the page address (see figure 2) for MPU accesses to the display data RAM. The contents of the Page Register are set by the Set Page Register Command.

Display Data RAM

The display data RAM stores the LCD display data, on a 1-bit per pixel basis. The relation-ship between display data, display address and the display is shown in figure 2.



(Example of duty 1/4,Display start line set to 08H.)

Figure 2 Display Data RAM Addressing

Common Timing Generator

This circuit generates common timing and frame (FR) signals from the basic clock CL. The "Select Duty Cycle" command selects a duty cycle of 1/3 or 1/4.

Display Data Latch Circuit

This latch stores one line of display data for use by the LCD driver interface circuitry. The output of this latch is controlled by the "Display ON/OFF" and "Static Driver ON/OFF" commands.

LCD Drive Circuit

The LCD driver circuitry generates the 77 4-level signals used to drive the LCD panel, using output from the display data latch and the common timing generator circuitry.

Display Timing Generator

This circuit generates the internal display timing signal using the basic clock OSC1, and the frame signal, FR. FR is used to generate the dual frame AC-drive waveform (type B drive) and to lock the line counter and common timing generator to the system frame rate. OSC1 is used to lock the line counter to the system line scan rate.

Oscillation Circuit

The oscillator is a low power RC oscillator whose frequency of oscillation is determined by the value of the feedback resistor Rf or an externally generated 50% duty cycle clock input via OSC1. If a slave S1D15400 is used, its OSC2 input is connected to the OSC2 output of the master driver.

Reset Circuit

This circuit senses both the edge and the level of the signal at the $\overline{RES}$ pin and uses this information to

- Initialization status

1. Display is off.
2. Display start line register is set to line 1.
3. Static drive is turned off.
4. Column address counter is set to address 0.
5. Page address register is set to page 0.
6. 1/4 duty is selected.
7. Forward ADC is selected (ADC command D0 is 0 and ADC status flag is 1).
8. Read-modify-write is turned off.

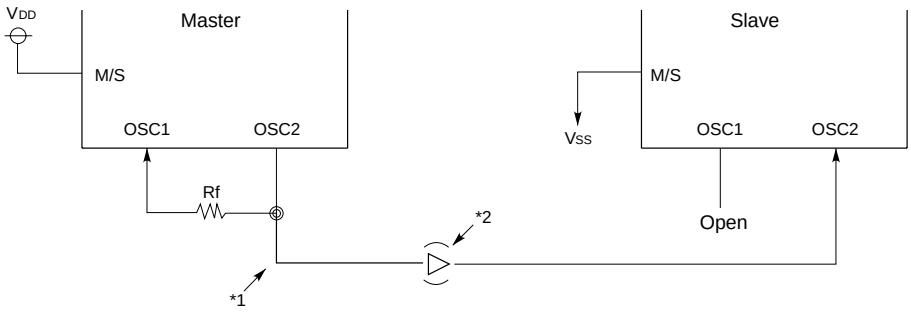
The input signal level at $\overline{RES}$ pin is sensed, and an MPU interface mode is selected as shown on Table 1. For the 80-series MPU, the $\overline{RES}$ input is passed through the inverter and the active high reset signal must be entered. For the 68-series MPU, the active low reset signal must be entered.

When the Reset command is issued, initialization items 2, 4 and 5 above are executed.

As shown for the MPU interface (reference example), the $\overline{RES}$ pin must be connected to the Reset pin and reset at the same time as the MPU initialization.

If the MPU is not initialized by the use of $\overline{RES}$ pin during power-on, an unrecoverable MPU failure may occur.

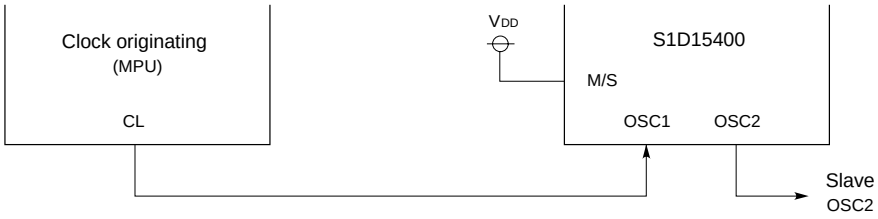
• Oscillator mounted



*1 Oscillating freguency shifts to low freguency side when parasitic capacity gets larger, So Rf should be smaller than the regular value.

*2 CMOS buffer is needed when connecting to more than two slave LSI.

• External clock operation



8. COMMANDS

Table 3

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
(1)Display On/OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns display on or off. 1: ON, 0: OFF *
(2)Display start line	0	1	0	1	1	0Display start address (0 to 31)						Specifies RAM line corresponding to top line of display.
(3)Set page address	0	1	0	1	0	1	1	1	0	Page (0 to 3)		Sets display RAM page in page address register.
(4)Set column (segment) address	0	1	0	0	Column address (0 to 72)							Sets display RAM column address in column address register.
(5)Read status	0	0	1	Busy	ADC	ON/OFF	Reset	0	0	0	0	Reads the following status: BUSY 1: busy 0: Ready ADC 1: Forward 0: Reverse ON/OFF 1: Display off 0: Display on RESET 1: being reset 0: Normal
(6)Write display data	1	1	0	Write data								Writes data from data bus into display RAM.
(7)Read display data	1	0	1	Read data								Reads data from display RAM onto data bus.
(8)Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	0: Forward, 1: Reverse
(9)Statis drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects static driving operation. 1: Static drive, 0: Normal driving
(10)Select duty	0	1	0	1	0	1	0	1	0	0	0/1	Selets LCD duty cycle 1: 1/4, 0: 1/3
(11)Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increments the column address register by 1 druing write only.
(12)End	0	1	0	1	1	1	0	1	1	1	0	Read modify write OFF
(13)Reset	0	1	0	1	1	1	0	0	0	1	0	Sets the display start line register to line 1, and sets the column address counter and page address register to 0.

* The Power Save mode is selected if the static drive is turned ON when the display is OFF.

Table 3 is the command table. The S1D15400 identifies a data bus using a combination of A0 and R/$\overline{W}$ ($\overline{RD}$ or $\overline{WR}$) signals. As the MPU translates a command in the internal timing only (independent from the external clock), its speed is very high. The busy check is usually not required.

(1) Display ON/OFF

This command turns the display on and off.
D=1: Display ON
D=0: Display OFF

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	1	1	1	D	AEH, AFH

(2) Display Start Line

This command specifies the line address shown in Figure 2 and indicates the display line that corresponds to COM0. The display area begins at the specified line address and continues in the line address increment direction. This area having the number of lines of the specified display duty is displayed. If the line address is changed dynamically by this command, the vertical smooth scrolling and paging can be used.

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	0	A_4	A_3	A_2	A_1	A_0	C0H to DFH

A_4	A_3	A_2	A_1	A_0	Line Address
0	0	0	0	0	0
0	0	0	0	1	1
		:			:
		:			:
1	1	1	1	1	31

See figure 2.

(3) Set Page Address

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified. The display status is not changed even when the page address is changed.

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	1	1	0	A_1	A_0	B8H to BBH

A_1	A_0	Page
0	0	0
0	1	1
1	0	2
1	1	3

igure 2.

(4) Set Column Address

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by 1 each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 80, and the page address is not changed continuously.

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	0	A_6	A_5	A_4	A_3	A_2	A_1	A_0	00H to 4FH

A_6	A_5	A_4	A_3	A_2	A_1	A_0	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			⋮				⋮
1	0	0	1	1	1	1	79

(5) Read Status

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Reading the command I/O register (A0=0) yields system status information.

- The BUSY bit indicates whether the driver will accept a command or not.
  Busy=1: The driver is currently executing a command or is resetting. No new command will be accepted.
  Busy=0: The driver will accept a new command.
- The ADC bit indicates the way column addresses are assigned to segment drivers.
  ADC=1: Normal. Column address n → segment driver n.
  ADC=0: Inverted. Column address 79-n → segment driver n.
- The ON/OFF bit indicates the current status of the display.
  ON/OFF=1: Display OFF
  RESET=0: Display ON
- The RESET bit indicates whether the driver is executing a reset or is in normal operating mode.
  RESET=1: Currently executing reset command
  RESET=0: Normal operation

(6) Write Display Data

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	Write data							

Writes 8-bits of data into the display data RAM at a location specified by the contents of the column address and page address registers, and increments the column address register by one.

(7) Read Display Data

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	Read data							

Reads 8-bits of data from the data I/O latch, updates the contents of the I/O buffer with display data from the display data RAM location specified by the contents of the column address and page address registers and increments the column address register.
After loading a new address into the column address register, one dummy read is required before valid data is obtained.

(8) Select ADC

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	0	0	0	D	A0H, A1H

Selects the relationship between display data RAM column addresses and segment drivers.
D=1: SEG0 ← column address 4FH, … (inverted)
D=0: SEG0 ← column address 00H, … (normal)
This command is provided to reduce restrictions on the placement of driver ICS and routing of traces during printed circuit board design. See figure 2 for a table of segments and column addresses for the two values of D.

(9) Static Drive ON/OFF

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	0	1	0	D	A4H, A5H

Forces display on and all common outputs to be selected.
D=1: Static drive on
D=0: Static drive off

(10) Select Duty

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	1	0	0	D	A8H, A9H

Sets the duty cycle of the LCD drive.
D=1: 1/4 duty cycle
D=0: 1/3 duty cycle

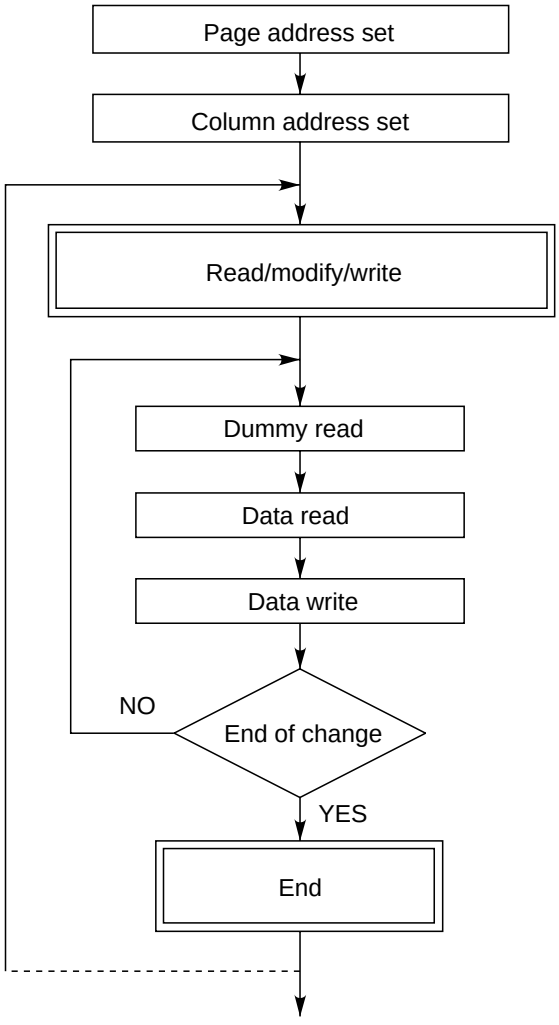
(11) Read-Modify-Write

This command is used in combination with the End command. Once the Read-Modify-Write command is entered, the column address is incremented by 1 only by the display data write command but not incremented by the display data read command. This status is kept until the End command is entered.
When the End command is entered, the column address is returned to the column address when the Read-Modify-Write command is entered. This function can reduce the load of MPU when it repeatedly changes data of the specific display area such as a blinking cursor.

A_0	$\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	0	0	0	0	E0H

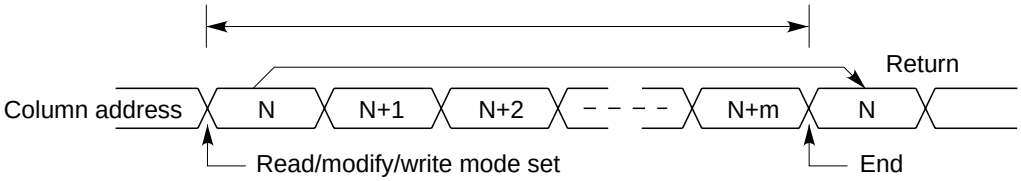
* Any command other than data read and write can be used during the Read-Modify-Write mode. However, the Column Address Set command cannot be used.

Sequence when the cursor is displayed



(12) End

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	1	1	1	0	EEH



Cancels read-modify-write mode and restores the contents of the column address register to their value prior to the receipt of the read-modify-write command.

(13) Reset

This command resets the display start line register, column address counter, and page address register to their initial status. This command does not affect on the display data RAM. For details, see the Reset circuit of the functional block explanation.

The counter and registers are reset after the Reset command has been entered.

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	0	0	1	0	E2H

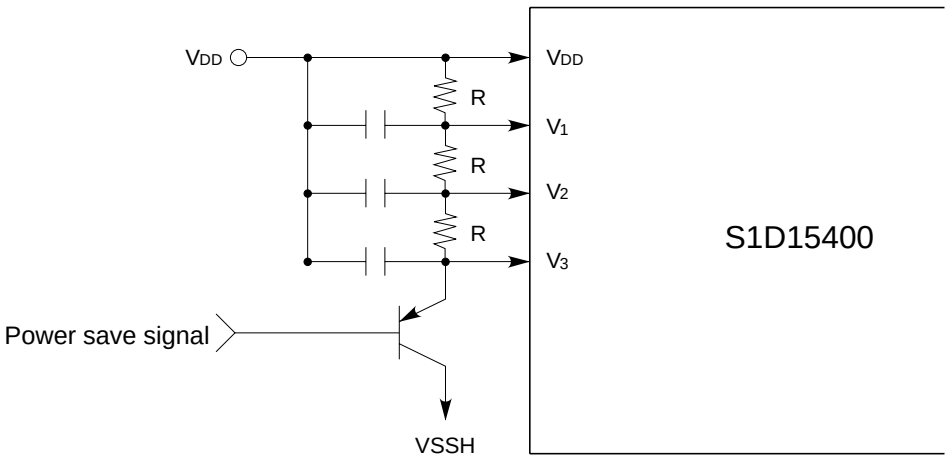
When the power supply is turned on, a Reset signal is entered in the $\overline{RES}$ pin. The Reset command cannot be used instead of this Reset signal.

Power Save (compound command)

The system enters the power save state by switching the static drive on in the display off state, reducing the consumed current almost to static current. The internal state in the power save state is as follows:

- The LCD drive is stopped, and the segment and common drivers output the V_{DD} level.
- Oscillating external clock entry is inhibited, and OSC2 becomes floating.
- The display data and the operation mode are held.

The power save state can be canceled by switching the display on or static drive off.
When the LCD drive voltage level is supplied by an externally-equipped resistance dividing circuit, the current flowing through the resistor must be cut by means of the power save signal.



9. ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Supply voltage (1)		V_{SS}	–8.0 to +0.3	V
Supply voltage (2)		V_3	–15.0 to +0.3	V
Supply voltage (3)		V_1, V_2, V_3	V3 to +0.3	V
Input voltage		V_{IN}	V_{SS}–0.3 to +0.3	V
Output voltage		V_O	V_{SS}–0.3 to +0.3	V
Power dissipation		P_D	250	mW
Operating temperature		T_{opr}	–40 to +85	°C
Storage temperature	QFP	Tstg	–65 to +150	°C
	chip		–55 to +125	
Soldering temperature × time (at lead)		T_{sol}	260, 10	°C, s

Notes: 1. All voltages are specified relative to V_{DD} = 0 V.
2. The following relation must always hold $V_{DD} \geq V_1 \geq V_2 \geq V_3$.
3. Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced during the soldering process, so care should be taken to avoid thermally stressing the package during board assembly.

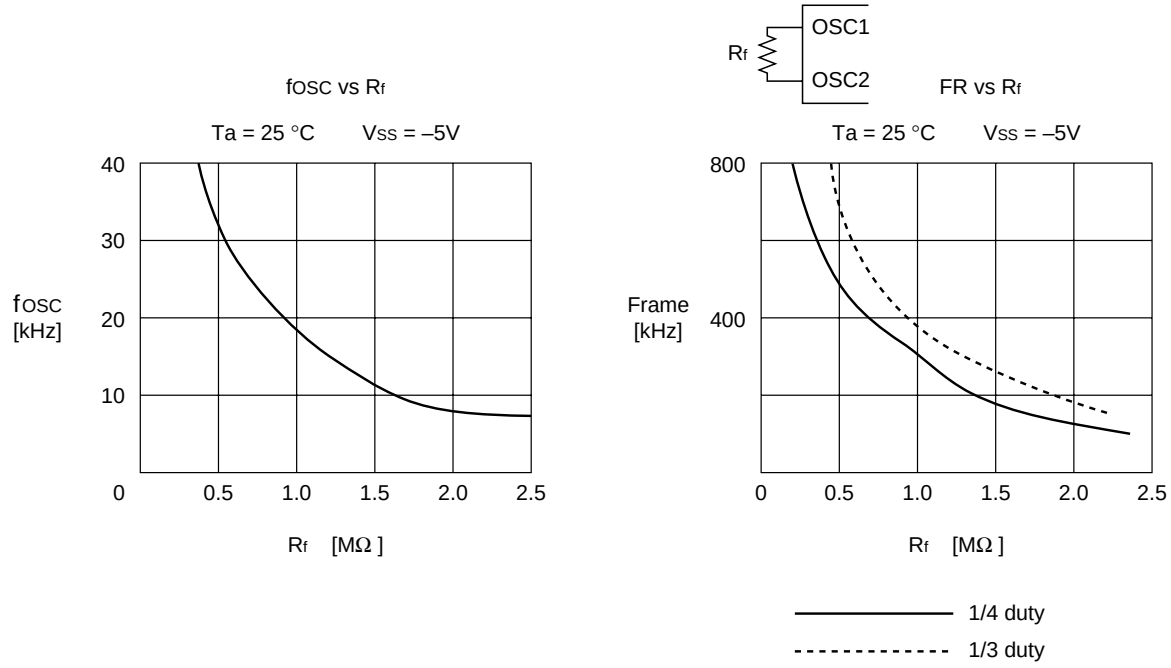
10. DC CHARACTERISTICS

(Ta = –20 to 75 °C, V_{DD} = 0 V)

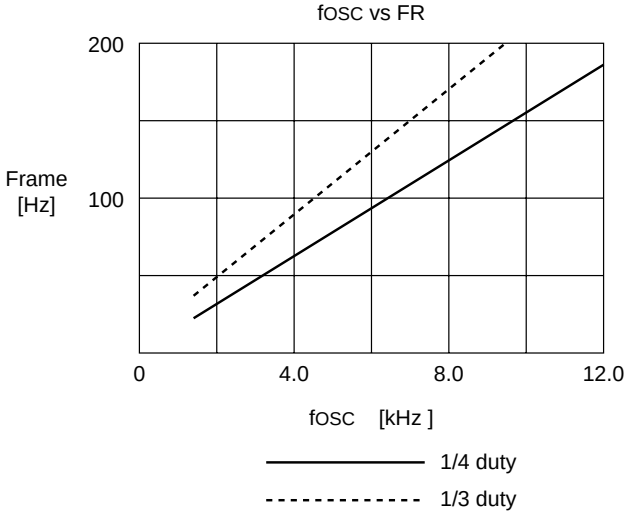
Parameter		Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Applicable Pin
Operating voltage (1) See note 1.	Recommended	V_{SS}			–5.5	–5.0	–4.5	V	V_{SS}
	Allowable				–7.0	—	–2.4		
Operating voltage (2)	Recommended	V_3			–11.0	—	–3.5	V	V_3, See note 10.
	Allowable				–11.0	—	–2.7		
	Allowable	V_1			0.6×V_3	—	V_{DD}	V	V_1
	Allowable	V_2			V_3	—	0.4×V_3	V	V_2
HIGH-level input voltage		V_{IHT}			V_{SS}+2.0	—	V_{DD}	V	See note 2
		V_{IHC}			0.2×V_{SS}	—	V_{DD}		See note 3
LOW-level input voltage		V_{ILT}			V_{SS}	—	V_{SS}+0.8	V	See note 2
		V_{ILC}			V_{SS}	—	0.8×V_{SS}		See note 3
HIGH-level output voltage		V_{OHT}	I_{OH} = –3.0 mA		V_{SS}+2.4	—	—	V	See note 4
		V_{OHC1}	I_{OH} = –2.0 mA		V_{SS}+2.4	—	—		See note 5
		V_{OHC2}	I_{OH} = –120 µA		0.2×V_{SS}	—	—		OSC2
LOW-level output voltage		V_{OLT}	I_{OL} = 3.0 mA		—	—	V_{SS}+0.4	V	See note 4
		V_{OLC1}	I_{OL} = 2.0 mA		—	—	V_{SS}+0.4		See note 5
		V_{OLC2}	I_{OL} = 120 µA		—	—	0.8×V_{SS}		OSC2
Input leakage current		I_{LI}			–1.0	—	1.0	µA	See note 6.
Output leakage current		I_{LO}			–3.0	—	3.0	µA	See note 7.
LCD driver ON resistor		R_{ON}	Ta = 25 °C	V_3 = –5.0 V	—	5.0	7.5	kΩ	SEG0 to 72, COM0 to 3. See note 11.
				V_3 = –3.5 V	—	10.0	50.0		
Static current dissipation		I_{DD0}	$\overline{CS}$ = CL = V_{DD}		—	0.05	1.0	µA	V_{DD}
Dynamic current dissipation		I_{DD} (1)	During display V_3 = –5.0 V	f_{OSC} = 4 kHz	—	1.5	4.0	µA	V_{DD}
				R_f = 1 MΩ	—	9.5	15.0		
		I_{DD} (2)	During assess fcyc = 200 kHz		—	300	500		See note 8.
Input pin capacitance		C_{IN}	Ta = 25 °C, f = 1 MHz		—	5.0	8.0	pF	All input pins
Oscillation frequency		f_{OSC}	R_f = 1.0 MΩ ±2%, Vss=-5.0V		15	18	21	kHz	See note 9.
			R_f = 1.0 MΩ ±2%, Vss=–5.0V		11	16	21		
Reset time		t_R			1.0	—	1000	µS	$\overline{RES}$

Notes:
1. Operation over the specified voltage range is guaranteed, except where the supply voltage changes suddenly during CPU access.
2. A0, D0 to D7, E (or $\overline{RD}$), R/$\overline{W}$ (or $\overline{WR}$) and $\overline{CS}$
3. CL, FR, M/$\overline{S}$ and $\overline{RES}$
4. D0 to D7
5. FR
6. A0, E (or $\overline{RD}$), R/$\overline{W}$ (or $\overline{WR}$), $\overline{CS}$, CL and M/$\overline{S}$, $\overline{RES}$
7. When D0 to D7 and FR are high impedance.
8. During continual write access at a frequency of t_{cyc}. Current consumption during access is effectively proportional to the access frequency.
9. See figure below for details
10. See figure below for details
11. For a voltage differential of 0.1 V between input (V_1, …, V_2) and output (COM, SEG) pins. All voltages within specified operating voltage range.

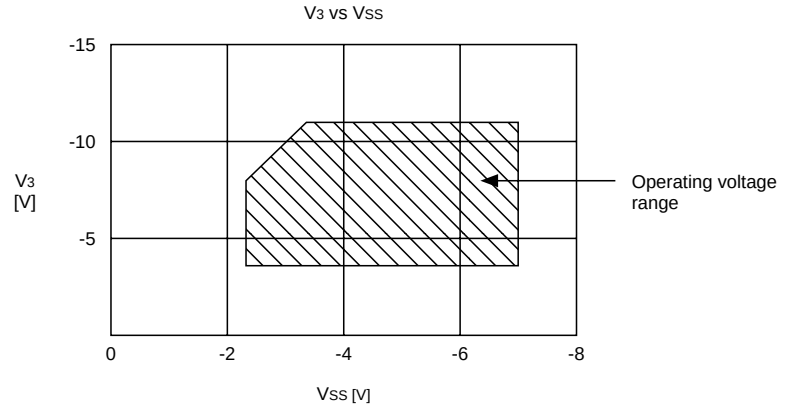
Relationship between f_{OSC}, f_{FR} and R_f



Relationship between f_{CL} and FR

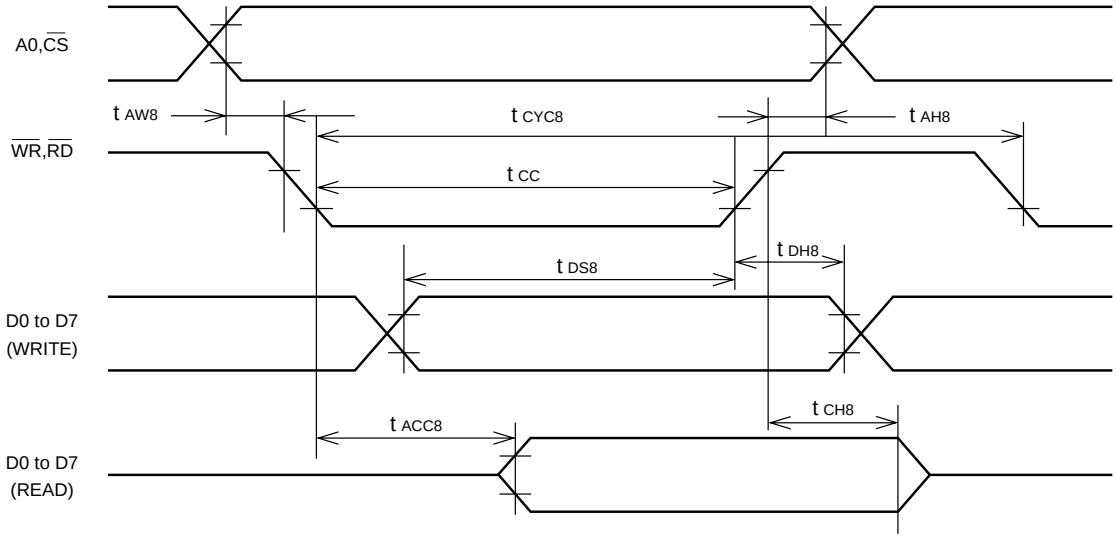


Operating bounds on V_{SS} and V_3



11. AC CHARACTERISTICS

- MPU Bus Read/Write I (80-family MPU)

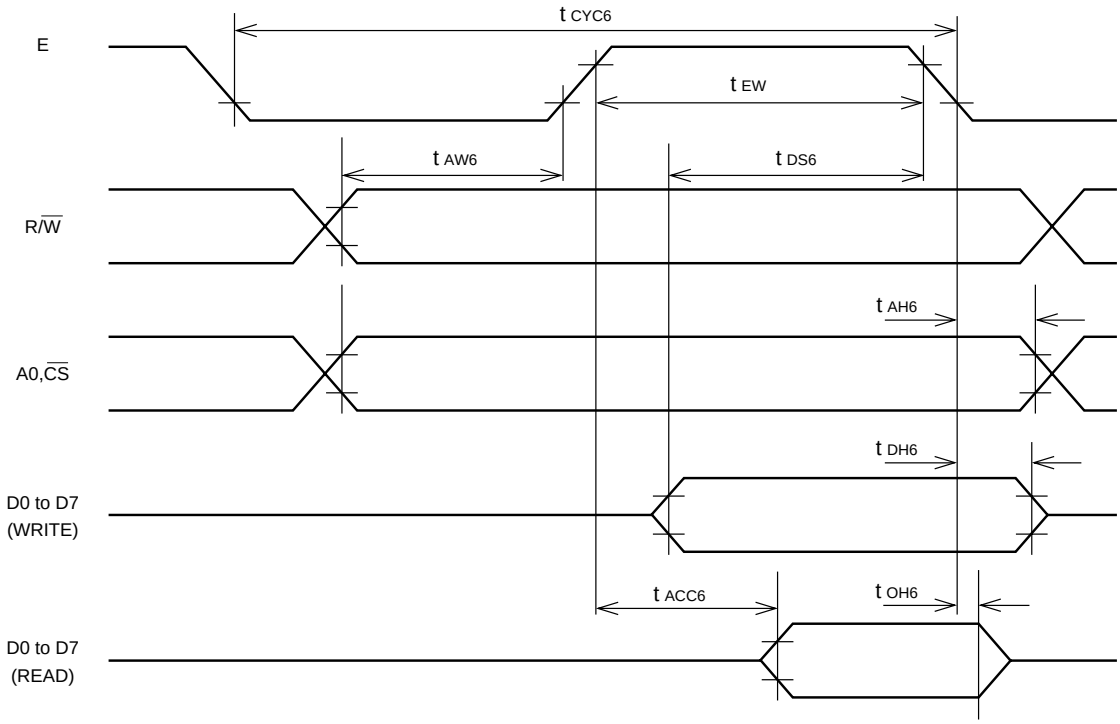


(Ta = –20 to 75 °C, Vss = –5.0 V ±10%)

Signal	Parameters	Symbol	Rating		Unit	Condition
			Min.	Max.		
A0, $\overline{CS}$	Address hold time	tAH8	10	—	ns	
	Address setup time	tAW8	20	—	ns	
$\overline{WR}$, $\overline{RD}$	System cycle time	tCYC8	1000	—	ns	
	Control pulsewidth	tCC	200	—	ns	
D0 to D7	Data setup time	tDS8	80	—	ns	
	Data setup time	tDH8	10	—	ns	
	$\overline{RD}$ access time	tACC8	—	90	ns	CL = 100 pF
	Output disable time	tCH8	10	60	ns	

Notes: 1. All parameter values for a Vss of –3.0 V are about 100% up of their value for a Vss of –5.0 V.
2. All inputs must have a rise and fall time of less than 15 ns.

• MPU Bus Read/Write II (68-family MPU)

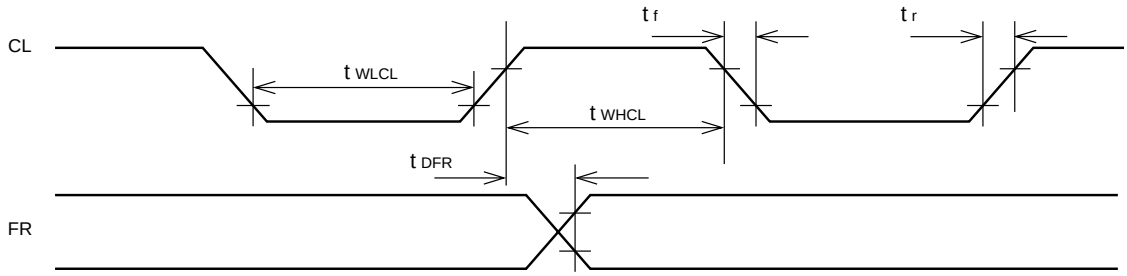


(Ta = –20 to 75 °C, VSS = –5 V ±10%)

Signal	Parameters		Symbol	Rating		Unit	Condition
				Min.	Max.		
A0, CS,R/W	System cycle time		tCYC6	1000	—	ns	
	Address setup time		tAW6	20	—	ns	
	Address hold time		tAH6	10	—	ns	
D0 to D7	Data setup time		tDS6	80	—	ns	
	Data hold time		tDH6	10	—	ns	
	Output disable time		tOH6	10	60	ns	CL = 100 pF
	Access time		tACC6	—	90	ns	
E	Enable pulse width	Read	tEW	100	—	ns	
		Write		8	—	ns	

Notes: 1. tcyc6 is the cycle time of CS.E, not the cycle time of E.
2. All parameter values for a VSS of –3.0 V are about 100% up of their value for a VSS of –5.0 V.
3. All inputs must have a rise and fall time of less than 15 ns.

- Display Control Signal Timing



Input

(Ta = –20 to 75 °C, VSS = –5.0 V ±10%)

Signal	Parameters	Symbol	Rating			Unit	Condition
			Min.	TYP.	Max.		
CL	LOW-level pulse width	tWLCL	35	—	—	µs	
	HIGH-level pulse width	tWHCL	35	—	—	µs	
	Rise time	tr	—	30	150	ns	
FR	Fall time	tf	—	30	150	ns	
	FR delay time	tDFR	-2.0	0.2	2.0	µs	

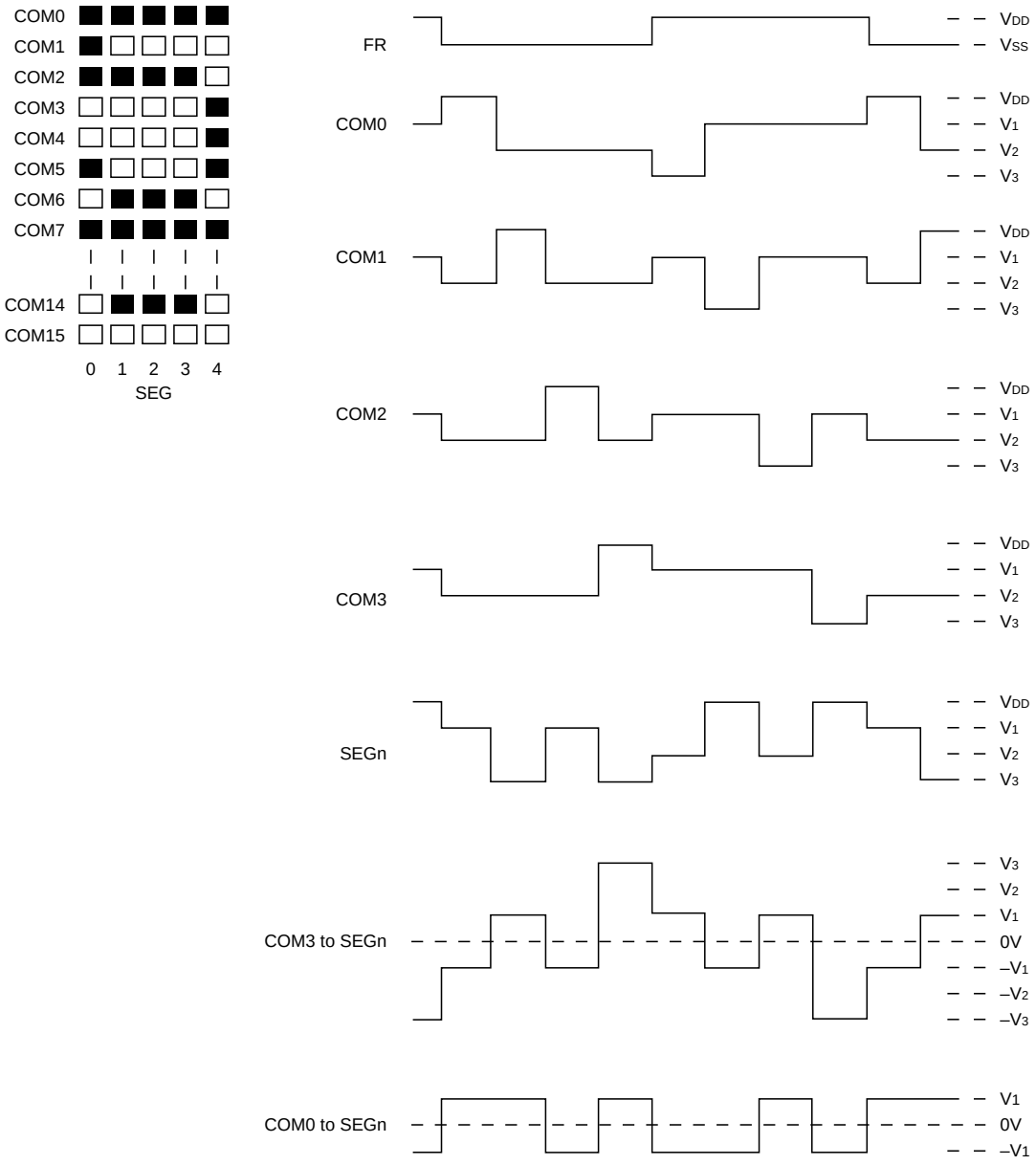
Output

(Ta = –20 to 75 °C, VSS = –5.0 V ±10%)

Signal	Parameters	Symbol	Rating			Unit	Condition
			Min.	TYP.	Max.		
FR	FR delay time	tDFR	—	0.2	0.4	µs	CL = 100 pF

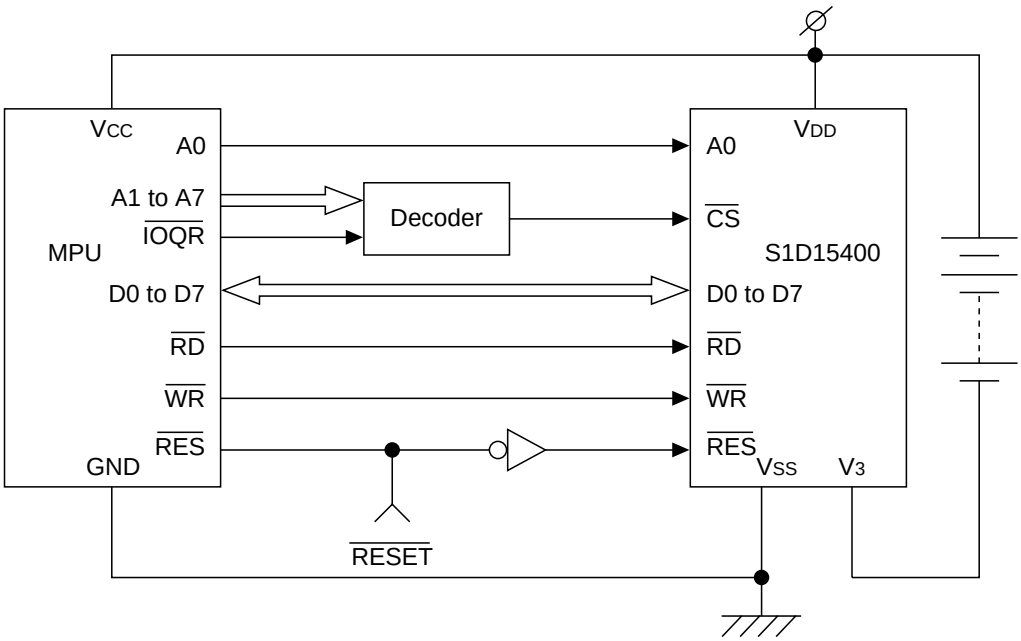
Notes: 1. The listed input tDFR applies to the S1D15400 in slave mode. The listed output tDFR applies to the S1D15400 in master mode.
2. All parameter values for a VSS of –3.0 V are about 100% up of their value for a VSS of –5.0 V.

Example Drive Waveforms (1/3 Bias, 1/4 duty)

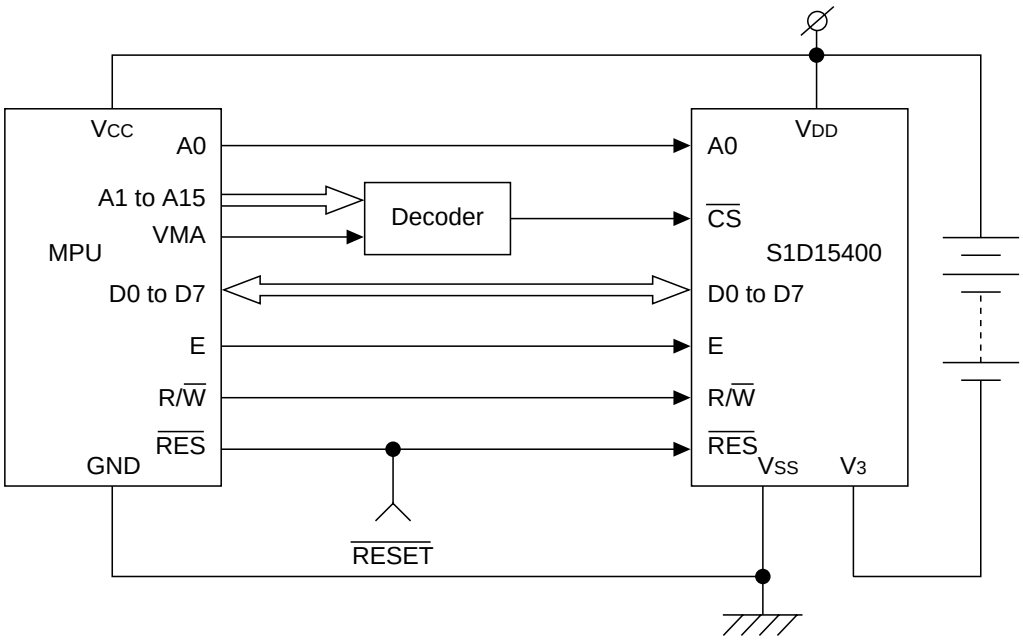


12. MPU INTERFACE CONFIGURATION

80 Family MPU

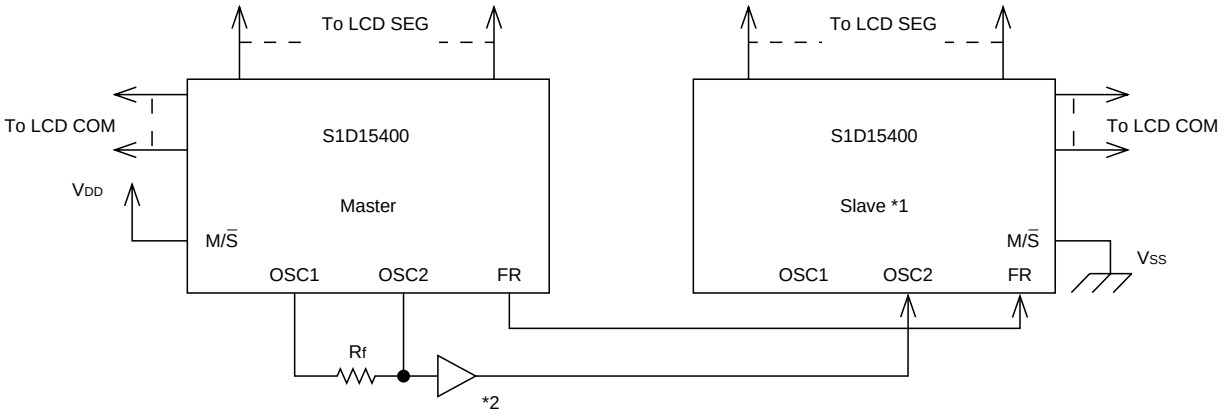


68 Family MPU

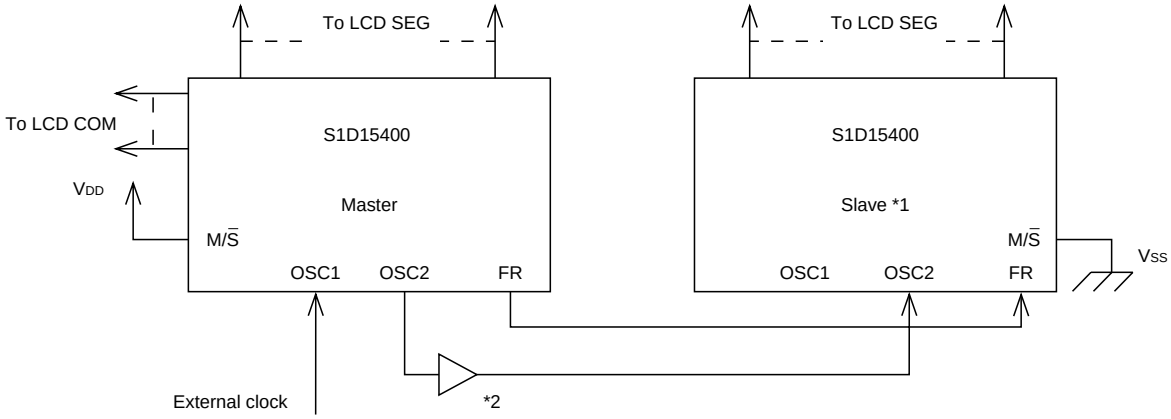


13. LCD DRIVE INTERFACE CONFIGURATION

S1D15400 - S1D15400 (Internal Oscillator)

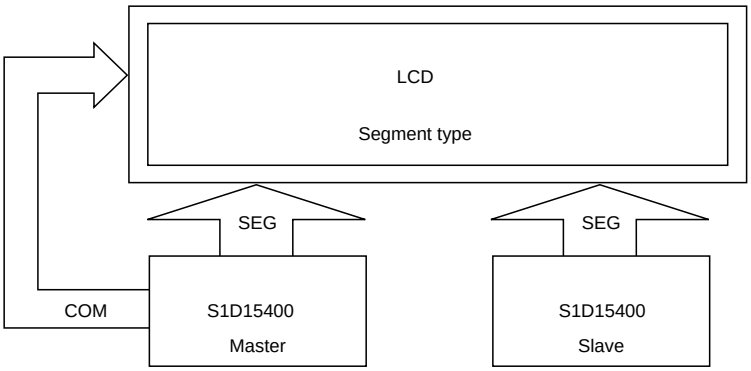


S1D15400 - S1D15400 (External clock)



Notes: 1. The duty cycle of the slave must be the same as that for the master.
2. If a system has two or more slave drivers a CMOS buffer will be required.

14. PANEL INTERFACE CONFIGURATION



7. S1D15600/601/602 Series

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1. DESCRIPTION

The S1D15600/601/602 series is a single-chip LCD driver for dot-matrix liquid crystal displays. It accepts serial or 8-bit parallel display data directly from a microprocessor and stores data in an on-chip 166 × 65-bit RAM.

The S1D15600/601/602 series features 167 common and segment outputs to drive either a 65 × 102-pixel (S1D15600) display (4 rows × 6 columns with 16 × 16-pixel characters) or a 33 × 134-pixel (S1D15601) display (2 rows × 8 columns with 16 × 16-pixel characters) or a 17 × 150-pixel (S1D15602) display (1 row × 9 columns with 16 × 16 characters). In addition, two S1D15600s can be connected together to drive a 65 × 268-pixel graphics display panel.

The S1D15600/601/602 series can read and write RAM data with the minimum current consumption as it does not require any external operation clock. Also, it has a built-in LCD power supply featuring the very low current consumption and, therefore, the display system of a high-performance but handy instrument can be realized by use of the minimum current consumption and LSI chip configuration.

The S1D15600/601/602 Series has the S1D15600, S1D15601 and S1D15602 available according to the duty.

2. FEATURES

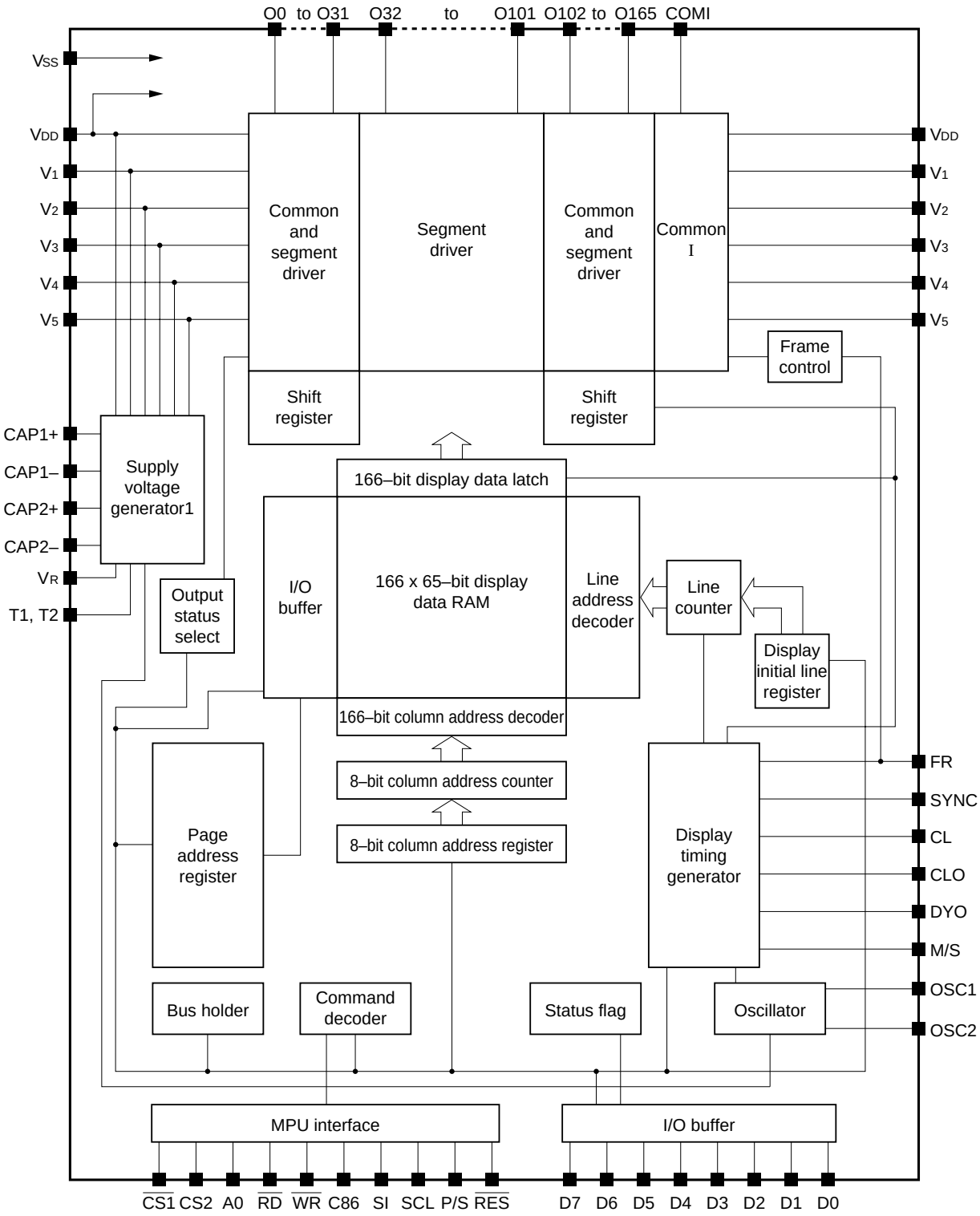
- Wide variety of duty and display areas

Model	Duty	LCD bias	Single-chip display area
S1D15600	1/65	1/9	65 × 102
	1/64		64 × 102
	1/49	1/7	49 × 102
	1/48		48 × 102
S1D15601	1/33	1/7	33 × 134
	1/32		32 × 134
	1/25	1/5	25 × 134
	1/24		24 × 134
S1D15602	1/17	1/5	17 × 150
	1/16		16 × 150

Note: The LCD bias is obtained if the built-in power supply is used.

- On-chip 166 × 65-bit display RAM
- Direct relationship between RAM bits and display pixels.
- High speed Interfaces to 6800- and 8080-series microprocessors
- Selectable 8-bit parallel/serial interface
- Many command functions
- On-chip LCD power circuit including DC/DC voltage converter, voltage regulator and voltage followers.
- On-Chip Contrast control.
- Two types of V_{REG} (Built-in power supply regulator temperature gradient).
- Type1 (S1D1560∗D00∗∗, S1D1560∗D10∗∗)...–0.2%/˚C
- Type2 (S1D15600D_{14}∗∗)...0.00%/˚C
- On-chip oscillator
- Ultra low power consumption
- Power Supply
  $V_{DD} – V_{SS}$ –2.4 V to –6.0 V
  $V_{DD} – V_5$ –3.5 V to –16.0 V
- Ta = –30 to 85°C
- CMOS process
- TCP, QTCP
- The system is not designed against the radio activity.

3. BLOCK DIAGRAM



4. PAD

Pad layout

Chip size : 8.08 × 5.28 mm
Pad pitch : 100 µm (Min.)
Chip thickness : 625 µm
: 300 µm (Al-pad)

- Au-Bump

Bump size A : 103 µm × 95 µm (Typ.) (Pad No. 1 ~ 6, 18, 36 ~ 42, 44 ~ 49)
Bump size B : 69 µm × 95 µm (Typ.) (other then the above)
Bump hight : 23 µm (Typ.)

- Al-pad

Pad size A : 111 µm × 102 µm (Typ.) (Pad No. 1 ~ 6, 18, 36 ~ 42, 44 ~ 49)
Bump size B : 77 µm × 99 µm (Typ.) (Other then the above)

S1D15600/601/602 Series

PAD Center Coordinates

Unit : μm

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	V_5	3640	2487	55	05	-3887	1794	109	059	-2411	-2487	163	0113	2989	-2487
2	V_4	3489	↓	56	06	↓	1694	110	060	-2311	↓	164	0114	3089	↓
3	V_3	3339	↓	57	07	↓	1594	111	061	-2211	↓	165	0115	3189	↓
4	V_2	3188	↓	58	08	↓	1494	112	062	-2111	↓	166	0116	3289	↓
5	V_1	3037	↓	59	09	↓	1394	113	063	-2011	↓	167	0117	3389	↓
6	V_{DD}	2889	↓	60	010	↓	1294	114	064	-1911	↓	168	0118	3489	↓
7	M/S	2755	↓	61	011	↓	1194	115	065	-1811	↓	169	0119	3589	↓
8	$\overline{RES}$	2604	↓	62	012	↓	1094	116	066	-1711	↓	170	0120	3689	↓
9	SCL	2453	↓	63	013	↓	994	117	067	-1611	↓	171	0121	3887	-2206
10	SI	2302	↓	64	014	↓	894	118	068	-1511	↓	172	0122	↓	-2106
11	P/S	2151	↓	65	015	↓	794	119	069	-1411	↓	173	0123	↓	-2006
12	$\overline{CS1}$	2001	↓	66	016	↓	694	120	070	-1311	↓	174	0124	↓	-1906
13	CS2	1850	↓	67	017	↓	594	121	071	-1211	↓	175	0125	↓	-1806
14	C86	1699	↓	68	018	↓	494	122	072	-1111	↓	176	0126	↓	-1706
15	A0	1548	↓	69	019	↓	394	123	073	-1011	↓	177	0127	↓	-1606
16	$\overline{WR}$	1397	↓	70	020	↓	294	124	074	-911	↓	178	0128	↓	-1506
17	$\overline{RD}$	1247	↓	71	021	↓	194	125	075	-811	↓	179	0129	↓	-1406
18	V_{SS}	1077	↓	72	022	↓	94	126	076	-711	↓	180	0130	↓	-1306
19	D0	945	↓	73	023	↓	-6	127	077	-611	↓	181	0131	↓	-1206
20	D1	794	↓	74	024	↓	-106	128	078	-511	↓	182	0132	↓	-1106
21	D2	643	↓	75	025	↓	-206	129	079	-411	↓	183	0133	↓	-1006
22	D3	493	↓	76	026	↓	-306	130	080	-311	↓	184	0134	↓	-906
23	D4	342	↓	77	027	↓	-406	131	081	-211	↓	185	0135	↓	-806
24	D5	191	↓	78	028	↓	-506	132	082	-111	↓	186	0136	↓	-706
25	D6	40	↓	79	029	↓	-606	133	083	-11	↓	187	0137	↓	-606
26	D7	-111	↓	80	030	↓	-706	134	084	89	↓	188	0138	↓	-506
27	DYO	-261	↓	81	031	↓	-806	135	085	189	↓	189	0139	↓	-406
28	CLO	-412	↓	82	032	↓	-906	136	086	289	↓	190	0140	↓	-306
29	SYNC	-563	↓	83	033	↓	-1006	137	087	389	↓	191	0141	↓	-206
30	FR	-714	↓	84	034	↓	-1106	138	088	489	↓	192	0142	↓	-106
31	CL	-865	↓	85	035	↓	-1206	139	089	589	↓	193	0143	↓	-6
32	OSC2	-1015	↓	86	036	↓	-1306	140	090	689	↓	194	0144	↓	94
33	OSC1	-1166	↓	87	037	↓	-1406	141	091	789	↓	195	0145	↓	194
34	T2	-1317	↓	88	038	↓	-1506	142	092	889	↓	196	0146	↓	294
35	T1	-1468	↓	89	039	↓	-1606	143	093	989	↓	197	0147	↓	394
36	V_{SS}	-1638	↓	90	040	↓	-1706	144	094	1089	↓	198	0148	↓	494
37	CAP1+	-1789	↓	91	041	↓	-1806	145	095	1189	↓	199	0149	↓	594
38	CAP1-	-1939	↓	92	042	↓	-1906	146	096	1289	↓	200	0150	↓	694
39	CAP2+	-2090	↓	93	043	↓	-2006	147	097	1389	↓	201	0151	↓	794
40	CAP2-	-2241	↓	94	044	↓	-2106	148	098	1489	↓	202	0152	↓	894
41	V_{OUT}	-2392	↓	95	045	↓	-2206	149	099	1589	↓	203	0153	↓	994
42	V_5	-2543	↓	96	046	-3711	-2487	150	0100	1689	↓	204	0154	↓	1094
43	V_R	-2674	↓	97	047	-3611	↓	151	0101	1789	↓	205	0155	↓	1194
44	V_{DD}	-2844	↓	98	048	-3511	↓	152	0102	1889	↓	206	0156	↓	1294
45	V_1	-2995	↓	99	049	-3411	↓	153	0103	1989	↓	207	0157	↓	1394
46	V_2	-3146	↓	100	050	-3311	↓	154	0104	2089	↓	208	0158	↓	1494
47	V_3	-3297	↓	101	051	-3211	↓	155	0105	2189	↓	209	0159	↓	1594
48	V_4	-3447	↓	102	052	-3111	↓	156	0106	2289	↓	210	0160	↓	1694
49	V_5	-3598	↓	103	053	-3011	↓	157	0107	2389	↓	211	0161	↓	1794
50	00	-3887	2294	104	054	-2911	↓	158	0108	2489	↓	212	0162	↓	1894
51	01	↓	2194	105	055	-2811	↓	159	0109	2589	↓	213	0163	↓	1994
52	02	↓	2094	106	056	-2711	↓	160	0110	2689	↓	214	0164	↓	2094
53	03	↓	1994	107	057	-2611	↓	161	0111	2789	↓	215	0165	↓	2194
54	04	↓	1894	108	058	-2511	↓	162	0112	2889	↓	216	COMI	↓	2294

5. PIN DESCRIPTION

Power Supply

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>V_{DD}</td><td>Supply</td><td>5V supply. Common to MPU power supply pin V_{CC}.</td><td>2</td></tr>
<tr><td>V_{SS}</td><td></td><td>Ground</td><td>2</td></tr>
<tr><td>V_1 to V_5</td><td>Supply</td><td>LCD driver supply voltages. The voltage determined by the LCD cellis impedance-converted by a resistive divider or an operational amplifier for application. Voltages should be determined on a V_{DD}- basis so as to satisfy the following relationship. The voltages must satisfy the following relationship.
$V_{DD} \geq V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$.
When master mode selects, these voltages are generated on-chip.
<table>
<tr><th></th><th>S1D15600D00B*</th><th>S1D15600D10B*
S1D15601D00B*</th><th>S1D15601D10B*
S1D15602D00B*</th></tr>
<tr><td>V_1</td><td>1/9 V_5</td><td>1/7 V_5</td><td>1/5 V_5</td></tr>
<tr><td>V_2</td><td>2/9 V_5</td><td>2/7 V_5</td><td>2/5 V_5</td></tr>
<tr><td>V_3</td><td>7/9 V_5</td><td>5/7 V_5</td><td>3/5 V_5</td></tr>
<tr><td>V_4</td><td>8/9 V_5</td><td>6/7 V_5</td><td>4/5 V_5</td></tr>
</table>
</td><td>11</td></tr>
</table>

LCD Driver Supplies

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>CAP1+</td><td>O</td><td>DC/DC voltage converter capacitor 1 positive connection</td><td>1</td></tr>
<tr><td>CAP1–</td><td>O</td><td>DC/DC voltage converter capacitor 1 negative connection</td><td>1</td></tr>
<tr><td>CAP2+</td><td>O</td><td>DC/DC voltage converter capacitor 2 positive connection</td><td>1</td></tr>
<tr><td>CAP2–</td><td>O</td><td>DC/DC voltage converter capacitor 2 negative connection</td><td>1</td></tr>
<tr><td>V_{OUT}</td><td>I/O</td><td>DC/DC voltage converter output1</td><td>1</td></tr>
<tr><td>V_R</td><td>I</td><td>Voltage adjustment pin. Applies voltage between V_{DD} and V_5 using a resistive divider.</td><td>1</td></tr>
<tr><td>T1, T2</td><td>I</td><td>Liquid crystal power control terminals
<table>
<tr><th>T1</th><th>T2</th><th>Boosting circuit</th><th>Voltage regulation circuit</th><th>V/F circuit</th></tr>
<tr><td>LOW</td><td>LOW</td><td>Valid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>Valid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>Invalid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>Invalid</td><td>Invalid</td><td>Valid</td></tr>
</table>
</td><td>2</td></tr>
</table>

Microprocessor Interface

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>D0 to D7</td><td>I/O</td><td>Data inputs/outputs</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Control/display data flag input. This is connected to the LSB of the microprocessor address bus.
When LOW, the data on D0 to D7 is control data.
When HIGH, the data on D0 to D7 is display data.</td><td>1</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>Reset input. System is reset and initialized when LOW.</td><td>1</td></tr>
<tr><td>$\overline{CS1}$, CS2</td><td>I</td><td>Chip select inputs. Data input/output is enabled when $\overline{CS1}$ is LOW and CS2 is HIGH.</td><td>2</td></tr>
<tr><td>$\overline{RD}$ (E)</td><td>I</td><td>Read enable input. See note. 1</td><td>1</td></tr>
<tr><td>$\overline{WR}$ (R/$\overline{W}$)</td><td>I</td><td>Write enable input. See note. 2</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>Microprocessor interface select input. LOW when interfacing to 8080-series. HIGH when interfacing to 6800-series.</td><td>1</td></tr>
<tr><td>SI</td><td>I</td><td>Serial data input</td><td>1</td></tr>
<tr><td>SCL</td><td>I</td><td>Serial clock input. Data is read on the rising edge of SCL and converted to 8-bit parallel data.</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>Parallel/serial data input select
<table>
<tr><th>P/S</th><th>Operating mode</th><th>Chip select</th><th>Data/command</th><th>Data input/ output</th><th>Read/write</th><th>Serial clock</th></tr>
<tr><td>HIGH</td><td>Parallel</td><td>$\overline{CS1}$, CS2</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$, $\overline{WR}$</td><td>—</td></tr>
<tr><td>LOW</td><td>Serial</td><td>$\overline{CS1}$, CS2</td><td>A0</td><td>SI</td><td>Write only</td><td>SCL</td></tr>
</table>
In serial mode, data cannot be read from the RAM, and D0 to D7, HZ, $\overline{RD}$ and $\overline{WR}$ must be HIGH or LOW. In parallel mode, SI and SCL must be HIGH or LOW.</td><td>1</td></tr>
</table>

Note 1
When interfacing to 8080-series microprocessors, $\overline{RD}$ is active-LOW. When interfacing to 6800-series microprocessors, they are active-HIGH.

Note 2
When interfacing to 8080-series microprocessors, $\overline{WR}$ is active-LOW. When interfacing to 6800-series microprocessors, It will be read mode when $\overline{WR}$ is high and It will be write mode when $\overline{WR}$ is LOW.

Oscillator and Timing Control

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>OSCI</td><td>I</td><td>Connecting pins for feedback resistors of the built-in oscillator When M/S = HIGH: Connect oscillator resistor Rf to the OSC1 and OSC2 pins. The OSC2 pin is used for output of the oscillator amplifier.</td><td>2</td></tr>
<tr><td>OSC2</td><td>I/O</td><td>When M/S = LOW: The OSC2 pin is used for input of oscillation signal. The OSC1 pin should be left open. Fix the CL pin to theV_{SS} level when using the internal oscillator circuit as the display clock.</td><td>2</td></tr>
<tr><td>CL</td><td>I</td><td>Display clock input. The line counter increments on the rising edge of CL and the display pattern is output on the falling edge. When use external display clock, OSC1 = HIGH, OSC2 = LOW and reset this LSI by $\overline{RES}$ pin.</td><td>1</td></tr>
<tr><td>CLO</td><td>O</td><td>Display clock output. When using the master operation, the clock signal is output on this pin. Connect CLO to YSCL on the common driver.</td><td>1</td></tr>
<tr><td>M/S</td><td>I</td><td>Master/slave select input. Master makes some signals for display, and slave gets them. This is for display syncronization.
<table>
<tr><th>Device</th><th>M/S</th><th>Operating mode</th><th>Internal oscillator</th><th>Power supply</th><th>FR</th><th>SYNC</th><th>OSC1</th><th>OSC2</th><th>DYO</th></tr>
<tr><td rowspan="2">156XD$_{OB}$</td><td>LOW</td><td>Slave</td><td>OFF</td><td>OFF</td><td>I</td><td>I</td><td>Open</td><td>I</td><td>O</td></tr>
<tr><td>HIGH</td><td>Master</td><td>ON</td><td>ON</td><td>O</td><td>O</td><td>I</td><td>O</td><td>O</td></tr>
</table>
Note
I = input mode
O = output mode</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>LCD AC drive signal input/output. If the S1D15600/601/602 series MPU’s are used in master and slave configuration, this pin must be connected to each FR pin. Also when the S1D15600/601/602 series isused as the master MPU, this pin must be connected to the FRpin of the common driver. Output is selected when M/S is HIGH, and input is selected when M/S is LOW.</td><td>1</td></tr>
<tr><td>SYNC</td><td>I/O</td><td>Display sync input/output. If the S1D15600/601/602 series MPU’s are used in master and slave configuration, this pin must be connected to each SYNC pin. Output is selected when M/S is HIGH, and Input is selected when M/S is LOW.</td><td>1</td></tr>
<tr><td>DYO</td><td>O</td><td>Start-up output for common driver. Connect to DIO of the common driver.</td><td>1</td></tr>
</table>

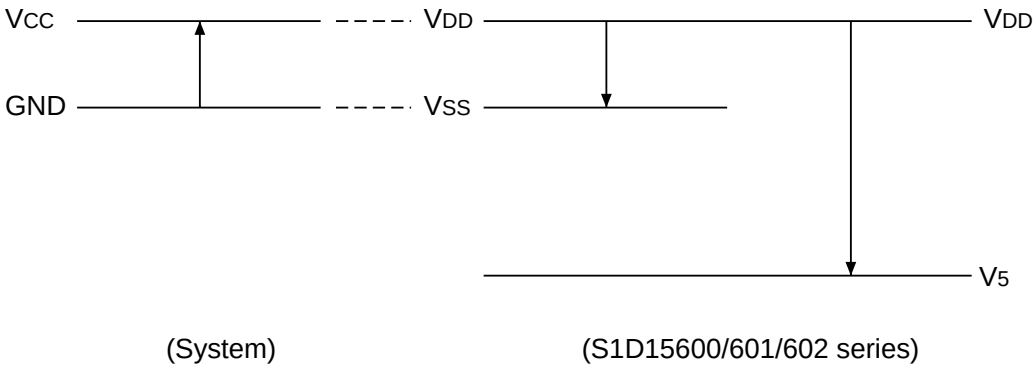
LCD Driver Outputs

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>O0 to O165</td><td>O</td><td>LCD driver outputs. O0 to O31 and O102 to O165 are selectable segment or common outputs, determined by a selection command. O32 to O101 are segment outputs only.

For segment outputs, the ON voltage level is given as shown in the following table.
<table>
<tr><th rowspan="2">RAM data</th><th rowspan="2">FR</th><th colspan="2">LCD ON voltage</th></tr>
<tr><th>Normal display</th><th>Inverse display</th></tr>
<tr><td rowspan="2">LOW</td><td>LOW</td><td>V_3</td><td>V_5</td></tr>
<tr><td>HIGH</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td rowspan="2">HIGH</td><td>LOW</td><td>V_5</td><td>V_3</td></tr>
<tr><td>HIGH</td><td>V_{DD}</td><td>V_2</td></tr>
</table>
For common outputs, the ON voltage is given as shown in the following table.
<table>
<tr><th>Scan data</th><th>FR</th><th>LCD ON voltage</th></tr>
<tr><td rowspan="2">LOW</td><td>LOW</td><td>V_4</td></tr>
<tr><td>HIGH</td><td>V_1</td></tr>
<tr><td rowspan="2">HIGH</td><td>LOW</td><td>V_{DD}</td></tr>
<tr><td>HIGH</td><td>V_5</td></tr>
</table></td><td>166</td></tr>
<tr><td>COMI</td><td>O</td><td>LCD driver common output. Common outputs when the “DUTY +1” command is executed are as follows:
<table>
<tr><th></th><th>“DUTY + 1” ON</th><th>“DUTY + 1” OFF</th></tr>
<tr><td>S1D15600
S1D15601
S1D15602</td><td>COM64, COM48
COM32, COM24
COM16</td><td>V_1 or V_4
V_1 or V_4
V_1 or V_4</td></tr>
</table>
Common output special for the indicator.</td><td>1</td></tr>
</table>

6.ABSOLUTE MAXMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{SS}	–7.0 +0.03	V
Supply voltage range (2) (DC/DC When in use)		–6.0 to 0.3 (when triple boosting)	
Driver supply voltage range (1)	V_5	–18.0 to 0.3	V
Driver supply voltage range (2)	V_1, V_2, V_3, V_4	V_5 to 0.3	V
Input voltage range	V_{IN}	V_{SS} –0.3 to 0.3	V
Output voltage range	Vo	V_{SS} –0.3 to 0.3	V
Operating temperature range	Topr	–30 to 85	°C
Storage temperature range (TCP)	Tstr	–55 to 100	°C



Notes: 1. The voltages shown are based on V_{DD} = 0 V.
2. Always keep the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ for voltages V_1, V_2, V_3 and V_4.
3. If LSIs are used over the absolute maximum rating, the LSIs may be destroyed permanently. It is desirable to use them under the electrical characteristic conditions for general operation. Otherwise, a malfunction of the LSI may be caused and LSI reliability may be affected.
4. A guarantee on operating temperature below –30°C may be studied individually.

DC Characteristics

V_{DD} = 0 V, V_{SS} = –5 V ± 10%, Ta = –30 to +85°C unless otherwise noted.

Item		Symbol	Condition		Min.	Typ.	Max.	Unit	Pin used
Power voltage (1)	Recommended operation	V_{SS}			–5.5	–5.0	–4.5	V	V_{SS}
	Operational				–6.0		–2.4		*1
Operating voltage (2)	Operational	V_5			–16.0		–4.0	V	V_5 *2
	Operational	V_1, V_2			0.4 × V_5		V_{DD}	V	V_1, V_2
	Operational	V_3, V_4			V_5		0.6 × V_5	V	V_3, V_4
High-level input voltage		V_{IHC1}			0.3 × V_{SS}		V_{DD}	V	*3
		V_{IHC2}			0.15 × V_{SS}		V_{DD}		*4
		V_{IHC1}	V_{SS} = –2.7 V		0.3 × V_{SS}		V_{DD}		*3
		V_{IHC2}	V_{SS} = –2.7 V		0.2 × V_{SS}		V_{DD}		*4
Low-level input voltage		V_{ILC1}			V_{SS}		0.7 × V_{SS}	V	*3
		V_{ILC2}			V_{SS}		0.85 × V_{SS}		*4
		V_{ILC1}	V_{SS} = –2.7 V		V_{SS}		0.7 × V_{SS}		*3
		V_{ILC2}	V_{SS} = –2.7 V		V_{SS}		0.8 × V_{SS}		*4
High-level output voltage		V_{OHC1}		I_{OH} = –1 mA	0.2 × V_{SS}		V_{DD}	V	*5
		V_{OHC2}		I_{OH} = –120 µA	0.2 × V_{SS}		V_{DD}		OSC2
		V_{OHC1}	V_{SS} = –2.7 V	I_{OH} = –0.5 mA	0.2 × V_{SS}		V_{DD}	V	*5
		V_{OHC2}	V_{SS} = –2.7 V	I_{OH} = –50 µA	0.2 × V_{SS}		V_{DD}		OSC2
Low-level output voltage		V_{OLC1}		I_{OL} = 1 mA	V_{SS}		0.8 × V_{SS}	V	*5
		V_{OLC2}		I_{OL} = 120 µA	V_{SS}		0.8 × V_{SS}		OSC2
		V_{OLC1}	V_{SS} = –2.7 V	I_{OL} = 0.5 mA	V_{SS}		0.8 × V_{SS}	V	*5
		V_{OLC2}	V_{SS} = –2.7 V	I_{OL} = 50 µA	V_{SS}		0.8 × V_{SS}		OSC2
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}		–1.0		1.0	µA	*6
Output leakage current		I_{LO}			–3.0		3.0	µA	*7
LCD driver ON resistance		R_{ON}	Ta = 25°C	V_5 = –14.0 V		2.0	3.0	kΩ	O0 to O166
				V_5 = –8.0 V		3.0	4.5		*8
Static power consumption		I_{SSQ}				0.00	5.0	µA	V_{SS}
		I_{5Q}	V_5 = –18.0V			0.01	15.0	µA	V_5
Input terminal capacity		C_{IN}	Ta = 25°C	f=1MHz		5.0	8.0	pF	*3 *4
Oscillation frequency		f_{OSC}	R_f=1 MΩ ±2%	V_{SS} = –5V	15	18	22	kHz	*9
				V_{SS} = –2.7V	11	16	21		

Reset time	t_R		1.0	µs	*10
Reset “L” pulse width	t_{RW}		1.0	µs	*11

Built-in power circuit	Input voltage	V_{SS}		–6.0		–2.4	V	*12
	Amplified output voltage	V_{OUT}	when triple boosting	–18.0			V	V_{OUT}
	Voltage regulator operation voltage	V_{OUT}		–16.0		–6.0	V	V_{OUT}
	Voltage regulutor operation voltage	V_5 ①	Supplied to S1D15600D00B★	–16.0		–6.0	V	*13
		V_5 ②	Supplied to S1D15601D00B★	–16.0		–5.0	V	
		V_5 ③	Supplied to S1D15601D10B★	–16.0		–4.0	V	
		V_5 ④	Supplied to S1D15602D00B★	–16.0		–4.5	V	
	Reference voltage	V_{REG}	Ta = 25°C	–2.35	–2.5	–2.65	V	

*V_{SS} = –2.4V is on the same basis as V_{SS} = –2.7V.

* See the 4-12 page for details.

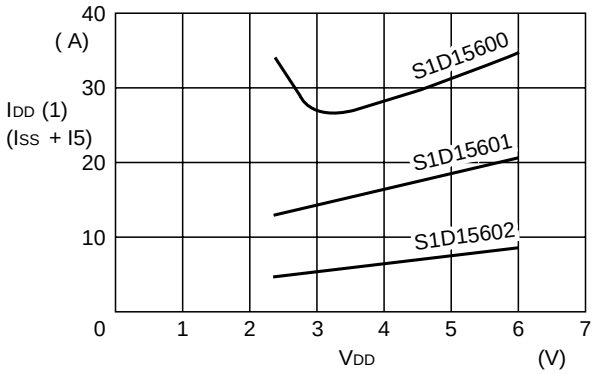
When dynamic current consumption (I) is displaye; the built-in power circuit is on and T1 = T2 = LOW.

V_{DD} = 0 V, V_{SS} = –5 V ± 10%, Ta = –30 to +85°C unless otherwise noted.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
S1D15600	I_{DD} (1)	V_5 = –12.5 V; 3 times amplified		169	340	µA	*16
S1D15601		V_5 = –8.0 V ; 3 times amplified		124	250	µA	
S1D15602		V_5 = –6.0 V ; 2 times amplified		53	110	µA	
		V_{SS} = –2.7 V; 3 times amplified V_5 = –6.0 V		66	130	µA	

Typical current consumption characteristics

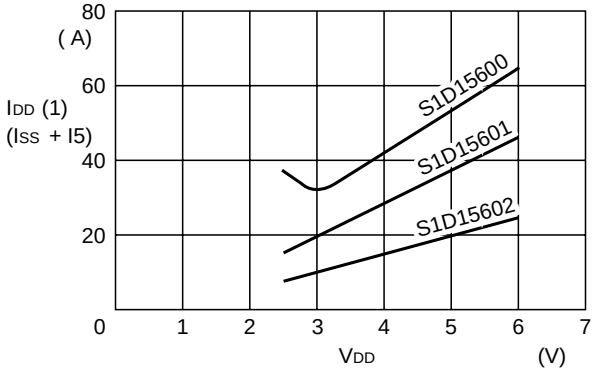
- Dynamic current consumption (I), if an external clock and an external power supply are used.



Conditions: The built-in power supply is off but the external one is used.
S1D15600 $V_5 – V_{DD}$ = –12.5 V
S1D15601 $V_5 – V_{DD}$ = –8.0 V
S1D15602 $V_5 – V_{DD}$ = –6.0 V
External clock:
S1D15600 f_{CL} = 4 kHz
S1D15601 f_{CL} = 2 kHz
S1D15602 f_{CL} = 1 kHz

Remarks: *14

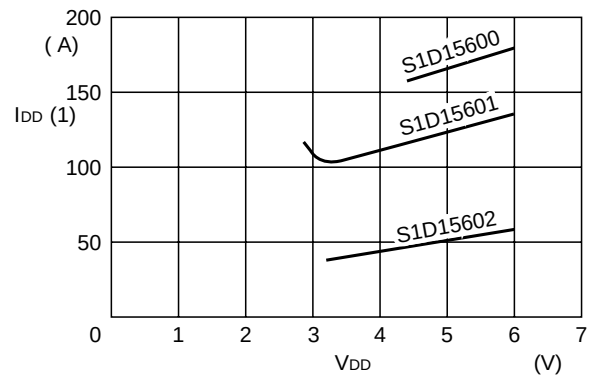
- Dynamic current consumption (I), if the built-in oscillator and the external power supply are used.



Conditions: The built-in power supply is off but the external one is used.
S1D15600 $V_5 – V_{DD}$ = –12.5 V
S1D15601 $V_5 – V_{DD}$ = –8.0 V
S1D15602 $V_5 – V_{DD}$ = –6.0 V
Internal oscillation:
S1D15600 R_f = 1 MΩ
S1D15601 R_f = 1 MΩ
S1D15602 R_f = 1 MΩ

Remarks: *15

- Dynamic current consumption (I), if the built-in power supply is used.



Conditions: The built-in power supply is on and T1 = T2 = Low.
S1D15600 $V_5 - V_{DD}$ = –12.5 V; 3 times amplified
S1D15601 $V_5 - V_{DD}$ = –8.0 V; 3 times amplified
S1D15602 $V_5 - V_{DD}$ = –6.0 V; 2 times amplified
Internal oscillation:
S1D15600 R_f = 1 MΩ
S1D15601 R_f = 1 MΩ
S1D15602 R_f = 1 MΩ

Remarks: *16

Notes: *1. Although the wide range of operating voltage is guaranteed, a spike voltage change during access to the MPU is not guaranteed.
*2. The operating voltage range of the V_{SS} and V_5 systems (see Figure 11).
The operating voltage range is applied if an external power supply is used.
*3. Pins A0, D0 to D7, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, FR, SYNC, M/S, C86, SI, P/S, T1 and T2.
*4. Pins CL, SCL, and $\overline{RES}$
*5. Pins D0 to D7, FR, SYNC, CL0, and DY0
*6. Pins A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CL, M/S, $\overline{RES}$, C86, SI, SCL, P/S, T1, and T2.
*7. Applied if pins D0 to D7, FR, and SYNC are high impedance.
*8. The resistance when the 0.1-volt voltage is applied between the "On" output terminal and each power terminal (V1, V2, V3 or V4). It must be within the operating voltage (2).
R ON = 0.1 V/ΔI
(ΔI is the current that flows when 0.1 VDC is applied during power-on.)
*9. The relationship between the oscillation frequency, frame and Rf value (see Figure 10).
*10. "tr" (reset time) indicates the period between the time when the $\overline{RES}$ signal rises and when the internal circuit has been reset. Therefore, the S1D1560∗ is usually operable after "tr" time.
*11. Specifies the minimum pulse width of $\overline{RES}$" signal. The LOW pulse greater than "t_{RW}" must be entered for reset.
*12. If the voltage is amplified three times by the built-in power circuit, the primary power V_{SS} must be used within the input voltage range.
*13. The V_5 voltage can be adjusted within the voltage follower operating range by the voltage regulator circuit.
*14, 15, 16 Indicates the current consumed by the separate IC. The current consumption due to the LCD panel capacity and wiring capacity is not included.
The current consumption is shown if the checker is used, the display is turned on, the output status of Case 6 is selected, and the S1D15600D00B∗ is set to 1/64 duty, the S1D15601D00B∗ is set to 1/32 duty, and the S1D15602D00B∗ is set to 1/16 duty.
*14. Applied if an external clock is used and if not accessed by the MPU.
*15. Applied if the built-in oscillation circuit is used and if not accessed by the MPU.
*16. Applied if the built-in oscillation circuit and the built-in power circuit are used (T1 = T2 = Low) and if not accessed by the MPU. Measuring conditions: C1 = 4.7 µF, C2 = 0.47 µF, Ra + Rb = 2 MΩ
This includes the current that flows through the voltage regulator resistor (Ra + Rb = 2 MΩ). If the built-in power circuit is used, the current consumption is equal to the current of V_{SS} power.

Oscillator frequency vs. frame vs. Rf [S1D1560∗D00B∗]

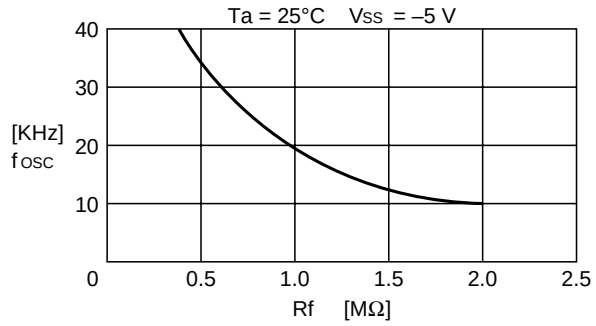


Figure 10 (a)

External clock (f_{CL}) vs. frame [S1D1560∗D00B∗]

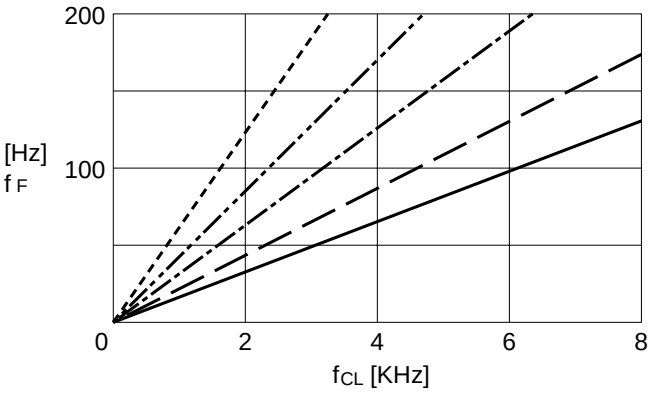


Figure 10 (b)

The relationship between oscillator frequency f_{OSC} and LCD frame frequency f_F is obtained from the following expression.

	Duty	f_F
S1D15600	1/64	$f_{OCS/256}$
	1/48	$f_{OCS/192}$
S1D15601	1/32	$f_{OCS/256}$
	1/24	$f_{OCS/192}$
S1D15602	1/16	$f_{OCS/256}$

(f_F indicates not f_F signal cycle but cycle of LCD AC.)

duty 1/64 S1D15600
duty 1/48
duty 1/32 S1D15601
duty 1/24
duty 1/16 S1D15602

Operating voltage range for V_{SS} and V_5

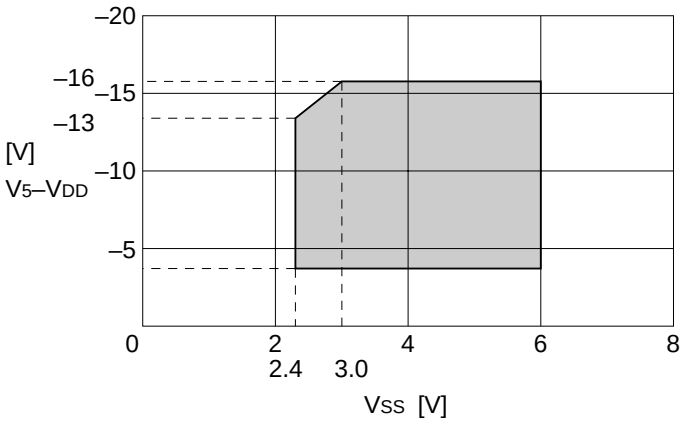


Figure 11

Power consumption during access (I_{DD} (2)) - MPU access cycle

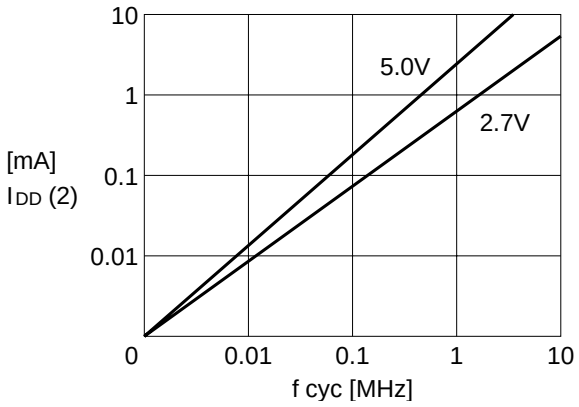


Figure 12

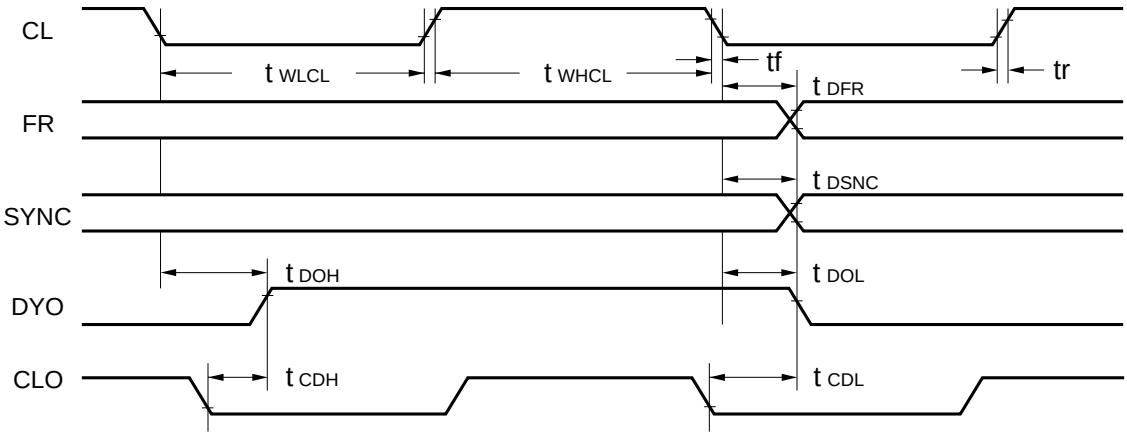
This graphic shows the current consumption when the vertical patterns are written during “fcyc”. If not accessed, I_{DD}(1) is only shown.

Reset

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Reset time	t_R	See note.	1.0	—	—	µs
Reset LOW-level pulsewidth	t_{RW}		1.0	—	—	µs

Note
t_R is measured from the rising edge of $\overline{RES}$. The S1D15600 enters normal operating mode after a reset.

Display control timing



Input timing

V_{SS} = –5.5 to –4.5 V, Ta = –30 to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
CL LOW-level pulsewidth	t_{WLCL}		35	—	—	µs
CL HIGH-level pulsewidth	t_{WHCL}		35	—	—	µs
CL rise time	tr		—	30	—	ns
CL fall time	tf		—	30	—	ns
FR delay time	t_{DFR}		–1.0	—	1.0	µs
SYNC delay time	t_{DSNC}		–1.0	—	1.0	µs

V_{SS} = –4.5 to –2.7 V, Ta = –30 to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
CL LOW-level pulsewidth	t_{WLCL}		35	—	—	µs
CL HIGH-level pulsewidth	t_{WHCL}		35	—	—	µs
CL rise time	tr		—	40	—	ns
CL fall time	tf		—	40	—	ns
FR delay time	t_{DFR}		–1.0	—	1.0	µs
SYNC delay time	t_{DSNC}		–1.0	—	1.0	µs

Notes: 1. Effective only when the S1D15600D00B∗ is in the master mode.
2. The FR/SYNC delay time input timing is provided in the slave operation.
The FR/SYNC delay time output timing is provided in the master operation.
3. Each timing is based on 20% and 80% of V_{SS}.
4. When usingin the range of V_{SS} = –2.4 ~ –4.5V, raise the above ratings for –2.7 ~ –4.5V equally by 30%.

Output timing

V_{SS} = –5.5 to –4.5 V, Ta = –30 to 85 °C

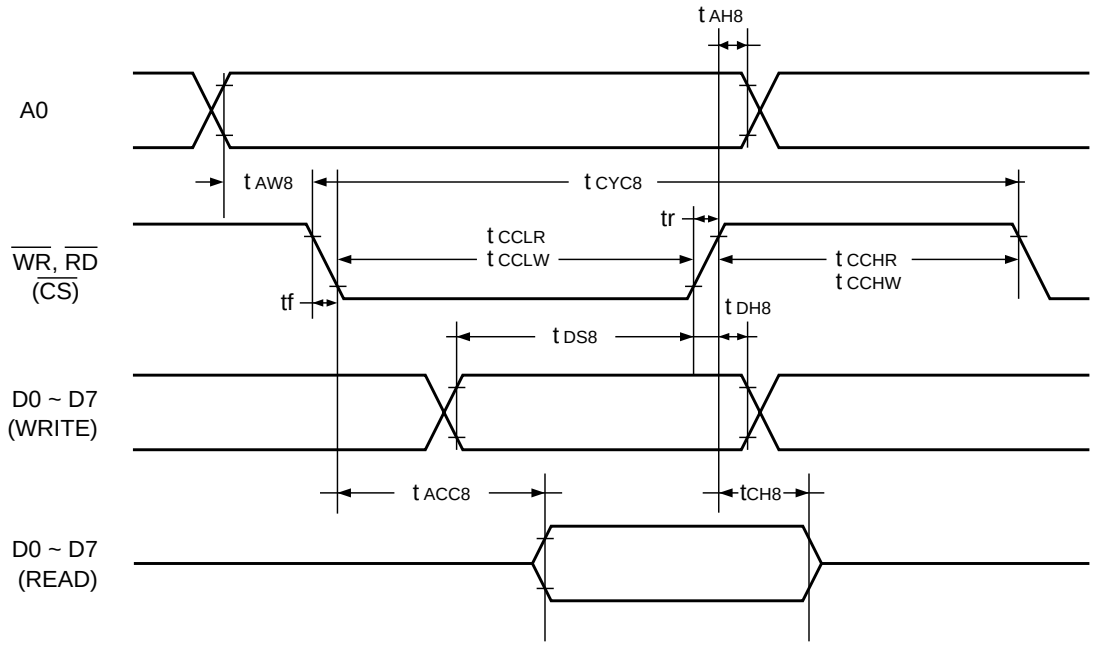
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
FR delay time	t_{DFR}	CL = 50 pF	—	60	150	ns
SYNC delay time	t_{DSNC}		—	60	150	ns
DYO LOW-level delay time	t_{DOL}		—	70	160	ns
DYO HIGH-level delay time	t_{DOH}		—	70	160	ns
CLO to DYO LOW-level delay time	t_{CDL}	S1D15600D0∗B∗ operating in master mode only	10	40	100	ns
CLO to DYO HIGH-level delay time	t_{CDH}	S1D15600D0∗B∗ operating in master mode only	10	40	100	ns

V_{SS} = –4.5 to –2.7 V, Ta = –30 to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
FR delay time	t_{DFR}	CL = 50 pF	—	120	240	ns
SYNC delay time	t_{DSNC}		—	120	240	ns
DYO LOW-level delay time	t_{DOL}		—	140	250	ns
DYO HIGH-level delay time	t_{DOH}		—	140	250	ns
CLO to DYO LOW-level delay time	t_{CDL}	S1D15600D0∗B∗ operating in master mode only	10	100	200	ns
CLO to DYO HIGH-level delay time	t_{CDH}	S1D15600D0∗B∗ operating in master mode only	10	100	200	ns

(1) System buses

Read/write characteristics I (80-series MPU)



V_{SS} = –5.0 ±10%, Ta = –30 to 85 °C

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Address hold time	A0, CS	t_{AH8}		10		ns
Address setup time		t_{AW8}		10		ns
System cycle time		t_{CYC8}		200		ns
Control LOW pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		22		ns
Control LOW pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		77		ns
Control HIGH pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		172		ns
Control HIGH pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		117		ns
Data setup time		t_{DS8}		20		ns
Data hold time		t_{DH8}		10		ns
$\overline{RD}$ access time	D0 to D7	t_{ACC8}	C_L = 100pF		70	ns
Output disable time		t_{CH8}		10	50	ns
Input signal change time		t_r, t_f			15	ns

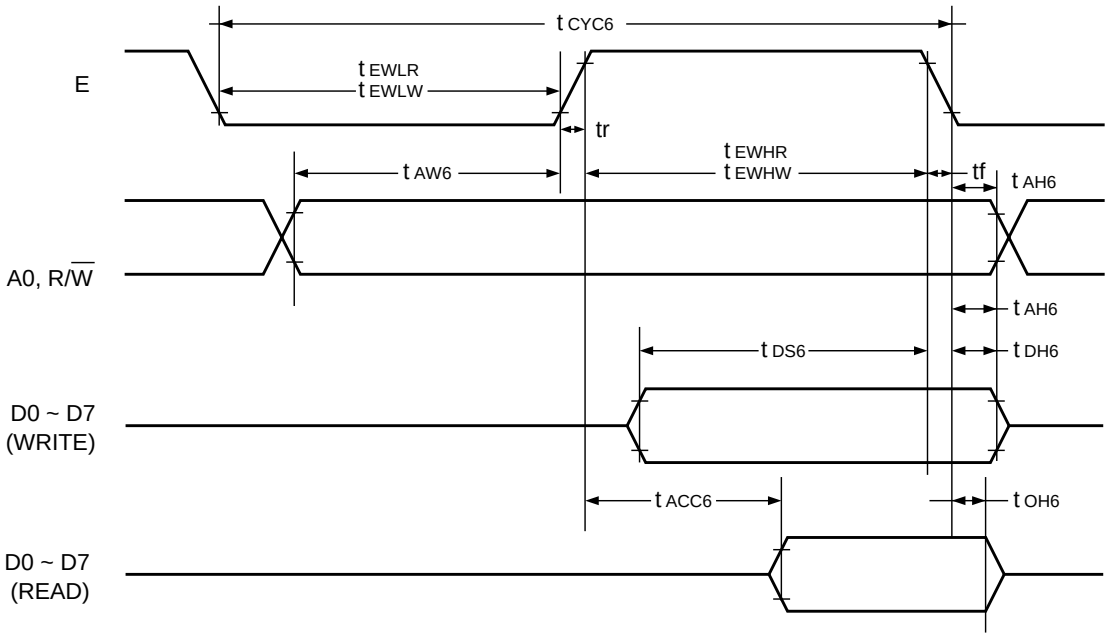
V_{SS} = –2.7 to –4.5 V, Ta = –30 to 85 °C

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Address hold time	A0, CS	t_{AH8}		0		ns
Address setup time		t_{AW8}		0		ns
System cycle time		t_{CYC8}		450		ns
Control LOW pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		44		ns
Control LOW pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		194		ns
Control HIGH pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		394		ns
Control HIGH pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		244		ns
Data setup time		t_{DS8}		20		ns
Data hold time		t_{DH8}		10		ns
$\overline{RD}$ access time	D0 to D7	t_{ACC8}	C_L = 100pF		140	ns
Output disable time		t_{CH8}		10	100	ns
Input signal change time		t_r, t_f			15	ns

Notes:
1. When using the system cycle time in the high-speed mode, it is limited by $t_r + t_f \le (t_{CYC8} - t_{CCLW} - t_{CCHW})$ or $t_r + t_f \le (t_{CYC8} - t_{CCLR} - t_{CCHR})$
2. All signal timings are limited based on the 20% and 80% of V_{SS} voltage.
3. Read/write operation is performed while CS ($\overline{CS1}$ and CS2) is active and the RD or WR signal is in the LOW level.
   If read/write operation is performed by the RD or WR signal while CS is active, it is determined by the $\overline{RD}$ or $\overline{WR}$ signal timing.
   If read/write operation is performed by CS while the RD or WR signal is in the low level, it is determined by the CS active timing.
4. When usingin the range of V_{SS} = –2.4 ~ –4.5V, raise the above ratings for –2.7 ~ –4.5V equally by 30%.

(2) System buses

Read/write characteristics II (68-series MPU)



V_{SS} = –5.0 V ± 10%, Ta = –30 ~ 85 °C

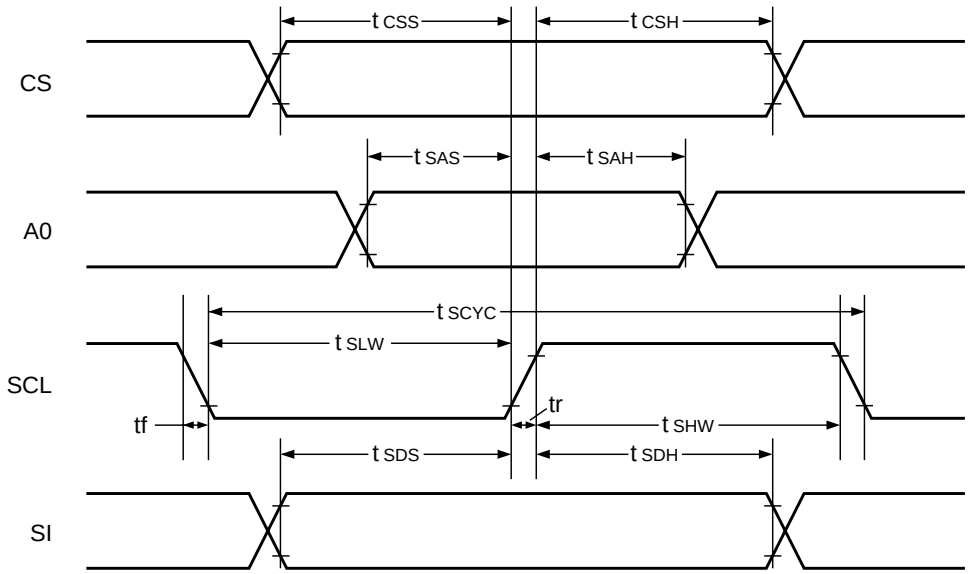
Item		Signal	Symbol	Conditions	Min.	Max.	Unit
System cycle time			t_{CYC6}		200		ns
Address setup time		(A0)	t_{AW6}		10		ns
Address hold time		R/$\overline{W}$	t_{AH6}		10		ns
Data setup time		D0~D7	t_{DS6}		20		ns
Data hold time			t_{DH6}		10		n
Output disable time			t_{OH6}	CL = 100pF	10	50	ns
Access time			t_{ACC5}			70	ns
Enable HIGH pulse width	READ	E	t_{EWHR}		77		ns
	WRITE		t_{EWHW}		22		ns
Enable LOW pulse width	READ	E	t_{EWLR}		117		ns
	WRITE		t_{EWLW}		172		ns
Input signal change time			t_r, t_f			15	ns

V_{SS} = –2.7 V ~ 4.5 V, Ta = –30 ~ 85 °C

Item		Signal	Symbol	Conditions	Min.	Max.	Unit
System cycle time			t_{CYC6}		450		ns
Address setup time		A0	t_{AW6}		0		ns
Address hold time		R/$\overline{W}$	t_{AH6}		0		ns
Data setup time		D0 to D7	t_{DS6}		20		ns
Data hold time			t_{DH6}		10		ns
Output disable time			t_{OH6}	CL = 100pF	20	100	ns
Access time			t_{ACC5}			140	ns
Enable HIGH pulse width	READ	E	t_{EWHR}		194		ns
	WRITE		t_{EWHW}		44		ns
Enable LOW pulse width	READ	E	t_{EWLR}		244		ns
	WRITE		t_{EWLW}		394		ns
Input signal change time			t_r, t_f			15	ns

Notes:
1. When using the system cycle time in the high-speed mode, it is limited by $t_r + t_f \le (t_{CYC6}-t_{EWLW}-t_{EWHW})$ or $t_r + t_f \le (t_{CYC6}-t_{EWLR}-t_{EWHR})$.
2. All signal timings are limited based on the 20% and 80% of V_{SS} voltage.
3. Read/write operation is performed while CS ($\overline{CS1}$ and CS2) is active and the E signal is in the high level. If read/write operation is performed by the E signal while CS is active, it is determined by the E signal timing.
   If read/write operation is performed by CS while the E signal is in the high level, it is determined by the CS active timing.
4. When usingin the range of V_{SS} = –2.4 ~ –4.5V, raise the above ratings for –2.7 ~ –4.5V equally by 30%.

(3) Serial interface



V_{SS} = –5.0 V ±10%, Ta = –30 ~ 85 °C

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Serial clock cycle	SCL	t_{SCYC}		250		ns
SCL HIGH pulse width		t_{SHW}		75		ns
SCL LOW pulse width		t_{SLW}		75		ns
Address setup time	A0	t_{SAS}		50		ns
Address hold time		t_{SAH}		200		ns
Data setup time	SI	t_{SDS}		50		ns
Data hold time		t_{SDH}		30		ns
CS-SCL time	CS	t_{CSS}		30		ns
		t_{CSH}		400		
Input signal change time		t_r, t_f			50	ns

V_{SS} = –2.7 V ~ –4.5 V, Ta = –30 ~ 85 °C

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Serial clock cycle	SCL	t_{SCYC}		500		ns
SCL HIGH pulse width		t_{SHW}		150		ns
SCL LOW pulse width		t_{SLW}		150		ns
Address setup time	A0	t_{SAS}		100		ns
Address hold time		t_{SAH}		400		ns
Data setup time	SI	t_{SDS}		100		ns
Data hold time		t_{SDH}		100		ns
CS-SCL time	CS	t_{CSS}		60		ns
		t_{CSH}		800		
Input signal change time		t_r, t_f			50	ns

*1. All signal timings are limited based on the 20% and 80% of V_{SS} voltage.
*2. When usingin the range of V_{SS} = –2.4 ~ –4.5V, raise the above ratings for –2.7 ~ –4.5V equally by 30%.

7. FUNCTIONAL DESCRIPTION

Microprocessor Interface

Parallel/serial interface

Parallel data can be transferred in either direction between the controlling microprocessor and the S1D15600/601/602 series through the 8-bit I/O buffer (D0 to D7). Serial data can be sent from the microprocessor to the S1D15600/601/602 series through the serial data input (SI), but not from the S1D15600/601/602 series to the microprocessor. The parallel or serial interface is selected by P/S as shown in table 1.

Table 1. Parallel/serial interface selection

P/S	Input type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	SI	SCL	D0 to D7
HIGH	Parallel	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	—	—	D0 to D7
LOW	Serial	$\overline{CS1}$	CS2	A0	—	—	—	SI	SCL	(Hz)

Note
"—" indicates fixed to either HIGH or to LOW

For the parallel interface, the type of microprocessor is selected by C86 as shown in table 2.

Table 2. Microprocessor selection for parallel interface

C86	MPU bus type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
HIGH	6800-series	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D0 to D7
LOW	8080-series	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7

Parallel interface

A0, $\overline{WR}$ (or R/$\overline{W}$) and $\overline{RD}$ (or E) identify the type of parallel data transfer to be made as shown in table 3.

Serial interface

The serial interface comprises an 8-bit shift register and a 3-bit counter. These are reset when $\overline{CS1}$ is HIGH and CS2 is LOW. When these states are reversed, serial data and clock pulses can be received from the microprocessor on SI and SCL, respectively.

Table 3. Parallel data transfer

Common	6800 series		8080 series		Description
A0	R/W	E	$\overline{RD}$	$\overline{WR}$	
1	1	1	0	1	Display data read out
1	0	1	1	0	Display data write
0	1	1	0	1	Status read
0	0	1	1	0	Write to internal reigister (command)

Serial data is read on the rising edge of SCL and must be input at SI in the sequence D7 to D0. On every eighth clock pulse, the data is transferred from the shift register and processed as 8-bit parallel data.
Input data is display data when A0 is HIGH and control data when A0 is LOW. A0 is read on the rising edge of every eighth clock signal.
The SLC signal is affected by the termination reflection and external noise caused by the line length. The operation check on the actual machine is recommended.

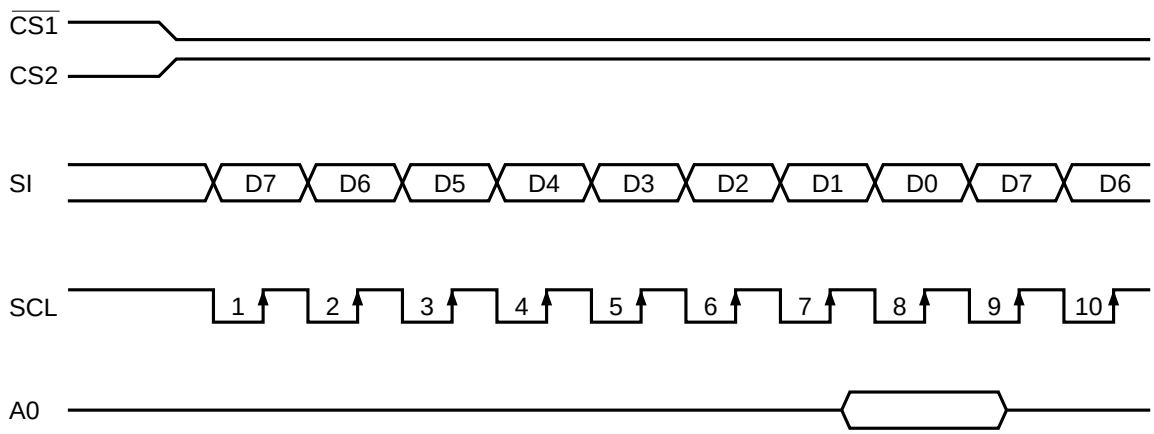


Figure 1. Serial interface timing

Chip select inputs

The S1D15600/601/602 series has two chip select pins: CS1 and CS2, and data exchange between the microprocessor and the S1D15600/601/602 series is enabled when CS1 is LOW and CS2 is HIGH. When these pins are set to any other combination, D0 to D7 are high impedance. The A0, RD, WR, SI and SCI inputs are disabled. If the serial input interface has been selected, the shift register and counter are reset. The Reset signal is entered independent from the CS1 and CS2 status.

Data Transfer

To match the timing of the display data RAM and registers to that of the controlling microprocessor, the S1D15600/601/602 series uses an internal data bus and bus buffer. A kind of pipeline processing takes place. When the microprocessor reads the contents of RAM, the data for the initial read cycle is first stored in the busbuffer (dummy read cycle). On the next read cycle, the data is read from the bus buffer onto the microprocessor bus. At the same time, the next block of data is transferred from RAM to the bus buffer. Likewise, when the microprocessor writes data to display data RAM, the data is first stored in the bus buffer before being written to RAM at the next write cycle.

When writing data from the microprocessor to RAM, there is no delay since data is automatically transferred from the bus buffer to the display data RAM. If the data rate is required to slow down, the microprocessor can insert an NOP instruction which has the same affect as executing a wait procedure.

When a sequence of address sets is executed, a dummy read cycle must be inserted between each pair of address sets. This is necessary because the addressed data from the RAM is delayed one cycle by the bus buffer, before it is sent to the microprocessor. A dummy read cycle is thus necessary after an address set and after a write cycle.

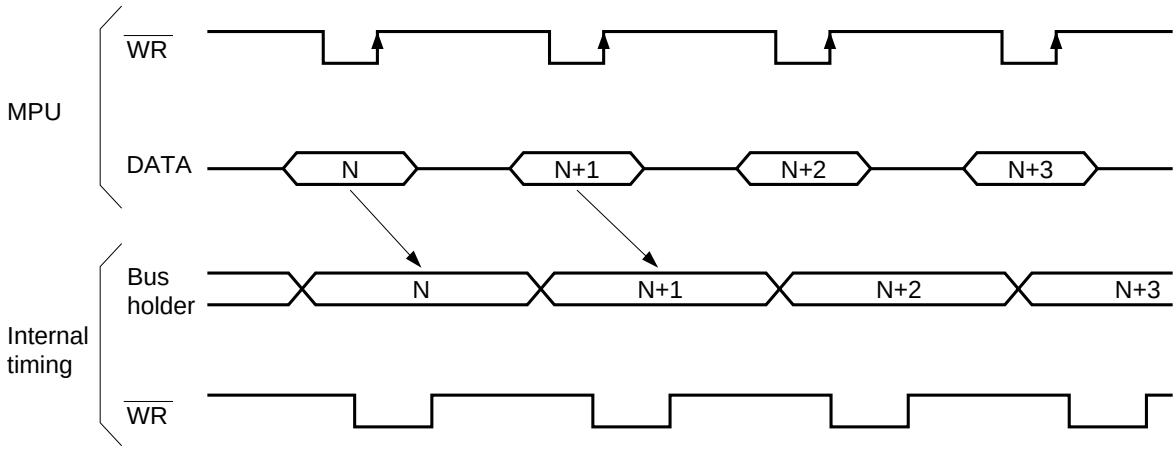


Figure 2. Write timing

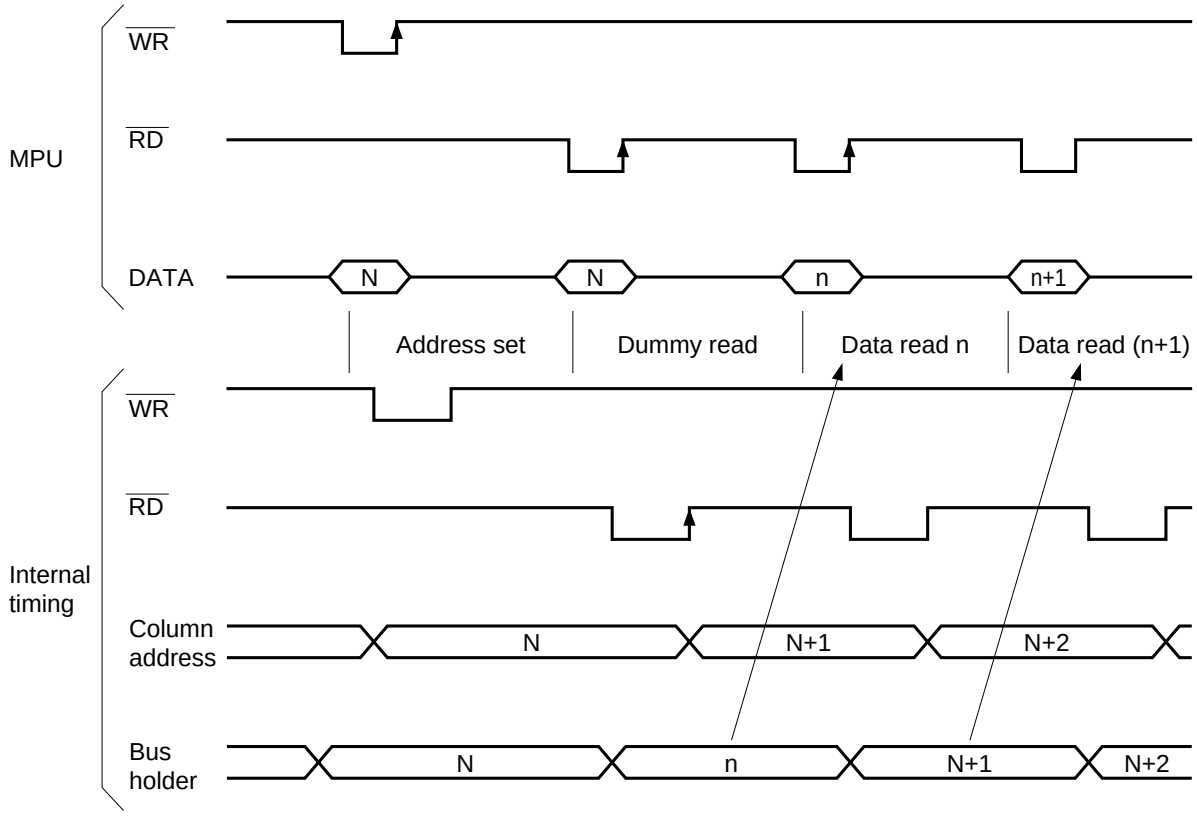


Figure 3. Read timing

Status Flag

The S1D15600/601/602 series has a single bit status flag, D7. When D7 is HIGH, the device is busy and will only accept a Status Read command. If cycle times are monitored ed carefully, this flag does not have to be checked before each command, and microprocessor capabilities can be fully utilized.

Display Data RAM

The display data RAM stores pixel data for the LCD. It is a 166-column × 65-row addressable array as shown in figure 4.

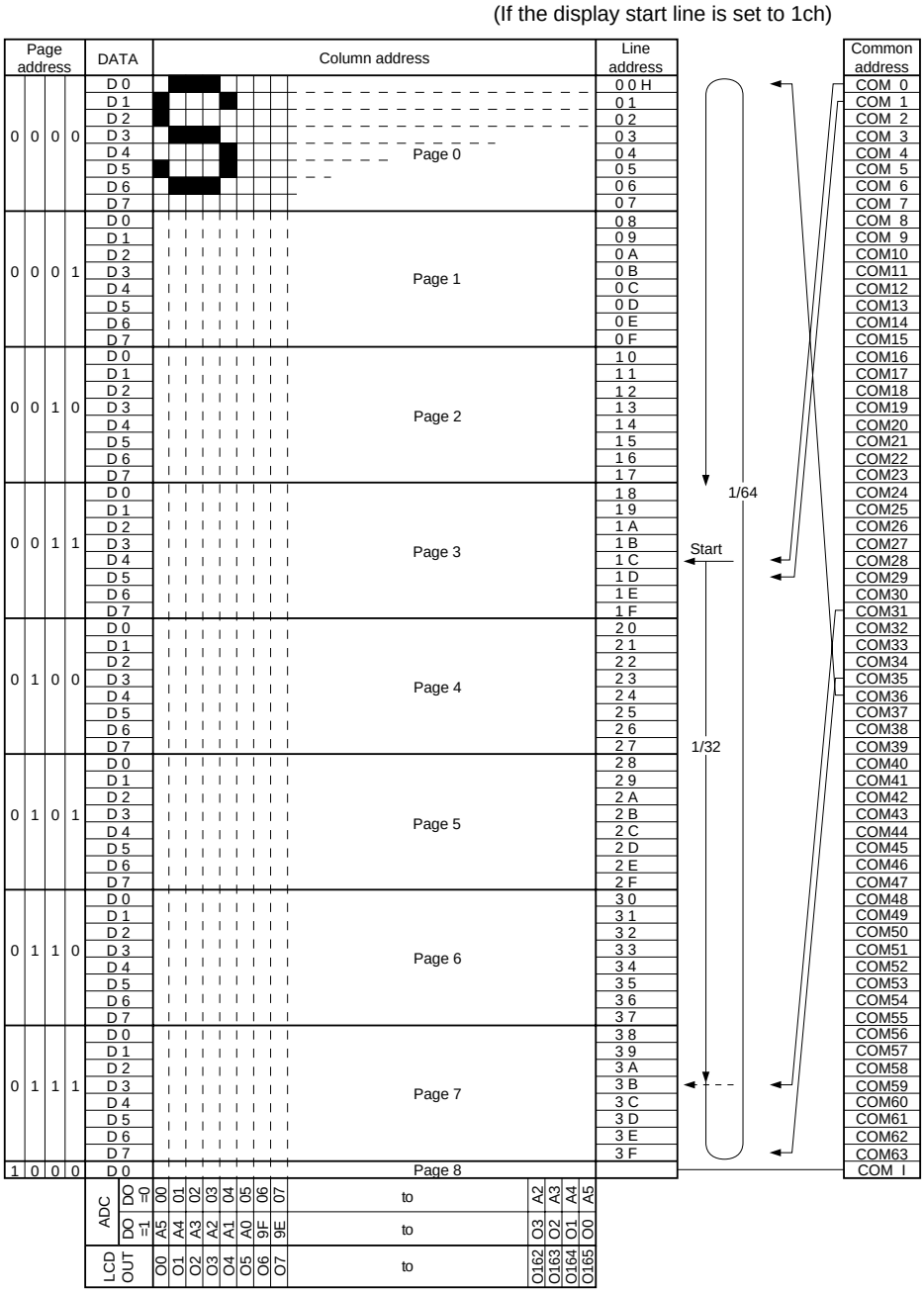


Figure 4. Display data RAM addressing

Note

For a 1/65 and 1/33 display duty cycles, page 8 is accessed following 1BH and 3BH, respectively.

The 65 rows are divided into 8 pages of 8 lines and a ninth page with a single line (D0 only). Data is read from or written to the 8 lines of each page directly through D0 to D7.

The time taken to transfer data is very short, because the microprocessor inputs D0 to D7 correspond to the LCD common lines as shown in figure 5. Large display configurations can thus be created using multiple S1D15600/601/602.

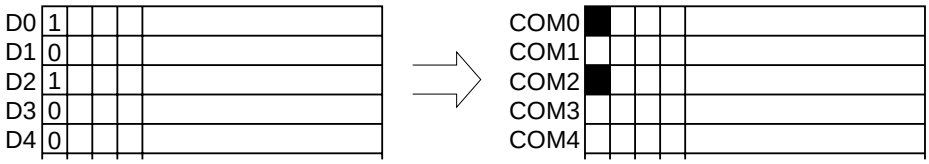


Figure 5. RAM-to-LCD data transfer

The microprocessor reads from and writes to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written to RAM at the same time as data is being displayed, without causing the LCD to flicker.

Column Address Counter

The column address counter is an 8-bit presettable counter that provides the column address to display data RAM. See figure 4. It is incremented by 1 each time a read or write command is received. The counter automatically stops at the highest address, A6H. The contents of the column address counter are changed by the Column Address Set command. This counter is independent of the page address register.
When the Select ADC command is used to select inverse display operation, the column address decoder inverts the relationship between the RAM column data and the display segment outputs.

Page Address Register

The 4-bit page address register provides the page address to display data RAM. The contents of the register are changed by the Page Address Set command.
Page address 8 (D3 = HIGH, D2, D1, D0 = LOW) is a special use RAM area for the indicator.

Initial Display Line Register

The initial display line register stores the address of the RAM line that corresponds to the first (normally the top) line (COM0) of the display. See figure 4. The contents of this 6-bit register are changed by the Initial Display Line command. At the start of each LCD frame, synchronized with SYNC, the initial line is copied to the line counter. The line counter is then incremented on the CL clock signal once for every display line. This generates the line addresses for the transfer of the 166 bits of RAM data to the LCD drivers.
If a 1/65 or 1/33 display duty cycle is selected by the Duty + 1 command, the line address corresponding to the 65th or 33rd SYNC signal is changed and the indicator special-use line address is selected. If the Duty + 1 command is not used, the indicator special-use line address is not selected.

Output Selection Circuit

The number of common (COM) and segment (SEG) driver outputs can be selected to fit different LCD panel configurations by the output selection circuit.
There are 70 segment-only outputs (O32 to O101) and 96 common or segment dual outputs (O0 to O31 and O102 to O165). A command select the status of the dual common/segment outputs. Figure 6 shows the six different LCD driver arrangements.
Necessary LCD driver voltage is automatically allocated to the COM/SEG dual outputs when their function is determined by the output selection circuit.
The S1D15600 selects Case 1, 2 or 6 while the S1D15601 selects Case 3, 4, 5 or 6. As to the S1D15602, COM/SEG output status cannot be selected, being fixed.

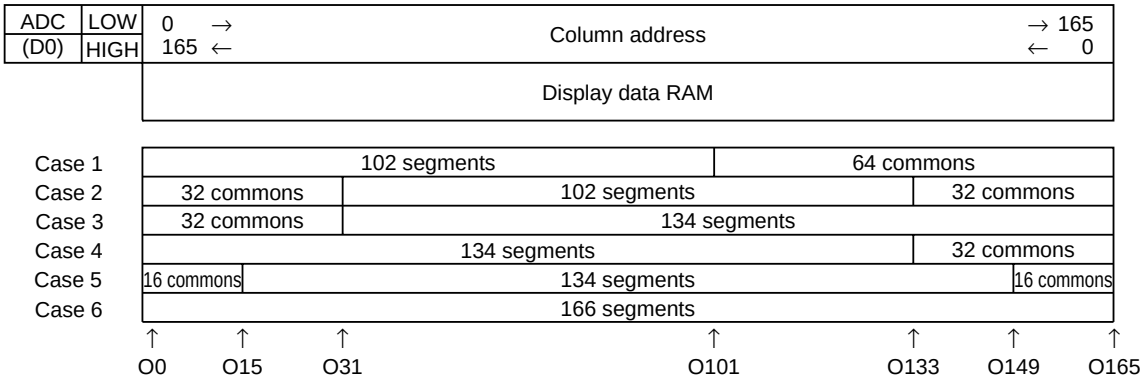


Figure 6. Output configuration selection

When COM outputs are assigned to the output drivers, the unused RAM area is not available. However, all RAM column addresses can still be accessed by the microprocessor.
Since duty setting and output selection are independent, the appropriate duty must be selected for each case.
Cases 1 to 6 are determined according to the three lowest bits in the output status register in the output selection circuit. The COM output scanning direction can be selected by setting bit D3 in the output status register to HIGH or LOW.

Table 4

	S1D15600		S1D15601		S1D15602
Duty	1/64	1/48	1/32	1/24	1/16
COM I function	COM64	COM48	COM32	COM24	COM16

When the DUTY + 1 command is executed, pin COM1 becomes as shown in Figure 4 irrelevant to output selection:
Since master/slave operation and the output selection circuit are completely independent in the S1D15600/601/602 series, a chip either on the master or slave side can be allocated to the COM output function in multi-chip configuration.
The LCD driver outputs shown in Table 5 become ineffective when the S1D15600 or S1D15601 is used with 1/48 or 1/24 duty, respectively. In this case, ineffective outputs are used in the open state.

Table 5

		Output status register				Ineffective output
		D3	D2	D1	D0	
S1D15600	Case 1	0	1	0	1	O150 to O165
		1	1	0	1	O102 to O117
	Case 2	0	1	0	0	O150 to O165
		1	1	0	0	O16 to O31
S1D15601	Case 3	0	0	1	1	O0 to O7
		1	0	1	1	O23 to O31
	Case 4	0	0	1	0	O158 to O165
		1	0	1	0	O134 to O141
	Case 5	0	0	0	1	O158 to O165
		1	0	0	1	O8 to O15

S1D15600 Output Status

The S1D15600 selects any output status from Cases 1, 2 and 6.

1/64 duty (Display Area 64 × 102)

Case	Status register				LCD driver output							
	D3	D2	D1	D0	O0	O31	O32	O101	O102	O133	O134	O165
1	0	1	0	1	SEG102				COM0 →			COM63
	1	1	0	1	SEG102				COM63 ←			COM0
2	0	1	0	0	COM31 ←	COM0	SEG102				COM32 →	COM63
	1	1	0	0	COM32 →	COM63	SEG102				COM31 ←	COM0
6	–	0	0	0	SEG166							

1/48 duty (Display Area 48 × 102)

Case	Status register				LCD driver output							
	D3	D2	D1	D0	O0	O31	O32	O101	O102	O133	O134	O165
1	0	1	0	1					COM0 →			COM47
	1	1	0	1						COM47 ←		COM0
2	0	1	0	0	COM31 ←	COM0	SEG102				COM32→47	
	1	1	0	0	COM32→47		SEG102				COM31 ←	COM0
6	–	0	0	0	SEG166							

S1D15601 Output Status

The S1D15601 selects any output status from Cases 3, 4, 5 and 6.

1/32 duty (Display Area 32 × 134)

Case	Status register				LCD driver output									
	D3	D2	D1	D0	O0	O15	O16	O31	O32	O133	O134	149	150	O165
3	0	0	1	1	COM31 ←		COM0		SEG134					
	1	0	1	1	COM0 →		COM31		SEG134					
4	0	0	1	0	SEG134						COM0 →			COM31
	1	0	1	0	SEG134						COM31 ←			COM0
5	0	0	0	1	15←COM0		SEG134							COM16→31
	1	0	0	1	COM16→31		SEG134							15←COM0
6	–	0	0	0	SEG166									

1/24 duty (Display Area 24 × 134)

Case	Status register				LCD driver output									
	D3	D2	D1	D0	O0	O15	O16	O31	O32	O133	O134	149	150	O165
3	0	0	1	1		COM23 ←		COM0	SEG134					
	1	0	1	1	COM0 →		COM23		SEG134					
4	0	0	1	0	SEG134						COM0 →			COM23
	1	0	1	0	SEG134							COM23 ←		COM0
5	0	0	0	1	15←COM0		SEG134							16→23
	1	0	0	1	16→23		SEG134							15←COM0
6	–	0	0	0	SEG166									

S1D15602 Output Status

COM/SEG output status of the S1D15602 is fixed.
1/16 duty (16 × 150)

LCD driver output			
00	0149	150	0165
SEG150		15 ◄——	COM0

Display Timers

Line counter and display data latch timing

The display clock, CL, provides the timing signals for the line counter and the display data latch. The RAM line address is generated synchronously using the display clock. The display data latch synchronizes the 166-bit display data with the display clock.
The timing of the LCD panel driver outputs is independent of the timing of the input data from the microprocessor.

FR and SYNC

The LCD AC signal, FR, and the synchronization signal, SYNC, are generated from the display clock. The FR controller generates the timing for the LCD panel driver outputs. Normally, 2-frame wave patterns are generated, but *n*-line inverse wave patterns can also be generated. These produce a high-quality display if *n* is based on the LCD panel being used.
SYNC synchronizes the timing of the line counter and common timers. It is also needed to synchronize the frame period and a 50% duty clock.

In a multiple-chip configuration, FR and SYNC are inputs. The SYNC signal from the master synchronizes the line counter and common timing of the slave.

Common timing signals

The internal common timing and the special-use common driver start signal, DYO, are generated from CL. As shown in figures 7 and 8, DYO outputs a HIGH-level pulse on the rising edge of the CL clock pulse that precedes a change on SYNC. DYO is generated by both the S1D15600D0B∗, regardless of whether the device is in master or slave mode. However, when operating in slave mode, the device duty and the external SYNC signal must be the same as that of the master. In a multiple-chip configuration, FR and SYNC must be supplied to the slave from the master.

Table 6. Master and slave timing signal status

Part number	Mode	FR	SYNC	CLO	DYO
SD1560∗D∗∗B∗	Master	Output	Output	CL output	Output
	Slave	Input	Input	High impedance	Output

2-frame AC driver waveform

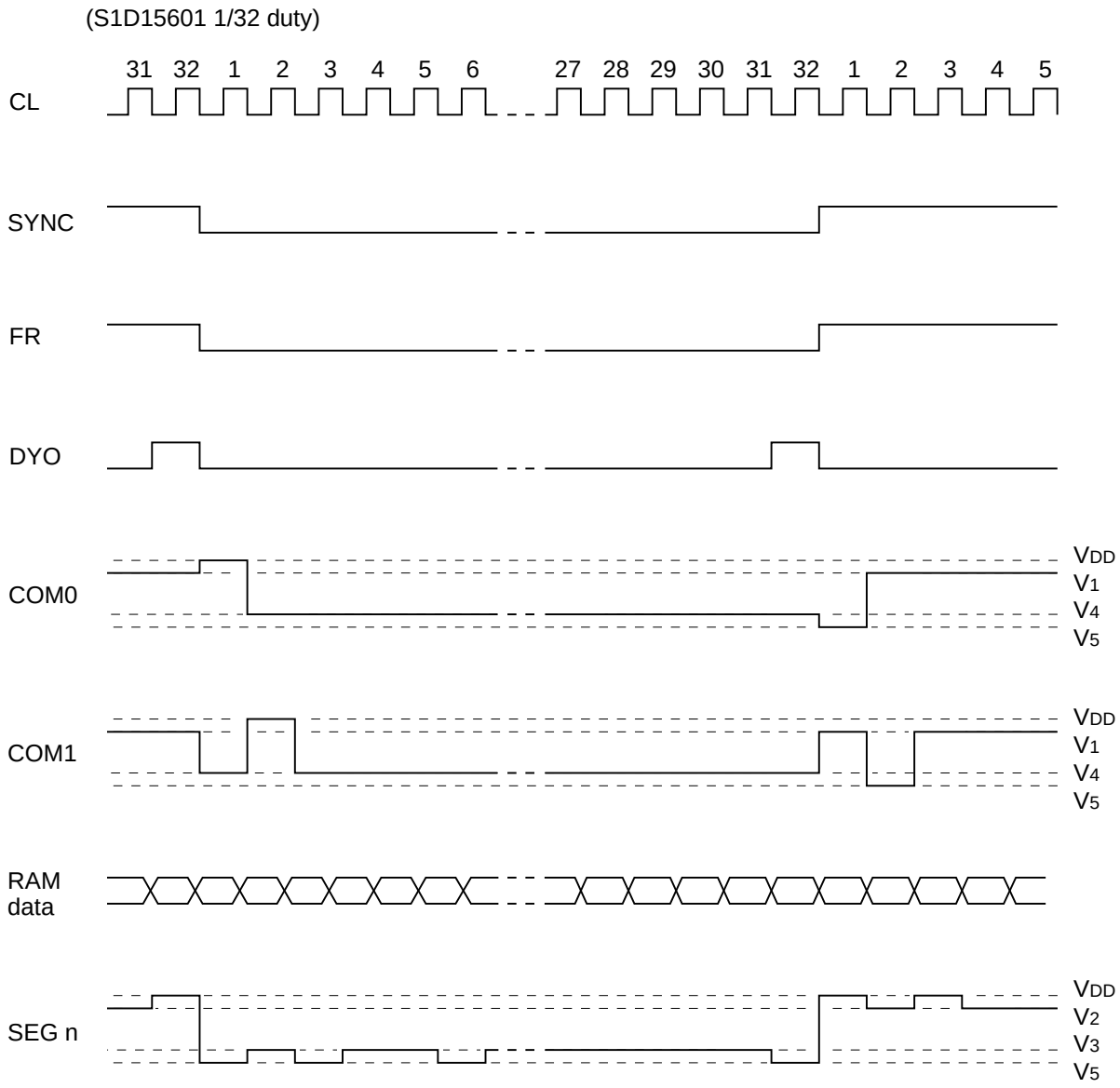


Figure 7. Frame driver timing

n line inverse driver waveform (n = 5, line inverse register 4)

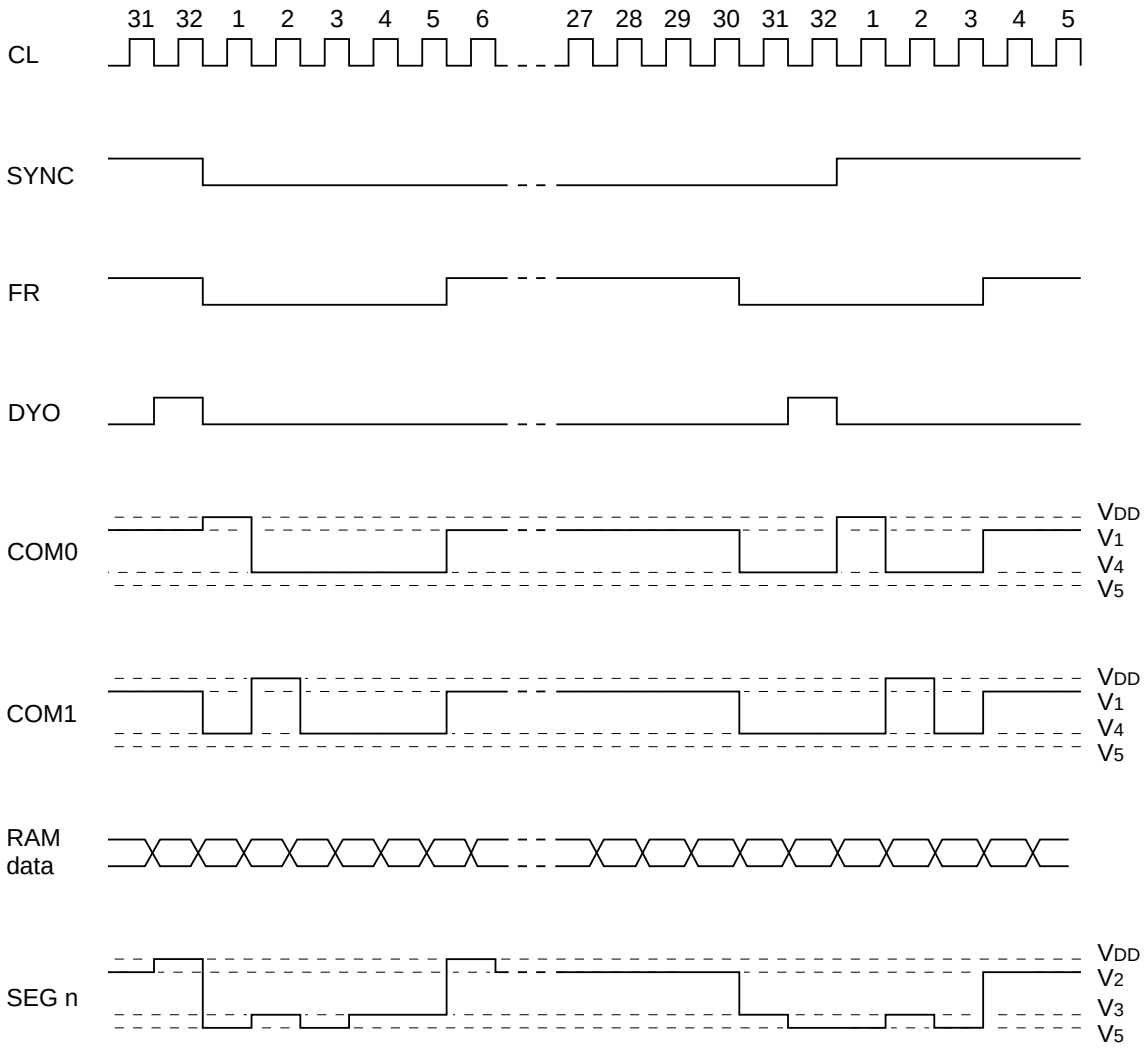


Figure 8. Line inverse driver timing

Note
When *n* = 5, the line inversion register is set to 4.

LCD Driver

The LCD driver converts RAM data into the 167 outputs that drive the LCD panel. There are 70 segment outputs, 96 segment or common dual outputs, and a COM1 output for the indicator display.

Two shift registers for the common/segment drivers are used to ensure that the common outputs are output in the correct sequence. The driver output voltages depend on the display data, the common scanning signal and FR.

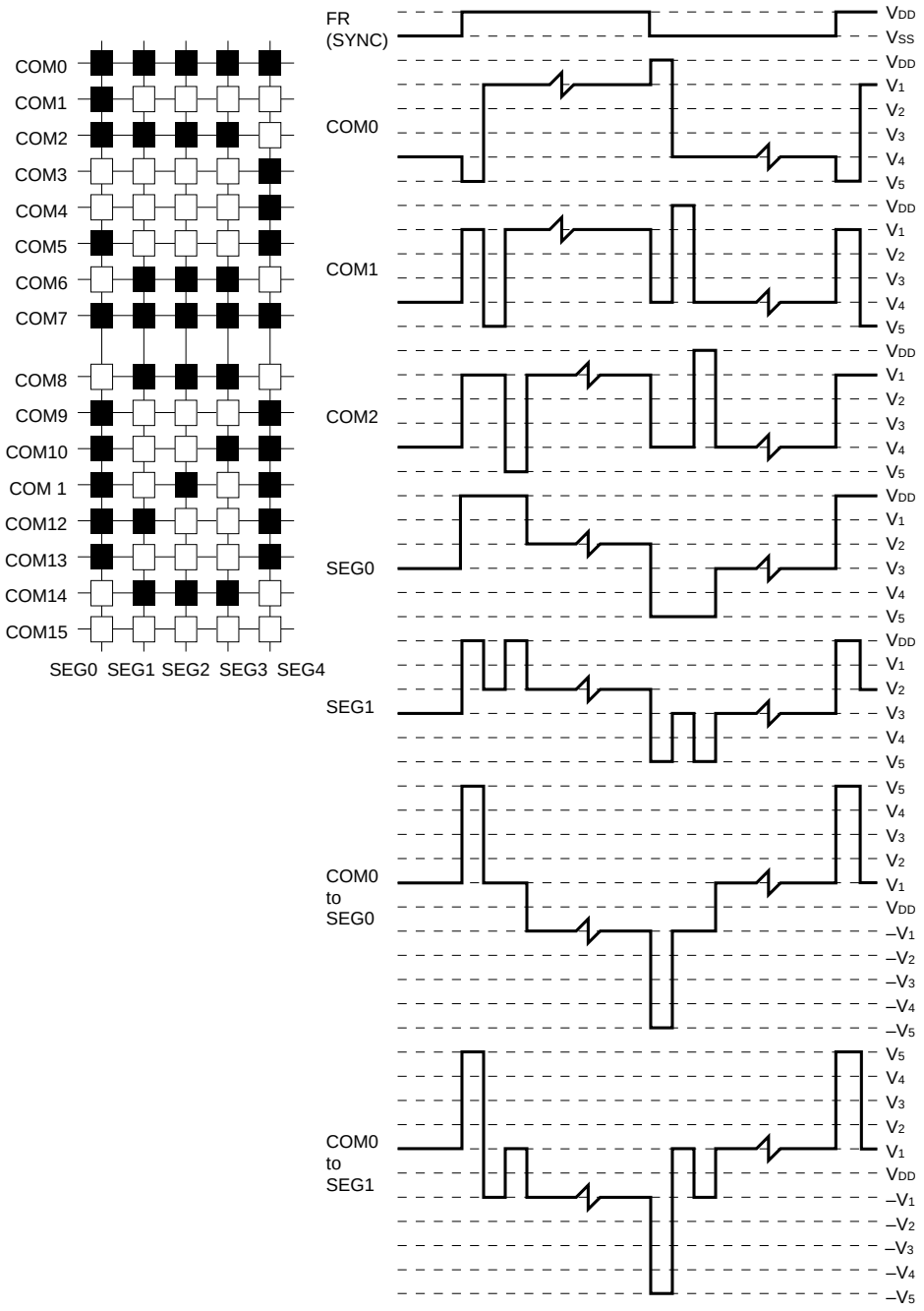


Figure 9. Example of segment and common timing

Display Data Latch Circuit

The display data latch circuit temporarily stores the output display data from the display data RAM to the LCD driver circuit in each common period. Since the Normal/Inverse Display, Display ON/OFF and Display All Points ON/OFF commands control the data in this latch, the data in the display data RAM is remains unchanged.

LCD Driver Circuit

This multiplexer generates 4-value levels for the LCD driver, having 167 outputs of 70 SEG outputs, 96 SEG/COM dual outputs and a COM output for the indicator display. The SEG/COM dual outputs have a shift register and sequentially transmits COM scanning signals. The LCD driver voltage is output according to the combination of display data, COM scanning signal and FR signal. Figure 9 shows a typical SEG/COM output waveform.

Oscillator Circuit

The low power consumption type CR oscillator adjusting the oscillator frequency by use of only oscillator resistor Rf is used as a display timing signal source or clock for the voltage raising circuit of the LCD power supply.
The oscillator circuit is only available in the master operation mode. When a signal from the oscillator circuit is used for display clock, fix the CL pin to the VSS level. When the oscillator circuit is not used, fix the OSC1 or OSC2 pin to the VDD or VSS level, respectively.
The oscillator signal frequency is divided and output from the CLO pin as display clock. The frequency is divided to one-fourth, one-eighth or one-sixteenth in the S1D15600, S1D15601 or S1D15602, respectively.

FR Control Circuit

The LCD driver voltage supplied to the LCD driver outputs is selected using FR signal.

Power Supply Circuit

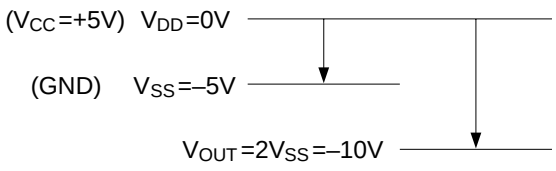
This is a power circuit to produce voltage needed to drive liquid crystals at a low power consumption. This circuit is valid only when the S1D1560∗D∗∗B∗ master is in opera-tion. The power circuit consists of voltage tripler, voltage regulator and the voltage follower.
The power circuit built into S1D1560∗D∗∗B∗ is set for smaller scale liquid crystal panels and it is not too suitable when the picture element is larger or to drive a liquid crystal panel with lager indication capacity using multiple chips. With liquid crystal panels with a larger load capacity, the quality of display may become very bad. Use an external power in such cases. (If an external amp circuit is configured, we recommend to use the S1F76600 and S1F76610.)
The power circuit can be controlled by the built-in power ON/OFF command. When the built-in power is turned off, all of the boosting circuit, voltage regulation circuit and voltage follower circuit goes open. In this case, the liquid crystal driving voltage V_1, V_2, V_3, V_4 and V_5 should be supplied from outside and the terminals CAP1+, CAP1-, CAP2+, CAP2-, Vout and V_R should be kept opened.
If the built-in power supply is turned on, you must always enter this command after the wait time of the built-in power supply turn-on completion command.
Various functions of the power circuit may be selected by combinations of the setting of the T1 and T2. It is also possible to make a combined use of the external power supply and a portion of the functions of the built-in power supply.

T1	T2	Voltage tripler	Voltage regulator	voltage follower	External voltage input	Voltage tripler terminals	V_R terminals
LOW	LOW	○	○	○	–		
LOW	HIGH	○	○	○	–		
HIGH	LOW	×	○	○	VOUT	OPEN	
HIGH	HIGH	×	×	○	V5	OPEN	OPEN

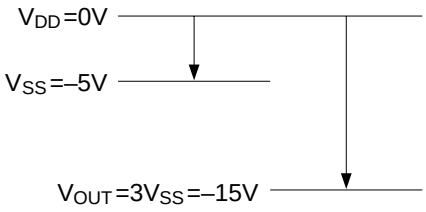
When (T1, T2) = (HIGH, LOW), the boosting circuit does not work and open the boosting circuit terminals (CAP1+, CAP1-, CAP2+ and CAP2-) and apply liquid crystal driving voltage to the Vout terminals from outside.
When (T1, T2) = (HIGH, HIGH), the boosting circuit and voltage regulation circuit do not work and open the boosting circuit terminals and the VR terminals and apply liquid crystal driving voltage connecting the V5 terminals.

Voltage tripler

By connecting capacitors C1 between CAP1+ and CAP1-, CAP2+ and CAP2- and VSS-Vout, the electric potential between VDD-VSS is boosted to the triple toward negative side and outputted from the Vout terminal. When a double boosting is required, disconnect the capacitor between CAP2+ and CAP2- and short-circuit the CAP2- and Vout terminals to obtain output boosted to the double out of the Vout (or CAP2-) terminal.
Signals from the oscillation circuit are used in the boosting circuit and it then is necessary that the oscillation circuit is in operation.
Electric potentials by the boosting functions are given below.



Electric potentials of double boosting



Electric potentials of triple boosting

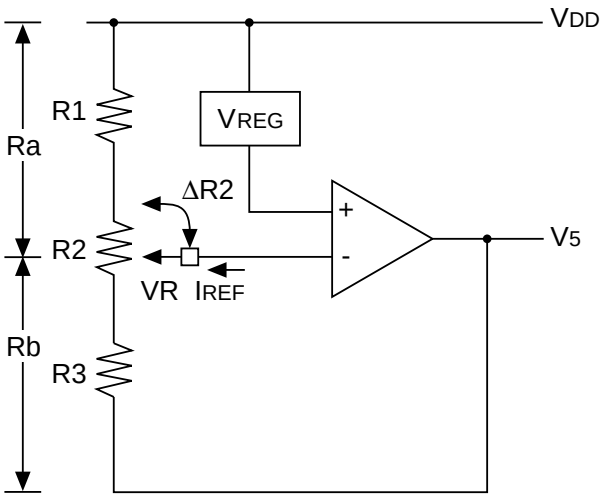
Voltage Regulator

The boosting voltage occurring at V_{OUT} is sent to the voltage regulator, and the V_5 liquid crystal display (LCD) driver voltage is output. This V_5 voltage can be determined by the following equation when resistors Ra and Rb (R1, R2 and R3) are adjusted within the range of $|V_5| < |V_{OUT}|$.

$$V_5=\left(1+\frac{Rb}{Ra}\right) V_{REG}+I_{REF} \cdot Rb$$

$$=\left(1+\frac{R3+R2-\Delta R2}{R1+\Delta R2}\right) V_{REG}$$

$$+I_{REF} \cdot (R3+R2-\Delta R2)$$



V_{REG} is the constant voltage source of the IC, and it is constant and $V_{REG} \fallingdotseq -2.5 \pm 0.15$ V (if V_{DD} is 0 V). To adjust the V_5 output voltage, insert a variable resistor between V_R, V_{DD} and V_5 as shown. A combination of R1 and R3 constant resistors and R2 variable resistor is recommended for fine-adjustment of V_5 voltage.

Setup example of resistors R1, R2 and R3: (In case of Type 1)

When the Electronic Volume Control Function is OFF (electronic volume control register values are (D4,D3,D2,D1,D0)=(0,0,0,0,0)):

$$V_5 = \frac{(1 + R3 + R2 - \Delta R2)}{R1 + \Delta R2} V_{REG} \quad \cdots\cdots\cdots\cdots \textcircled{1}$$

(As $I_{REF} = 0$ A)

- $R1 + R2 + R3 = 5M\Omega$ ..... ②
  (Determined by the current passing between V_{DD} and V_5)
- Variable voltage range by R2 $V_5 = -6$ to -10 V
  (Determined by the LCD characteristics)
  $\Delta R2 = O\Omega$, $V_{REG} = -2.55$V
  To obtain $V_5 = -10$ V, from equation ①:
  $R2 + R3 = 2.92 \times R1$ ..... ③
  $\Delta R2 = R2$, $V_{REG} = -2.55$V
  To obtain $V_5 = -6$ V, from equation ①:
  $1.35 \times (R1 + R2) = R3$ ..... ④

From equations ②, ③ and ④:
R1=1.27MΩ
R2=0.85MΩ
R3=2.88MΩ

The voltage regulator has a temperature gradient of approximately -0.2%/°C as the V_{REG} voltage. To obtain another temperature gradient, use the Electronic Volume Control Function for software processing using the MPU.

As the VR pin has a high input impedance, the shielded and short lines must be protected from a noise interference.
In case of Type 2, similarly preset R1, R2 and R3 on the basis of $V_{REG} = V_{SS}$.

Voltage regulator using the Electronic Volume Control Function

The Electronic Volume Control Function can adjust the intensity (brightness level) of liquid crystal display (LCD) screen by command control of V_5 LCD driver voltage. This function sets five-bit data in the electronic volume control register, and the V_5 LCD driver voltage can be one of 32-state voltages.
To use the Electronic Volume Control Function, issue the Set Power Control command to simultaneously operate both the voltage regulator circuit and voltage follower circuit.
Also, when the boosting circuit is off, the voltage must be supplied from V_{OUT} terminal.
When the Electronic Volume Control Function is used, the V_5 voltage can be expressed as follows:

$$V_5 = (1 + \frac{Rb}{Ra})\, V_{REG} + Rb \times \Delta I_{REF} \quad \text{..... ⑤}$$

Variable voltage range

The increased V_5 voltage is controlled by use of I_{REF} current source of the IC. (For 32 voltage levels, $\Delta I_{REF} = I_{REF}/31$)

The minimum setup voltage of the V_5 absolute value is determined by the ratio of external Ra and Rb, and the increased voltage by the Electronic Volume Control Function is determined by resistor Rb. Therefore, the resistors must be set as follows:

1) Determine Rb resistor depending on the V_5 variable voltage range by use of the Electronic Volume Control.

$$Rb = \frac{V_5 \text{ variable voltage range}}{I_{REF}}$$

2) To obtain the minimum voltage of the V_5 absolute value, determine Ra using the Rb of Step 1) above.

$$Ra = \frac{Rb}{\frac{V_5}{V_{REG}} - 1} \qquad \{V_5 = (1 + Rb/Ra) \times V_{REG}\}$$

The S1D15206 series have the built-in V_{REG} reference voltage and I_{REF} current source which are constant during voltage variation. However, they may change due to the variation occurring in IC manufacturing and due to the temperature change as shown below.
Consider such variation and temperature change, and set the Ra and Rb appropriate to the LCD used.

V_{REG} = –2.5V±0.15V } Type1
V_{REG} = –0.2%/˚C
V_{REG} = V_{SS} }Type2
V_{REG} = 0.00%/˚C
V_{REG} = –0.2%/°C
I_{REF} = –3.2µA±40% (For 16 levels)
I_{REF} = 0.023µA/°C
–6.5µA±40% (For 32 levels)
0.052µA/°C

Ra is a variable resistor that is used to correct the V_5 voltage change due to V_{REG} and I_{REF} variation. Also, the contrast adjustment is recommended for each IC chip.
Before adjusting the LCD screen contrast, set the electronic volume control register values to (D4,D3,D2,D1,D0)=(1,0,0,0,0) or (0,1,1,1,1) first.
When not using the Electronic Volume Control Function, set the register values to (D4,D3,D2,D1,D0)=(0,0,0,0,0) by sending the $\overline{RES}$ signal or the Set Electronic Volume Control Register command.

Setup example of constants when Electronic Volume Control Function is used:

V_5 maximum voltage:	V_5 = –6 V (Electronic volume control register values (D4,D3,D2,D1,D0) = (0,0,0,0,0))
V_5 minimum voltages:	V_5 = –10 V (Electronic volume control register values (D4,D3,D2,D1,D0) = (1,1,1,1,1))
V_5 variable voltage range:	4 V
Variable voltage levels:	32 levels

1) Determining the Rb:

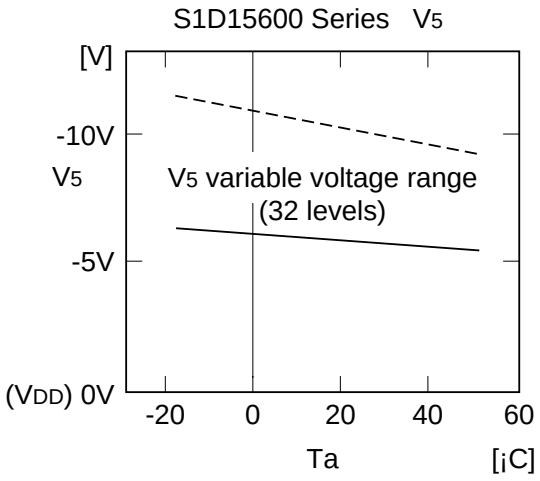
$$R3 = \frac{V_5 \text{ variable voltage range}}{|\, I_{REF} \,|} = \frac{4V}{6.5\mu A}$$

$$\underline{Rb = 625K\Omega}$$

2) Determining the Ra:

$$Ra = \frac{Rb}{\frac{V_5 max}{V_{REG}} - 1} = \frac{625K\Omega}{\frac{-6V}{-2.55V} - 1}$$

$$\underline{Ra = 462K\Omega}$$



According to the V_5 voltage and temperature change, equation ⑤ can be as follows (if V_{DD} = 0 V reference):

Ta=25°C

$V_5max = (1+Rb/Ra) \times V_{REG}$
$= (1+625k/442k) \times (-2.55V)$
$= -6.0V$
$V_5min = V_5 max + Rb \times I_{REF}$
$= -6V + 625k \times (-6.5\mu A)$
$= -10.0V$

Ta=–10°C

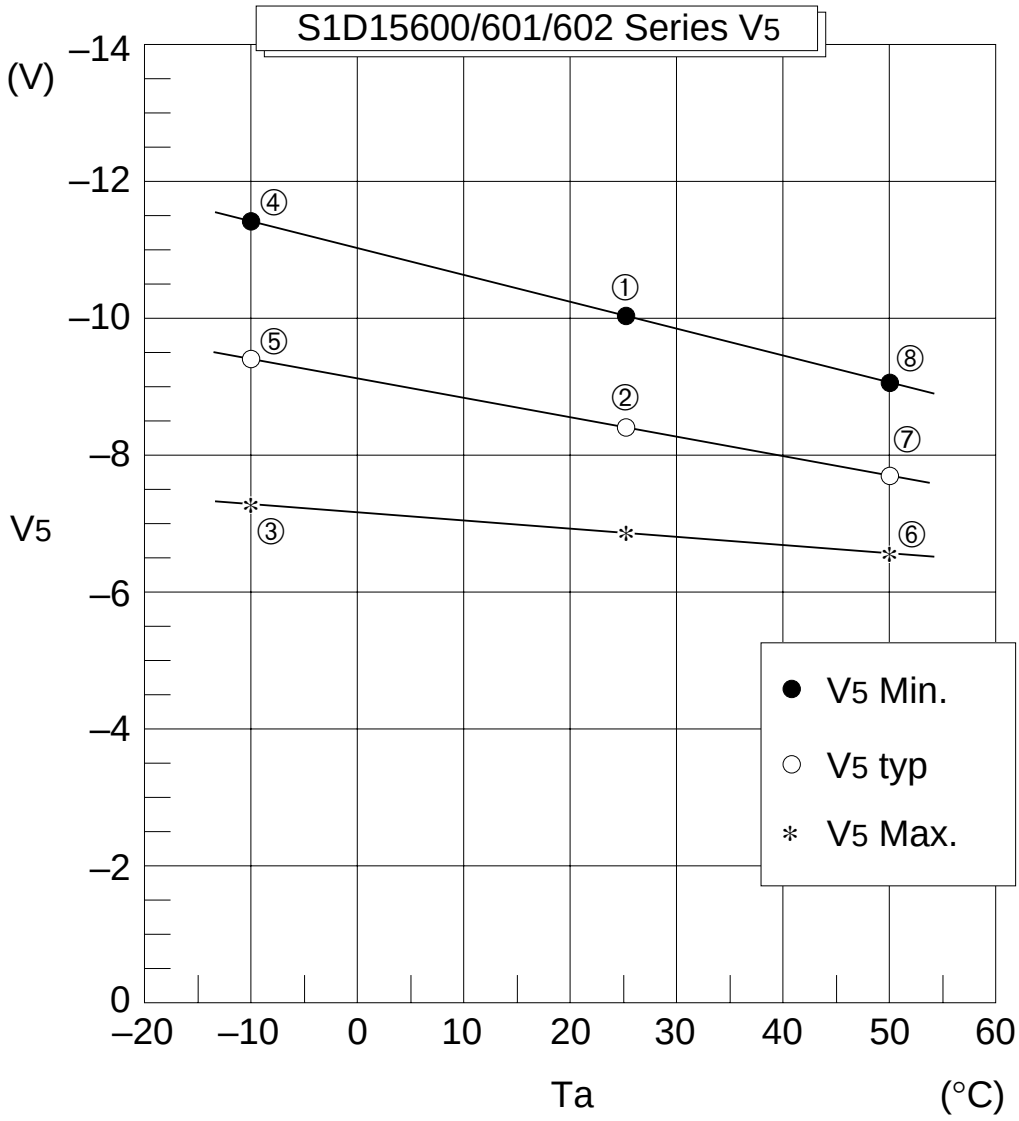
$V_5max = (1+Rb/Ra) \times V_{REG}$ (Ta=–10°C)
$= (1+625k/462k) \times (-2.55V)$
$\times \{1+(-0.2\%/°C) \times (-10°C-25°C)\}$
$= -6.42V$
$V_5min = V_5max + Rb \times I_{REF}$ (Ta=–10°C)
$= -6.42V + 625k$
$\times \{-6.5\mu A+(0.052\mu A/°C) \times$
$(-10°C-25°C)\}$
$= -11.63V$

Ta=–50°C

$V_5max = (1+Rb/Ra) \times V_{REG}$ (Ta=50°C)
$= (1+625k/462k) \times (-2.55V)$
$\times \{1+(-0.2\%/°C) \times (50°C-25°C)\}$
$= -5.7V$
$V_5min = V_5max + Rb \times I_{REF}$ (Ta=50°C)
$= -5.7V + 625k$
$\times \{-6.5\mu A+(0.052\mu A/°C) \times$
$(50°C-25°C)\}$
$= -8.95V$

The margin must also be determined in the same procedure given above by considering the V_{REG} and I_{REF} variation. This margin calculation results show that the V_5 center value is affected by the V_{REG} and I_{REF} variation. The voltage setup width of the Electronic Volume Control depends on the I_{REF} variation. When the typical value of 0.2 V/step is set, for example, the maximum variation range of 0.12 to 0.28 V must be considered.
In case of Type 2, it so becomes that $V_{REG} = V_{SS}$ (V_{DD} basis) and there is no temperature gradient. However, I_{REF} carries the same temperature characteristics as with Type 1.

Example of V_5 Voltage When Using S1D15600/601/602 Series Electronic Volume



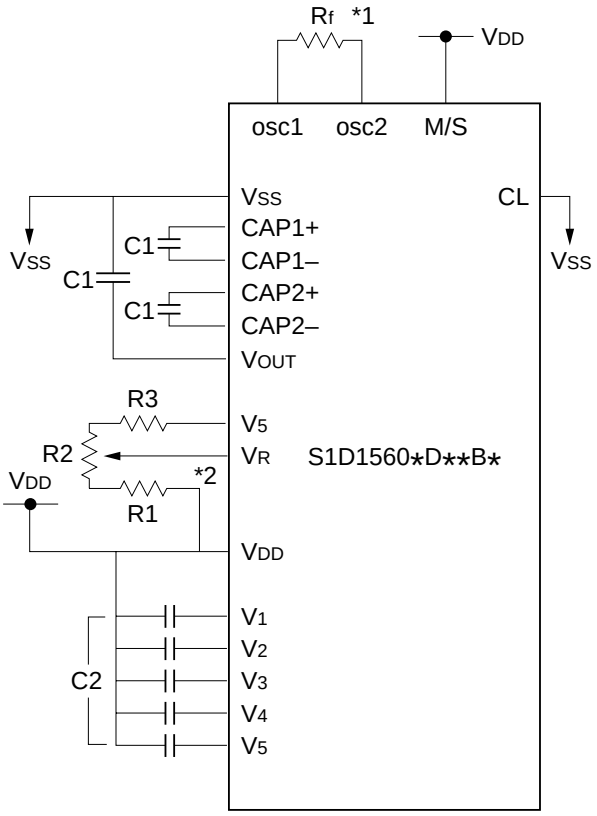
Liquid Crystal Voltage Generating Circuit

A V_5 potential is resistively divided within the IC to cause V_1, V_2, V_3 and V_4 potentials needed for driving of liquid crystals. The V_1, V_2, V_3 and V_4 potentials are further converted in the impedance by the voltage follower before supplied to the liquid crystal driving circuit. The liquid crystal driving voltage is fixed with each type.

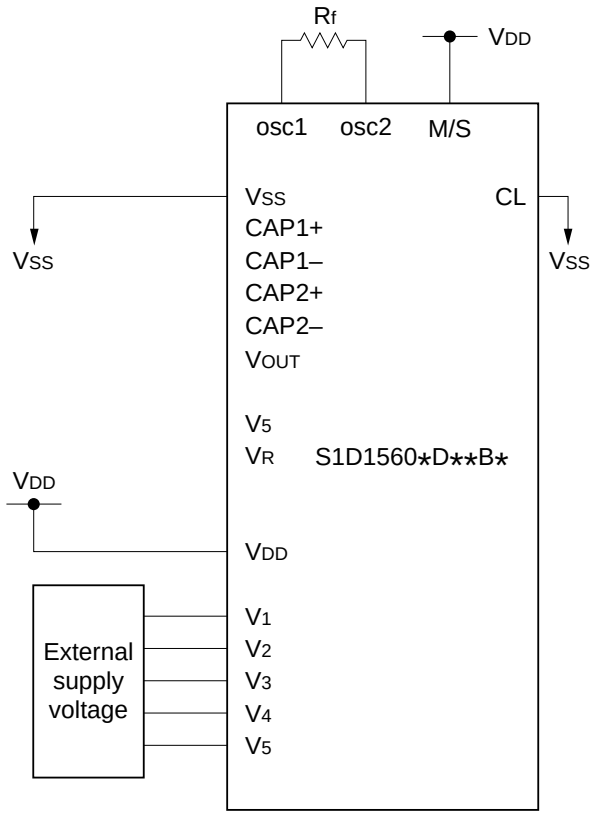
types	Liquid crystal driving voltage
S1D15600D00B∗	1/9 bias voltage
S1D15600D10B∗	1/7 bias voltage
S1D15601D00B∗	1/7 bias voltage
S1D15601D10B∗	1/5 bias voltage
S1D15602D00B∗	1/5 bias voltage

As shown in Fig. 8, it needs to connect, externally voltage stabilizing capacitors C2 to the liquid crystal power terminals. When selecting such capacitor C2 make actual liquid crystal displays matching to the display capacity of the liquid crystal display panel, before determining on the capacitance as the constant value for voltage stabilization.

When the built-in power circuit is used



When the built-in power circuit is not used



Reference set values:

S1D15600 V_5 ≒ –11~ –13 V
S1D15601 V_5 ≒ –7~ –9 V
S1D15602 V_5 ≒ –5~ –7 V (Variable)

	S1D15600	S1D15601	S1D15602
C1	4.7 µF	2.2 to 4.7 µF	2.2 to 4.7 µF
C2	0.1 to 0.47 µF	0.1 to 0.47 µF	0.1 µF
R1	1 MΩ	700 kΩ	500 kΩ
R2	200 kΩ	200 kΩ	200 kΩ
R3	4 MΩ	1.6 MΩ	700 kΩ
LCD SIZE	32×51 mm	16×67 mm	8×75 mm
DOT	64×102	32×134	16×150

*1 Connect oscillator feedback resistor R_f as short as possible and place it close to the IC for preventing a malfunction.

*2 Use short wiring or shielded cables for the VR pin due to high input impedance.

*3 Determine C1, C2 depending on the size of LCD panel driven. You must set these values so that the LCD driving voltage becomes stable. Set (T1, T2)=(HIGH, LOW) and supply an external voltage to V_{OUT}. Display the LCD heavy load pattern and determine C2 so that the LCD driving voltages (V_1 to V_5) become stable. Then, set (T1, T2)=(LOW, LOW) and determine C1. Set the same capacitance for C2.

*4 The "LCD SIZE" indicates the vertical and horizontal length of the LCD panel display area.

* Precautions when installing the COG

When installing the COG, it is necessary to duly consider the fact that there exists a resistance of the ITO wiring occurring between the driver chip and the externally connected parts (such as capacitors and resistors). By the influence of this resistance, non-conformity may occur with the indications on the liquid crystal display.
Therefore, when installing the COG design the module paying sufficient considerations to the following three points.

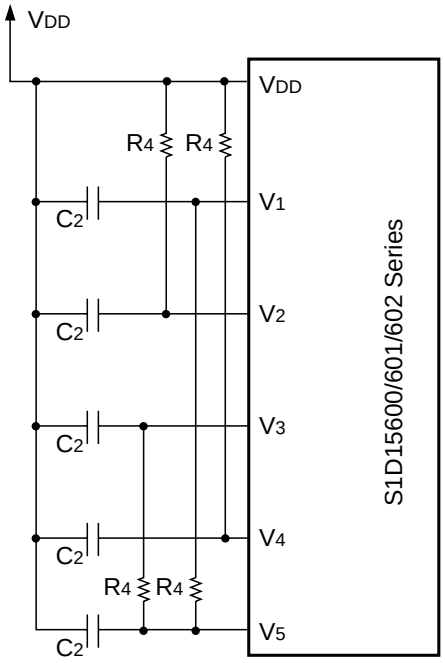
1. Suppress the resistance occurring between the driver chip pin to the externally connected parts as much as possible.
2. Suppress the resistance connecting to the power supply pin of the driver chip.
3. Make various COG module samples with different ITO sheet resistance to select the module with the sheet resistance with sufficient operation margin.

Also, as for this driver IC, pay sufficient attention to the following points when connecting to external parts for the characteristics of the circuit.

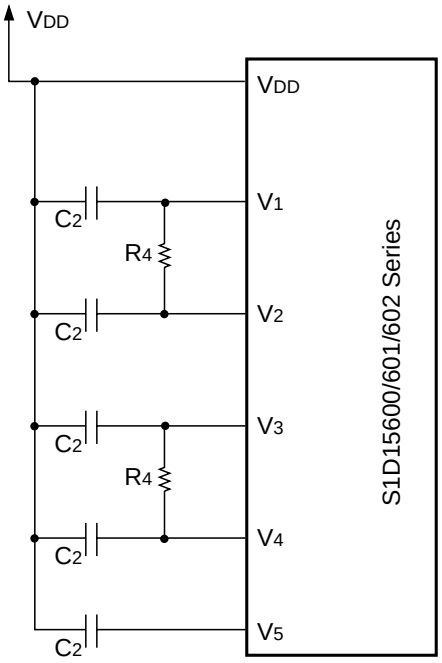
1. Connection to the boosting capacitors The boosting capacitors (the capacitors connecting to respective CAP pins and capacitor being inserted between V_{OUT} and V_{SS2}) of this IC are being switched over by use of the transistor with very low ON-resistance of about 10Ω. However, when installing the COG, the resistance of ITO wiring is being inserted in series with the switching transistor, thus dominating the boosting ability.
   Consequently, the boosting ability will be hindered as a result and pay sufficient attention to the wiring to respective boosting capacitors.
2. Connection of the smoothing capacitors for the liquid crystal drive
   The smoothing capacitors for the liquid crystal driving potentials (V_1. V_2, V_3 and V_4) are indispensable for liquid crystal drives not only for the purpose of mere stabilization of the voltage levels. If the ITO wiring resistance which occurs pursuant to installation of the COG is supplemented to these smoothing capacitors, the liquid crystal driving potentials become unstable to cause non-conformity with the indications of the liquid crystal display. Therefore, when using the COG module, we definitely recommend to connect reinforcing resistors externally.
   Reference value of the resistance is 100kΩ to 1MΩ. Meanwhile, because of the existence of these reinforcing resistors, current consumption will increase.

Indicated below is an exemplary connection diagram of external resistors.
Please make sufficient evaluation work for the display statuses with any connection tests.

Exemplary connection diagram 1.



Exemplary connection diagram 2.



Reset

When power is turned ON, the S1D15600/601/602 series is initialized on the rising edge of RES. Initial settings are as follows.

1. Display : OFF
2. Display mode : Normal
3. *n*-line inversion : OFF
4. Duty cycle : 1/64 (S1D15600)
   1/32 (S1D15601)
5. ADC select : Normal (D0 = L)
6. Read/write modify : OFF
7. Internal power supply : OFF
8. Serial interface register data : Cleared
9. Display initial line register : Line 1
10. Column address counter : 0
11. Page address register : Page 0
12. Output selection circuit : Case 6
13. *n*-line inversion register : 16
14. Set the electronic control register to zero (0).

$\overline{RES}$ should be connected to the microprocessor reset terminal so that both devices are reset at the same time. $\overline{RES}$ must be LOW for at least 1 µs to correctly reset the S1D15600/601/602 series. Normal operation starts 1 µs after the rising edge on $\overline{RES}$.

If the built-in LCD power circuit of the S1D1560∗D∗∗B∗ is not used, the $\overline{RES}$ signal must be low when the external LCD power supply is turned on. When the $\overline{RES}$ goes low, each register is cleared to the above listed initial status. However, the oscillation circuit and output pins (OSC2, FR, SYNC, CLD, DYO, D0 to D7 pins) are not affected. If the S1D15600 is not properly initialized when power is turned ON, it can lock itself into a state that cannot be cancelled.

Although S1D15600/601/602 Series devices maintain the operation status under commands, when external noise of excessive levels enters, their internal statys may be changed. Consequently, it is necessary to provide means to suppress noise occurring from package or the system or orovide means to avoid influence of such noise.

Also, to cope with sudden noise, we suggest you to set up the software so the operation status can be periodically refreshed.

When the Reset command is used, only initial settings 9 to 14 are active.

8. COMMANDS

The Command Set

A0, $\overline{RD}$(E) and $\overline{WR}$(R/$\overline{W}$) identify the data bus commands. Interpretation and execution of commands are synchronized to the internal clock. Since a busy check is normally not needed, commands can be processed at high speed.

For the 80-series MPU interface, the command is activated when a low pulse is entered in the $\overline{RD}$ pin during read or when a low pulse is entered in the $\overline{WR}$ pin during write. While the 68-series MPU interface is set to the read status when a high pulse is entered in the R/$\overline{W}$ pin, and it is set to the write status when a low pulse is entered in this pin. The command is activated when a high pulse is entered in the E pin. (For their timings, see Section 10 "Timing Characteristics.") Therefore, the 68-series MPU interface differs from the 80-series MPU interface in the point where the $\overline{RD}$ (or E) signal is 1 (or high) during status read and during display data read explained in the command description and on the command table. The following command description uses an 80-series MPU interface example.

If the serial interface is selected, data is sequentially entered from D7.

Table 7. S1D15600/601/602 series command table

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1)Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	Turns the LCD display ON and OFF 0 : OFF 1 : ON
(2)Display START Line set	0	1	0	0	1	Dispaly start address						Determines the RAM display line for COM 0
(3)Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM pages in the Page Address register.
(4)Column address set; high-order 4 bits	0	1	0	0	0	0	1	High-order column address				Sets the high order 4 bits of the display RAM column address in the register.
(4)Column address set; low-order 4 bits	0	1	0	0	0	0	0	Low-order column address				Sets the low-order 4 bits of the display RA column address in the register.
(5)Status read	0	0	1	Status				0	0	0	0	Reads the status information.
(6)Display data write	1	1	0	Write Data								Writes data in the display RAM.
(7)Display data read	1	0	1	Read Data								Reads data from the display RAM.
(8)ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Outputs the display RAM address for SEG. 0: Normal 1: Reversed
(9)Normal/reverse display	0	1	0	1	0	1	0	0	1	1	0 1	Displays the LCD image in normal or reverse mode. 0: Normal 1: Reversed
(10)Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Lights all segments. 0: Normal display 1: All ON
(11)Duty select	0	1	0	1	0	1	0	1	0	0	0 1	Sets LCD drive duty (1). 0:1/24, 48 1:1/32, 64
(12)Duty +1	0	1	0	1	0	1	0	1	0	1	0 1	Sets LCD drive duty (2). 0: Normal 1: Duty+1
(13)n-line reverse register set	0	1	0	0	0	1	1	No. of reversed n-lines				Sets the line reverse driving and No. of reverse lines in the line reverse register.
(14)n-line reverse register release	0	1	0	0	0	1	0	0	0	0	0	Releases the line reverse driving.

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(15)Read Modify write	0	1	0	1	1	1	0	0	0	0	0	Increments by 1 during write of column address counter, and set to 0 during read.
(16)End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read Modify write mode.
(17)Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(18)Output status register set	0	1	0	1	1	0	0	Output status				Sets the COM and SEG status in registers.
(19)LCD Power supply ON/OFF	0	1	0	0	0	1	0	0	1	0	0 1	0: Power OFF 1: Power ON
(20)Built-in power supply ON/OFF	0	1	0	1	1	1	0	1	1	0	1	Completes the turn-on sequence of built-in power supply.
(21)Electronic volume control register set	0	1	0	1	0	0	Electronic control value					Sets the V_5 output voltage in the electronic control register.
(22)Power save												A complex command to turn off the display and light all indictors.

(1) Display ON/OFF

Alternatively turns the display ON and OFF.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

Note
D = 0 Display OFF
D = 1 Display ON

(2) Display Start Line Set

Loads the RAM line address of the initial display line, COM0, into the initial display line register. The RAM display data becomes the top line of the LCD screen. It is followed by the higher number lines in ascending order, corresponding to the duty cycle. The screen can be scrolled using this command by incrementing the line address.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
↓						↓
1	1	1	1	1	0	62
1	1	1	1	1	1	63

(3) Page Address Set

Loads the RAM page address from the microprocessor into the page address register. A page address, along with a column address, defines a RAM location for writing or reading display data. When the page address is changed, the display status is not affected.
Page address 8 is a special use RAM area for the indicator. Only D0 is available for data exchange.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Page
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

(4) Column Address Set

Loads the RAM column address from the microprocessor into the column address register. The column address is divided into two parts-4 high-order bits and 4 low-order bits.
When the microprocessor reads or writes display data to or from RAM, column addresses are automatically incremented, starting with the address stored in the column address register and ending with address 166. The page address is not incremented automatically.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	1	A7	A6	A5	A4

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
↓								↓
1	0	1	0	0	1	0	1	165

(5) Status read

Indicates to the microprocessor the four S1D15600 status conditions.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	Busy	ADC	ON/ OFF	RES- ET	0	0	0	0

BUSY Indicates whether or not the S1D15600 will accept a command. If BUSY is 1, the device is currently executing a command or is resetting, and no new commands can be accepted. If BUSY is 0, a new command can be accepted. It is not necessary for the microprocessor to check the status of this bit if enough time is allowed for the last cycle to be completed.

ADC Indicates the relationship between RAM column addresses and the segment drivers. If ADC is 1, the relationship is normal and column address *n* corresponds to segment driver *n*. If ADC is 0, the relationship is inverted and column address (165 – *n*) corresponds to segment driver *n*.

ON/OFF Indicates whether the display is ON or OFF. If ON/OFF is 1, the display is OFF. If ON/OFF is 0, the display is ON. Note that this is the opposite of the Display ON/OFF command.

RESET Indicates when initialization is in process as the result of RES or the Reset command.

(6) Display Data Write

Writes bytes of display data from the microprocessor to the RAM location specified by the column address and page address registers. The column address is incremented automatically so that the microprocessor can continuously write data to the addressed page.

A_0	E ($\overline{RD}$)	R/$\overline{W}$ ($\overline{WR}$)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	Write data							

(7) Display Data Read

Sends bytes of display data to the microprocessor from the RAM location specified by the column address and page address registers. The column address is incremented automatically so that the microprocessor can continously read data from the addressed page. A dummy read is required after loading an address into the column address register.

Display data cannot be read through the serial interface.

A_0	E ($\overline{RD}$)	R/$\overline{W}$ ($\overline{WR}$)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	Read data							

(8) ADC Select

Selects the relationship between the RAM column addresses and the segment drivers. When reading or writing display data, the column address is incremented as shown in figure 4.

A_0	E ($\overline{RD}$)	R/$\overline{W}$ ($\overline{WR}$)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	0	0	0	D

Note

D = 0 Rotate right (normal direction)

D = 1 Rotate left (reverse direction)

The output pin relationship can also be changed by the microprocessor. There are very few restrictions on pin assignments when constructing an LCD module.

(9) Normal/Reverse Display

Determines whether the data in RAM is displayed normally or inverted.

A_0	E ($\overline{RD}$)	R/$\overline{W}$ ($\overline{WR}$)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	0	1	1	D

Note

D = 0 LCD segment is ON when RAM data is 1 (normal).

D = 1 LCD segment is ON when RAM data is 0 (inverse).

(10) Display All Points ON/OFF

Turns all LCD points ON independently of the display data in RAM. The RAM contents are not changed. This command has priority over the normal/inverse display command.

A_0	E ($\overline{RD}$)	R/$\overline{W}$ ($\overline{WR}$)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	0	1	0	D

Note

D = 0 Normal display status

D = 1 All display segments ON

If this command is received when the display status is OFF, the Power Save command is executed.

(11) Duty Select

Selects the LCD driver duty.
Since this is independent from contents of the output status register, the duty must be selected according to the LCD output status.
In multi-chip configuration, the master and slave devices must have the same duty.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	D

Model	D	Duty
S1D15600	0 1	1/48 1/64
S1D15601	0 1	1/24 1/32
S1D15602	0 1	1/16 1/16

(12) Duty + 1

Increases the duty by 1. If 1/48 or 1/64 duty is selected in the S1D15600 for example, 1/49 or 1/65 is set, respectively and COM1 functions as either the COM48 or COM64 output. The display line always accesses the RAM area corresponding to page address 8, D0. (Refer to Figure 4.)
In multi-chip configuration, the Duty + 1 command must be executed to both the master and slave sides.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	1	D

Model	D	Duty
S1D15600	0 1	1/48 or 1/64 1/49 or 1/65
S1D15601	0 1	1/24 or 1/32 1/25 or 1/33
S1D15602	0 1	1/16 1/17

(13) *n*-line Reverse Register Set

Selects the number of inverse lines for the LCD AC controller. The value of *n* is set between 2 to 16 and is stored in the *n*-line inversion register.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Number of inverted lines
0	0	0	0	–
0	0	0	1	2
0	0	1	0	3
↓				↓
1	1	1	0	15
1	1	1	1	16

Do not use this command when using the votage follower of the built-in power supply, the characteristics of the built-in power supply cannot then be guaranteed to stay within the specification.

(14) *n*-line Reverse Register Release

Cancels *n*-line inversion and restores the normal 2-frame AC control. The contents of the *n*-line inversion register are not changed.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	0	0	0

(15) Read Modify Write

Following this command, the column address is no longer incremented automatically by a Read Display Data command. The column address is still incremented by the Write Display Data command. This mode is cancelled by the End command. The column address is then returned to its value prior to the Modify Read command. This command makes it easy to manage the duplication of data from a particular display area for features such as cursor blinking.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Note that the Column Address Set command cannot be used in modify-read mode.

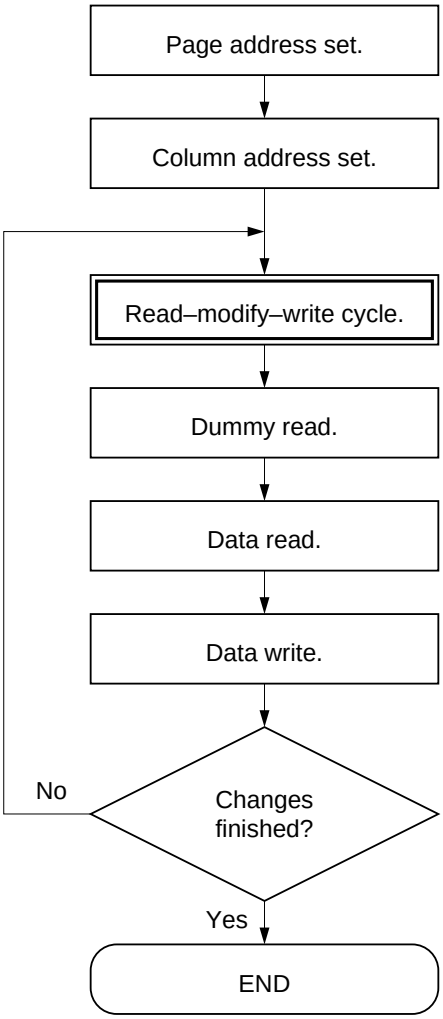


Figure 13. Command sequence for cursor blinking

(16) End

Cancels the modify read mode. The column address prior to the Modify Read command is restored.

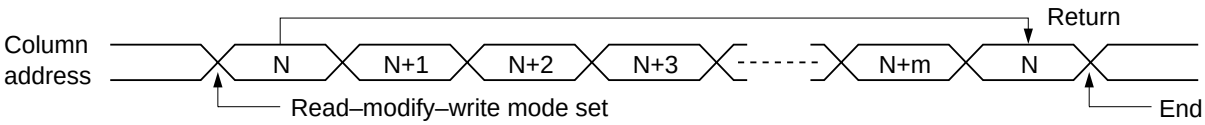
A0	E/RD	R/W/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

(17) Reset

Resets the initial display line, column address, page address, and *n*-line inversion registers to their initial values. This command does not affect the display data in RAM.

A0	E/RD	R/W/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The reset command does not initialize the LCD power supply. Only RES can be used to initialize the supplies.



(18) Output Status Register Set

Available only in the S1D15600 and S1D15601.
This command selects the role of the COM/SEG dual pins and determines the LCD driver output status.
The COM output scanning direction can be selected by setting A3 to HIGH or LOW. For details, refer to the Output Status Circuit in each function description.

A0	E/RD	R/W/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	A3	A2	A1	A0

A3: Selection of the COM output scanning direction

A_2 A_1 A_0	Output Status	Number of COM/SEG Output pins	Remarks
0 0 0	Case 6	SEG 166	Applies to the SED1560/61
0 0 1	Case 5	SEG 134, COM 32	Applies to the SED1561
0 1 0	Case 4	SEG 134, COM 32	
0 1 1	Case 3	SEG 134, COM 32	
1 0 0	Case 2	SEG 102, COM 64	Applies to the SED1560
1 0 1	Case 1	SEG 102, COM 64	
1 1 0	Case 6	SEG 166	Applies to the SED1560/61
1 1 1	Case 6	SEG 166	

(19) LCD Power Supply ON/OFF

Turns the S1D1560∗D∗∗B∗ internal LCD power supply ON or OFF. When the power supply is ON, the voltage converter, the voltage regulator circuit and the voltage followers are operating. For the converter to function, the oscillator must also be operating.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	1	0	D

Note
D = 0 Supply OFF
D = 1 Supply ON

When an external power supply is used with the S1D15600D∗∗B∗, the internal supply must be OFF. If the S1D15600D∗∗B∗ is used in a multiple-chip configu-ration, an external power supply that meets the specifications of the LCD panel must be used. An S1D15600 operating as a slave must have its internal power supply turned OFF.

(20) Built-in Power Supply ON/OFF

This command turns on the built-in power supply.

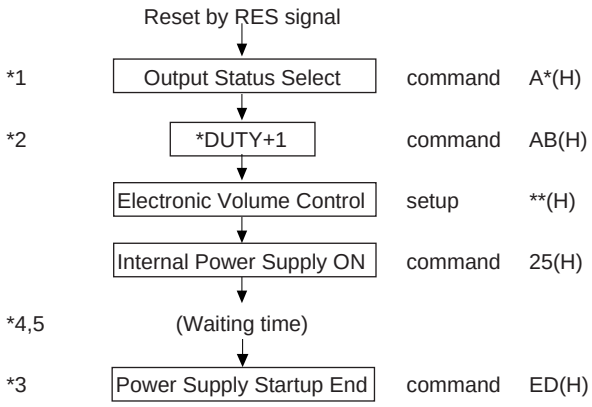
A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	0	1

The S1D15600 series has the built-in, low-power LCD driving voltage generator circuit which can cut almost all currents except those required for LCD display. This is the primary advantage of the S1D15600 series product. However, it has the LOW power and you need perform the following power-on sequence when turning on the built-in power supply:

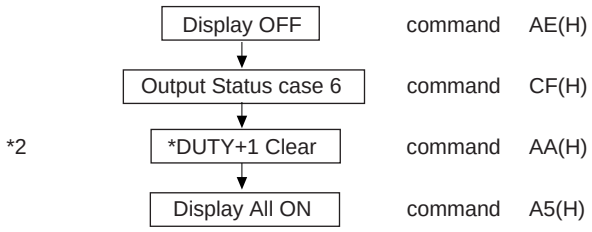
Sequence in the Built-in Power supply ON/OFF Status

To turn on built-in power supply, execute the above built-in power supply ON sequence. To turn off internal power supply execute the power save sequence as shown in the following power supply OFF status. Accordingly, to turn on built-in power supply again after turn it off (power save), execute the “Power Save Clear Sequence” that will be described afterwards.

Built-in power supply ON status



Built-in power supply OFF status

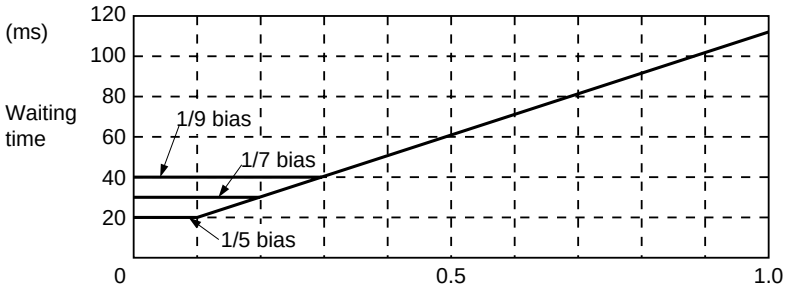


*1: Regarding the S1D15602, it is not necessary to execute a command to decide an output status.

*2: When the COMI pin is not used, it is not necessary to enter the DUTY+1 and DUTY+1 Clear commands.

*3: When the built-in power supply startup end command is not executed, current is consumed stationarily.
Built-in power supply startup end command must always be used in a pair with built-in power supply ON command.

*4: The waiting time depends on the externally-installed capacitance C2 (refer to 7-37). After the waiting time shown in Graph 1, the power supply can be started surely.



Graph 1

V5 voltage conditions
1/9 bias V5 = –6.0 to –16.0 V
1/7 bias V5 = –5.0 to –12.0 V
1/5 bias V5 = –4.5 to –8.0 V

*5: Within the waiting time in built-in power supply ON status, any command other than built-in power supply control commands such as Power Save, and display ON/OFF command, display normal rotation/reverse command, display all ON command, output status select command and DUTY+1 clear command can accept another command without any problem. RAM read and write operations can be freely performed.

(21) Electronic Volume Control Register Set

Through these commands, the liquid crystal driving voltage V5 being outputted from the voltage regulation circuit of the built-in liquid crystal power supply, in order to adjust the contrast of the liquid crystal display.
By setting data to the 4 bit register, one of the 16 voltage status may be selected for the liquid crystal driving voltage V5. External resistors are used for setting the voltage regulation range of the V5. For details refer to the paragraph of the voltage regulation circuit in the Clause for the explanation of functions.

A0	$\overline{E}$ / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	A4	A3	A2	A1	A0

A4	A3	A2	A1	A0	| V5 |
0	0	0	0	0	Small (as the absolute value)
		:			
		:			
1	1	1	1	1	Large (as the absolute value)

When not using the electronic volume control function, set to (0, 0, 0, 0, 0).

(22) Power Save (Complex Command)

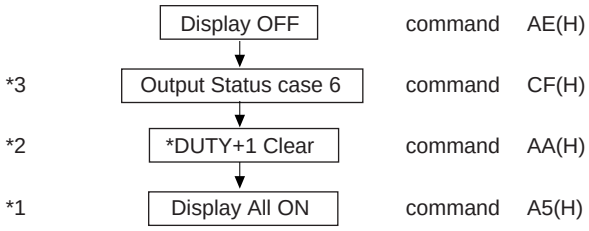
If the Display All Points ON command is specified in the display OFF state, the system enters the power save status, reducing the power consumption to approximate the static power consumption value. The internal state in the power save status is as follows:
(a) The oscillator and power supply circuits are stopped.
(b) The LCD driver is stopped and segment and common driver outputs output the VDD level.
(c) An input of an external clock is inhibited and OSC2 enters the high-impedance state.
(d) The display data and operation mode before execution of the power save command are held.
(e) All LCD driver voltages are fixed to the VDD level.

The power save mode is cancelled by entering either the Display ON command or the Display All Points OFF command (display operation state). When external voltage driver resistors are used to supply the LCD driver voltage level, the current through them must be cut off by the power save signal.
If an external power supply is used, it must be turned OFF using the power save signal in the same manner and voltage levels must be fixed to the floating or VDD level.

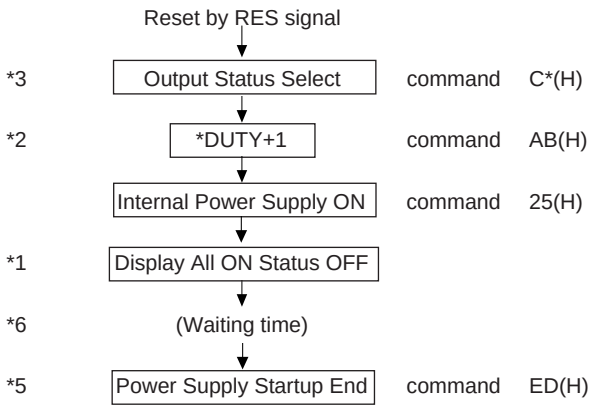
Sequence in the Power Save Status

Power Save and Power Save Clear must be executed according to the following sequence.
To give a liquid crystal driving voltage level by the externally-installed resistance dividing circuit, the current flowing in this resistance must be cut before or concurrently with putting the S1D15600/601/602 series into the power save status so that it may be fixed to the floating or VDD level.
When using an external power supply, likewise, its function must be stopped before or concurrently with putting the S1D15600/601/602 series ino the power save status so that it may be fixed to the floating or VDD level.
In a configurationinwhich an exclusive common driver such as S1D16700 is combined with the S1D15600/601/602 series, it is necessary to stop the external power supply function after putting all the common output into non-selection level.

Power save sequence



Power save clear sequence



*1: In the power save sequence, the power save status is provided after the display all ON command. In the power save clear sequence, the power save status is cleared after the display all ON status OFF command.

*2 When the COMI pin is not used, it is not necessary to eneter the DUTY+1 command and DUTY+1 clear command.

*3 In the S1D15602, it is not necessary to execute a command to decide an output status.

*4 The display ON command can be executed anywhere if it is later than the display all ON status OFF command.

*5 When internal power supply startup end command is not executed, current is consumed stationarily. Internal power supply startup end command must always be used in a pair with internal power supply ON command.

*6 The waiting time depends on the Externally-installed capacitance C2 (refer to 7-46). After the waiting time shown in the above Graph 1, the power supply can be started surely.

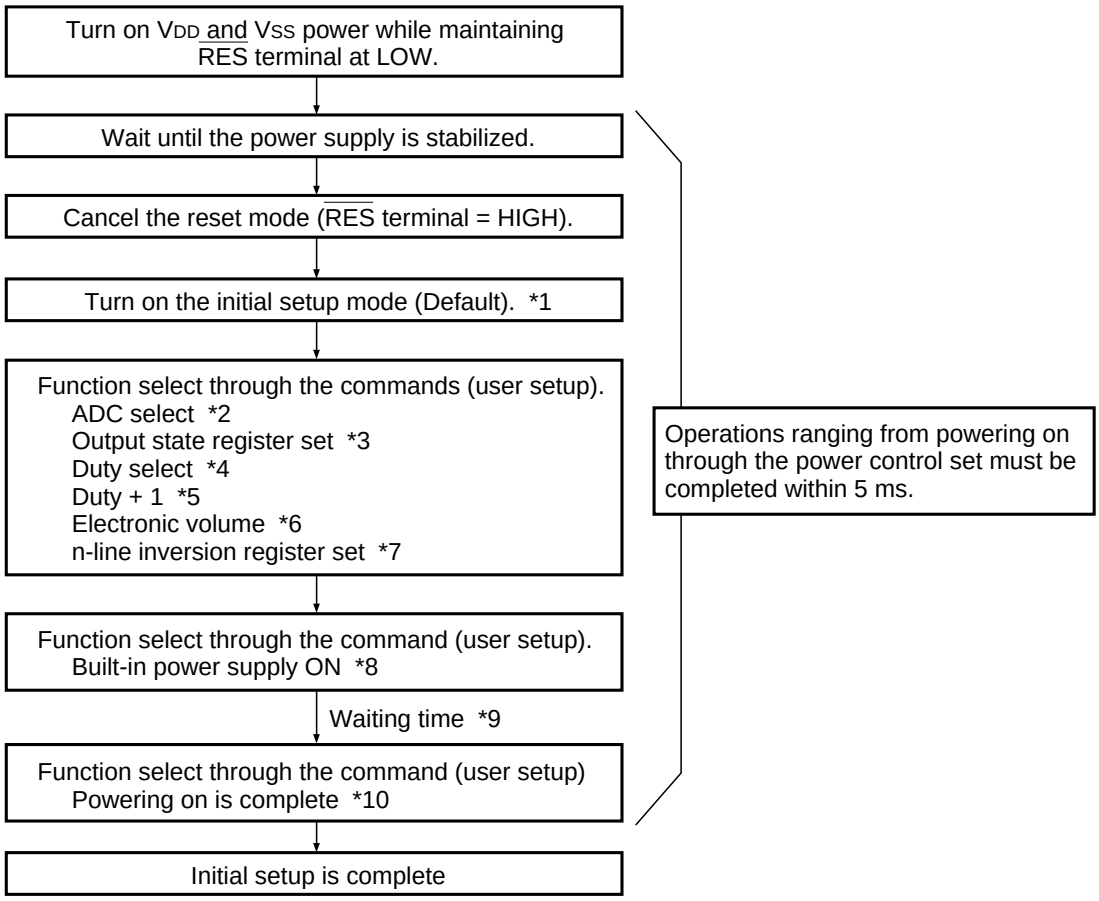
9. COMMAND DESCRIPTION – INSTRUCTION SETUP EXAMPLES

Instruction Setup Examples

Initial setup

Note: As power is turned on, this IC outputs non-LCD-drive potentials V_2 – V_3 from SEG terminal (generates output for driving the LCD) and V_1 –V_4 from COM terminal (also used for generating the LCD drive output). If charge remains on the smoothing capacitor being inserted between the above LCD driving terminals, the display screen can be blacked out momentarily. In order to avoid this trouble, it is recommended to employ the following powering on procedure.

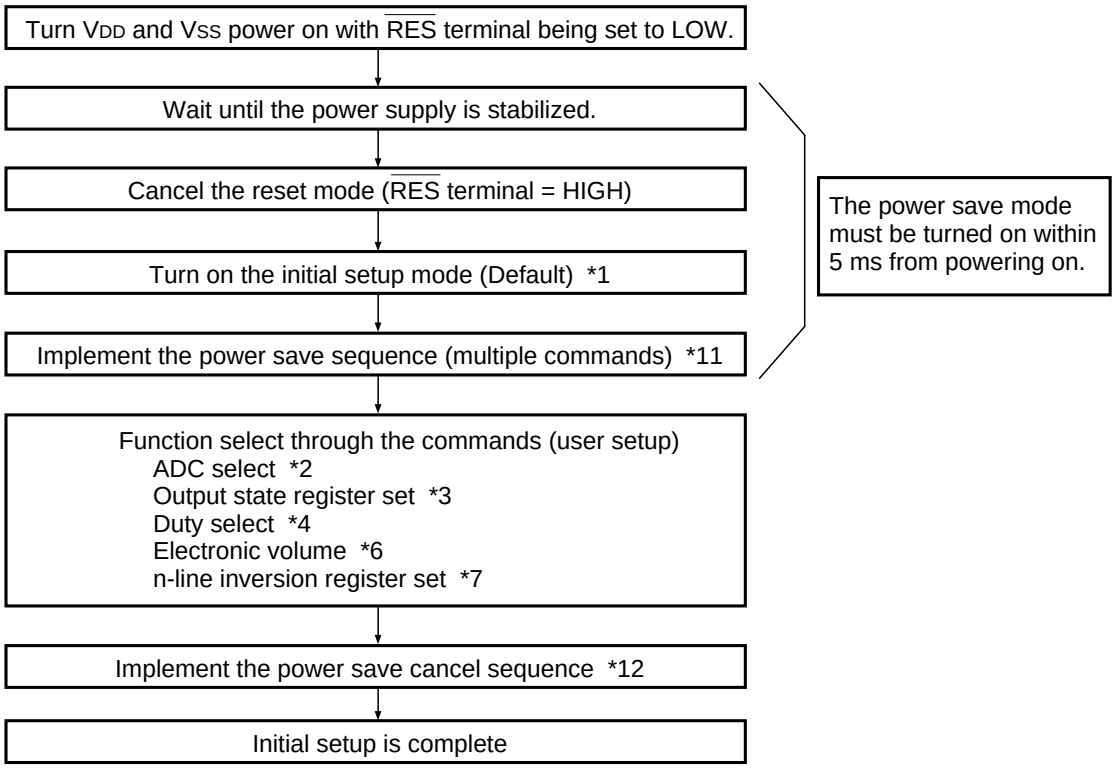
- **When the built-in power is used immediately after the main power is turned on:**



* This duration of 5 ms depends on the panel characteristics as well as capacity of the capacitor concerned. Check them on the actual system.

Notes: *1: Refer to the “Reset Circuit” in the Function Description.
*2: Refer to the “ADC Select” in the Command Selection (8).
*3: Refer to the “Output State Register Set” in the Command Description (18).
*4: Refer to the “Duty Select” in the Command Description (11).
*5: Refer to the “Duty + 1” in the Command Description.
*6: Refer to the “Supply Circuit” in the Function Description and the “Electronic Volume Register Set” in the Command Description (21).
*7: Refer to the “n-line Inversion Register Set” in the Command Description (13).
*8: Refer to the “Built-in Power Supply ON/OFF” in the Command Description (21).
*9: Refer to the “Built-in Power Supply ON/OFF Sequence” in the Command Description.
*10: Refer to the “Built-in Power Supply ON Complete” in the Command Description (20).

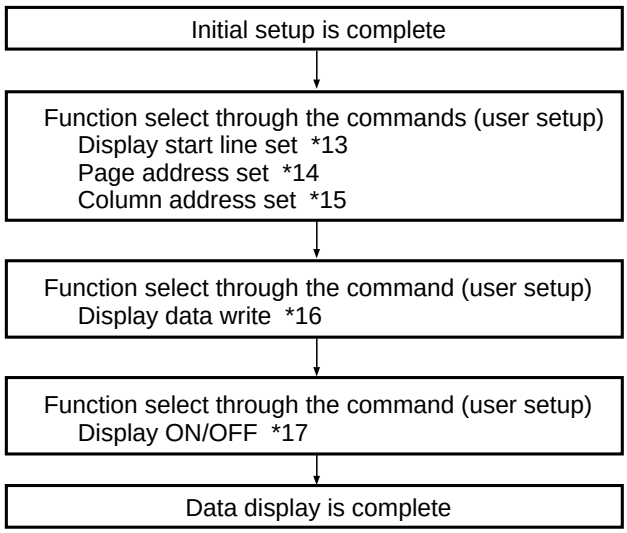
- **When the built-in power supply is not used immediately after the main power is turned on:**



* This duration of 5 ms depends on the panel characteristics as well as capacity of the capacitor concerned. Check them on the actual system.

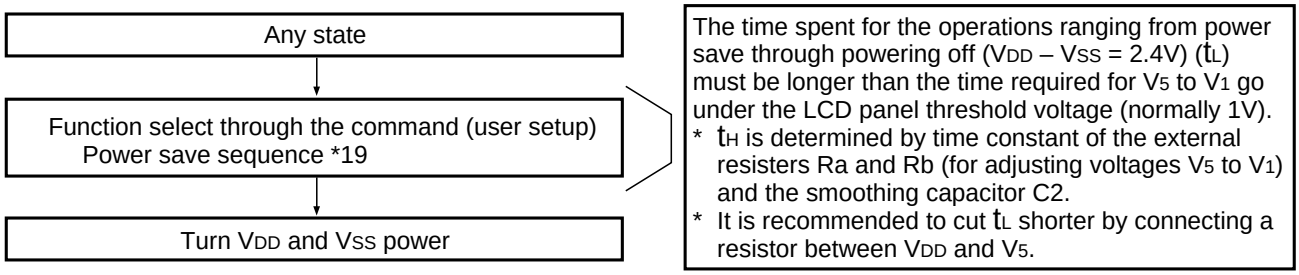
Notes: *1: Refer to the “Reset Circuit” in the Function Description.
*2: Refer to the “ADC Select” in the Command Description (8).
*3: Refer to the “Output State Register Set” in the Command Description (18)
*4: Refer to the “Duty Select” in the Command Description (11).
*6: Refer to the “Supply Circuit” in the Function Description and the “Electronic Volume Register Set” in the Command Description (21).
*7: Refer to the “n-line Inversion Register Set” in the Command Description (13).
*8: Refer to the “Built-in Power Supply ON/OFF” in the Command Description (19).
*11,12: You can select either the sleep mode or standby mode for the power save mode. Refer to the “Power Save (Multiple Commands)” in the Command Description (22).

- **Data Display**



Notes: *13: Refer to the "Display Line Set" in the Command Description (2).
*14: Refer to the "Page Address Set" in the Command Description (3).
*15: Refer to the "Column Address Set" in the Command Description (4).
*16: Refer to the "Display Data Write" in the Command Description (6).
*17: Refer to the "Display ON/OFF" in the Command Description (1).
It is recommended to avoid the all-white-display of the display start data.

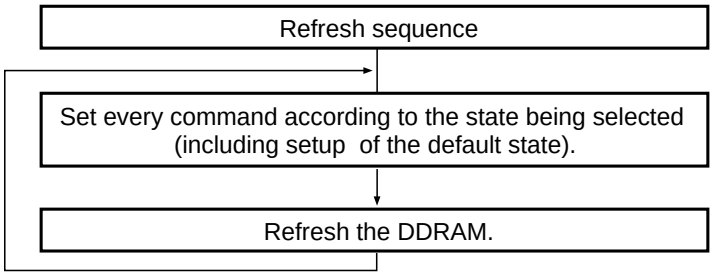
- **Powering Off** *18



Notes: *18: This IC functions as the logic circuit of the power supplies VDD – VSS, and used for controlling the driver of LCD power supplies VDD – V5. Thus, if power supplies VDD – VSS are turned off while voltage is still present on LCD power supplies VDD – V5, drivers (COM and SEG) may output uncontrolled voltage. Therefore, you are required to observe the following powering off procedure: Turn the built-in power supply off, then turn off the IC power supplies (VDD – VSS) only after making sure that potential of V5 – V1 is below the LCD panel threshold voltage level. Refer to the "Supply Circuit" in the Function Description.
*19: When the power save command is entered, you must not implement reset from RES terminal until VDD – VSS power are turned off. Refer to the "Power Save" in the Command Description.

- **Refresh**

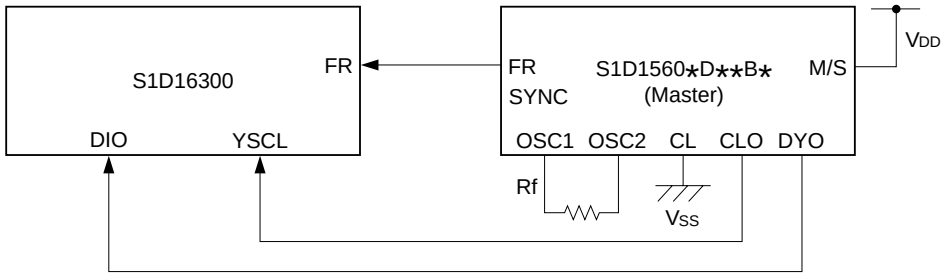
It is recommended that the operating modes and display contens be refreshed periodically,to prevent the effect of unexpected noise. This sequence, however, must not be turned on as long as the initial setup, data display or powering off sequence is taking place.



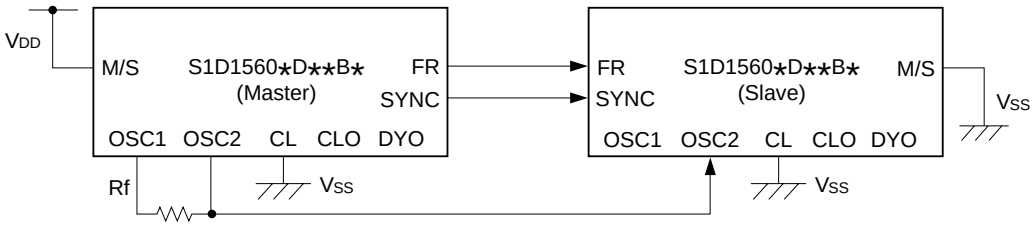
Connection between LCD drivers

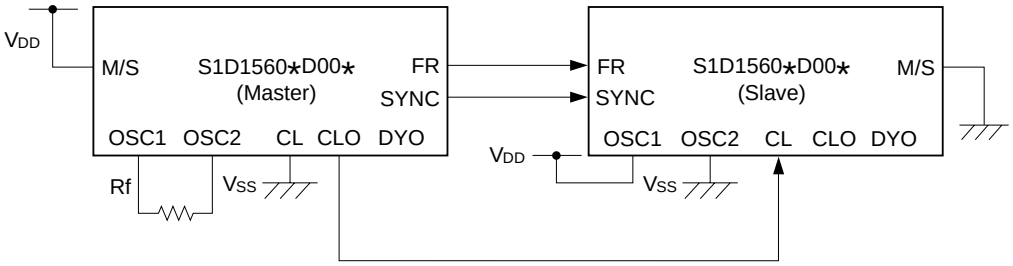
The LCD display area can be increased by using the S1D15600/601/602 series in a multiple-chip configuration or with the S1D15600/601/602 series special common driver (S1D16300).
Application with external Driver

S1D1560∗D∗∗B∗–S1D16300

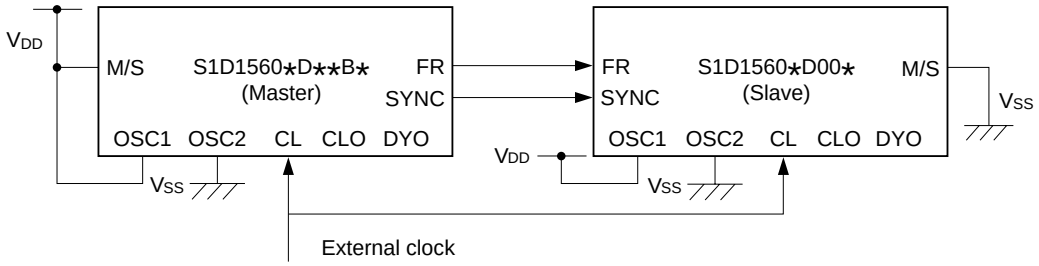


S1D1560∗D∗∗B∗–S1D1560∗D∗∗B∗
(when oscillator circuit is used)





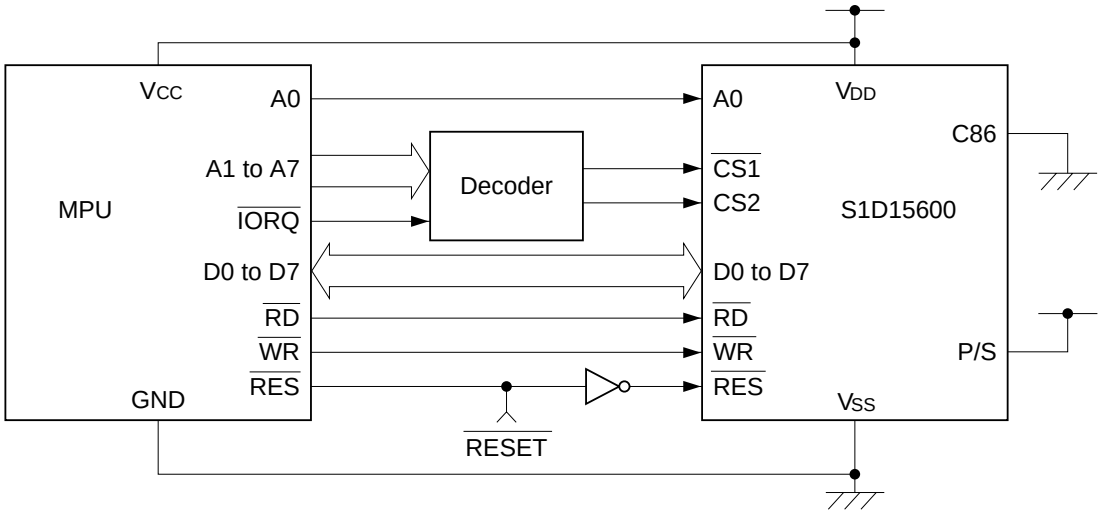
S1D1560∗D∗∗B∗–S1D1560∗D∗∗B∗ (External clock)



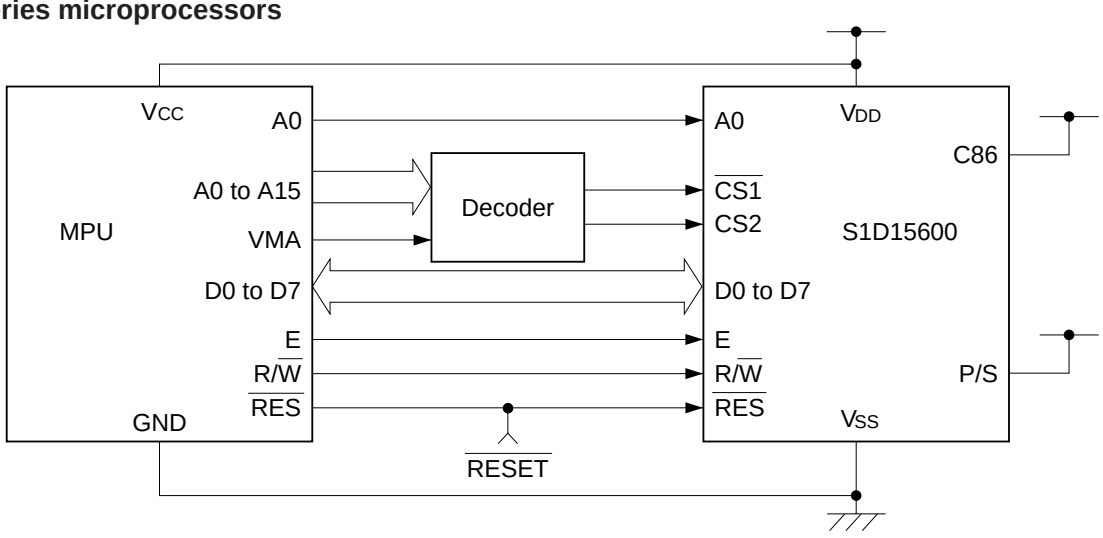
Microprocessor Interface

The S1D15600/601/602 series interfaces to either 8080- or 6800-series microprocessors. The number of connections to the microprocessor can be minimized by using a serial interface. When used in a multiple-chip configuration, the S1D15600 is controlled by the chip select signals from the microprocessor.

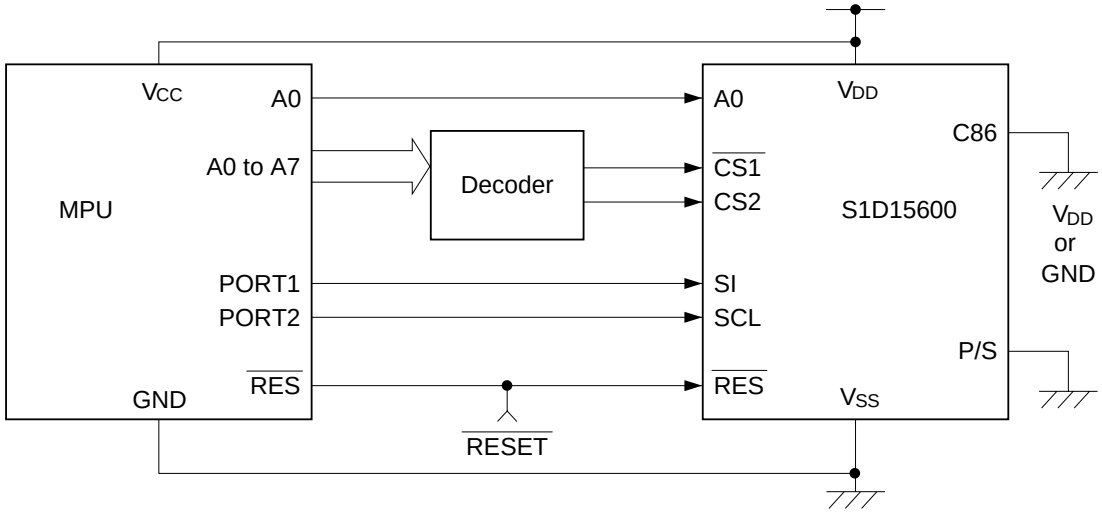
8080-series microprocessors



6800-series microprocessors

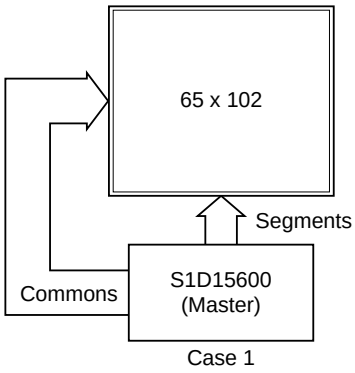


Serial interface

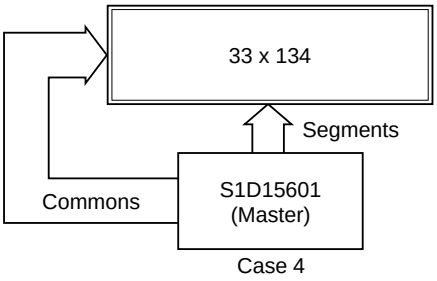


LCD Panel Interface Examples

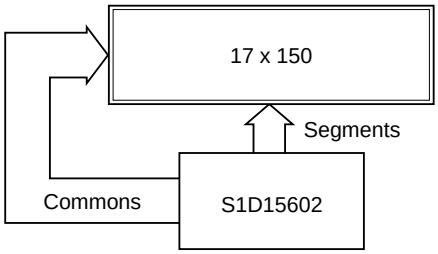
Single-chip configurations



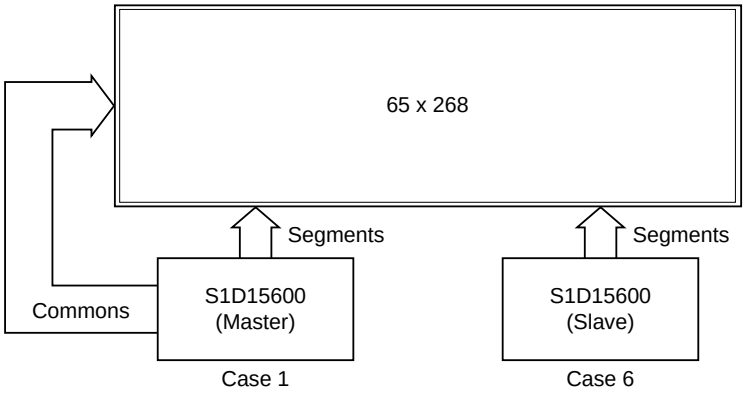
Case 1



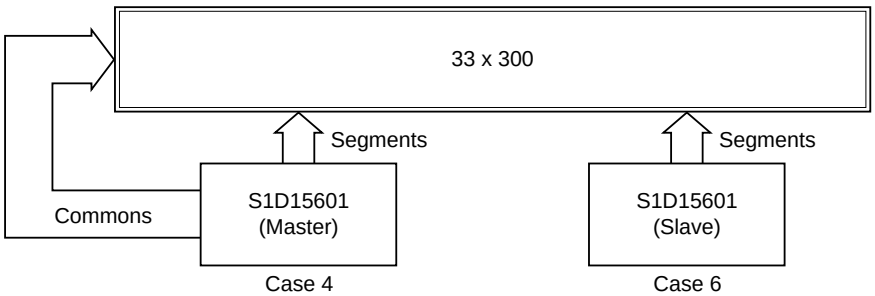
Case 4



Multiple-chip configurations

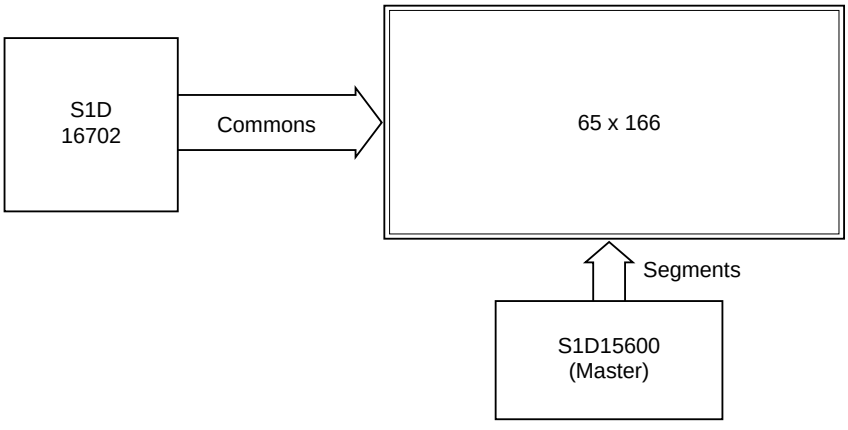


Case 1 Case 6



Case 4 Case 6

Special Common Driver Configurations

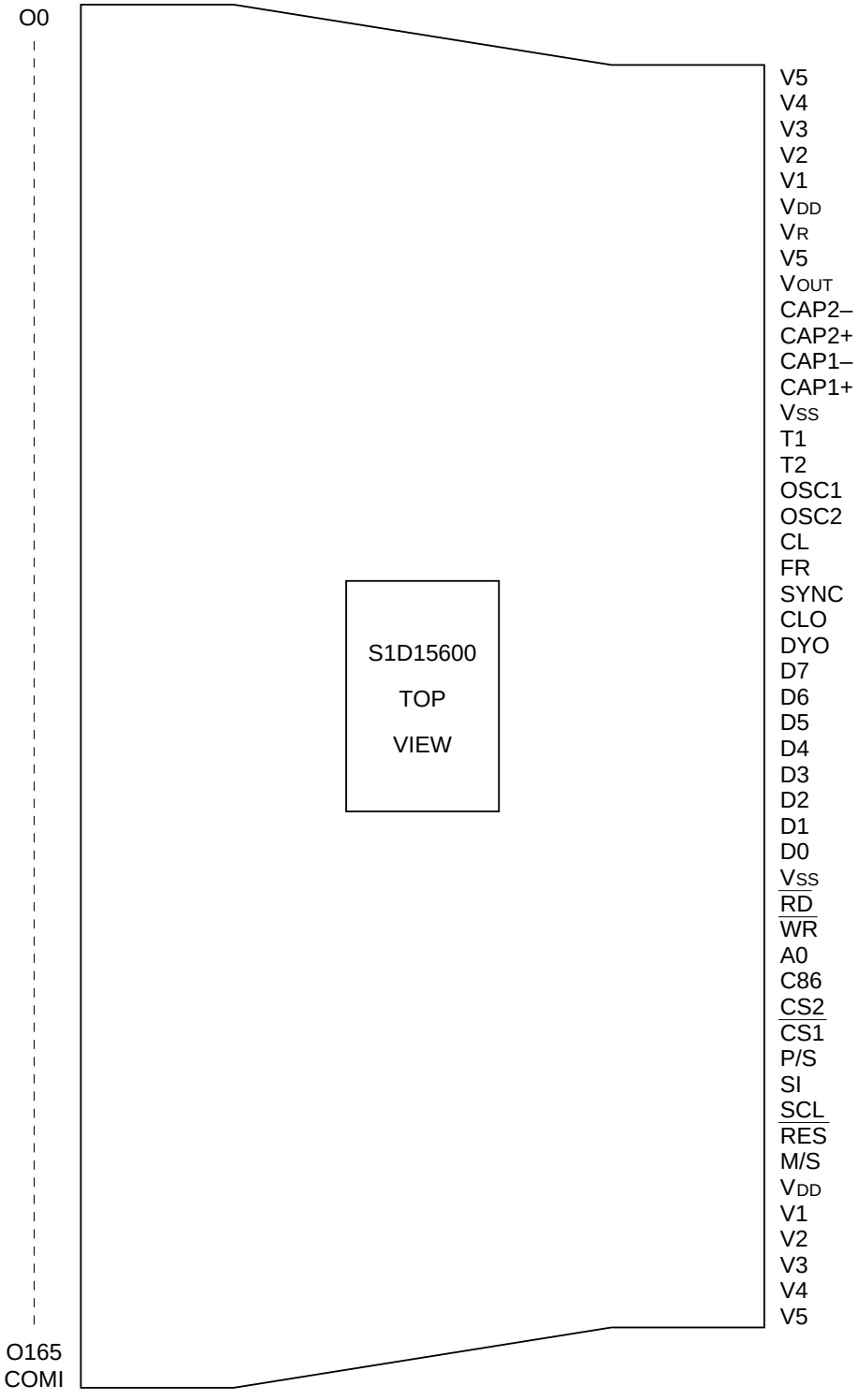


Case 6

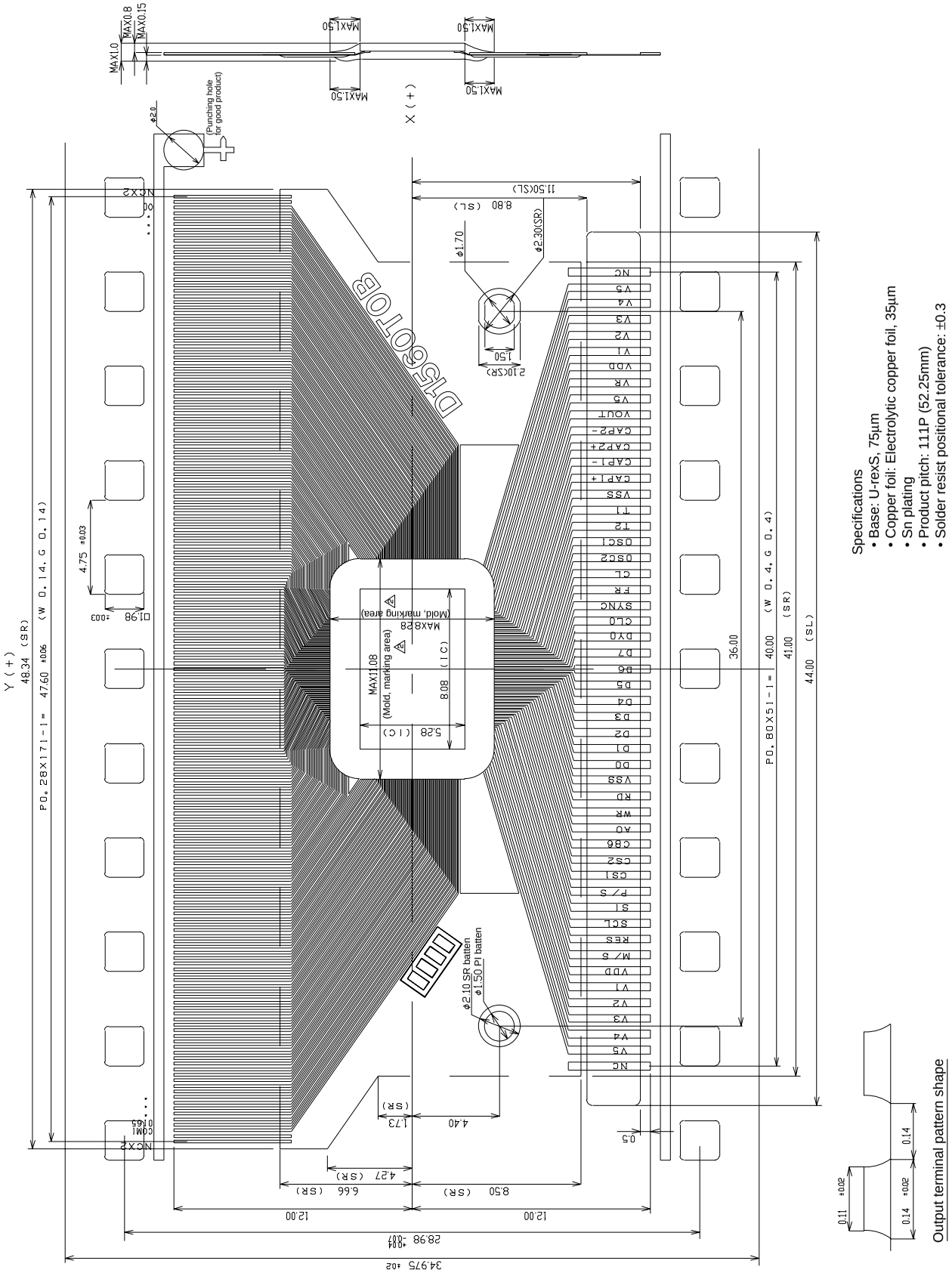
* If an external amp circuit is configured, we recommend to use the S1F76600 and S1F76610.

SED1560T TCP Pin Layout

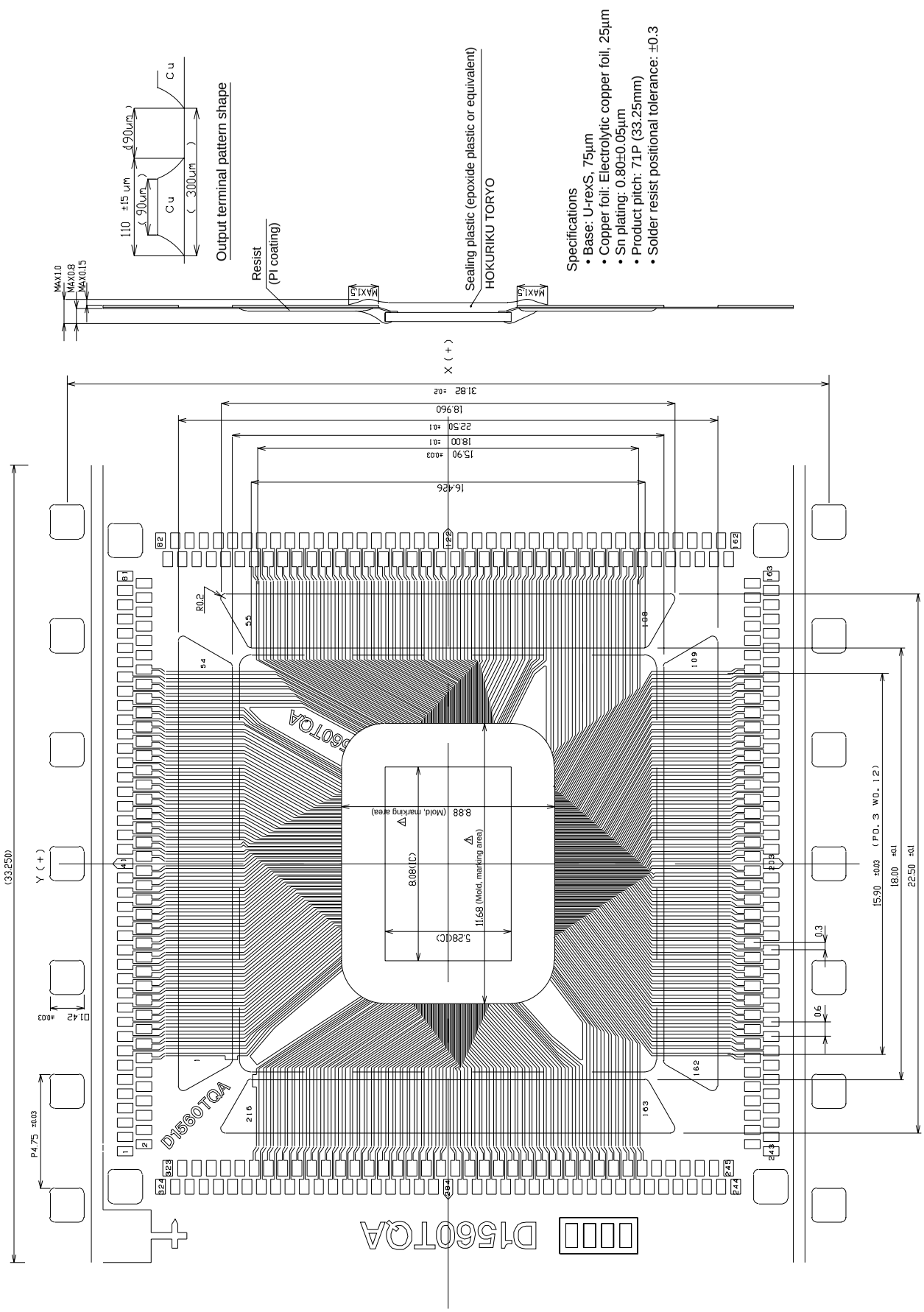
This drawing is not for specifying the TCP outline shape.



TCP DIMENSIONS (2 ways)



TCP DIMENSIONS (4 ways)



8. S1D15605 Series

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1. DESCRIPTION

The S1D15605 Series is a series of single-chip dot matrix liquid crystal display drivers that can be connected directly to a microprocessor bus. 8-bit parallel or serial display data sent from the microprocessor is stored in the internal display data RAM and the chip generates a liquid crystal drive signal independent of the microprocessor. Because the chips in the S1D15605***** contain 65 × 132 bits of display data RAM and there is a 1-to-1 correspondence between the liquid crystal panel pixels and the internal RAM bits, these chips enable displays with a high degree of freedom.
The S1D15606***** chips contain 49 common output circuits and 132 segment output circuits, so that a single chip can drive a 49 × 132 dot display (capable of displaying 8 columns × 4 rows of a 16 × 16 dot kanji font). The S1D15607***** chips contain 33 common output circuits and 132 segment output circuits, so that a single chip can drive 33 × 132 dot display (capable of displaying 8 columns × 2 rows of 16 × 16 dot kanji fonts). Thanks to the built-in 55 common output circuits and 132 segment output circuits, the S1D15608***** is capable of displaying 55 × 132 dots (11 columns × 4 lines using 11 × 12 dots Kanji font) with a single chip.
The S1D15609***** chips contain 53 common output circuits and 132 segment output circuits, so that a single chip can drive 53 × 132 dot display (capable of displaying 11 columns × 4 rows of 11 × 12 dot kanji fonts). Moreover, the capacity of the display can be extended through the use of master/slave structures between chips.
The chips are able to minimize power consumption because no external operating clock is necessary for the display data RAM read/write operation. Furthermore, because each chip is equipped internally with a low-power liquid crystal driver power supply, resistors for liquid crystal driver power voltage adjustment and a display clock CR oscillator circuit, the S1D15605 Series chips can be used to create the lowest power display system with the fewest components for high-performance portable devices.

2. FEATURES

- Direct display of RAM data through the display data RAM.
  RAM bit data: "1" Display on
  "0" Display off
  (during normal display)
- RAM capacity
  65 × 132 = 8580 bits
- Display driver circuits
  S1D15605*****:65 common output and 132 segment outputs
  S1D15606*****:49 common output and 132 segment outputs
  S1D15607*****:33 common outputs and 132 segment outputs
  S1D15608*****:55 common outputs and 132 segment outputs
  S1D15609*****:53 common outputs and 132 segment outputs
- High-speed 8-bit MPU interface (The chip can be connected directly to the both the 80x86 series MPUs and the 68000 series MPUs)
  /Serial interfaces are supported.
- Abundant command functions
  Display data Read/Write, display ON/OFF, Normal/Reverse display mode, page address set, display start line set, column address set, status read, display all points ON/OFF, LCD bias set, electronic volume, read/modify/write, segment driver direction select, power saver, static indicator, common output status select, V5 voltage regulation internal resistor ratio set.
- Static drive circuit equipped internally for indicators. (1 system, with variable flashing speed.)
- Low-power liquid crystal display power supply circuit equipped internally.
  Booster circuit (with Boost ratios of Double/Triple/Quad, where the step-up voltage reference power supply can be input externally)
  High-accuracy voltage adjustment circuit (Thermal gradient –0.05%/°C or –0.2%/°C or external input)
  V_5 voltage regulator resistors equipped internally, V_1 to V_4 voltage divider resistors equipped internally, electronic volume function equipped internally, voltage follower.
- CR oscillator circuit equipped internally (external clock can also be input)
- Extremely low power consumption
  Operating power when the built-in power supply is used (an example)
  S1D15605D00B∗ /S1D15605D11B∗ 81 µA ($V_{DD} – V_{SS} = V_{DD} – V_{SS2}$= 3.0 V, Quad voltage, $V_5 – V_{DD}$ = –11.0 V)
  S1D15606D00B∗ /S1D15606D11B∗ 43 µA ($V_{DD} – V_{SS} = V_{DD} – V_{SS2}$ = 3.0 V, Triple voltage, $V_5 – V_{DD}$ = –8.0 V)
  S1D15607D00B∗ /S1D15607D11B∗ 29 µA ($V_{DD} – V_{SS} = V_{DD} – V_{SS2}$ = 3.0 V, Triple voltage, $V_5 – V_{DD}$ = –8.0 V)
  S1D15608D00B∗/S1D15608D11B∗ /S1D15609D00B∗/S1D15609D11B∗ 46µA ($V_{DD} – V_{SS} = V_{DD} – V_{SS2}$ = 3.0 V, Triple voltage, $V_5 – V_{DD}$ = – 8.0 V)
  Conditions: When all displays are in white and the normal mode is selected (see page 60 *12 for details of the conditions).
- Power supply
  Operable on the low 1.8 voltage
  Logic power supply $V_{DD} – V_{SS}$ = 1.8 V to 5.5 V
  Boost reference voltage: $V_{DD} – V_{SS2}$ = 1.8 V to 6.0 V
  Liquid crystal drive power supply: $V5 – V_{DD}$ = –4.5 V to –16.0 V
- Wide range of operating temperatures: –40 to 85°C
- CMOS process
- Shipping forms include bare chip and TCP.
- These chips not designed for resistance to light or resistance to radiation.

Series Specifications

Bare chip

Product Name	Duty	Bias	SEG Dr	COM Dr	V_{REG} Temperature Gradient	Chip Thickness
S1D15605D00B∗	1/65	1/9, 1/7	132	65	–0.05%/°C	625 µm
S1D15605D11B∗	1/65	1/9, 1/7	132	65	–0.05%/°C	625 µm
S1D15605D11E∗	1/65	1/9, 1/7	132	65	–0.05%/°C	300 µm
S1D15605D01B∗	1/65	1/9, 1/7	132	65	–0.2%/°C	625 µm
S1D15605D02B∗	1/65	1/9, 1/7	132	65	External Input	625 µm
S1D15606D00B∗	1/49	1/8, 1/6	132	49	–0.05%/°C	625 µm
S1D15606D01B∗	1/49	1/8, 1/6	132	49	–0.2%/°C	625 µm
S1D15606D02B∗	1/49	1/8, 1/6	132	49	External Input	625 µm
S1D15606D11B∗	1/49	1/8, 1/6	132	49	–0.05%/°C	625 µm
S1D15607D00B∗	1/33	1/6, 1/5	132	33	–0.05%/°C	625 µm
S1D15607D01B∗	1/33	1/6, 1/5	132	33	–0.2%/°C	625 µm
S1D15607D02B∗	1/33	1/6, 1/5	132	33	External Input	625 µm
S1D15607D11B∗	1/33	1/6, 1/5	132	33	–0.05%/°C	625 µm
S1D15608D00B∗	1/55	1/8, 1/6	132	55	–0.05%/°C	625 µm
S1D15609D00B∗	1/53	1/8, 1/6	132	53	–0.05%/°C	625 µm

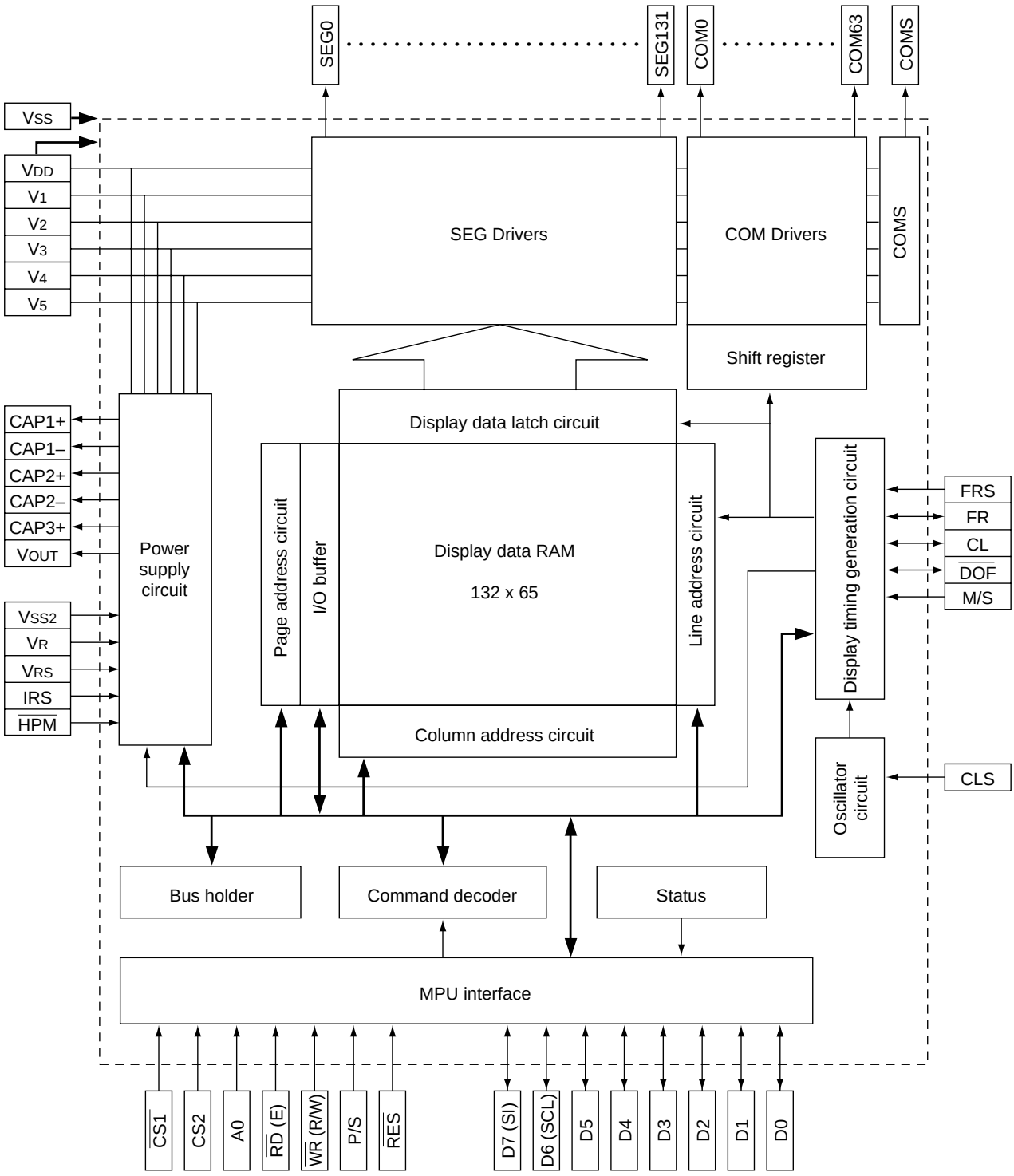
TCP

Product Name	Duty	Bias	SEG Dr	COM Dr	V_{REG} Temperature Gradient
S1D15605T00∗∗	1/65	1/9, 1/7	132	65	–0.05%/°C
S1D15606T00∗∗	1/49	1/8, 1/6	132	49	–0.05%/°C
S1D15607T00∗∗	1/33	1/6, 1/5	132	33	–0.05%/°C

Product name of custom TCP can be coped with specially.

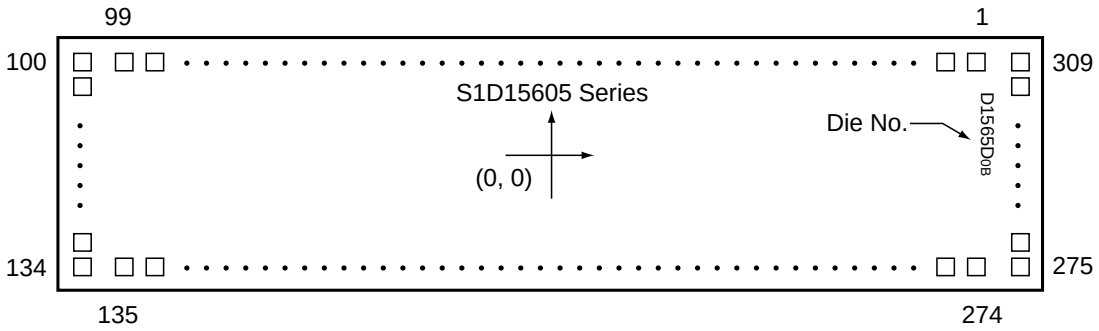
3. BLOCK DIAGRAM

Example: S1D15605*****



4. PAD

Pad Layout



Chip Size	10.82 mm × 2.81 mm	
Chip Thickness	0.625 mm	
Bump Pitch	71 μm (Min.)	
Bump Size	PAD No. 1~24	85 μm × 85 μm
	PAD No. 25~82	64 μm × 85 μm
	PAD No. 83~99	85 μm × 85 μm
	PAD No. 100	85 μm × 73 μm
	PAD No. 101~133	85 μm × 47 μm
	PAD No. 134	85 μm × 73 μm
	PAD No. 135	73 μm × 85 μm
	PAD No. 136~273	47 μm × 85 μm
	PAD No. 274	73 μm × 85 μm
	PAD No. 275	86 μm × 73 μm
	PAD No. 276~308	85 μm × 47 μm
	PAD No. 309	85 μm × 73 μm
Bump Height	17 μm (Typ.)	

S1D15605***** Pad Center Coordinates

Units: μm

PAD No.	PIN Name	X	Y
1	(NC)	4973	1246
2	FRS	4853	
3	FR	4734	
4	CL	4614	
5	$\overline{DOF}$	4494	
6	TEST0	4375	
7	V_{SS}	4255	
8	$\overline{CS1}$	4136	
9	CS2	4016	
10	V_{DD}	3896	
11	$\overline{RES}$	3777	
12	A0	3657	
13	V_{SS}	3538	
14	$\overline{WR}$, R/$\overline{W}$	3418	
15	$\overline{RD}$, E	3298	
16	V_{DD}	3179	
17	D0	3059	
18	D1	2940	
19	D2	2820	
20	D3	2700	
21	D4	2581	
22	D5	2461	
23	D6, SCL	2342	
24	D7, SI	2222	
25	(NC)	2119	
26	V_{DD}	2030	
27	V_{DD}	1941	
28	V_{DD}	1852	
29	V_{DD}	1763	
30	V_{SS}	1674	
31	V_{SS}	1585	
32	V_{SS}	1496	
33	V_{SS2}	1407	
34	V_{SS2}	1318	
35	V_{SS2}	1229	
36	V_{SS2}	1140	
37	(NC)	1051	
38	V_{OUT}	962	
39	V_{OUT}	873	
40	CAP3–	784	

PAD No.	PIN Name	X	Y
41	CAP3–	695	1246
42	(NC)	605	
43	CAP1+	516	
44	CAP1+	427	
45	CAP1–	338	
46	CAP1–	249	
47	CAP2–	160	
48	CAP2–	71	
49	CAP2+	–18	
50	CAP2+	–107	
51	V_{SS}	–196	
52	V_{SS}	–285	
53	V_{RS}	–374	
54	V_{RS}	–463	
55	V_{DD}	–552	
56	V_{DD}	–641	
57	V_1	–730	
58	V_1	–819	
59	V_2	–908	
60	V_2	–997	
61	(NC)	–1086	
62	V_3	–1176	
63	V_3	–1265	
64	V_4	–1354	
65	V_4	–1443	
66	V_5	–1532	
67	V_5	–1621	
68	(NC)	–1710	
69	V_R	–1799	
70	V_R	–1888	
71	V_{DD}	–1977	
72	V_{DD}	–2066	
73	TEST1	–2155	
74	TEST1	–2244	
75	TEST2	–2333	
76	TEST2	–2422	
77	(NC)	–2511	
78	TEST3	–2600	
79	TEST3	–2689	
80	TEST4	–2778	

PAD No.	PIN Name	X	Y
81	TEST4	–2867	1246
82	(NC)	–2957	
83	V_{DD}	–3059	
84	M/S	–3179	
85	CLS	–3298	
86	V_{SS}	–3418	
87	C86	–3538	
88	P/S	–3657	
89	V_{DD}	–3777	
90	$\overline{HPM}$	–3896	
91	V_{SS}	–4016	
92	IRS	–4136	
93	V_{DD}	–4255	
94	TEST5	–4375	
95	TEST6	–4494	
96	TEST7	–4614	
97	TEST8	–4734	
98	TEST9	–4853	
99	(NC)	–4973	
100	(NC)	–5252	1248
101	COM31		1163
102	COM30		1090
103	COM29		1017
104	COM28		945
105	COM27		872
106	COM26		799
107	COM25		727
108	COM24		654
109	COM23		581
110	COM22		509
111	COM21		436
112	COM20		363
113	COM19		291
114	COM18		218
115	COM17		145
116	COM16		73
117	COM15		0
118	COM14		–73
119	COM13		–145
120	COM12		–218

Units: μm

PAD No.	PIN Name	X	Y
121	COM11	–5252	–291
122	COM10		–363
123	COM9		–436
124	COM8		–509
125	COM7		–581
126	COM6		–654
127	COM5		–727
128	COM4		–800
129	COM3		–872
130	COM2		–945
131	COM1		–1018
132	COM0		–1090
133	COMS		–1163
134	(NC)		–1248
135	(NC)	–5009	–1246
136	(NC)	–4924	
137	(NC)	–4853	
138	(NC)	–4781	
139	SEG0	–4709	
140	SEG1	–4637	
141	SEG2	–4565	
142	SEG3	–4493	
143	SEG4	–4421	
144	SEG5	–4349	
145	SEG6	–4277	
146	SEG7	–4206	
147	SEG8	–4134	
148	SEG9	–4062	
149	SEG10	–3990	
150	SEG11	–3918	
151	SEG12	–3846	
152	SEG13	–3774	
153	SEG14	–3702	
154	SEG15	–3630	
155	SEG16	–3559	
156	SEG17	–3487	
157	SEG18	–3415	
158	SEG19	–3343	
159	SEG20	–3271	
160	SEG21	–3199	

PAD No.	PIN Name	X	Y
161	SEG22	–3127	–1246
162	SEG23	–3055	
163	SEG24	–2983	
164	SEG25	–2912	
165	SEG26	–2840	
166	SEG27	–2768	
167	SEG28	–2696	
168	SEG29	–2624	
169	SEG30	–2552	
170	SEG31	–2480	
171	SEG32	–2408	
172	SEG33	–2336	
173	SEG34	–2265	
174	SEG35	–2193	
175	SEG36	–2121	
176	SEG37	–2049	
177	SEG38	–1977	
178	SEG39	–1905	
179	SEG40	–1833	
180	SEG41	–1761	
181	SEG42	–1689	
182	SEG43	–1618	
183	SEG44	–1546	
184	SEG45	–1474	
185	SEG46	–1402	
186	SEG47	–1330	
187	SEG48	–1258	
188	SEG49	–1186	
189	SEG50	–1114	
190	SEG51	–1042	
191	SEG52	–971	
192	SEG53	–899	
193	SEG54	–827	
194	SEG55	–755	
195	SEG56	–683	
196	SEG57	–611	
197	SEG58	–539	
198	SEG59	–467	
199	SEG60	–395	
200	SEG61	–324	

PAD No.	PIN Name	X	Y
201	SEG62	–252	–1246
202	SEG63	–180	
203	SEG64	–108	
204	SEG65	–36	
205	SEG66	36	
206	SEG67	108	
207	SEG68	180	
208	SEG69	252	
209	SEG70	324	
210	SEG71	395	
211	SEG72	467	
212	SEG73	539	
213	SEG74	611	
214	SEG75	683	
215	SEG76	755	
216	SEG77	827	
217	SEG78	899	
218	SEG79	971	
219	SEG80	1042	
220	SEG81	1114	
221	SEG82	1186	
222	SEG83	1258	
223	SEG84	1330	
224	SEG85	1402	
225	SEG86	1474	
226	SEG87	1546	
227	SEG88	1618	
228	SEG89	1689	
229	SEG90	1761	
230	SEG91	1833	
231	SEG92	1905	
232	SEG93	1977	
233	SEG94	2049	
234	SEG95	2121	
235	SEG96	2193	
236	SEG97	2265	
237	SEG98	2336	
238	SEG99	2408	
239	SEG100	2480	
240	SEG101	2552	

Units: μm

PAD No.	PIN Name	X	Y
241	SEG102	2624	–1246
242	SEG103	2696	
243	SEG104	2768	
244	SEG105	2840	
245	SEG106	2912	
246	SEG107	2983	
247	SEG108	3055	
248	SEG109	3127	
249	SEG110	3199	
250	SEG111	3271	
251	SEG112	3343	
252	SEG113	3415	
253	SEG114	3487	
254	SEG115	3558	
255	SEG116	3630	
256	SEG117	3702	
257	SEG118	3774	
258	SEG119	3846	
259	SEG120	3918	
260	SEG121	3990	
261	SEG122	4062	
262	SEG123	4134	
263	SEG124	4206	
264	SEG125	4277	
265	SEG126	4349	
266	SEG127	4421	
267	SEG128	4493	
268	SEG129	4565	
269	SEG130	4637	
270	SEG131	4709	
271	(NC)	4781	
272	(NC)	4853	
273	(NC)	4924	
274	(NC)	5009	
275	(NC)	5252	–1248
276	COM32		–1163
277	COM33		–1090
278	COM34		–1018
279	COM35		–945
280	COM36		–872

PAD No.	PIN Name	X	Y
281	COM37	5252	–800
282	COM38		–727
283	COM39		–654
284	COM40		–581
285	COM41		–509
286	COM42		–436
287	COM43		–363
288	COM44		–291
289	COM45		–218
290	COM46		–145
291	COM47		–73
292	COM48		0
293	COM49		73
294	COM50		145
295	COM51		218
296	COM52		291
297	COM53		363
298	COM54		436
299	COM55		509
300	COM56		581
301	COM57		654
302	COM58		727
303	COM59		799
304	COM60		872
305	COM61		945
306	COM62		1017
307	COM63		1090
308	COMS		1163
309	(NC)		1248

S1D15606***** Pad Center Coordinates

Units: μm

PAD No.	PIN Name	X	Y
1	(NC)	4973	1246
2	FRS	4853	
3	FR	4734	
4	CL	4614	
5	$\overline{DOF}$	4494	
6	TEST0	4375	
7	V_{SS}	4255	
8	$\overline{CS1}$	4136	
9	CS2	4016	
10	V_{DD}	3896	
11	$\overline{RES}$	3777	
12	A0	3657	
13	V_{SS}	3538	
14	$\overline{WR}$, R/$\overline{W}$	3418	
15	$\overline{RD}$, E	3298	
16	V_{DD}	3179	
17	D0	3059	
18	D1	2940	
19	D2	2820	
20	D3	2700	
21	D4	2581	
22	D5	2461	
23	D6, SCL	2342	
24	D7, SI	2222	
25	(NC)	2119	
26	V_{DD}	2030	
27	V_{DD}	1941	
28	V_{DD}	1852	
29	V_{DD}	1763	
30	V_{SS}	1674	
31	V_{SS}	1585	
32	V_{SS}	1496	
33	V_{SS2}	1407	
34	V_{SS2}	1318	
35	V_{SS2}	1229	
36	V_{SS2}	1140	
37	(NC)	1051	
38	V_{OUT}	962	
39	V_{OUT}	873	
40	CAP3–	784	

PAD No.	PIN Name	X	Y
41	CAP3–	695	1246
42	(NC)	605	
43	CAP1+	516	
44	CAP1+	427	
45	CAP1–	338	
46	CAP1–	249	
47	CAP2–	160	
48	CAP2–	71	
49	CAP2+	–18	
50	CAP2+	–107	
51	V_{SS}	–196	
52	V_{SS}	–285	
53	V_{RS}	–374	
54	V_{RS}	–463	
55	V_{DD}	–552	
56	V_{DD}	–641	
57	V_1	–730	
58	V_1	–819	
59	V_2	–908	
60	V_2	–997	
61	(NC)	–1086	
62	V_3	–1176	
63	V_3	–1265	
64	V_4	–1354	
65	V_4	–1443	
66	V_5	–1532	
67	V_5	–1621	
68	(NC)	–1710	
69	V_R	–1799	
70	V_R	–1888	
71	V_{DD}	–1977	
72	V_{DD}	–2066	
73	TEST1	–2155	
74	TEST1	–2244	
75	TEST2	–2333	
76	TEST2	–2422	
77	(NC)	–2511	
78	TEST3	–2600	
79	TEST3	–2689	
80	TEST4	–2778	

PAD No.	PIN Name	X	Y
81	TEST4	–2867	1246
82	(NC)	–2957	
83	V_{DD}	–3059	
84	M/S	–3179	
85	CLS	–3298	
86	V_{SS}	–3418	
87	C86	–3538	
88	P/S	–3657	
89	V_{DD}	–3777	
90	HPM	–3896	
91	V_{SS}	–4016	
92	IRS	–4136	
93	V_{DD}	–4255	
94	TEST5	–4375	
95	TEST6	–4494	
96	TEST7	–4614	
97	TEST8	–4734	
98	TEST9	–4853	
99	(NC)	–4973	
100	(NC)	–5252	1248
101	(NC)		1163
102	(NC)		1090
103	COM23		1017
104	(NC)		945
105	COM22		872
106	(NC)		799
107	COM21		727
108	COM20		654
109	COM19		581
110	COM18		509
111	COM17		436
112	COM16		363
113	COM15		291
114	COM14		218
115	COM13		145
116	COM12		73
117	COM11		0
118	COM10		–73
119	COM9		–145
120	COM8		–218

Units: μm

PAD No.	PIN Name	X	Y
121	COM7	–5252	–291
122	COM6		–363
123	COM5		–436
124	COM4		–509
125	COM3		–581
126	COM2		–654
127	COM1		–727
128	(NC)		–800
129	COM0		–872
130	(NC)		–945
131	COMS		–1018
132	(NC)		–1090
133	(NC)		–1163
134	(NC)		–1248
135	(NC)	–5009	–1246
136	(NC)	–4924	
137	(NC)	–4853	
138	(NC)	–4781	
139	SEG0	–4709	
140	SEG1	–4637	
141	SEG2	–4565	
142	SEG3	–4493	
143	SEG4	–4421	
144	SEG5	–4349	
145	SEG6	–4277	
146	SEG7	–4206	
147	SEG8	–4134	
148	SEG9	–4062	
149	SEG10	–3990	
150	SEG11	–3918	
151	SEG12	–3846	
152	SEG13	–3774	
153	SEG14	–3702	
154	SEG15	–3630	
155	SEG16	–3559	
156	SEG17	–3487	
157	SEG18	–3415	
158	SEG19	–3343	
159	SEG20	–3271	
160	SEG21	–3199	

PAD No.	PIN Name	X	Y
161	SEG22	–3127	–1246
162	SEG23	–3055	
163	SEG24	–2983	
164	SEG25	–2912	
165	SEG26	–2840	
166	SEG27	–2768	
167	SEG28	–2696	
168	SEG29	–2624	
169	SEG30	–2552	
170	SEG31	–2480	
171	SEG32	–2408	
172	SEG33	–2336	
173	SEG34	–2265	
174	SEG35	–2193	
175	SEG36	–2121	
176	SEG37	–2049	
177	SEG38	–1977	
178	SEG39	–1905	
179	SEG40	–1833	
180	SEG41	–1761	
181	SEG42	–1689	
182	SEG43	–1618	
183	SEG44	–1546	
184	SEG45	–1474	
185	SEG46	–1402	
186	SEG47	–1330	
187	SEG48	–1258	
188	SEG49	–1186	
189	SEG50	–1114	
190	SEG51	–1042	
191	SEG52	–971	
192	SEG53	–899	
193	SEG54	–827	
194	SEG55	–755	
195	SEG56	–683	
196	SEG57	–611	
197	SEG58	–539	
198	SEG59	–467	
199	SEG60	–395	
200	SEG61	–324	

PAD No.	PIN Name	X	Y
201	SEG62	–252	–1246
202	SEG63	–180	
203	SEG64	–108	
204	SEG65	–36	
205	SEG66	36	
206	SEG67	108	
207	SEG68	180	
208	SEG69	252	
209	SEG70	324	
210	SEG71	395	
211	SEG72	467	
212	SEG73	539	
213	SEG74	611	
214	SEG75	683	
215	SEG76	755	
216	SEG77	827	
217	SEG78	899	
218	SEG79	971	
219	SEG80	1042	
220	SEG81	1114	
221	SEG82	1186	
222	SEG83	1258	
223	SEG84	1330	
224	SEG85	1402	
225	SEG86	1474	
226	SEG87	1546	
227	SEG88	1618	
228	SEG89	1689	
229	SEG90	1761	
230	SEG91	1833	
231	SEG92	1905	
232	SEG93	1977	
233	SEG94	2049	
234	SEG95	2121	
235	SEG96	2193	
236	SEG97	2265	
237	SEG98	2336	
238	SEG99	2408	
239	SEG100	2480	
240	SEG101	2552	

Units: μm

PAD No.	PIN Name	X	Y
241	SEG102	2624	–1246
242	SEG103	2696	
243	SEG104	2768	
244	SEG105	2840	
245	SEG106	2912	
246	SEG107	2983	
247	SEG108	3055	
248	SEG109	3127	
249	SEG110	3199	
250	SEG111	3271	
251	SEG112	3343	
252	SEG113	3415	
253	SEG114	3487	
254	SEG115	3558	
255	SEG116	3630	
256	SEG117	3702	
257	SEG118	3774	
258	SEG119	3846	
259	SEG120	3918	
260	SEG121	3990	
261	SEG122	4062	
262	SEG123	4134	
263	SEG124	4206	
264	SEG125	4277	
265	SEG126	4349	
266	SEG127	4421	
267	SEG128	4493	
268	SEG129	4565	
269	SEG130	4637	
270	SEG131	4709	
271	(NC)	4781	
272	(NC)	4853	
273	(NC)	4924	
274	(NC)	5009	
275	(NC)	5252	–1248
276	(NC)		–1163
277	(NC)		–1090
278	COM24		–1018
279	(NC)		–945
280	COM25		–872

PAD No.	PIN Name	X	Y
281	(NC)	5252	–800
282	COM26		–727
283	COM27		–654
284	COM28		–581
285	COM29		–509
286	COM30		–436
287	COM31		–363
288	COM32		–291
289	COM33		–218
290	COM34		–145
291	COM35		–73
292	COM36		0
293	COM37		73
294	COM38		145
295	COM39		218
296	COM40		291
297	COM41		363
298	COM42		436
299	COM43		509
300	COM44		581
301	COM45		654
302	COM46		727
303	(NC)		799
304	COM47		872
305	(NC)		945
306	COMS		1017
307	(NC)		1090
308	(NC)		1163
309	(NC)		1248

S1D15607***** Pad Center Coordinates

Units: μm

PAD No.	PIN Name	X	Y
1	(NC)	4973	1246
2	FRS	4853	
3	FR	4734	
4	CL	4614	
5	$\overline{DOF}$	4494	
6	TEST0	4375	
7	V_{SS}	4255	
8	$\overline{CS1}$	4136	
9	CS2	4016	
10	V_{DD}	3896	
11	$\overline{RES}$	3777	
12	A0	3657	
13	V_{SS}	3538	
14	$\overline{WR}$, R/$\overline{W}$	3418	
15	$\overline{RD}$, E	3298	
16	V_{DD}	3179	
17	D0	3059	
18	D1	2940	
19	D2	2820	
20	D3	2700	
21	D4	2581	
22	D5	2461	
23	D6, SCL	2342	
24	D7, SI	2222	
25	(NC)	2119	
26	V_{DD}	2030	
27	V_{DD}	1941	
28	V_{DD}	1852	
29	V_{DD}	1763	
30	V_{SS}	1674	
31	V_{SS}	1585	
32	V_{SS}	1496	
33	V_{SS2}	1407	
34	V_{SS2}	1318	
35	V_{SS2}	1229	
36	V_{SS2}	1140	
37	(NC)	1051	
38	V_{OUT}	962	
39	V_{OUT}	873	
40	CAP3–	784	

PAD No.	PIN Name	X	Y
41	CAP3–	695	1246
42	(NC)	605	
43	CAP1+	516	
44	CAP1+	427	
45	CAP1–	338	
46	CAP1–	249	
47	CAP2–	160	
48	CAP2–	71	
49	CAP2+	–18	
50	CAP2+	–107	
51	V_{SS}	–196	
52	V_{SS}	–285	
53	V_{RS}	–374	
54	V_{RS}	–463	
55	V_{DD}	–552	
56	V_{DD}	–641	
57	V_1	–730	
58	V_1	–819	
59	V_2	–908	
60	V_2	–997	
61	(NC)	–1086	
62	V_3	–1176	
63	V_3	–1265	
64	V_4	–1354	
65	V_4	–1443	
66	V_5	–1532	
67	V_5	–1621	
68	(NC)	–1710	
69	V_R	–1799	
70	V_R	–1888	
71	V_{DD}	–1977	
72	V_{DD}	–2066	
73	TEST1	–2155	
74	TEST1	–2244	
75	TEST2	–2333	
76	TEST2	–2422	
77	(NC)	–2511	
78	TEST3	–2600	
79	TEST3	–2689	
80	TEST4	–2778	

PAD No.	PIN Name	X	Y
81	TEST4	–2867	1246
82	(NC)	–2957	
83	V_{DD}	–3059	
84	M/S	–3179	
85	CLS	–3298	
86	V_{SS}	–3418	
87	C86	–3538	
88	P/S	–3657	
89	V_{DD}	–3777	
90	$\overline{HPM}$	–3896	
91	V_{SS}	–4016	
92	IRS	–4136	
93	V_{DD}	–4255	
94	TEST5	–4375	
95	TEST6	–4494	
96	TEST7	–4614	
97	TEST8	–4734	
98	TEST9	–4853	
99	(NC)	–4973	
100	(NC)	–5252	1248
101	COM15		1163
102	COM15		1090
103	COM14		1017
104	COM14		945
105	COM13		872
106	COM13		799
107	COM12		727
108	COM12		654
109	COM11		581
110	COM11		509
111	COM10		436
112	COM10		363
113	COM9		291
114	COM9		218
115	COM8		145
116	COM8		73
117	COM7		0
118	COM7		–73
119	COM6		–145
120	COM6		–218

Units: μm

PAD No.	PIN Name	X	Y
121	COM5	–5252	–291
122	COM5		–363
123	COM4		–436
124	COM4		–509
125	COM3		–581
126	COM3		–654
127	COM2		–727
128	COM2		–800
129	COM1		–872
130	COM1		–945
131	COM0		–1018
132	COM0		–1090
133	COMS		–1163
134	(NC)		–1248
135	(NC)	–5009	–1246
136	(NC)	–4924	
137	(NC)	–4853	
138	(NC)	–4781	
139	SEG0	–4709	
140	SEG1	–4637	
141	SEG2	–4565	
142	SEG3	–4493	
143	SEG4	–4421	
144	SEG5	–4349	
145	SEG6	–4277	
146	SEG7	–4206	
147	SEG8	–4134	
148	SEG9	–4062	
149	SEG10	–3990	
150	SEG11	–3918	
151	SEG12	–3846	
152	SEG13	–3774	
153	SEG14	–3702	
154	SEG15	–3630	
155	SEG16	–3559	
156	SEG17	–3487	
157	SEG18	–3415	
158	SEG19	–3343	
159	SEG20	–3271	
160	SEG21	–3199	

PAD No.	PIN Name	X	Y
161	SEG22	–3127	–1246
162	SEG23	–3055	
163	SEG24	–2983	
164	SEG25	–2912	
165	SEG26	–2840	
166	SEG27	–2768	
167	SEG28	–2696	
168	SEG29	–2624	
169	SEG30	–2552	
170	SEG31	–2480	
171	SEG32	–2408	
172	SEG33	–2336	
173	SEG34	–2265	
174	SEG35	–2193	
175	SEG36	–2121	
176	SEG37	–2049	
177	SEG38	–1977	
178	SEG39	–1905	
179	SEG40	–1833	
180	SEG41	–1761	
181	SEG42	–1689	
182	SEG43	–1618	
183	SEG44	–1546	
184	SEG45	–1474	
185	SEG46	–1402	
186	SEG47	–1330	
187	SEG48	–1258	
188	SEG49	–1186	
189	SEG50	–1114	
190	SEG51	–1042	
191	SEG52	–971	
192	SEG53	–899	
193	SEG54	–827	
194	SEG55	–755	
195	SEG56	–683	
196	SEG57	–611	
197	SEG58	–539	
198	SEG59	–467	
199	SEG60	–395	
200	SEG61	–324	

PAD No.	PIN Name	X	Y
201	SEG62	–252	–1246
202	SEG63	–180	
203	SEG64	–108	
204	SEG65	–36	
205	SEG66	36	
206	SEG67	108	
207	SEG68	180	
208	SEG69	252	
209	SEG70	324	
210	SEG71	395	
211	SEG72	467	
212	SEG73	539	
213	SEG74	611	
214	SEG75	683	
215	SEG76	755	
216	SEG77	827	
217	SEG78	899	
218	SEG79	971	
219	SEG80	1042	
220	SEG81	1114	
221	SEG82	1186	
222	SEG83	1258	
223	SEG84	1330	
224	SEG85	1402	
225	SEG86	1474	
226	SEG87	1546	
227	SEG88	1618	
228	SEG89	1689	
229	SEG90	1761	
230	SEG91	1833	
231	SEG92	1905	
232	SEG93	1977	
233	SEG94	2049	
234	SEG95	2121	
235	SEG96	2193	
236	SEG97	2265	
237	SEG98	2336	
238	SEG99	2408	
239	SEG100	2480	
240	SEG101	2552	

Units: μm

PAD No.	PIN Name	X	Y
241	SEG102	2624	–1246
242	SEG103	2696	
243	SEG104	2768	
244	SEG105	2840	
245	SEG106	2912	
246	SEG107	2983	
247	SEG108	3055	
248	SEG109	3127	
249	SEG110	3199	
250	SEG111	3271	
251	SEG112	3343	
252	SEG113	3415	
253	SEG114	3487	
254	SEG115	3558	
255	SEG116	3630	
256	SEG117	3702	
257	SEG118	3774	
258	SEG119	3846	
259	SEG120	3918	
260	SEG121	3990	
261	SEG122	4062	
262	SEG123	4134	
263	SEG124	4206	
264	SEG125	4277	
265	SEG126	4349	
266	SEG127	4421	
267	SEG128	4493	
268	SEG129	4565	
269	SEG130	4637	
270	SEG131	4709	
271	(NC)	4781	
272	(NC)	4853	
273	(NC)	4924	
274	(NC)	5009	
275	(NC)	5252	–1248
276	COM16		–1163
277	COM16		–1090
278	COM17		–1018
279	COM17		–945
280	COM18		–872

PAD No.	PIN Name	X	Y
281	COM18	5252	–800
282	COM19		–727
283	COM19		–654
284	COM20		–581
285	COM20		–509
286	COM21		–436
287	COM21		–363
288	COM22		–291
289	COM22		–218
290	COM23		–145
291	COM23		–73
292	COM24		0
293	COM24		73
294	COM25		145
295	COM25		218
296	COM26		291
297	COM26		363
298	COM27		436
299	COM27		509
300	COM28		581
301	COM28		654
302	COM29		727
303	COM29		799
304	COM30		872
305	COM30		945
306	COM31		1017
307	COM31		1090
308	COMS		1163
309	(NC)		1248

S1D15608***** Pad Center Coordinates

Units: μm

PAD No.	PIN Name	X	Y
1	(NC)	4973	1246
2	FRS	4853	
3	FR	4734	
4	CL	4614	
5	$\overline{DOF}$	4494	
6	TEST0	4375	
7	V_{SS}	4255	
8	$\overline{CS1}$	4136	
9	CS2	4016	
10	V_{DD}	3896	
11	$\overline{RES}$	3777	
12	A0	3657	
13	V_{SS}	3538	
14	$\overline{WR}$, R/$\overline{W}$	3418	
15	$\overline{RD}$, E	3298	
16	V_{DD}	3179	
17	D0	3059	
18	D1	2940	
19	D2	2820	
20	D3	2700	
21	D4	2581	
22	D5	2461	
23	D6, SCL	2342	
24	D7, SI	2222	
25	(NC)	2119	
26	V_{DD}	2030	
27	V_{DD}	1941	
28	V_{DD}	1852	
29	V_{DD}	1763	
30	V_{SS}	1674	
31	V_{SS}	1585	
32	V_{SS}	1496	
33	V_{SS2}	1407	
34	V_{SS2}	1318	
35	V_{SS2}	1229	
36	V_{SS2}	1140	
37	(NC)	1051	
38	V_{OUT}	962	
39	V_{OUT}	873	
40	CAP3–	784	
41	CAP3–	695	1246
42	(NC)	605	
43	CAP1+	516	
44	CAP1+	427	
45	CAP1–	338	
46	CAP1–	249	
47	CAP2–	160	
48	CAP2–	71	
49	CAP2+	–18	
50	CAP2+	–107	
51	V_{SS}	–196	
52	V_{SS}	–285	
53	V_{RS}	–374	
54	V_{RS}	–463	
55	V_{DD}	–552	
56	V_{DD}	–641	
57	V_1	–730	
58	V_1	–819	
59	V_2	–908	
60	V_2	–997	
61	(NC)	–1086	
62	V_3	–1176	
63	V_3	–1265	
64	V_4	–1354	
65	V_4	–1443	
66	V_5	–1532	
67	V_5	–1621	
68	(NC)	–1710	
69	V_R	–1799	
70	V_R	–1888	
71	V_{DD}	–1977	
72	V_{DD}	–2066	
73	TEST1	–2155	
74	TEST1	–2244	
75	TEST2	–2333	
76	TEST2	–2422	
77	(NC)	–2511	
78	TEST3	–2600	
79	TEST3	–2689	
80	TEST4	–2778	
81	TEST4	–2867	1246
82	(NC)	–2957	
83	V_{DD}	–3059	
84	M/S	–3179	
85	CLS	–3298	
86	V_{SS}	–3418	
87	C86	–3538	
88	P/S	–3657	
89	V_{DD}	–3777	
90	$\overline{HPM}$	–3896	
91	V_{SS}	–4016	
92	IRS	–4136	
93	V_{DD}	–4255	
94	TEST5	–4375	
95	TEST6	–4494	
96	TEST7	–4614	
97	TEST8	–4734	
98	TEST9	–4853	
99	(NC)	–4973	
100	(NC)	–5252	1248
101	(NC)		1163
102	COM26		1090
103	(NC)		1017
104	COM25		945
105	COM25		872
106	COM23		799
107	COM22		727
108	COM21		654
109	COM20		581
110	COM19		509
111	COM18		436
112	COM17		363
113	COM16		291
114	COM15		218
115	COM14		145
116	COM13		73
117	COM12		0
118	COM11		–73
119	COM10		–145
120	COM9		–218

Units: μm

PAD No.	PIN Name	X	Y
121	COM8	–5252	–291
122	COM7		–363
123	COM6		–436
124	COM5		–509
125	COM4		–581
126	COM3		–654
127	COM2		–727
128	COM1		–800
129	(NC)		–872
130	COM0		–945
131	(NC)		–1018
132	COMS		–1090
133	(NC)		–1163
134	(NC)		–1248
135	(NC)	–5009	–1246
136	(NC)	–4924	
137	(NC)	–4853	
138	(NC)	–4781	
139	SEG0	–4709	
140	SEG1	–4637	
141	SEG2	–4565	
142	SEG3	–4493	
143	SEG4	–4421	
144	SEG5	–4349	
145	SEG6	–4277	
146	SEG7	–4206	
147	SEG8	–4134	
148	SEG9	–4062	
149	SEG10	–3990	
150	SEG11	–3918	
151	SEG12	–3846	
152	SEG13	–3774	
153	SEG14	–3702	
154	SEG15	–3630	
155	SEG16	–3559	
156	SEG17	–3487	
157	SEG18	–3415	
158	SEG19	–3343	
159	SEG20	–3271	
160	SEG21	–3199	

PAD No.	PIN Name	X	Y
161	SEG22	–3127	–1246
162	SEG23	–3055	
163	SEG24	–2983	
164	SEG25	–2912	
165	SEG26	–2840	
166	SEG27	–2768	
167	SEG28	–2696	
168	SEG29	–2624	
169	SEG30	–2552	
170	SEG31	–2480	
171	SEG32	–2408	
172	SEG33	–2336	
173	SEG34	–2265	
174	SEG35	–2193	
175	SEG36	–2121	
176	SEG37	–2049	
177	SEG38	–1977	
178	SEG39	–1905	
179	SEG40	–1833	
180	SEG41	–1761	
181	SEG42	–1689	
182	SEG43	–1618	
183	SEG44	–1546	
184	SEG45	–1474	
185	SEG46	–1402	
186	SEG47	–1330	
187	SEG48	–1258	
188	SEG49	–1186	
189	SEG50	–1114	
190	SEG51	–1042	
191	SEG52	–971	
192	SEG53	–899	
193	SEG54	–827	
194	SEG55	–755	
195	SEG56	–683	
196	SEG57	–611	
197	SEG58	–539	
198	SEG59	–467	
199	SEG60	–395	
200	SEG61	–324	

PAD No.	PIN Name	X	Y
201	SEG62	–252	–1246
202	SEG63	–180	
203	SEG64	–108	
204	SEG65	–36	
205	SEG66	36	
206	SEG67	108	
207	SEG68	180	
208	SEG69	252	
209	SEG70	324	
210	SEG71	395	
211	SEG72	467	
212	SEG73	539	
213	SEG74	611	
214	SEG75	683	
215	SEG76	755	
216	SEG77	827	
217	SEG78	899	
218	SEG79	971	
219	SEG80	1042	
220	SEG81	1114	
221	SEG82	1186	
222	SEG83	1258	
223	SEG84	1330	
224	SEG85	1402	
225	SEG86	1474	
226	SEG87	1546	
227	SEG88	1618	
228	SEG89	1689	
229	SEG90	1761	
230	SEG91	1833	
231	SEG92	1905	
232	SEG93	1977	
233	SEG94	2049	
234	SEG95	2121	
235	SEG96	2193	
236	SEG97	2265	
237	SEG98	2336	
238	SEG99	2408	
239	SEG100	2480	
240	SEG101	2552	

Units: μm

PAD No.	PIN Name	X	Y
241	SEG102	2624	–1246
242	SEG103	2696	
243	SEG104	2768	
244	SEG105	2840	
245	SEG106	2912	
246	SEG107	2983	
247	SEG108	3055	
248	SEG109	3127	
249	SEG110	3199	
250	SEG111	3271	
251	SEG112	3343	
252	SEG113	3415	
253	SEG114	3487	
254	SEG115	3558	
255	SEG116	3630	
256	SEG117	3702	
257	SEG118	3774	
258	SEG119	3846	
259	SEG120	3918	
260	SEG121	3990	
261	SEG122	4062	
262	SEG123	4134	
263	SEG124	4206	
264	SEG125	4277	
265	SEG126	4349	
266	SEG127	4421	
267	SEG128	4493	
268	SEG129	4565	
269	SEG130	4637	
270	SEG131	4709	
271	(NC)	4781	
272	(NC)	4853	
273	(NC)	4924	
274	(NC)	5009	
275	(NC)	5252	–1248
276	(NC)		–1163
277	COM27		–1090
278	(NC)		–1018
279	COM28		–945
280	(NC)		–872

PAD No.	PIN Name	X	Y
281	COM29	5252	–800
282	COM30		–727
283	COM31		–654
284	COM32		–581
285	COM33		–509
286	COM34		–436
287	COM35		–363
288	COM36		–291
289	COM37		–218
290	COM38		–145
291	COM39		–73
292	COM40		0
293	COM41		73
294	COM42		145
295	COM43		218
296	COM44		291
297	COM45		363
298	COM46		436
299	COM47		509
300	COM48		581
301	COM48		654
302	COM50		727
303	COM51		799
304	COM52		872
305	COM53		945
306	(NC)		1017
307	COMS		1090
308	(NC)		1163
309	(NC)		1248

S1D15609***** Pad Center Coordinates

Units: μm

PAD No.	PIN Name	X	Y
1	(NC)	4973	1246
2	FRS	4853	
3	FR	4734	
4	CL	4614	
5	$\overline{DOF}$	4494	
6	TEST0	4375	
7	V_{SS}	4255	
8	$\overline{CS1}$	4136	
9	CS2	4016	
10	V_{DD}	3896	
11	$\overline{RES}$	3777	
12	A0	3657	
13	V_{SS}	3538	
14	$\overline{WR}$, R/$\overline{W}$	3418	
15	$\overline{RD}$, E	3298	
16	V_{DD}	3179	
17	D0	3059	
18	D1	2940	
19	D2	2820	
20	D3	2700	
21	D4	2581	
22	D5	2461	
23	D6, SCL	2342	
24	D7, SI	2222	
25	(NC)	2119	
26	V_{DD}	2030	
27	V_{DD}	1941	
28	V_{DD}	1852	
29	V_{DD}	1763	
30	V_{SS}	1674	
31	V_{SS}	1585	
32	V_{SS}	1496	
33	V_{SS2}	1407	
34	V_{SS2}	1318	
35	V_{SS2}	1229	
36	V_{SS2}	1140	
37	(NC)	1051	
38	V_{OUT}	962	
39	V_{OUT}	873	
40	CAP3–	784	

PAD No.	PIN Name	X	Y
41	CAP3–	695	1246
42	(NC)	605	
43	CAP1+	516	
44	CAP1+	427	
45	CAP1–	338	
46	CAP1–	249	
47	CAP2–	160	
48	CAP2–	71	
49	CAP2+	–18	
50	CAP2+	–107	
51	V_{SS}	–196	
52	V_{SS}	–285	
53	V_{RS}	–374	
54	V_{RS}	–463	
55	V_{DD}	–552	
56	V_{DD}	–641	
57	V_1	–730	
58	V_1	–819	
59	V_2	–908	
60	V_2	–997	
61	(NC)	–1086	
62	V_3	–1176	
63	V_3	–1265	
64	V_4	–1354	
65	V_4	–1443	
66	V_5	–1532	
67	V_5	–1621	
68	(NC)	–1710	
69	V_R	–1799	
70	V_R	–1888	
71	V_{DD}	–1977	
72	V_{DD}	–2066	
73	TEST1	–2155	
74	TEST1	–2244	
75	TEST2	–2333	
76	TEST2	–2422	
77	(NC)	–2511	
78	TEST3	–2600	
79	TEST3	–2689	
80	TEST4	–2778	

PAD No.	PIN Name	X	Y
81	TEST4	–2867	1246
82	(NC)	–2957	
83	V_{DD}	–3059	
84	M/S	–3179	
85	CLS	–3298	
86	V_{SS}	–3418	
87	C86	–3538	
88	P/S	–3657	
89	V_{DD}	–3777	
90	$\overline{HPM}$	–3896	
91	V_{SS}	–4016	
92	IRS	–4136	
93	V_{DD}	–4255	
94	TEST5	–4375	
95	TEST6	–4494	
96	TEST7	–4614	
97	TEST8	–4734	
98	TEST9	–4853	
99	(NC)	–4973	
100	(NC)	–5252	1248
101	(NC)		1163
102	COM25		1090
103	(NC)		1017
104	COM24		945
105	(NC)		872
106	COM23		799
107	COM22		727
108	COM21		654
109	COM20		581
110	COM19		509
111	COM18		436
112	COM17		363
113	COM16		291
114	COM15		218
115	COM14		145
116	COM13		73
117	COM12		0
118	COM11		–73
119	COM10		–145
120	COM9		–218

Units: μm

PAD No.	PIN Name	X	Y
121	COM8	–5252	–291
122	COM7		–363
123	COM6		–436
124	COM5		–509
125	COM4		–581
126	COM3		–654
127	COM2		–727
128	COM1		–800
129	(NC)		–872
130	COM0		–945
131	(NC)		–1018
132	COMS		–1090
133	(NC)		–1163
134	(NC)		–1248
135	(NC)	–5009	–1246
136	(NC)	–4924	
137	(NC)	–4853	
138	(NC)	–4781	
139	SEG0	–4709	
140	SEG1	–4637	
141	SEG2	–4565	
142	SEG3	–4493	
143	SEG4	–4421	
144	SEG5	–4349	
145	SEG6	–4277	
146	SEG7	–4206	
147	SEG8	–4134	
148	SEG9	–4062	
149	SEG10	–3990	
150	SEG11	–3918	
151	SEG12	–3846	
152	SEG13	–3774	
153	SEG14	–3702	
154	SEG15	–3630	
155	SEG16	–3559	
156	SEG17	–3487	
157	SEG18	–3415	
158	SEG19	–3343	
159	SEG20	–3271	
160	SEG21	–3199	

PAD No.	PIN Name	X	Y
161	SEG22	–3127	–1246
162	SEG23	–3055	
163	SEG24	–2983	
164	SEG25	–2912	
165	SEG26	–2840	
166	SEG27	–2768	
167	SEG28	–2696	
168	SEG29	–2624	
169	SEG30	–2552	
170	SEG31	–2480	
171	SEG32	–2408	
172	SEG33	–2336	
173	SEG34	–2265	
174	SEG35	–2193	
175	SEG36	–2121	
176	SEG37	–2049	
177	SEG38	–1977	
178	SEG39	–1905	
179	SEG40	–1833	
180	SEG41	–1761	
181	SEG42	–1689	
182	SEG43	–1618	
183	SEG44	–1546	
184	SEG45	–1474	
185	SEG46	–1402	
186	SEG47	–1330	
187	SEG48	–1258	
188	SEG49	–1186	
189	SEG50	–1114	
190	SEG51	–1042	
191	SEG52	–971	
192	SEG53	–899	
193	SEG54	–827	
194	SEG55	–755	
195	SEG56	–683	
196	SEG57	–611	
197	SEG58	–539	
198	SEG59	–467	
199	SEG60	–395	
200	SEG61	–324	

PAD No.	PIN Name	X	Y
201	SEG62	–252	–1246
202	SEG63	–180	
203	SEG64	–108	
204	SEG65	–36	
205	SEG66	36	
206	SEG67	108	
207	SEG68	180	
208	SEG69	252	
209	SEG70	324	
210	SEG71	395	
211	SEG72	467	
212	SEG73	539	
213	SEG74	611	
214	SEG75	683	
215	SEG76	755	
216	SEG77	827	
217	SEG78	899	
218	SEG79	971	
219	SEG80	1042	
220	SEG81	1114	
221	SEG82	1186	
222	SEG83	1258	
223	SEG84	1330	
224	SEG85	1402	
225	SEG86	1474	
226	SEG87	1546	
227	SEG88	1618	
228	SEG89	1689	
229	SEG90	1761	
230	SEG91	1833	
231	SEG92	1905	
232	SEG93	1977	
233	SEG94	2049	
234	SEG95	2121	
235	SEG96	2193	
236	SEG97	2265	
237	SEG98	2336	
238	SEG99	2408	
239	SEG100	2480	
240	SEG101	2552	

Units: μm

PAD No.	PIN Name	X	Y
241	SEG102	2624	–1246
242	SEG103	2696	
243	SEG104	2768	
244	SEG105	2840	
245	SEG106	2912	
246	SEG107	2983	
247	SEG108	3055	
248	SEG109	3127	
249	SEG110	3199	
250	SEG111	3271	
251	SEG112	3343	
252	SEG113	3415	
253	SEG114	3487	
254	SEG115	3558	
255	SEG116	3630	
256	SEG117	3702	
257	SEG118	3774	
258	SEG119	3846	
259	SEG120	3918	
260	SEG121	3990	
261	SEG122	4062	
262	SEG123	4134	
263	SEG124	4206	
264	SEG125	4277	
265	SEG126	4349	
266	SEG127	4421	
267	SEG128	4493	
268	SEG129	4565	
269	SEG130	4637	
270	SEG131	4709	
271	(NC)	4781	
272	(NC)	4853	
273	(NC)	4924	
274	(NC)	5009	
275	(NC)	5252	–1248
276	(NC)		–1163
277	COM26		–1090
278	(NC)		–1018
279	COM27		–945
280	(NC)		–872

PAD No.	PIN Name	X	Y
281	COM28	5252	–800
282	COM29		–727
283	COM30		–654
284	COM31		–581
285	COM32		–509
286	COM33		–436
287	COM34		–363
288	COM35		–291
289	COM36		–218
290	COM37		–145
291	COM38		–73
292	COM39		0
293	COM40		73
294	COM41		145
295	COM42		218
296	COM43		291
297	COM44		363
298	COM45		436
299	COM46		509
300	COM47		581
301	COM48		654
302	COM49		727
303	COM50		799
304	(NC)		872
305	COM51		945
306	(NC)		1017
307	COMS		1090
308	(NC)		1163
309	(NC)		1248

5. PIN DESCRIPTIONS

Power Supply Pins

Pin Name	I/O	Function	No. of Pins
V_{DD}	Power Supply	Shared with the MPU power supply terminal V_{CC}.	13
V_{SS}	Power Supply	This is a 0V terminal connected to the system GND.	9
V_{SS2}	Power Supply	This is the reference power supply for the step-up voltage circuit for the liquid crystal drive.	4
V_{RS}	Power Supply	This is the externally-input VREG power supply for the LCD power supply voltage regulator. These are only enabled for the models with the VREG external input option.	2
V_1, V_2, V_3, V_4, V_5	Power Supply	This is a multi-level power supply for the liquid crystal drive. The voltage applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on V_{DD}, and must maintain the relative magnitudes shown below. V_{DD} (= V_0) ≥ V_1 ≥ V_2 ≥ V_3 ≥ V_4 ≥ V_5 Master operation: When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.	10

	S1D15605*****		S1D15606*****		S1D15607*****		S1D15608*****		S1D15609*****	
V_1	1/9•V_5	1/7•V_5	1/8•V_5	1/6•V_5	1/6•V_5	1/5•V_5	1/8•V_5	1/6•V_5	1/8•V_5	1/6•V_5
V_2	2/9•V_5	2/7•V_5	2/8•V_5	2/6•V_5	2/6•V_5	2/5•V_5	2/8•V_5	2/6•V_5	2/8•V_5	2/6•V_5
V_3	7/9•V_5	5/7•V_5	6/8•V_5	4/6•V_5	4/6•V_5	3/5•V_5	6/8•V_5	4/6•V_5	6/8•V_5	4/6•V_5
V_4	8/9•V_5	6/7•V_5	7/8•V_5	5/6•V_5	5/6•V_5	4/5•V_5	7/8•V_5	5/6•V_5	7/6•V_5	5/6•V_5

LCD Power Supply Circuit Terminals

Pin Name	I/O	Function	No. of Pins
CAP1+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.	2
CAP1–	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.	2
CAP2+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.	2
CAP2–	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal.	2
CAP3–	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.	2
V_{OUT}	I/O	DC/DC voltage converter. Connect a capacitor between this terminal and V_{SS2}.	2
V_R	I	Output voltage regulator terminal. Provides the voltage between V_{DD} and V5 through a resistive voltage divider. These are only enabled when the V_5 voltage regulator internal resistors are not used (IRS = LOW). These cannot be used when the V_5 voltage regulator internal resistors are used (IRS = HIGH).	2

System Bus Connection Terminals

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>D7 to D0

(SI)
(SCL)</td><td>I/O</td><td>This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus.
When the serial interface is selected (P/S = LOW), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance.
When the chip select is inactive, D0 to D7 are set to high impedance.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command.
A0 = HIGH: Indicates that D0 to D7 are display data.
A0 = LOW: Indicates that D0 to D7 are display control data.</td><td>1</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>When $\overline{RES}$ is set to LOW, the settings are initialized.
The reset operation is performed by the $\overline{RES}$ signal level.</td><td>1</td></tr>
<tr><td>$\overline{CS1}$
CS2</td><td>I</td><td>This is the chip select signal. When $\overline{CS1}$ = LOW and CS2 = HIGH, then the chip select becomes active, and data/command I/O is enabled.</td><td>2</td></tr>
<tr><td>$\overline{RD}$
(E)</td><td>I</td><td>• When connected to an 8080 MPU, this is active LOW.
This pin is connected to the $\overline{RD}$ signal of the 8080 MPU, and the S1D15605 series data bus is in an output status when this signal is LOW.
• When connected to a 6800 Series MPU, this is active HIGH.
This is the 6800 Series MPU enable clock input terminal.</td><td>1</td></tr>
<tr><td>$\overline{WR}$
(R/$\overline{W}$)</td><td>I</td><td>• When connected to an 8080 MPU, this is active LOW.
This terminal connects to the 8080 MPU $\overline{WR}$ signal. The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal.
• When connected to a 6800 Series MPU:
This is the read/write control signal input terminal.
When R/$\overline{W}$ = HIGH: Read.
When R/$\overline{W}$ = LOW: Write.</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>This is the MPU interface switch terminal.
C86 = HIGH: 6800 Series MPU interface.
C86 = LOW: 8080 MPU interface.</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>This is the parallel data input/serial data input switch terminal.
P/S = HIGH: Parallel data input.
P/S = LOW: Serial data input.
The following applies depending on the P/S status:
<table><tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr><tr><td>HIGH</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$, $\overline{WR}$</td><td></td></tr><tr><td>LOW</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr></table>When P/S = LOW, D0 to D5 are HZ. D0 to D5 may be HIGH, LOW or Open.
$\overline{RD}$ (E) and $\overline{WR}$ (P/$\overline{W}$) are fixed to either HGIH or LOW.
With serial data input, RAM display data reading is not supported.</td><td>1</td></tr>
<tr><td>CLS</td><td>I</td><td>Terminal to select whether or enable or disable the display clock internal oscillator circuit.
CLS = HIGH: Internal oscillator circuit is enabled
CLS = LOW: Internal oscillator circuit is disabled (requires external input)
When CLS = LOW, input the display clock through the CL terminal.
When using the S1D15605 Series as a master or slave, set respective CLS pins at the same level.
<table><tr><th>Display clock</th><th>Master</th><th>Slave</th></tr><tr><td>Built-in oscillator circuit used</td><td>HIGH</td><td>HIGH</td></tr><tr><td>External input</td><td>LOW</td><td>LOW</td></tr></table></td><td>1</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>M/S</td><td>I</td><td>This terminal selects the master/slave operation for the S1D15605 Series chips. Master operation outputs the timing signals that are required for the LCD display, while slave operation inputs the timing signals required for the liquid crystal display, synchronizing the liquid crystal display system.
M/S = HIGH: Master operation
M/S = LOW: Slave operation
The following is true depending on the M/S and CLS status:
<table>
<tr><th>M/S</th><th>CLS</th><th>Oscillator Circuit</th><th>Power Supply Circuit</th><th>CL</th><th>FR</th><th>FRS</th><th>DOF</th></tr>
<tr><td>HIGH</td><td>HIGH
LOW</td><td>Enabled
Disabled</td><td>Enabled
Enabled</td><td>Output
Input</td><td>Output
Output</td><td>Output
Output</td><td>Output
Output</td></tr>
<tr><td>LOW</td><td>HIGH
LOW</td><td>Disabled
Disabled</td><td>Disabled
Disabled</td><td>Input
Input</td><td>Input
Input</td><td>Output
Output</td><td>Input
Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>This is the display clock input terminal
The following is true depending on the M/S and CLS status.
<table>
<tr><th>M/S</th><th>CLS</th><th>CL</th></tr>
<tr><td>HIGH</td><td>HIGH
LOW</td><td>Output
Input</td></tr>
<tr><td>LOW</td><td>HIGH
LOW</td><td>Input
Input</td></tr>
</table>When the S1D15605 Series chips are used in master/slave mode, the various CL terminals must be connected.</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>This is the liquid crystal alternating current signal I/O terminal.
M/S = HIGH: Output
M/S = LOW: Input
When the S1D15605 Series chip is used in master/slave mode, the various FR terminals must be connected.</td><td>1</td></tr>
<tr><td>$\overline{DOF}$</td><td>I/O</td><td>This is the liquid crystal display blanking control terminal.
M/S = HIGH: Output
M/S = LOW: Input
When the S1D15605 Series chip is used in master/slave mode, the various $\overline{DOF}$ terminals must be connected.</td><td>1</td></tr>
<tr><td>FRS</td><td>O</td><td>This is the output terminal for the static drive.
This terminal is only enabled when the static indicator display is ON when in master operation mode, and is used in conjunction with the FR terminal.</td><td>1</td></tr>
<tr><td>IRS</td><td>I</td><td>This terminal selects the resistors for the V_5 voltage level adjustment.
IRS = HIGH: Use the internal resistors
IRS = LOW: Do not use the internal resistors. The V_5 voltage level is regulated by an external resistive voltage divider attached to the VR terminal.
This pin is enabled only when the master operation mode is selected.
It is fixed to either HIGH or LOW when the slave operation mode is selected.</td><td>1</td></tr>
<tr><td>$\overline{HPM}$</td><td>I</td><td>This is the power control terminal for the power supply circuit for liquid crystal drive.
$\overline{HPM}$ = HIGH: Normal mode
$\overline{HPM}$ = LOW: High power mode
This pin is enabled only when the master operation mode is selected.
It is fixed to either HIGH or LOW when the slave operation mode is selected.</td><td>1</td></tr>
</table>

Liquid Crystal Drive Terminals

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>SEG0
to
SEG131</td><td>O</td><td>These are the liquid crystal segment drive outputs. Through a combination of the contents of the display RAM and with the FR signal, a single level is selected from V_{DD}, V_2, V_3, and V_5.
<table>
<tr><th>RAM DATA</th><th>FR</th><th colspan="2">Output Voltage</th></tr>
<tr><td></td><td></td><td>Normal Display</td><td>Reverse Display</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>V_{DD}</td><td>V_2</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>V_5</td><td>V_3</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td>LOW</td><td>LOW</td><td>V_3</td><td>V_5</td></tr>
<tr><td>Power save</td><td>—</td><td colspan="2">V_{DD}</td></tr>
</table></td><td>132</td></tr>
<tr><td>COM0
to
COMn</td><td>O</td><td>These are the liquid crystal common drive outputs.
<table>
<tr><th>Part No.</th><th>COM</th></tr>
<tr><td>S1D15605*****</td><td>COM 0 ~ COM 63</td></tr>
<tr><td>S1D15606*****</td><td>COM 0 ~ COM 47</td></tr>
<tr><td>S1D15607*****</td><td>COM 0 ~ COM 31</td></tr>
<tr><td>S1D15608*****</td><td>COM 0 ~ COM 53</td></tr>
<tr><td>S1D15609*****</td><td>COM 0 ~ COM 51</td></tr>
</table>
<table>
<tr><th>Part No.</th><th>No. of pins</th></tr>
<tr><td>S1D15605*****</td><td>64</td></tr>
<tr><td>S1D15606*****</td><td>48</td></tr>
<tr><td>S1D15607*****</td><td>32</td></tr>
<tr><td>S1D15608*****</td><td>54</td></tr>
<tr><td>S1D15609*****</td><td>52</td></tr>
</table>
Through a combination of the contents of the scan data and with the FR signal, a single level is selected from V_{DD}, V_1, V_4, and V_5.
<table>
<tr><th>Scan Data</th><th>FR</th><th>Output Voltage</th></tr>
<tr><td>HIGH</td><td>HIGH</td><td>V_5</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>V_{DD}</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>V_1</td></tr>
<tr><td>LOW</td><td>LOW</td><td>V_4</td></tr>
<tr><td>Power Save</td><td>—</td><td>V_{DD}</td></tr>
</table></td><td></td></tr>
<tr><td>COMS</td><td>O</td><td>These are the COM output terminals for the indicator. Both terminals output the same signal.
Leave these open if they are not used.
When in master/slave mode, the same signal is output by both master and slave.</td><td>2</td></tr>
</table>

Test Terminals

Pin Name	I/O	Function	No. of Pins
TEST0 to 9	I/O	These are terminals for IC chip testing. TEST0 to 4 and 7 to 9 should be open, TEST 5 and 6 should be fixed to HIGH.	14

Total: 288 pins for the S1D15605*****.
272 pins for the S1D15606*****.
256 pins for the S1D15607*****.
278 pins for the S1D15608*****.
276 pins for the S1D15609*****.

6. DESCRIPTION OF FUNCTIONS

The MPU Interface

Selecting the Interface Type

With the S1D15605 Series chips, data transfers are done through an 8-bit bi-directional data bus (D7 to D0) or through a serial data input (SI). Through selecting the P/S terminal polarity to the HIGH or LOW it is possible to select either parallel data input or serial data input as shown in Table 1.

Table 1

P/S	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5~D0
HIGH: Parallel Input	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5~D0
LOW: Serial Input	CS1	CS2	A0	—	—	—	SI	SCL	(HZ)

"—" indicates fixed to either HIGH or to LOW. HZ is in the state of High Impedance.

The Parallel Interface

When the parallel interface has been selected (P/S = HIGH), then it is possible to connect directly to either an 8080-system MPU or a 6800 Series MPU (as shown in Table 2) by selecting the C86 terminal to either HIGH or to LOW.

Table 2

P/S	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7~D0
HIGH: 6800 Series MPU Bus	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D7~D0
LOW: 8080 MPU Bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7~D0

Moreover, data bus signals are recognized by a combination of A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$) signals, as shown in Table 3.

Table 3

Shared	6800 Series	8080 Series		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	1	0	1	Status read
0	0	1	0	Write control data (command)

The Serial Interface

When the serial interface has been selected (P/S = LOW) then when the chip is in active state ($\overline{CS1}$ = LOW and CS2 = HIGH) the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the eighth serial clock for the processing.
The A0 input is used to determine whether or the serial data input is display data or command data; when A0 = HIGH, the data is display data, and when A0 = LOW then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active.
Figure 1 is a serial interface signal chart.

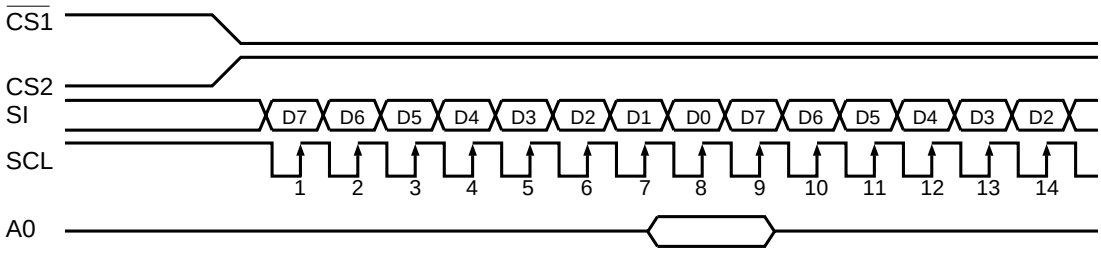


Figure 1

* When the chip is not active, the shift registers and the counter are reset to their initial states.
* Reading is not possible while in serial interface mode.
* Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

The Chip Select

The S1D15605 Series chips have two chip select terminals: $\overline{CS1}$ and CS2. The MPU interface or the serial interface is enabled only when $\overline{CS1}$ = LOW and CS2 = HIGH.
When the chip select is inactive, D0 to D7 enter a high impedance state, and the A0, $\overline{RD}$, and $\overline{WR}$ inputs are inactive. When the serial interface is selected, the shift register and the counter are reset.

Accessing the Display Data RAM and the Internal Registers

Data transfer at a higher speed is ensured since the MPU is required to satisfy the cycle time (t_{CYC}) requirement alone in accessing the S1D15605 Series. Wait time may not be considered.
And, in the S1D15605 Series chips, each time data is sent from the MPU, a type of pipeline process between LSIs is performed through the bus holder attached to the internal data bus.
For example, when the MPU writes data to the display data RAM, once the data is stored in the bus holder, then it is written to the display data RAM before the next data write cycle. Moreover, when the MPU reads the display data RAM, the first data read cycle (dummy) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle.
There is a certain restriction in the read sequence of the display data RAM. Please be advised that data of the specified address is not generated by the read instruction issued immediately after the address setup. This data is generated in data read of the second time. Thus, a dummy read is required whenever the address setup or write cycle operation is conducted.
This relationship is shown in Figure 2.

The Busy Flag

When the busy flag is "1" it indicates that the S1D15605 Series chip is running internal processes, and at this time no command aside from a status read will be received. The busy flag is outputted to D7 pin with the read instruction. If the cycle time (t_{CYC}) is maintained, it is not necessary to check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.

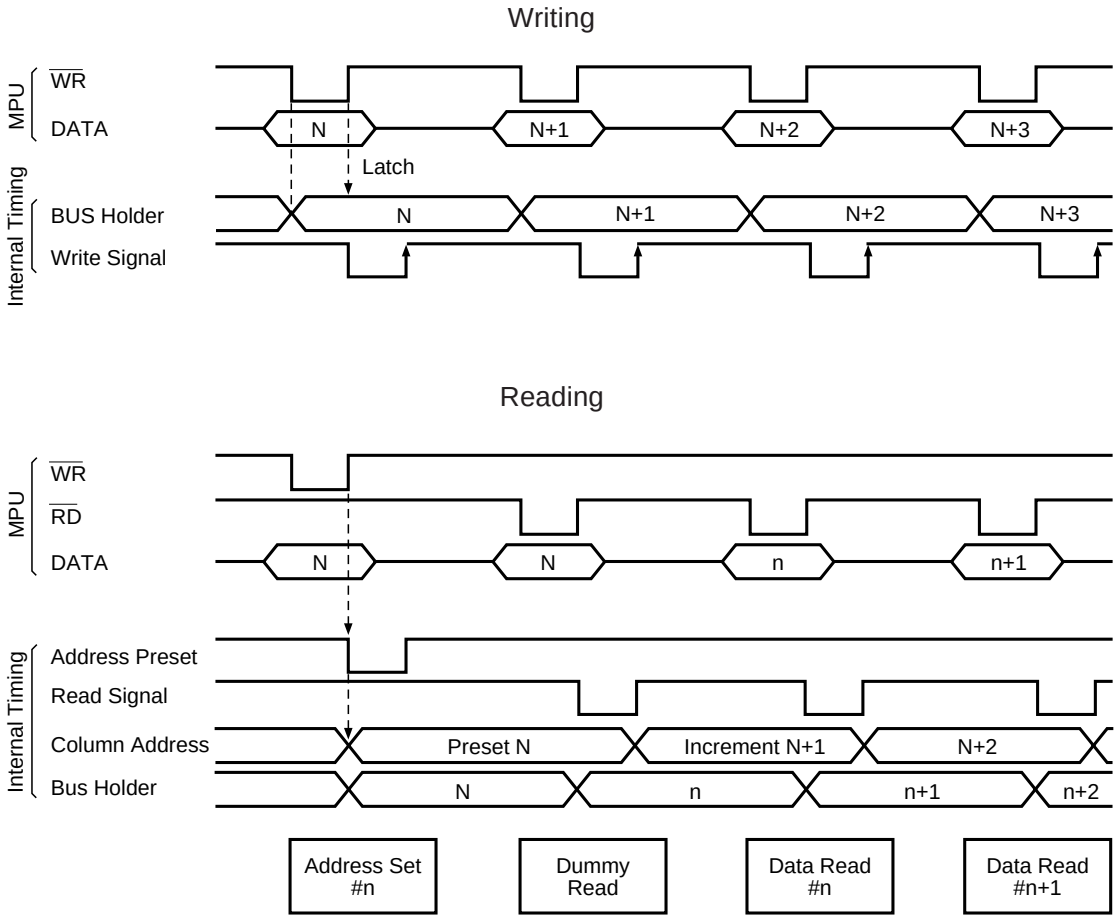


Figure 2

Display Data RAM

Display Data RAM

The display data RAM is a RAM that stores the dot data for the display. It has a 65 (8 page × 8 bit +1) × 132 bit structure. It is possible to access the desired bit by specifying the page address and the column address.
Because, as is shown in Figure 3, the D7 to D0 display data from the MPU corresponds to the liquid crystal display common direction, there are few constraints at the time of display data transfer when multiple S1D15605 series chips are used, thus and display structures can be created easily and with a high degree of freedom.
Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).

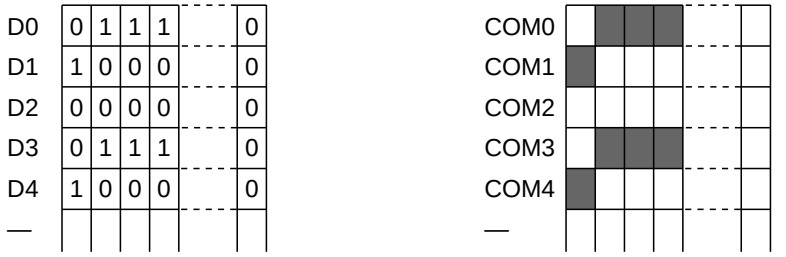


Figure 3

The Page Address Circuit

As shown in Figure 6-4, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.
Page address 8 (D3, D2, D1, D0 = 1, 0, 0, 0) is the page for the RAM region used only by the indicators, and only display data D0 is used.

The Column Addresses

As is shown in Figure 4, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously.
Moreover, the incrementation of column addresses stops with 83H. Because the column address is independent of the page address, when moving, for example, from page 0 column 83H to page 1 column 00H, it is necessary to respecify both the page address and the column address.
Furthermore, as is shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized.

Table 4

SEG Output	SEG0		SEG 131
ADC "0"	0 (H) →	Column Address	→ 83 (H)
(D0) "1"	83 (H) ←	Column Address	← 0 (H)

The Line Address Circuit

The line address circuit, as shown in Table 4, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COM63 output for S1D15605 Series, COM47 output for S1D15606 Series, COM31 output for the S1D15607 Series, COM53 output for S1D15608***** and COM51 output for S1D15609*****) when the common output mode is reversed. The display area is a 65 line area for the S1D15605 Series, a 49 line are for the S1D15606, a 33 line area for the S1D15607 Series , 55 line area for the S1D15608***** and 53 line area for the S1D15609***** from the display start line address.
If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. can be performed.

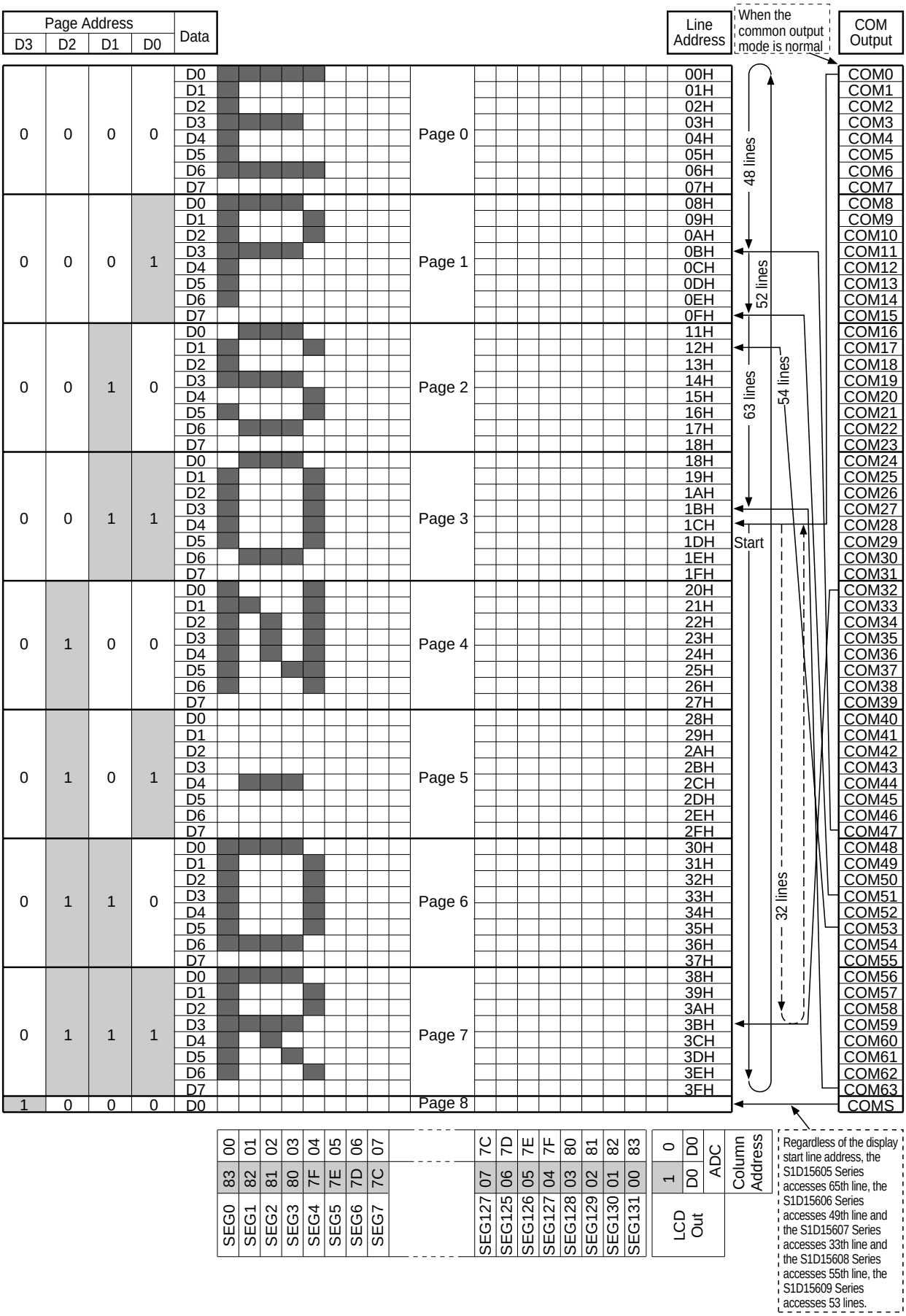

Page Address
D3 D2 D1 D0
Data
Line Address
When the common output mode is normal
COM Output
Page 0
Page 1
Page 2
Page 3
Page 4
Page 5
Page 6
Page 7
Page 8
48 lines
52 lines
63 lines
54 lines
32 lines
Start
COM0 COM1 COM2 COM3 COM4 COM5 COM6 COM7 COM8 COM9 COM10 COM11 COM12 COM13 COM14 COM15 COM16 COM17 COM18 COM19 COM20 COM21 COM22 COM23 COM24 COM25 COM26 COM27 COM28 COM29 COM30 COM31 COM32 COM33 COM34 COM35 COM36 COM37 COM38 COM39 COM40 COM41 COM42 COM43 COM44 COM45 COM46 COM47 COM48 COM49 COM50 COM51 COM52 COM53 COM54 COM55 COM56 COM57 COM58 COM59 COM60 COM61 COM62 COM63 COMS
SEG0 SEG1 SEG2 SEG3 SEG4 SEG5 SEG6 SEG7
SEG127 SEG125 SEG126 SEG127 SEG128 SEG129 SEG130 SEG131
LCD Out
ADC
Column Address
Regardless of the display start line address, the S1D15605 Series accesses 65th line, the S1D15606 Series accesses 49th line and the S1D15607 Series accesses 33th line and the S1D15608 Series accesses 55th line, the S1D15609 Series accesses 53 lines.

Figure 4

The Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM.
Because the display normal/reverse status, display ON/OFF status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the display data RAM itself.

The Oscillator Circuit

This is a CR-type oscillator that produces the display clock. The oscillator circuit is only enabled when M/S = HIGH and CLS = HIGH.
When CLS = LOW the oscillation stops, and the display clock is input through the CL terminal.

Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of accesses to the display data RAM by the MPU. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, there is absolutely no adverse effect (such as flickering) on the display.
Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive wave form using a 2 frame alternating current drive method, as is shown in Figure 5, for the liquid crystal drive circuit.

Two-frame alternating current drive wave form (S1D15605*****)

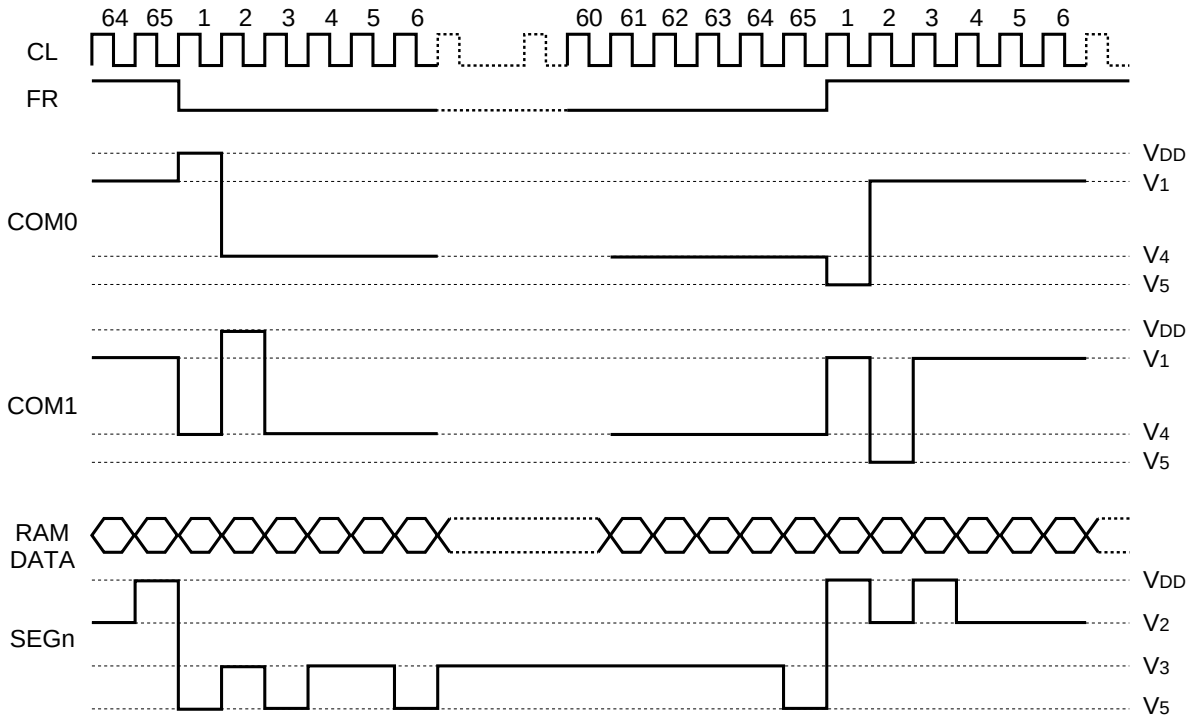


Figure 5

When multiple S1D15605 Series chips are used, the slave chips must be supplied the display timing signals (FR, CL, $\overline{DOF}$) from the master chip[s].
Table 5 shows the status of the FR, CL, and $\overline{DOF}$ signals.

Table 5

Operating Mode		FR	CL	$\overline{DOF}$
Master (M/S = HIGH)	The internal oscillator circuit is enabled (CLS = HIGH)	Output	Output	Output
	The internal oscillator circuit is disabled (CLS = LOW)	Output	Input	Output
Slave (M/S = LOW)	Set the CLS pin to the same level as with the master.	Input	Input	Input
		Input	Input	Input

The Common Output Status Select Circuit

In the S1D15605 Series chips, the COM output scan direction can be selected by the common output status select command. (See Table 6.) Consequently, the constraints in IC layout at the time of LCD module assembly can be minimized.

Table 6

Status	COM Scan Direction				
	S1D15605*****	S1D15606*****	S1D15607*****	S1D15608*****	S1D15609*****
Normal	COM0 → COM63	COM0 → COM47	COM0 → COM31	COM0 → COM53	COM0 → COM51
Reverse	COM63 → COM0	COM47 → COM0	COM31 → COM0	COM53 → COM0	COM51 → COM0

The Liquid Crystal Driver Circuits

These are a 197-channel (S1D15605 Series), a 181-channel (S1D15606 Series) multiplexers 165-channel (S1D15607 Series), 187-channel (S1D15608 Series) and a 185-channel (S1D15609 Series) that generate four voltage levels for driving the liquid crystal. The combination of the display data, the COM scan signal, and the FR signal produces the liquid crystal drive voltage output.
Figure 6 shows examples of the SEG and COM output wave form.

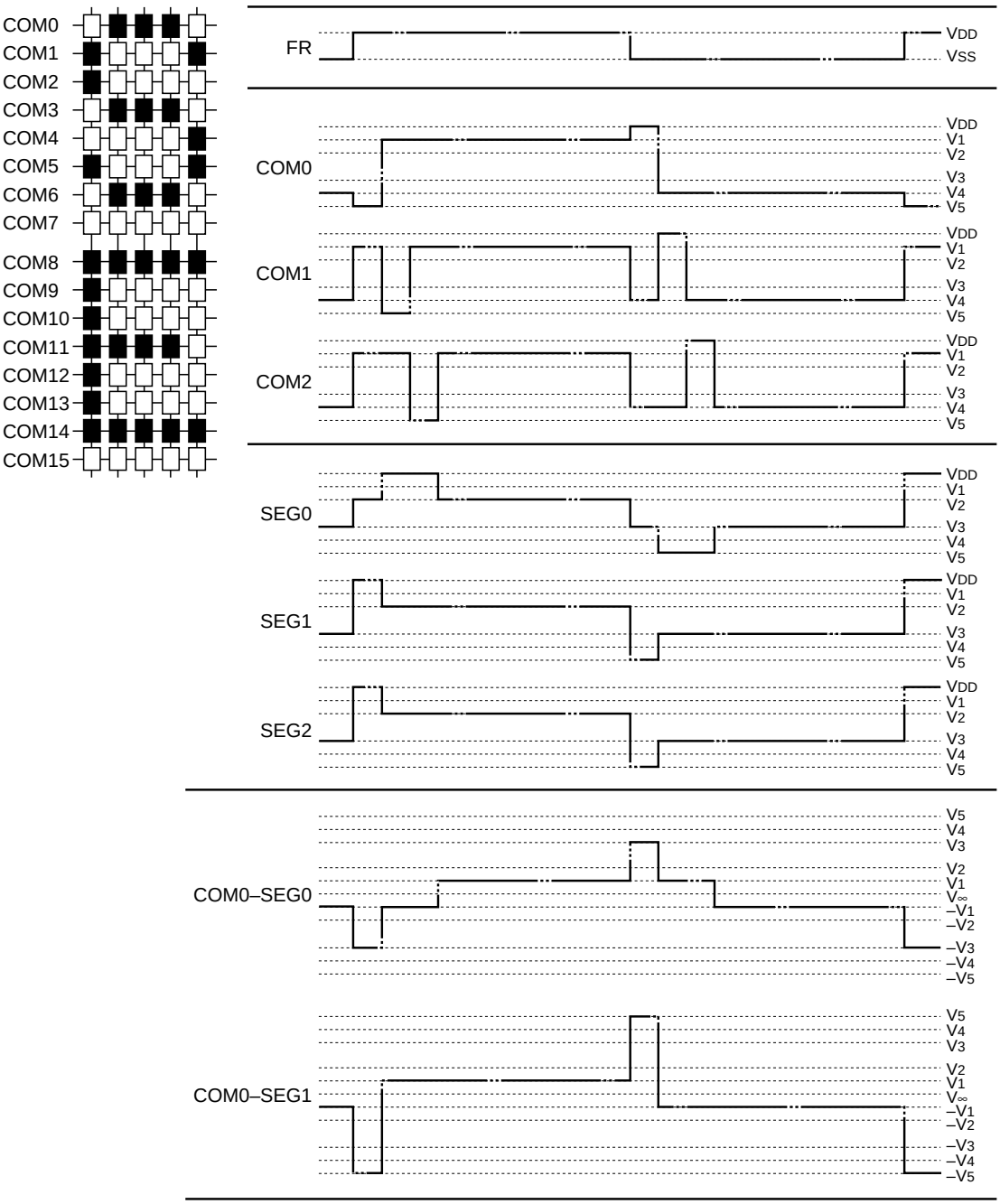

COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15
FR
VDD
VSS
COM0
COM1
COM2
V1
V2
V3
V4
V5
SEG0
SEG1
SEG2
COM0–SEG0
COM0–SEG1
V∞
–V1
–V2
–V3
–V4
–V5

Figure 6

The Power Supply Circuits

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the liquid crystal drivers. They comprise Booster circuits, voltage regulator circuits, and voltage follower circuits. They are only enabled in master operation.

The power supply circuits can turn the Booster circuits, the voltage regulator circuits, and the voltage follower circuits ON of OFF independently through the use of the Power Control Set command. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel. Table 7 shows the Power Control Set Command 3-bit data control function, and Table 8 shows reference combinations.

Table 7 The Control Details of Each Bit of the Power Control Set Command

Item	Status "1"	Status "0"
D2 Booster circuit control bit	ON	OFF
D1 Voltage regulator circuit (V regulator circuit) control bit	ON	OFF
D0 Voltage follower circuit (V/F circuit) control bit	ON	OFF

Table 8 Reference Combinations

Use Settings	D2	D1	D0	Step-up circuit	V regulator circuit	V/F circuit	External voltage input	Step-up voltage system terminal
① Only the internal power supply is used	1	1	1	O	O	O	V_{SS2}	Used
② Only the V regulator circuit and the V/F circuit are used	0	1	1	X	O	O	V_{OUT}, V_{SS2}	Open
③ Only the V/F circuit is used	0	0	1	X	X	O	V_5, V_{SS2}	Open
④ Only the external power supply is used	0	0	0	X	X	X	V_1 to V_5	Open

* The "step-up system terminals" refer CAP1+, CAP1–, CAP2+, CAP2–, and CAP3–.

* While other combinations, not shown above, are also possible, these combinations are not recommended because they have no practical use.

The Step-up Voltage Circuits

Using the step-up voltage circuits equipped within the S1D15605 Series chips it is possible to product a Quad step-up, a Triple step-up, and a Double step-up of the $V_{DD} – V_{SS2}$ voltage levels.

Quad step-up: Connect capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2–, between CAP1+ and CAP3–, and between V_{SS2} and V_{OUT}, to produce a voltage level in the negative direction at the V_{OUT} terminal that is 4 times the voltage level between V_{DD} and V_{SS2}.

Triple step-up: Connect capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2– and between V_{SS2} and V_{OUT}, and short between CAP3– and V_{OUT} to produce a voltage level in the negative direction at the V_{OUT} terminal that is 3 times the voltage difference between V_{DD} and V_{SS2}.

Double step-up: Connect capacitor C1 between CAP1+ and CAP1–, and between V_{SS2} and V_{OUT}, leave CAP2+ open, and short between CAP2–, CAP3– and V_{OUT} to produce a voltage in the negative direction at the V_{OUT} terminal that is twice the voltage between V_{DD} and V_{SS2}.

The step-up voltage relationships are shown in Figure 7.

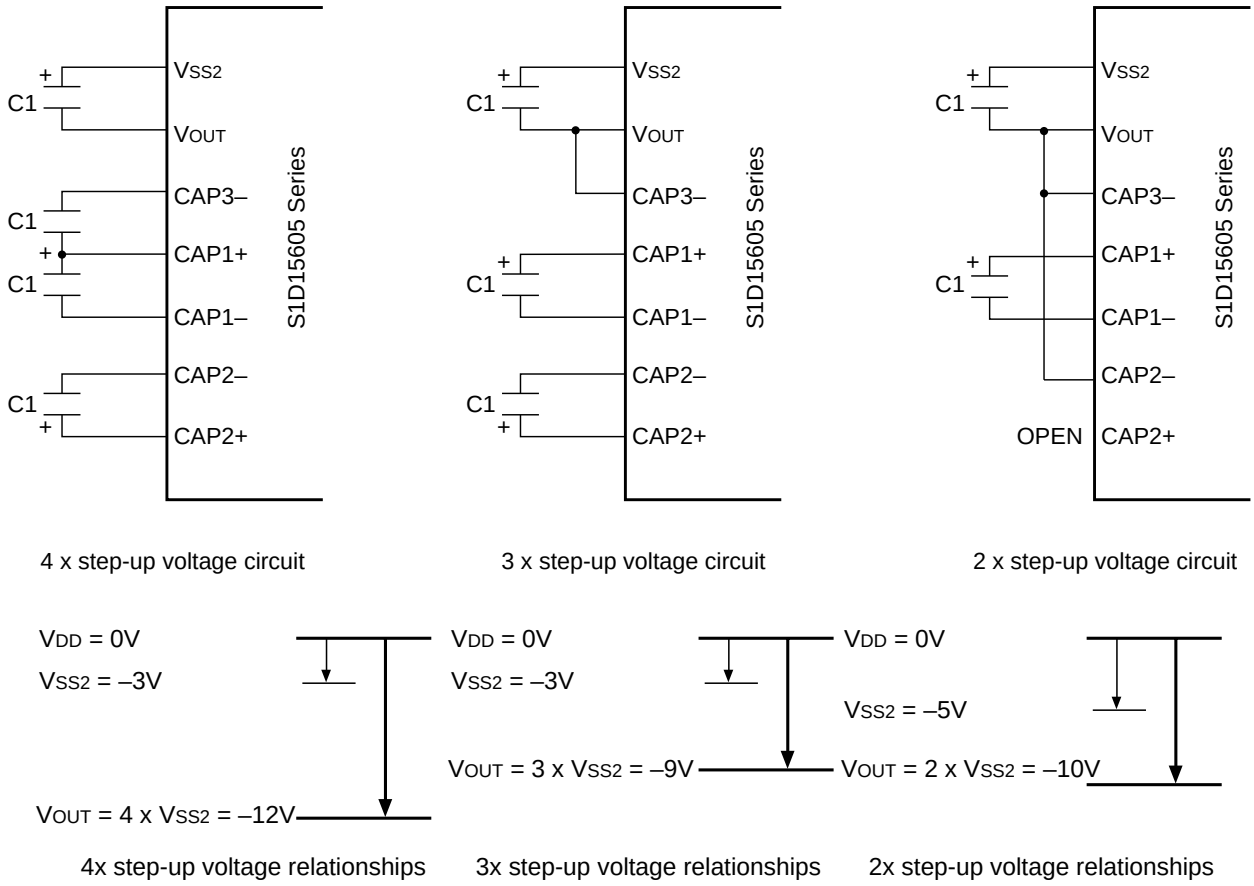


Figure 7

* The V_{SS2} voltage range must be set so that the V_{OUT} terminal voltage does not exceed the absolute maximum rated value.

The Voltage Regulator Circuit

The step-up voltage generated at V_{OUT} outputs the liquid crystal driver voltage V_5 through the voltage regulator circuit.

Because the S1D15605 Series chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V_5 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components.

Moreover, in the S1D15605 Series, three types of thermal gradients have been prepared as V_{REG} options: (1) approximately -0.05%/°C (2) approximately -0.2%/°C, and (3) external input (supplied to the V_{RS} terminal).

(A) When the V_5 Voltage Regulator Internal Resistors Are Used

Through the use of the V_5 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V_5 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V_5 voltage can be calculated using equation A-1 over the range where $|V_5| < |V_{OUT}|$.

$$V_5 = \left(1 + \frac{Rb}{Ra}\right) \cdot V_{EV}$$
$$= \left(1 + \frac{Rb}{Ra}\right) \cdot \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}$$
$$\left[\because V_{EV} = \left(1 - \alpha/162\right) \cdot V_{REG}\right] \qquad \text{(Equation A-1)}$$

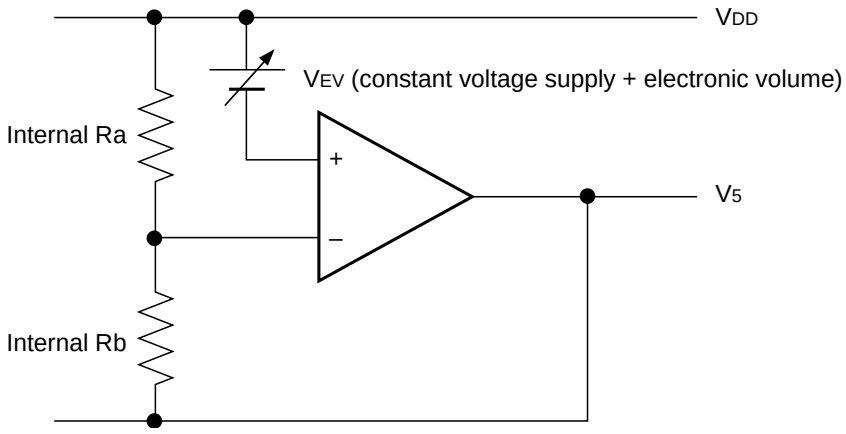


Figure 8

VREG is the IC-internal fixed voltage supply, and its voltage at Ta = 25°C is as shown in Table 9.

Table 9

Equipment Type	Thermal Gradient	Units	VREG	Units
(1) Internal Power Supply	–0.05	[%/°C]	–2.1	[V]
(2) Internal Power Supply	–0.2	[%/°C]	–4.9	[V]
(3) External Input	—	—	VRS	[V]

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume register. Table 10 shows the value for α depending on the electronic volume register settings.

Table 10

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
		⋮				⋮
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

Rb/Ra is the V5 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V5 voltage regulator internal resistor ratio set command. The (1 + Rb/Ra) ratio assumes the values shown in Table 11 depending on the 3-bit data settings in the V5 voltage regulator internal resistor ratio register.

V_5 voltage regulator internal resistance ratio register value and (1 + Rb/Ra) ratio (Reference value)

Table 11

Register			S1D15605*****			S1D15606*****		
			Equipment Type by Thermal Gradient [Units: %/°C]			Equipment Type by Thermal Gradient [Units: %/°C]		
D2	D1	D0	(1) –0.05	(2) –0.2	(3) V_{REG} External Input	(1) –0.05	(2) –0.2	(3) V_{REG} External Input
0	0	0	3.0	1.3	1.5	3.0	1.3	1.5
0	0	1	3.5	1.5	2.0	3.5	1.5	2.0
0	1	0	4.0	1.8	2.5	4.0	1.8	2.5
0	1	1	4.5	2.0	3.0	4.5	2.0	3.0
1	0	0	5.0	2.3	3.5	5.0	2.3	3.5
1	0	1	5.5	2.5	4.0	5.4	2.5	4.0
1	1	0	6.0	2.8	4.5	5.9	2.8	4.5
1	1	1	6.4	3.0	5.0	6.4	3.0	5.0

Register			S1D15607*****			S1D15608*****/S1D15609*****
			Equipment Type by Thermal Gradient [Units: %/°C]			Equipment Type by Thermal Gradient [Units: %/°C]
D2	D1	D0	(1) –0.05	(2) –0.2	(3) V_{REG} External Input	–0.05
0	0	0	3.0	1.3	1.5	3
0	0	1	3.5	1.5	2.0	3.5
0	1	0	4.0	1.8	2.5	4
0	1	1	4.5	2.0	3.0	4.5
1	0	0	5.0	2.3	3.5	5
1	0	1	5.4	2.5	4.0	5.4
1	1	0	5.9	2.8	4.5	5.9
1	1	1	6.4	3.0	5.0	6.4

For the internal resistance ratio, a manufacturing dispersion of up to ±7% should be taken into account. When not within the tolerance, adjust the V_5 voltage by externally mounting Ra and Rb.
Figs. 9, 10, 11 (for S1D15605 Series), 12, 13, 14 (for S1D15606 Series), 15, 16, 17 (for S1D15607 Series), 18 (for S1D15608D00B∗) and Figs. 19 (for S1D15609D00B∗) show V_5 voltage measured by values of the internal resistance ratio resistor for V_5 voltage adjustment and electric volume resister for each temperature grade model, when Ta = 25 °C.

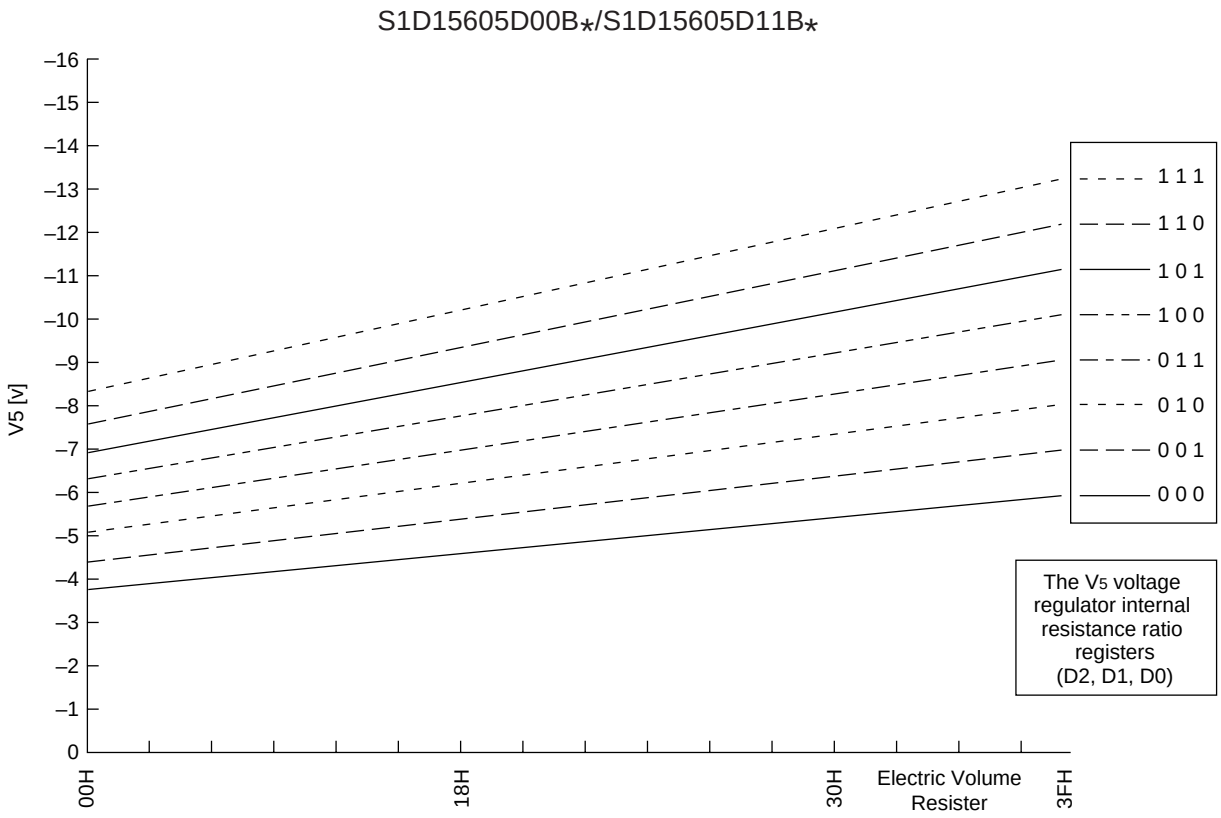


Figure 9: S1D15605D00B*/S1D15605D11B* (1) For Models Where the Thermal Gradient = -0.05%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

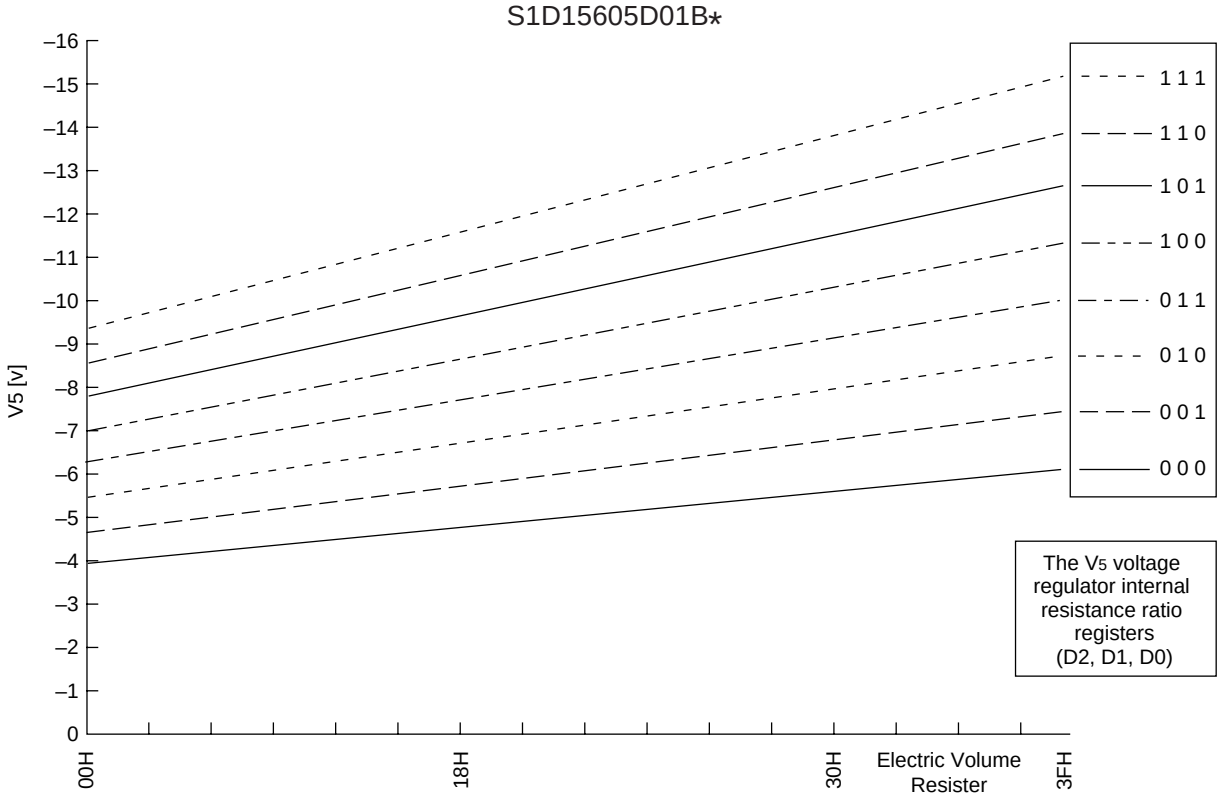


Figure 10: S1D15605D01B* (2) For Models Where the Thermal Gradient = -0.2%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

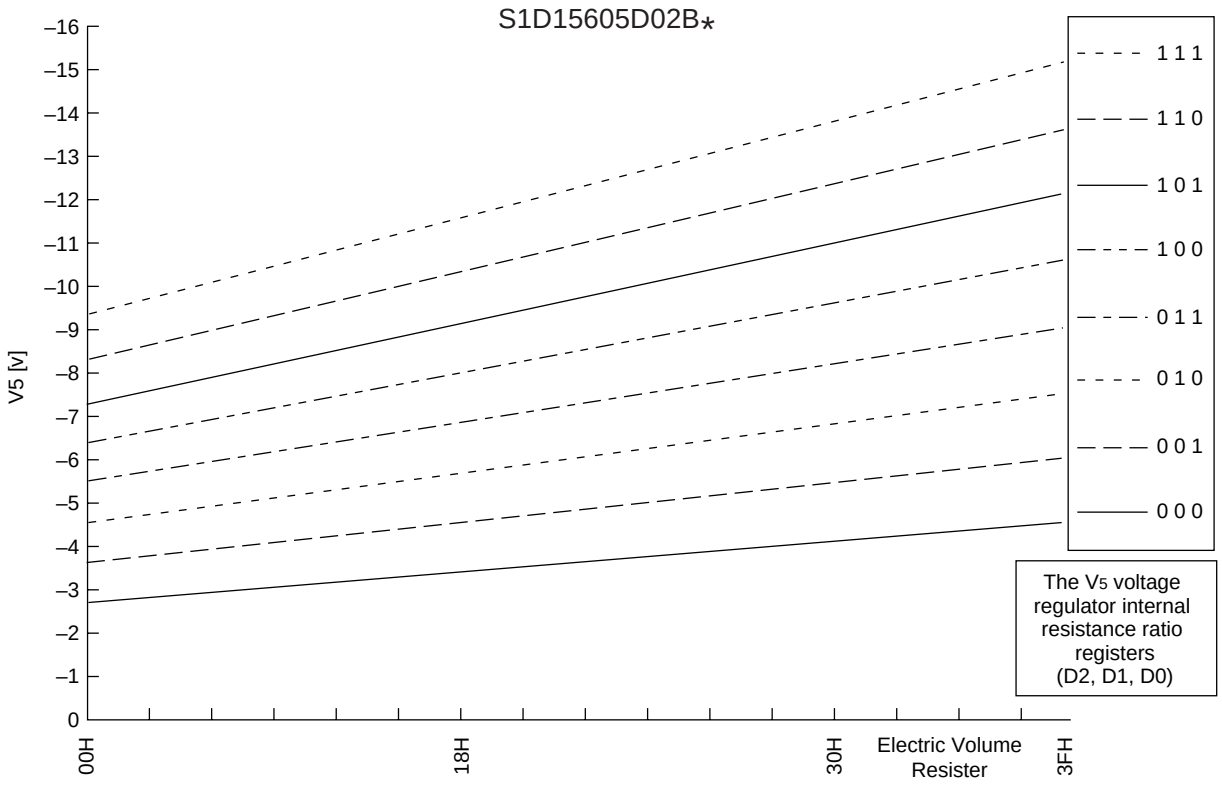


Figure 11: S1D15605D02B* (3) For models with External Input

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

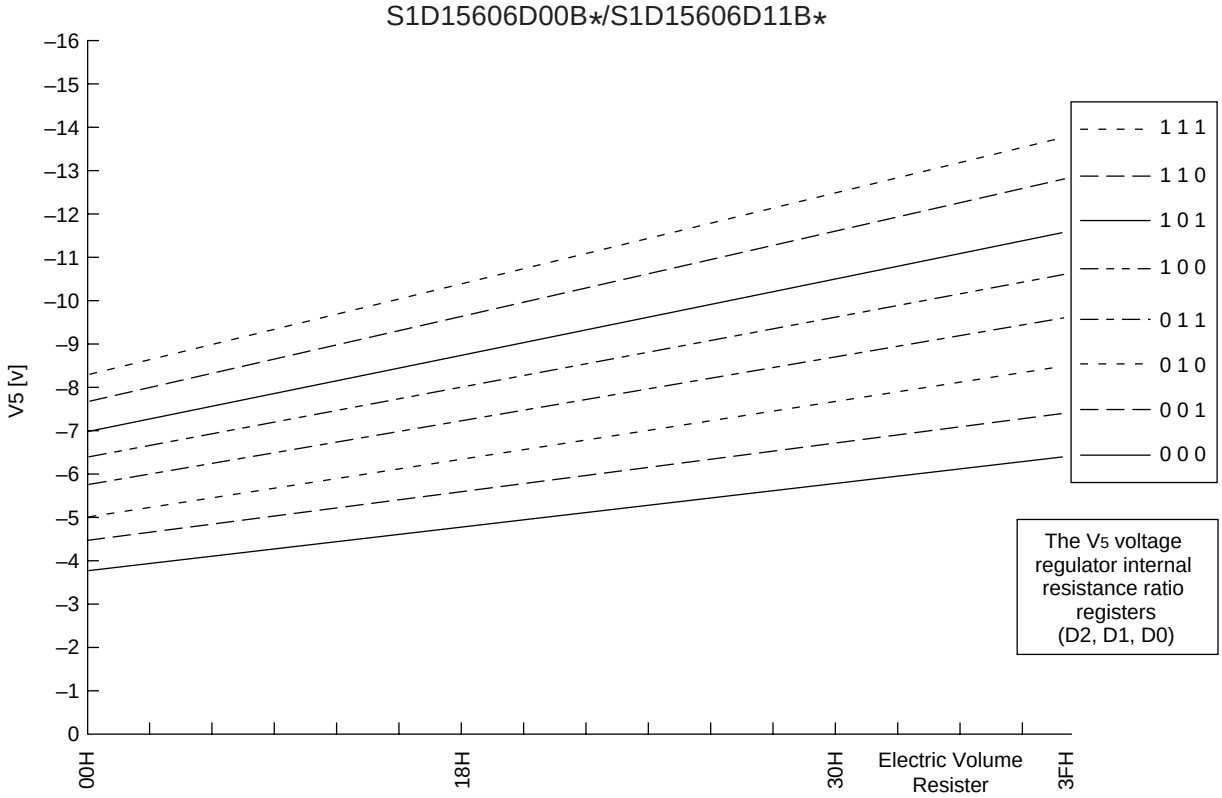


Figure 12: S1D15606D00B*/S1D15606D11B* (1) For Models Where the Thermal Gradient = -0.05%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

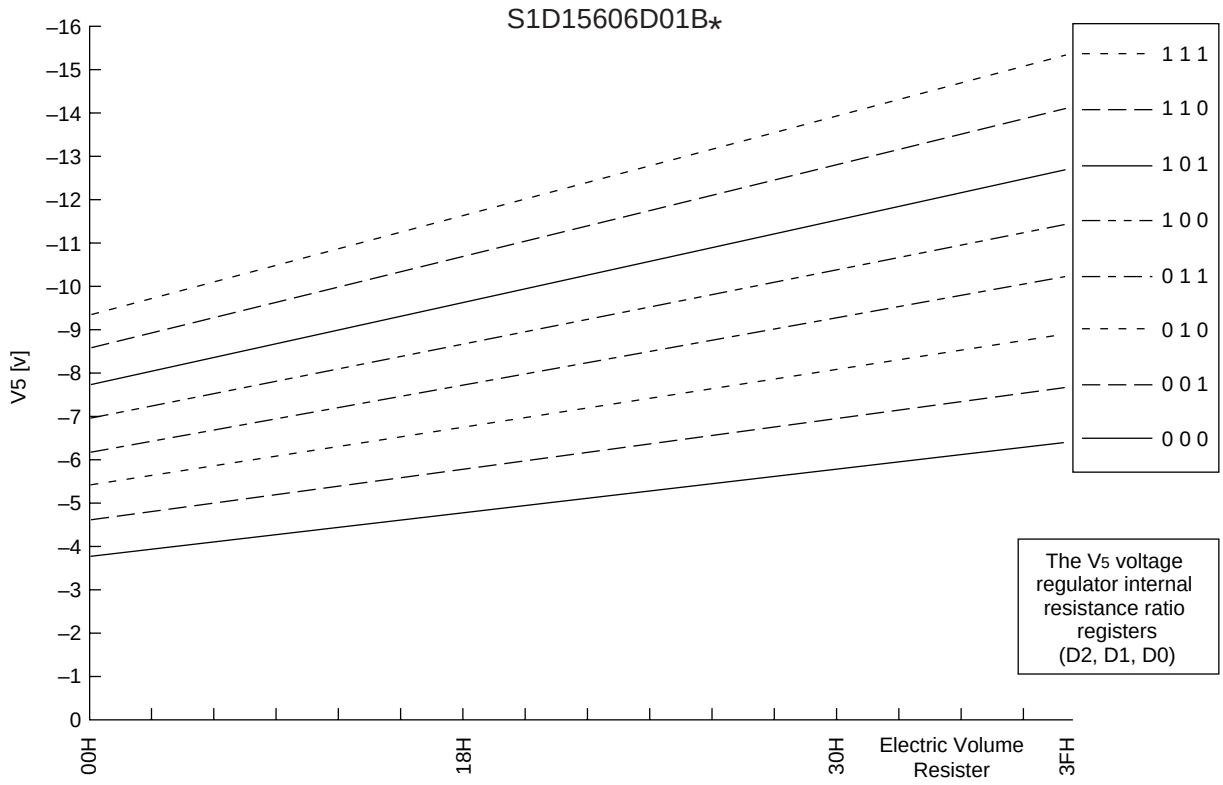


Figure 13: S1D15606D01B* (2) For Models Where the Thermal Gradient = -0.2%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

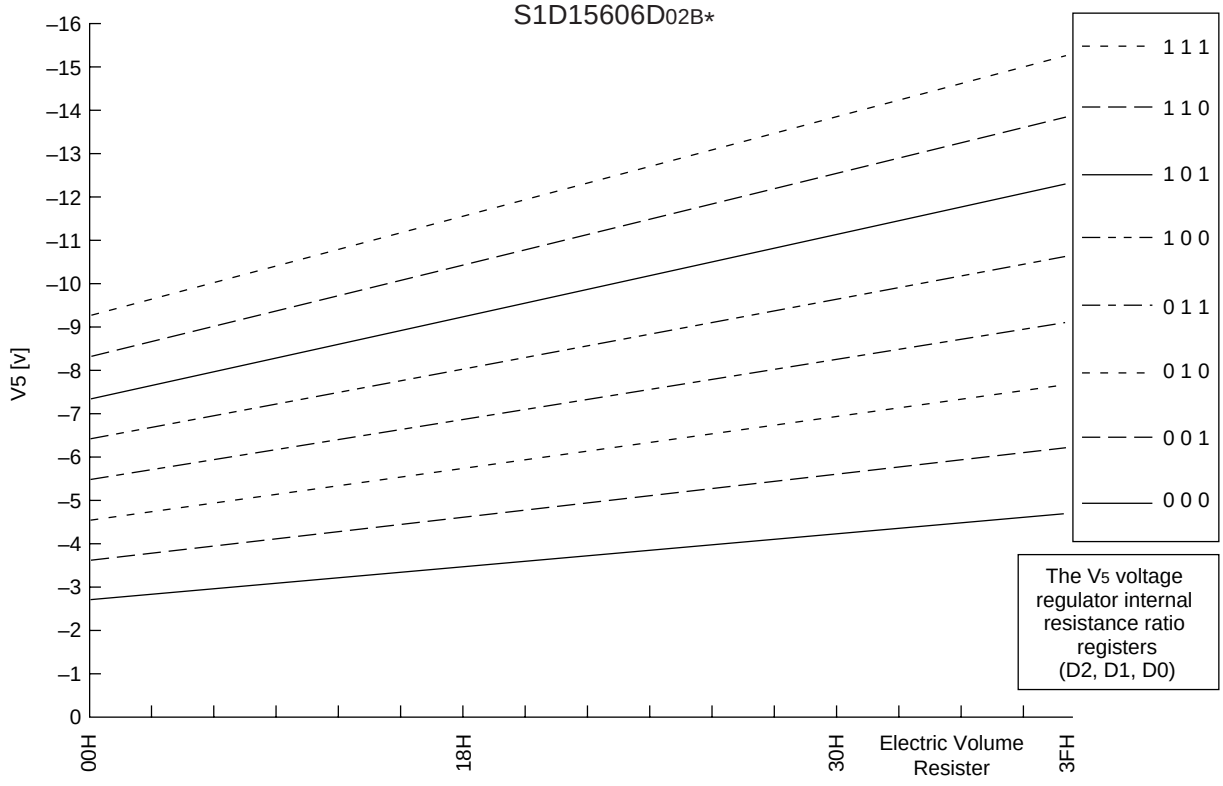


Figure 14: S1D15606D02B* (3) For models with External Input

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

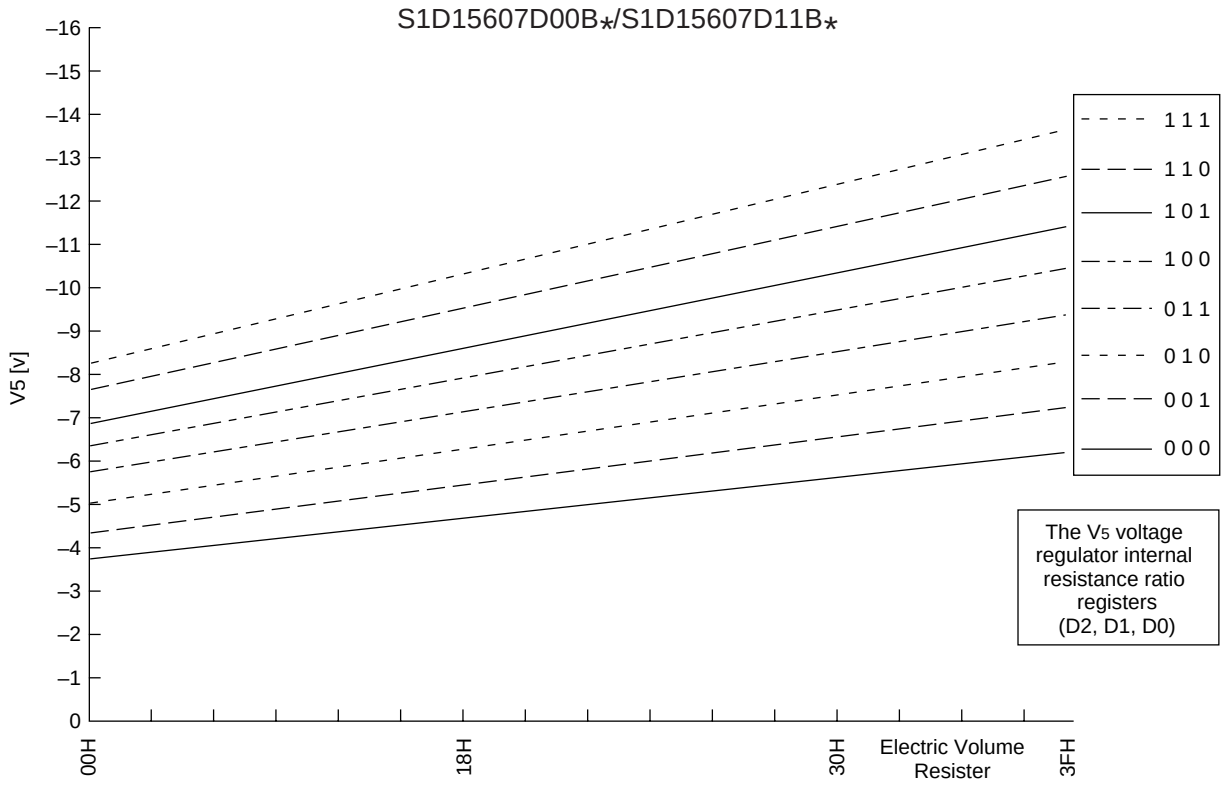


Figure 15: S1D15607D00B*/S1D15607D11B* (1) For Models Where the Thermal Gradient = -0.05%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

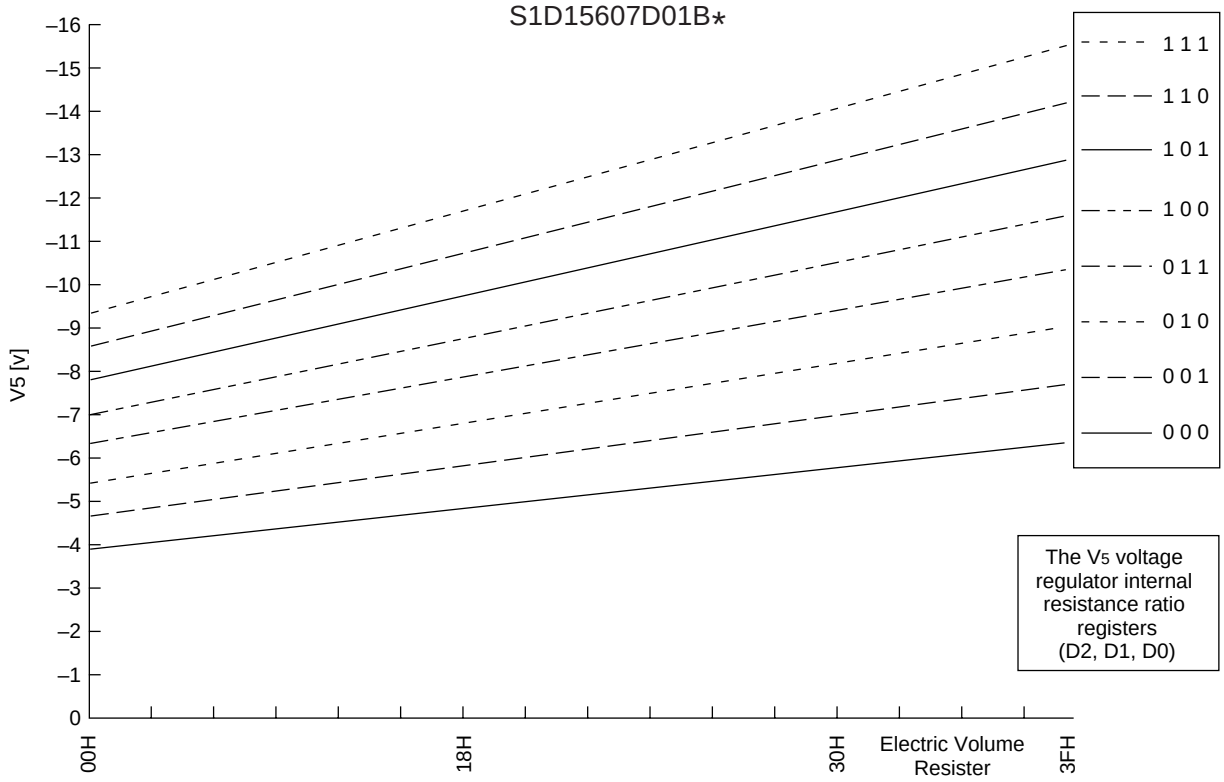


Figure 16: S1D15607D01B* (2) For Models Where the Thermal Gradient = -0.2%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

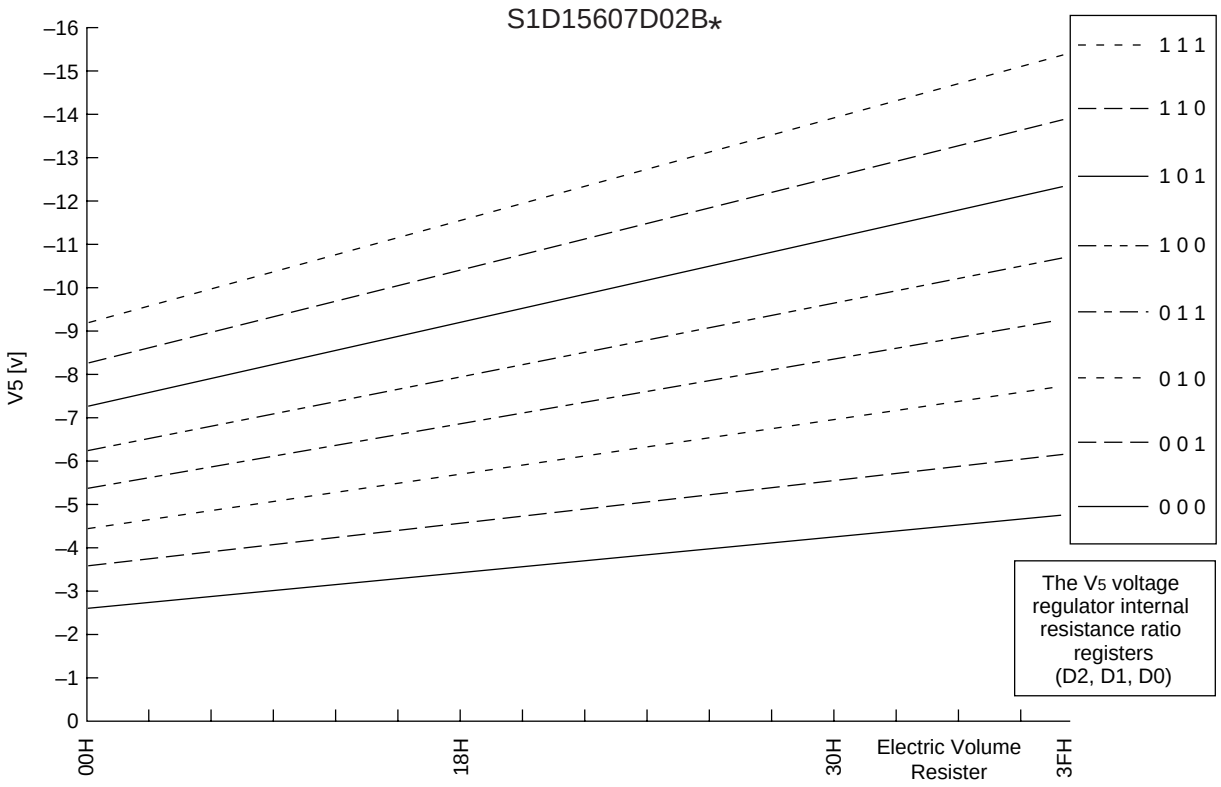


Figure 17: S1D15607D02B* (3) For models with External Input

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

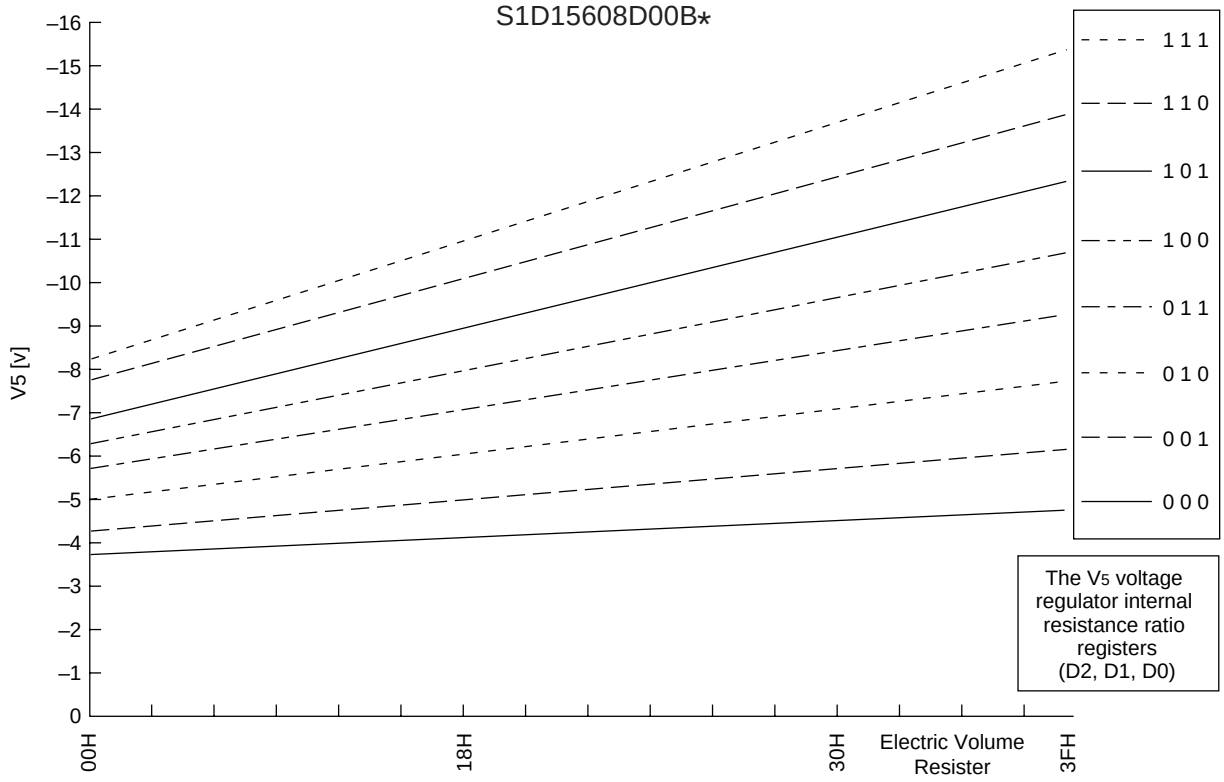


Figure 18: S1D15608D00B* (1) For Models Where the Thermal Gradient = –0.05%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

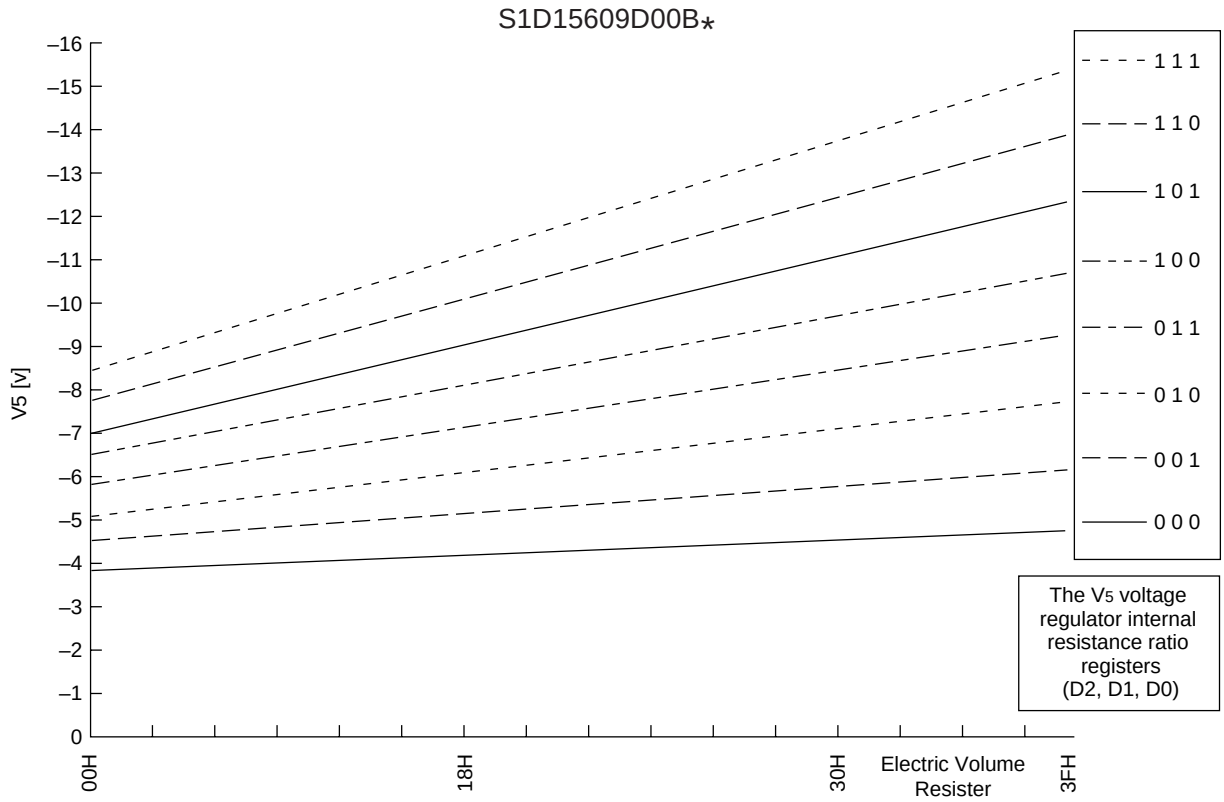


Figure 19: S1D15609D00B* Temperature Gradient = –0.05%/°C Model

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

Setup example: When selecting Ta = 25°C and V_5 = 7 V for an S1D15607 model on which Temperature gradient = –0.05%/°C.
Using Figure 15 and the equation A-1, the following setup is enabled.

Table 12

Contents	Register					
	D5	D4	D3	D2	D1	D0
For V_5 voltage regulator	—	—	—	0	1	0
Electronic Volume	1	0	0	1	0	1

At this time, the variable range and the notch width of the V_5 voltage is, as shown Table 13, as dependent on the electronic volume.

Table 13

V_5	Min.	Typ.	Max.	Units
Variable Range	–8.4 (63 levels)	–6.8 (central value)	–5.1 (0 level)	[V]
Notch width		51		[mV]

(B) When an External Resistance is Used (i.e., The V5 Voltage Regulator Internal Resistors Are Not Used) (1)

The liquid crystal power supply voltage V5 can also be set without using the V5 voltage regulator internal resistors (IRS terminal = LOW) by adding resistors Ra' and Rb' between VDD and VR, and between VR and V5, respectively. When this is done, the use of the electronic volume function makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal power supply voltage V5 through commands. In the range where | V5 | < | VOUT |, the V5 voltage can be calculated using equation B-1 based on the external resistances Ra' and Rb'.

$$V_5 = \left(1+\frac{Rb'}{Ra'}\right)\cdot V_{EV}$$
$$= \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG}$$
$$\left[\because V_{EV} = \left(1-\alpha/162\right)\cdot V_{REG}\right] \qquad \text{(Equation B-1)}$$

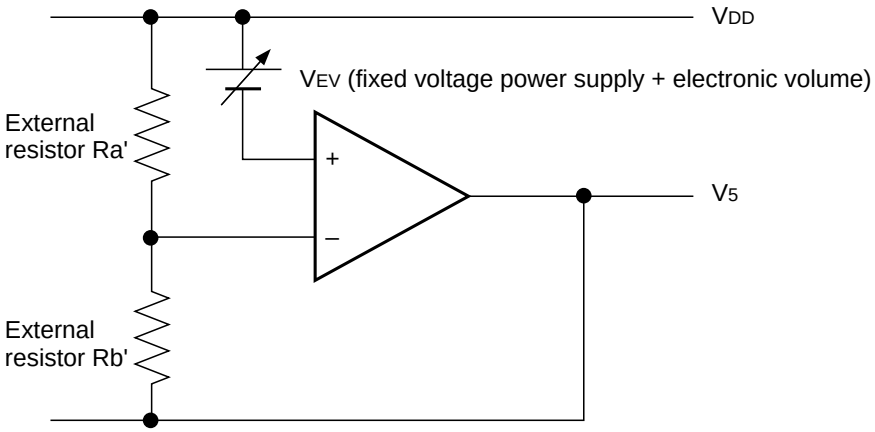


Figure 20

Setup example: When selecting Ta = 25°C and V5 = –7 V for an S1D15607 Series model where the temperature gradient = –0.05%/°C.
When the central value of the electron volume register is (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0), then α = 31 and VREG = –2.1 V so, according to equation B-1,

$$V_5 = \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG}$$
$$-11V = \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{31}{162}\right)\cdot(-2.1) \quad \text{(Equation B-2)}$$

Moreover, when the value of the current running through Ra' and Rb' is set to 5 μA,

$$Ra' + Rb' = 1.4M\Omega \qquad \text{(Equation B-3)}$$

Consequently, by equations B-2 and B-3,

$$\frac{Rb'}{Ra'} = 3.12$$
$$Ra' = 340k\Omega$$
$$Rb' = 1060k\Omega$$

At this time, the V5 voltage variable range and notch width, based on the electron volume function, is as given in Table 14.

Table 14

V5	Min.	Typ.	Max.	Units
Variable Range	–8.6 (63 levels)	–7.0 (central value)	–5.3 (0 level)	[V]
Notch width		52		[mV]

(C) When External Resistors are Used (i.e. The V_5 Voltage Regulator Internal Resistors Are Not Used). (2)

When the external resistor described above are used, adding a variable resistor as well makes it possible to perform fine adjustments on Ra' and Rb', to set the liquid crystal drive voltage V_5. In this case, the use of the electronic volume function makes it possible to control the liquid crystal power supply voltage V_5 by commands to adjust the liquid crystal display brightness. In the range where $|V_5| < |V_{OUT}|$ the V_5 voltage can be calculated by equation C-1 below based on the R_1 and R_2 (variable resistor) and R_3 settings, where R_2 can be subjected to fine adjustments (ΔR_2).

$$V_5 = \left(1 + \frac{R_3 + R_2 - \Delta R_2}{R_1 + \Delta R_2}\right) \cdot V_{EV}$$

$$= \left(1 + \frac{R_3 + R_2 - \Delta R_2}{R_1 + \Delta R_2}\right) \cdot \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \alpha/162\right) \cdot V_{REG}\right] \qquad \text{(Equation C-1)}$$

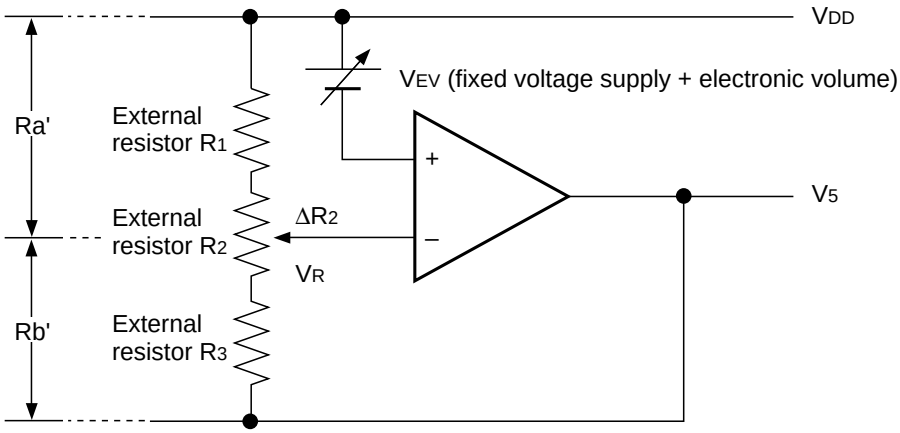


Figure 21

Setup example: When selecting Ta = 25°C and V_5 = –5 to –9 V (using R2) for an S1D15607 model where the temperature gradient = –0.05%/°C.
When the central value for the electronic volume register is set at (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0),

$$\alpha = 31$$

$$V_{REG} = -2.1V$$

so, according to equation C-1, when $\Delta R_2 = 0\ \Omega$, in order to make V_5 = –9 V,

$$-9V = \left(1 + \frac{R_3 + R_2}{R_1}\right) \cdot \left(1 - \frac{31}{162}\right) \cdot (-2.1)$$

(Equation C-2)

When $\Delta R_2 = R_2$, in order to make V = –5 V,

$$-5V = \left(1 + \frac{R_3}{R_1 + R_2}\right) \cdot \left(1 - \frac{31}{162}\right) \cdot (-2.1)$$

(Equation C-3)

Moreover, when the current flowing V_{DD} and V_5 is set to 5 µA,

$$R_1 + R_2 + R_3 = 1.4M\Omega \qquad \text{(Equation C-4)}$$

With this, according to equation C-2, C-3 and C-4,

$$R_1 = 264k\Omega$$

$$R_2 = 211k\Omega$$

$$R_3 = 925k\Omega$$

At this time, the V_5 voltage variable range and notch width based on the electron volume function is as shown in Table 15.

Table 15

V_5	Min.	Typ.	Max.	Units
Variable Range	–8.7 (63 levels)	–7.0 (central value)	–5.3 (0 level)	[V]
Notch width		53		[mV]

* When the V_5 voltage regulator internal resistors or the electronic volume function is used, it is necessary to at least set the voltage regulator circuit and the voltage follower circuit to an operating mode using the power control set commands. Moreover, it is necessary to provide a voltage from V_{OUT} when the Booster circuit is OFF.
* The V_R terminal is enabled only when the V_5 voltage regulator internal resistors are not uesd (i.e. the IRS terminal = LOW). When the V_5 voltage regulator internal resistors are uesd (i.e. when the IRS terminal = HIGH), then the V_R terminal is left open.
* Because the input impedance of the V_R terminal is high, it is necessary to take into consideration short leads, shield cables, etc. to handle noise.

The Liquid Crystal Voltage Generator Circuit

The V_5 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V_1, V_2, V_3, and V_4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V_1, V_2, V_3 and V_4 to the liquid crystal drive circuit. 1/9 bias or 1/7 bias for S1D15605 Series, 1/8 bias or 1/6 bias for S1D15606 Series, 1/6 bias or 1/5 bias for the S1D15607 Series, 1/8 bias or 1/6 bias for S1D15608 Series and 1/8 bias or 1/6 bias for S1D15609 Series can be selected.

High Power Mode

The power supply circuit equipped in the S1D15605 Series chips has very low power consumption (normal mode: $\overline{HPM}$ = HIGH). However, for LCDs or panels with large loads, this low-power power supply may cause display quality to degrade. When this occurs, setting the $\overline{HPM}$ terminal to LOW (high power mode) can improve the quality of the display. We recommend that the display be checked on actual equipment to determine whether or not to use this mode.
Moreover, if the improvement to the display is inadequate even after high power mode has been set, then it is necessary to add a liquid crystal drive power supply externally.

The Internal Power Supply Shutdown Command Sequence

The sequence shown in Figure 22 is recommended for shutting down the internal power supply, first placing the power supply in power saver mode and then turning the power supply OFF.

Sequence	Details (Command, status)	Command address D7	D6	D5	D4	D3	D2	D1	D0	
Step1	Display OFF	1	0	1	0	1	1	1	0	Power saver commands (compound)
↓										
Step2	Display all points ON	1	0	1	0	0	1	0	1	
↓										
End	Internal power supply OFF									

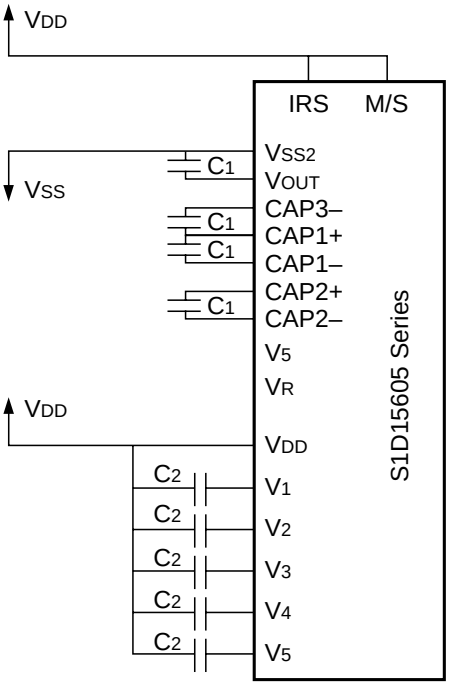
Figure 22

Reference Circuit Examples

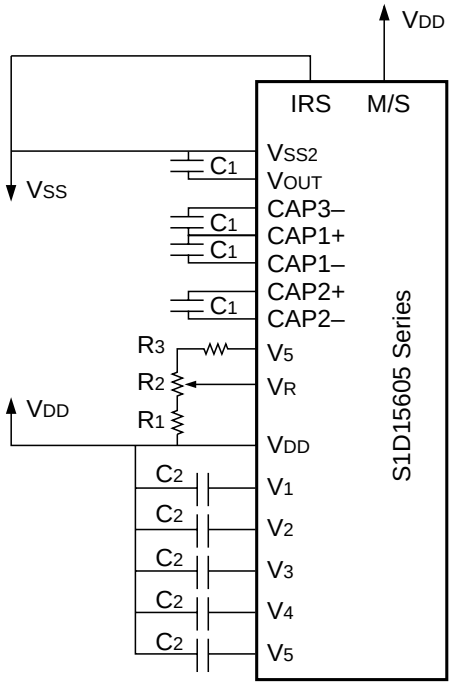
Figure 22 shows reference circuit examples.

① When used all of the step-up circuit, voltage regulating circuit and V/F circuit

(1) When the voltage regulator internal resistor is used.
(Example where $V_{SS2} = V_{SS}$, with 4x step-up)

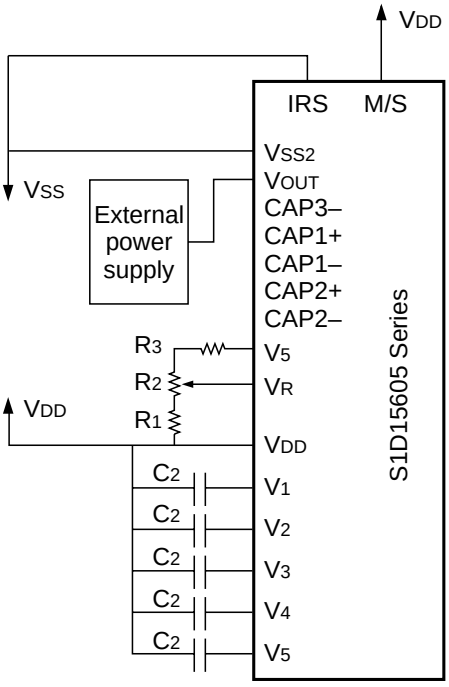


(2) When the voltage regulator internal resistor is not used.
(Example where $V_{SS2} = V_{SS}$, with 4x step-up)

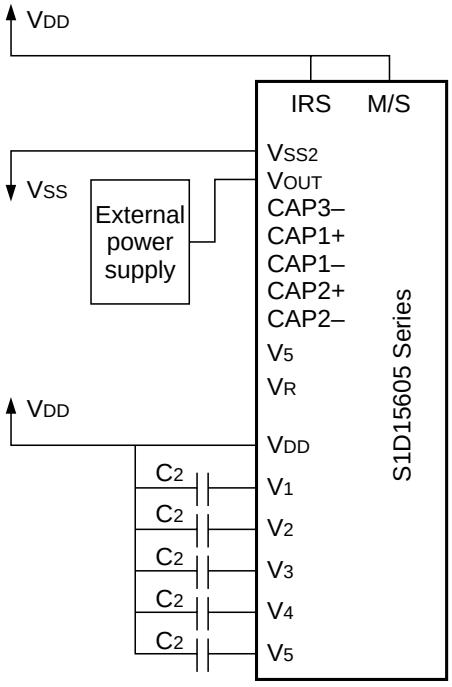


② When the voltage regulator circuit and V/F circuit alone are used

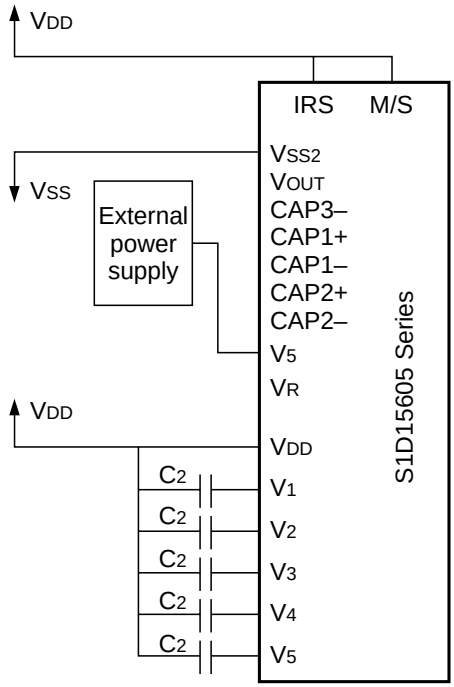
(1) When the V_5 voltage regulator internal resistor is not used.



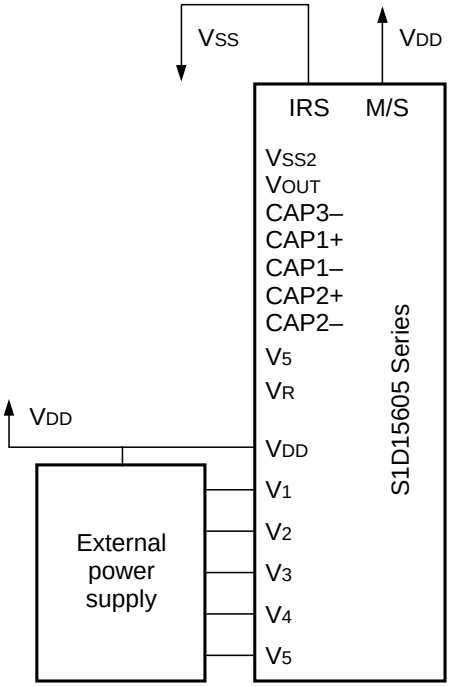
(2) When the V_5 voltage regulator internal resistor is used.



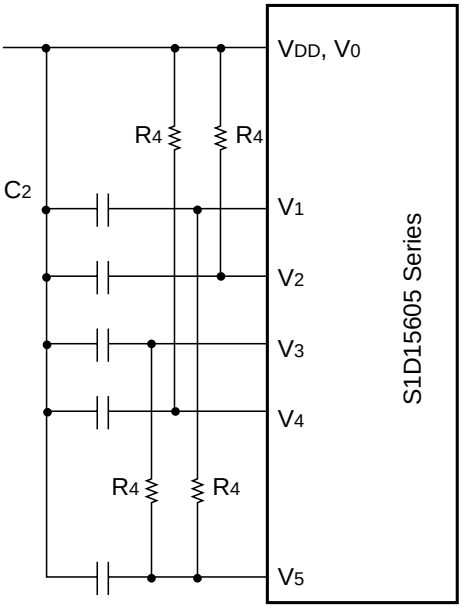
③ When the V/F circuit alone is used



④ When the built-in power is not used



⑤ When the built-in power circuit is used to drive a liquid crystal panel heavily loaded with AC or DC, it is recommended to connect an external resistor to stabilize potentials of V_1, V_2, V_3 and V_4 which are output from the built-in voltage follower.



Examples of shared reference settings
When V_5 can vary between –8 and 12 V

Item	Set value	Units
C_1	1.0 to 4.7	µF
C_2	0.01 to 1.0	µF

Reference set value R_4: 100kΩ ~ 1MΩ
It is recommended to set an optimum resistance value R_4 taking the liquid crystal display and the drive waveform.

Figure 23

* 1 Because the V_R terminal input impedance is high, use short leads and shielded lines.
* 2 C1 and C2 are determined by the size of the LCD being driven. Select a value that will stabilize the liquid crystal drive voltage.

Example of the Process by which to Determine the Settings:

- Turn the voltage regulator circuit and voltage follower circuit ON and supply a voltage to V_{OUT} from the outside.
- Determine C2 by displaying an LCD pattern with a heavy load (such as horizontal stripes) and selecting a C2 that stabilizes the liquid crystal drive voltages (V_1 to V_5). Note that all C2 capacitors must have the same capacitance value.
- Next turn all the power supplies ON and determine C1.

* Precautions when installing the COG

When installing the COG, it is necessary to duly consider the fact that there exists a resistance of the ITO wiring occurring between the driver chip and the externally connected parts (such as capacitors and resistors). By the influence of this resistance, non-conformity may occur with the indications on the liquid crystal display.
Therefore, when installing the COG design the module paying sufficient considerations to the following three points.

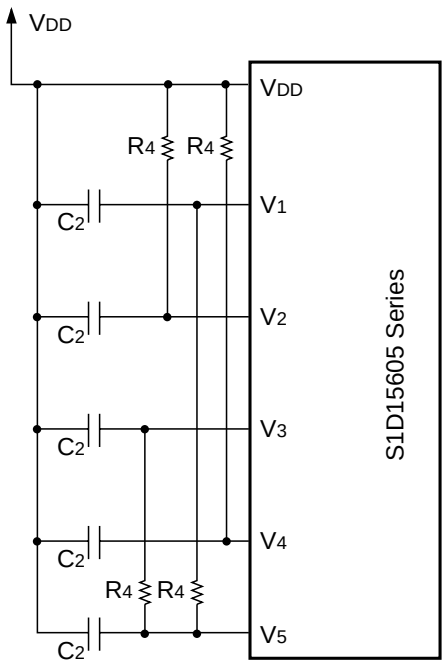
1. Suppress the resistance occurring between the driver chip pin to the externally connected parts as much as possible.
2. Suppress the resistance connecting to the power supply pin of the driver chip.
3. Make various COG module samples with different ITO sheet resistance to select the module with the sheet resistance with sufficient operation margin.

Also, as for this driver IC, pay sufficient attention to the following points when connecting to external parts for the characteristics of the circuit.

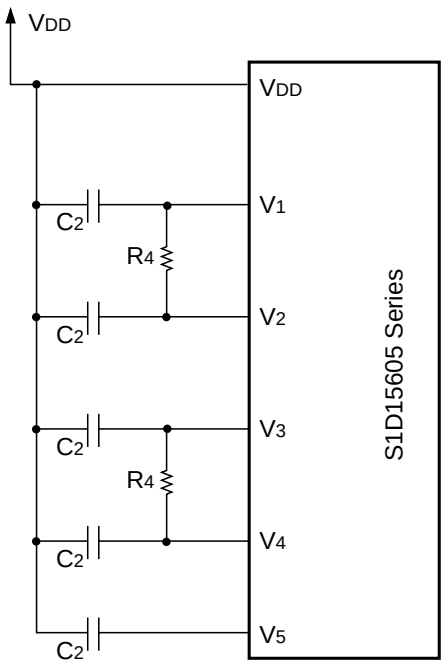
1. Connection to the boosting capacitors The boosting capacitors (the capacitors connecting to respective CAP pins and capacitor being inserted between V_{OUT} and V_{SS2}) of this IC are being switched over by use of the transistor with very low ON-resistance of about 10Ω. However, when installing the COG, the resistance of ITO wiring is being inserted in series with the switching transistor, thus dominating the boosting ability.
   Consequently, the boosting ability will be hindered as a result and pay sufficient attention to the wiring to respective boosting capacitors.
2. Connection of the smoothing capacitors for the liquid crystal drive
   The smoothing capacitors for the liquid crystal driving potentials (V_1. V_2, V_3 and V_4) are indispensable for liquid crystal drives not only for the purpose of mere stabilization of the voltage levels. If the ITO wiring resistance which occurs pursuant to installation of the COG is supplemented to these smoothing capacitors, the liquid crystal driving potentials become unstable to cause non-conformity with the indications of the liquid crystal display. Therefore, when using the COG module, we definitely recommend to connect reinforcing resistors externally.
   Reference value of the resistance is 100kΩ to 1MΩ. Meanwhile, because of the existence of these reinforcing resistors, current consumption will increase.

Indicated below is an exemplary connection diagram of external resistors.
Please make sufficient evaluation work for the display statuses with any connection tests.

Exemplary connection diagram 1.



Exemplary connection diagram 2.



The Reset Circuit

When the $\overline{RES}$ input comes to the LOW level, these LSIs return to the default state. Their default states are as follows:

1. Display OFF
2. Normal display
3. ADC select: Normal (ADC command D0 = LOW)
4. Power control register: (D2, D1, D0) = (0, 0, 0)
5. Serial interface internal register data clear
6. LCD power supply bias rate:
   S1D15605***** ..... 1/9 bias
   S1D15606*****, 15608*****, 15609*****
   ..... 1/8 bias
   S1D15607********* ..... 1/6 bias
7. All-indicator lamps-on OFF (All-indicator lamps ON/OFF command D0 = LOW)
8. Power saving clear
9. V_5 voltage regulator internal resistors Ra and Rb separation
   (In case of S1D15605D11B*, S1D15606D11B*, S1D15607D11B*, S1D15608D11B* and S1D15609D11B*, internal resistors are connected while $\overline{RES}$ is LOW.)
10. Output conditions of SEG and COM terminals
    SEG : V_2/V_3, COM : V_1/V_4
    (In case of S1D15605D11B*, S1D15606D11B*, S1D15607D11B*, S1D15608D11B* and S1D15609D11B*, both the SEG terminal and the COM terminal output the VDA level while $\overline{RES}$ is LOW. In case of other models, the SEG terminal outputs V_2 and the COM terminal outputs V_1 while $\overline{RES}$ is LOW.)
11. Read modify write OFF
12. Static indicator OFF
    Static indicator register : (D1, D2) = (0, 0)
13. Display start line set to first line
14. Column address set to Address 0
15. Page address set to Page 0
16. Common output status normal
17. V_5 voltage regulator internal resistor ratio set mode clear
18. Electronic volume register set mode clear
    Electronic volume register : (D5, D4, D3, D2, D1, D0) = (1, 0. 0, 0, 0, 0)
19. Test mode clear

On the other hand, when the reset command is used, the above default settings from 11 to 19 are only executed.

When the power is turned on, the IC internal state becomes unstable, and it is necessary to initialize it using the $\overline{RES}$ terminal. After the initialization, each input terminal should be controlled normally.
Moreover, when the control signal from the MPU is in the high impedance, an overcurrent may flow to the IC. After applying a current, it is necessary to take proper measures to prevent the input terminal from getting into the high impedance state.
If the internal liquid crystal power supply circuit is not used on S1D15605D11B*, S1D15606D11B*, S1D15607D11B*, S1D15608D11B* and S1D15609D11B*, it is necessary that $\overline{RES}$ is HIGH when the external liquid crystal power supply is turned on. This IC has the function to discharge V_5 when $\overline{RES}$ is LOW, and the external power supply short-circuits to V_{DD} when $\overline{RES}$ is LOW.
While $\overline{RES}$ is LOW, the oscillator and the display timing generator stop, and the CL, FR, $\overline{FRS}$ and DOF terminals are fixed to HIGH. The terminals D0 to D7 are not affected. The V_{DD} level is output from the SEG and COM output terminals. This means that an internal resistor is connected between V_{DD} and V_5.
When the internal liquid crystal power supply circuit is not used on other models of S1D15605 series, it is necessary that RE is LOWwhen the external liquid crystal power supply is turned on.
While $\overline{RES}$ is LOW, the oscillator works but the display timing generator stops, and the CL, FR, FRS and $\overline{DOF}$ terminals are fixed to HIGH. The terminals D0 to D7 are not affected.

7. COMMANDS

The S1D15605 Series chips identify the data bus signals by a combination of A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$) signals. Command interpretation and execution does not depend on the external clock, but rather is performed through internal timing only, and thus the processing is fast enough that normally a busy check is not required.
In the 8080 MPU interface, commands are launched by inputting a low pulse to the $\overline{RD}$ terminal for reading, and inputting a low pulse to the $\overline{WR}$ terminal for writing. In the 6800 Series MPU interface, the interface is placed in a read mode when an HIGH signal is input to the R/$\overline{W}$ terminal and placed in a write mode when a LOW signal is input to the R/$\overline{W}$ terminal and then the command is launched by inputting a high pulse to the E terminal. (See "10. Timing Characteristics" regarding the timing.) Consequently, the 6800 Series MPU interface is different than the 80x86 Series MPU interface in that in the explanation of commands and the display commands the status read and display data read $\overline{RD}$ (E) becomes "1(H)". In the explanations below the commands are explained using the 8080 Series MPU interface as the example.
When the serial interface is selected, the data is input in sequence starting with D7.
<Explanation of Commands>

(1) Display ON/OFF

This command turns the display ON and OFF.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

When the display OFF command is executed when in the display all points ON mode, power saver mode is entered. See the section on the power saver for details.

(2) Display Start Line Set

This command is used to specify the display start line address of the display data RAM shown in Figure 4. For further details see the explanation of this function in "The Line Address Circuit".

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	0	0	1	0	2
								↓			↓
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

(3) Page Address Set

This command specifies the page address corresponding to the low address when the MPU accesses the display data RAM (see Figure 4). Specifying the page address and column address enables to access a desired bit of the display data RAM. Changing the page address does not accompany a change in the status display. See the page address circuit in the Function Description (page 1–20) for the detail.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
									↓		↓
							0	1	1	1	7
							1	0	0	0	8

(4) Column Address Set

This command specifies the column address of the display data RAM shown in Figure 4. The column address is split into two sections (the higher 4 bits and the lower 4 bits) when it is set (fundamentally, set continuously). Each time the display data RAM is accessed, the column address automatically increments (+1), making it possible for the MPU to continuously read from/write to the display data. The column address increment is topped at 83H. This does not change the page address continuously. See the function explanation in "The Column Address Circuit," for details.

	A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0	Column address
HIGH bits →	0	1	0	0	0	0	1	A7	A6	A5	A4	0	0	0	0	0	0	0	0	0
LOW bits →							0	A3	A2	A1	A0	0	0	0	0	0	0	0	1	1
												0	0	0	0	0	0	1	0	2
	↓	↓																		
												1	0	0	0	0	0	1	0	130
												1	0	0	0	0	0	1	1	131

(5) Status Read

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	When BUSY = 1, it indicates that either processing is occurring internally or a reset condition is in process. While the chip does not accept commands until BUSY = 0, if the cycle time can be satisfied, there is no need to check for BUSY conditions.
ADC	This shows the relationship between the column address and the segment driver. 0: Reverse (column address 131-n ↔ SEG n) 1: Normal (column address n ↔ SEG n) (The ADC command switches the polarity.)
ON/OFF	ON/OFF: indicates the display ON/OFF state. 0: Display ON 1: Display OFF (This display ON/OFF command switches the polarity.)
RESET	This indicates that the chip is in the process of initialization either because of a $\overline{RES}$ signal or because of a reset command. 0: Operating state 1: Reset in progress

(6) Display Data Write

This command writes 8-bit data to the specified display data RAM address. Since the column address is automatically incremented by "1" after the write, the MPU can write the display data.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

(7) Display Data Read

This command reads 8-bit data from the specified display data RAM address. Since the column address is automatically incremented by "1" after the read, the CPU can continuously read multiple-word data. One dummy read is required immediately after the column address has been set. See the function explanation in "Display Data RAM" for the explanation of accessing the internal registers. When the serial interface is used, reading of the display data becomes unavailable.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

(8) ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence between the display RAM data column address and the segment driver output. Thus, sequence of the segment driver output pins may be reversed by the command. See the column address circuit (page 1–20) for the detail. Increment of the column address (by "1") accompanying the reading or writing the display data is done according to the column address indicated in Figure 4.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

(9) Display Normal/Reverse

This command can reverse the lit and unlit display without overwriting the contents of the display data RAM. When this is done the display data RAM contents are maintained.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM Data HIGH LCD ON voltage (normal)
										1	RAM Data LOW LCD ON voltage (reverse)

(10) Display All Points ON/OFF

This command makes it possible to force all display points ON regardless of the content of the display data RAM. The contents of the display data RAM are maintained when this is done. This command takes priority over the display normal/reverse command.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display mode
										1	Display all points ON

When the display is in an OFF mode, executing the display all points ON command will place the display in power save mode. For details, see the (20) Power Save section.

(11) LCD Bias Set

This command selects the voltage bias ratio required for the liquid crystal display. This command can be valid while the V/F circuit of Power Supply circuit is in operation.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Select Status				
											S1D15605*****	S1D15606*****	S1D15607*****	S1D15608*****	S1D15609*****
0	1	0	1	0	1	0	0	0	1	0	1/9 bias	1/8 bias	1/6 bias	1/8 bias	1/8 bias
										1	1/7 bias	1/6 bias	1/5 bias	1/6 bias	1/6 bias

(12) Read/Modify/Write

This command is used paired with the "END" command. Once this command has been input, the display data read command does not change the column address, but only the display data write command increments (+1) the column address. This mode is maintained until the END command is input. When the END command is input, the column address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

* Even in read/modify/write mode, other commands aside from display data read/write commands can also be used. However, the column address set command cannot be used.

- The sequence for cursor display

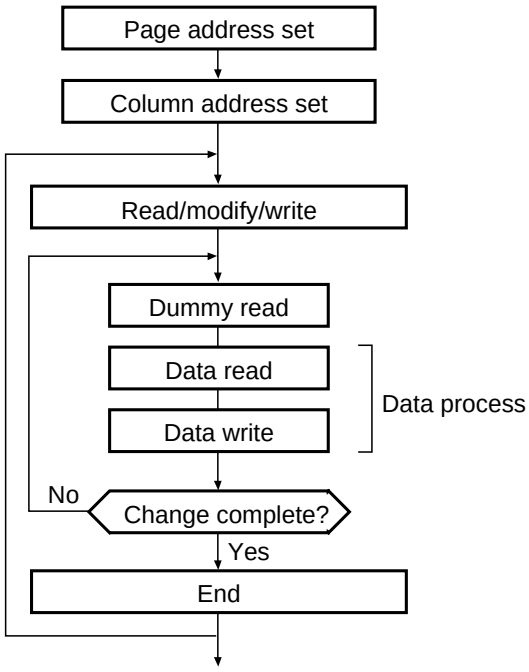


Figure 24

(13) End

This command releases the read/modify/write mode, and returns the column address to the address it was at when the mode was entered.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

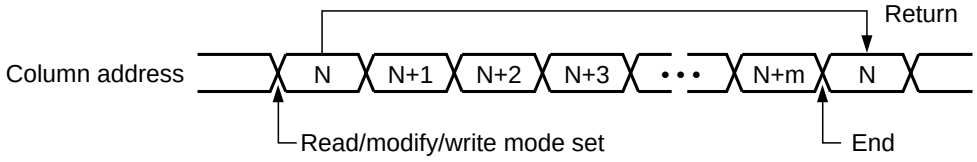


Figure 25

(14) Reset

This command initializes the display start line, the column address, the page address, the common output mode, the V_5 voltage regulator internal resistor ratio, the electronic volume, and the static indicator are reset, and the read/modify/write mode and test mode are released. There is no impact on the display data RAM. See the function explanation in "Reset" for details.
The reset operation is performed after the reset command is entered.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The initialization when the power supply is applied must be done through applying a reset signal to the $\overline{RES}$ terminal. The reset command must not be used instead.

(15) Common Output Mode Select

This command can select the scan direction of the COM output terminal. For details, see the function explanation in "Common Output Mode Select Circuit."

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0		Selected Mode				
												S1D15605*****	S1D15606*****	S1D15607*****	S1D15608*****	S1D15609*****
0	1	0	1	1	0	0	0	*	*	*	Normal	COM0→COM63	COM0→COM47	COM0→COM31	COM0→COM53	COM0→COM51
							1				Reverse	COM63→COM0	COM47→COM0	COM31→COM0	COM53→COM0	COM51→COM0

* Disabled bit

(16) Power Controller Set

This command sets the power supply circuit functions. See the function explanation in "The Power Supply Circuit," for details

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	0	0	1	0	1	0			Booster circuit: OFF
								1			Booster circuit: ON
									0		Voltage regulator circuit: OFF
									1		Voltage regulator circuit: ON
										0	Voltage follower circuit: OFF
										1	Voltage follower circuit: ON

[Translator's Note: the abbreviations explained within these parentheses for V and V/F have been written out in the English translation and are therefore no longer necessary.]

(17) V_5 Voltage Regulator Internal Resistor Ratio Set

This command sets the V_5 voltage regulator internal resistor ratio. For details, see the function explanation is "The Power Supply Circuits."

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									↓		↓
								1	1	0	
								1	1	1	Large

(18) The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal drive voltage V_5 through the output from the voltage regulator circuits of the internal liquid crystal power supply. This command is a two byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

• The Electronic Volume Mode Set

When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

• Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal drive voltage V_5 assumes one of the 64 voltage levels.
When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	| V5 |
0	1	0	*	*	0	0	0	0	0	1	Small
0	1	0	*	*	0	0	0	0	1	0	
0	1	0	*	*	0	0	0	0	1	1	
						↓					↓
0	1	0	*	*	1	1	1	1	1	0	
0	1	0	*	*	1	1	1	1	1	1	Large

* Inactive bit

When the electronic volume function is not used, set this to (1, 0, 0, 0, 0, 0)

• The Electronic Volume Register Set Sequence

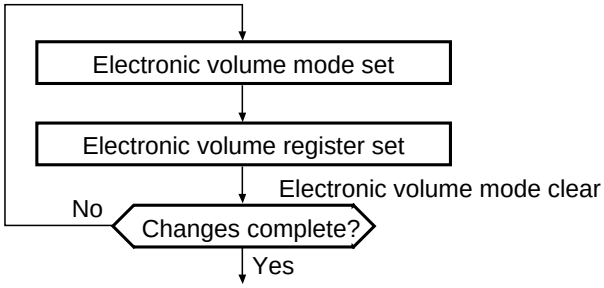


Figure 26

(19) Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands.
This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes.
The static indicator ON command is a double byte command paired with the static indicator register set command, and thus one must execute one after the other. (The static indicator OFF command is a single byte command.)

• Static Indicator ON/OFF

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Static Indicator
0	1	0	1	0	1	0	1	1	0	0	OFF
										1	ON

• Static Indicator Register Set

This command sets two bits of data into the static indicator register, and is used to set the static indicator into a blinking mode.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Indicator Display State
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON (blinking at approximately one second intervals)
									1	0	ON (blinking at approximately 0.5 second intervals)
									1	1	ON (constantly on)

* Disabled bit

• Static Indicator Register Set Sequence

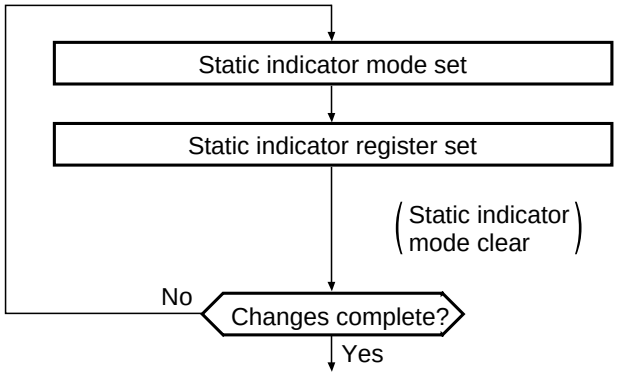


Figure 27

(20) Power Save (Compound Command)

When the display all points ON is performed while the display is in the OFF mode, the power saver mode is entered, thus greatly reducing power consumption.
The power saver mode has two different modes: the sleep mode and the standby mode. When the static indicator is OFF, it is the sleep mode that is entered. When the static indicator is ON, it is the standby mode that is entered.
In the sleep mode and in the standby mode, the display data is saved as is the operating mode that was in effect before the power saver mode was initiated, and the MPU is still able to access the display data RAM.
Refer to figure 28 for power save off sequence.

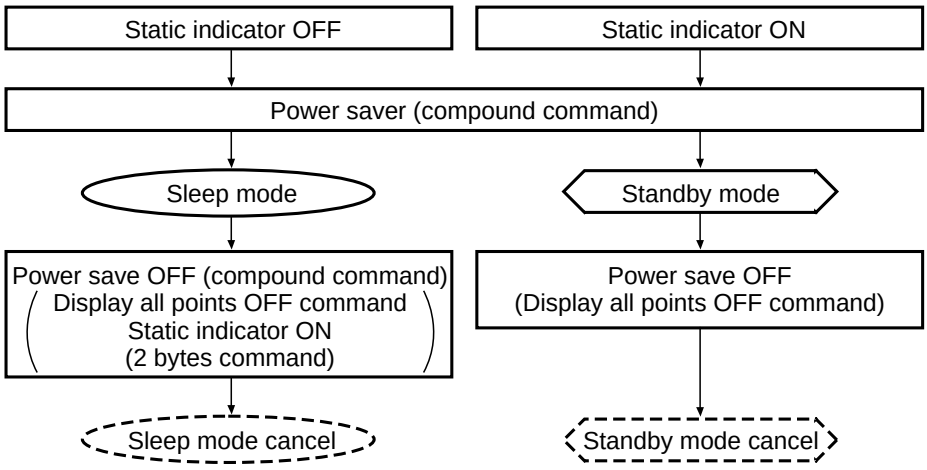


Figure 28

• Sleep Mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:

① The oscillator circuit and the LCD power supply circuit are halted.
② All liquid crystal drive circuits are halted, and the segment in common drive outputs output a VDD level.

• Standby Mode

The duty LCD display system operations are halted and only the static drive system for the indicator continues to operate, providing the minimum required consumption current for the static drive. The internal modes are in the following states during standby mode.

① The LCD power supply circuits are halted. The oscillator circuit continues to operate.
② The duty drive system liquid crystal drive circuits are halted and the segment and common driver outputs output a VDD level. The static drive system does not operate.

When a reset command is performed while in standby mode, the system enters sleep mode.

* When an external power supply is used, it is recommended that the functions of the external power supply circuit be stopped when the power saver mode is started. For example, when the various levels of liquid crystal drive voltage are provided by external resistive voltage dividers, it is recommended that a circuit be added in order to cut the electrical current flowing through the resistive voltage divider circuit when the power saver mode is in effect. The S1D15605 series chips have a liquid crystal display blanking control terminal $\overline{DOF}$. This terminal enters an LOW state when the power saver mode is launched. Using the output of $\overline{DOF}$, it is possible to stop the function of an external power supply circuit.
* When the master is turned on, the oscillator circuit is operable immediately after the powering on.

(21) NOP

Non-OPeration Command

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

(22) Test

This is a command for IC chip testing. Please do not use it. If the test command is used by accident, it can be cleared by applying a LOW signal to the RES input by the reset command or by using an NOP.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

* Inactive bit

Note: The S1D15605 Series chips maintain their operating modes until something happens to change them. Consequently, excessive external noise, etc., can change the internal modes of the S1D15605 Series chip. Thus in the packaging and system design it is necessary to suppress the noise or take measure to prevent the noise from influencing the chip. Moreover, it is recommended that the operating modes be refreshed periodically to prevent the effects of unanticipated noise.

Table 16 Table of S1D15605 Series Commands

	Command	Command Code A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2)	Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3)	Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4)	Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address.
	Column address set lower bit	0	1	0	0	0	0	0	Least significant column address				Sets the least significant 4 bits of the display RAM column address.
(5)	Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6)	Display data write	1	1	0	Write data								Writes to the display RAM
(7)	Display data read	1	0	1	Read data								Reads from the display RAM
(8)	ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9)	Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10)	Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11)	LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio S1D15605***** .. 0: 1/9, 1: 1/7 S1D15606***** /S1D15608***** /S1D15609***** . 0: 1/8, 1: 1/6 S1D15607***** .. 0: 1/6, 1: 1/5
(12)	Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13)	End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14)	Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15)	Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction, 1: reverse direction
(16)	Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17)	V_5 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio (Rb/Ra) mode
(18)	Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	
	Electronic volume register set	0	1	0	*	*	Electronic volume value						Set the V_5 output voltage electronic volume register
(19)	Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1	0: OFF, 1: ON
	Static indicator register set	0	1	0	*	*	*	*	*	*	Mode		Set the flashing mode
(20)	Power saver												Display OFF and display all points ON compound command
(21)	NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(22)	Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

(Note) *: disabled data

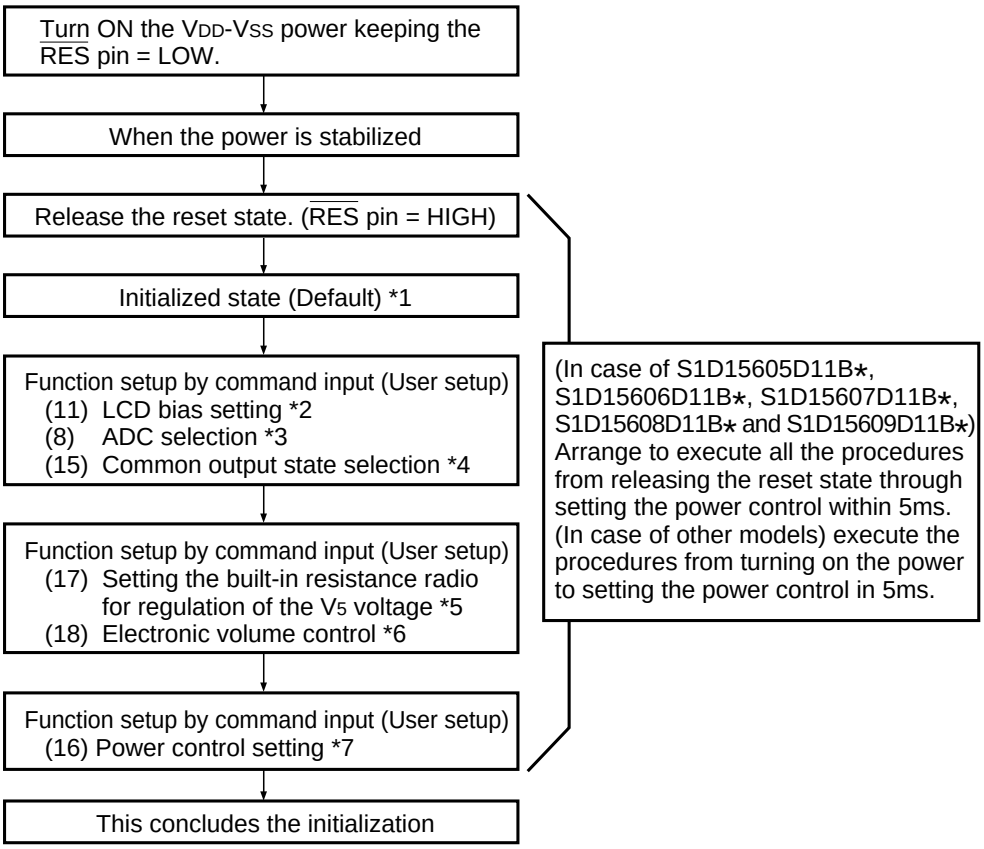
8. COMMAND DESCRIPTION

Instruction Setup: Reference (reference)

(1) Initialization

Note: With this IC, when the power is applied, LCD driving non-selective potentials V_2 and V_3 (SEG pin) and V_1 and V_4 (COM pin) are output through the LCD driving output pins SEG and COM. When electric charge is remaining in the smoothing capacitor connecting between the LCD driving voltage output pins (V_1 ~ V_5) and the V_{DD} pin, the picture on the display may become totally dark instantaneously when the power is turned on. To avoid occurrence of such a failure, we recommend the following flow when turning on the power.

① When the built-in power is being used immediately after turning on the power:

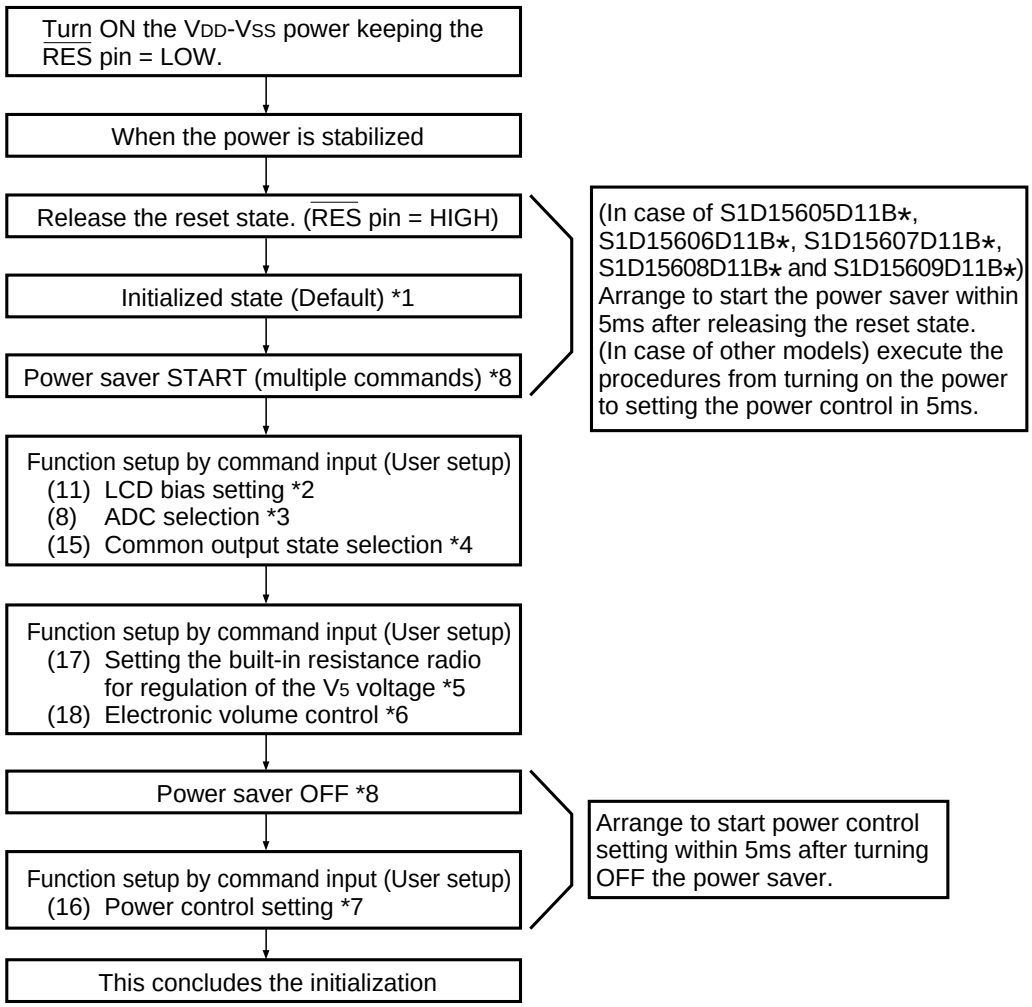


* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Notes: Refer to respective sections or paragraphs listed below.

*1: 6. Description of functions; “Resetting circuit” (If takes not more than 2 ms from Power Supply ON to the stability of internal oscillating circuit.)
*2: 7. Command description; “(11) LCD bias setting”
*3: 7. Command description; “(8) ADC selection”
*4: 7. Command description; “(15) Common output state selection”
*5: 6. Description of functions; “Power circuit” & Command description; “(17) Setting the built-in resistance radio for regulation of the V_5 voltage”
*6: 6. Description of functions; “Power circuit” & Command description; “(18) Electronic volume control”
*7: 6. Description of functions; “Power circuit” & Command description; “(16) Power control setting”

② When the built-in power is not being used immediately after turning on the power:

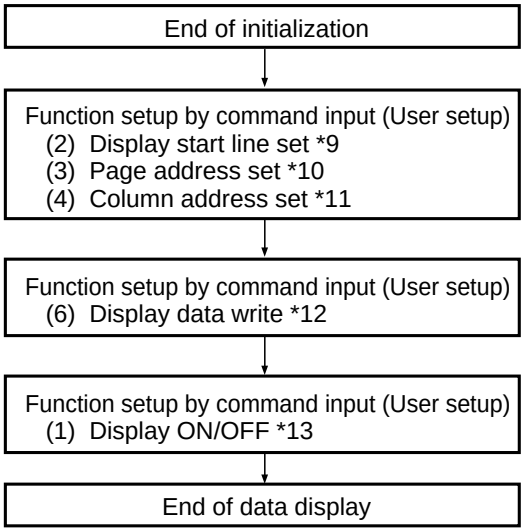


* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Notes: Refer to respective sections or paragraphs listed below.

*1: 6. Description of functions; “Resetting circuit” (The contents of DDRAM can be variable even in the initial setting (Default) at the reset state.)
*2: 7. Command description; “(11) LCD bias setting”
*3: 7. Command description; “(8) ADC selection”
*4: 7. Command description; “(15) Common output state selection”
*5: 6. Description of functions; “Power circuit” & “(17) Command description; Setting the built-in resistance radio for regulation of the V5 voltage”
*6: 6. Description of functions; “Power circuit” & “(18) Command description; Electronic volume control”
*7: 6. Description of functions; “Power circuit” & “(16) Command description; Power control setting”
*8: 7. The power saver ON state can either be in sleep state or stand-by state.
Command description; “Power saver START (multiple commands)”

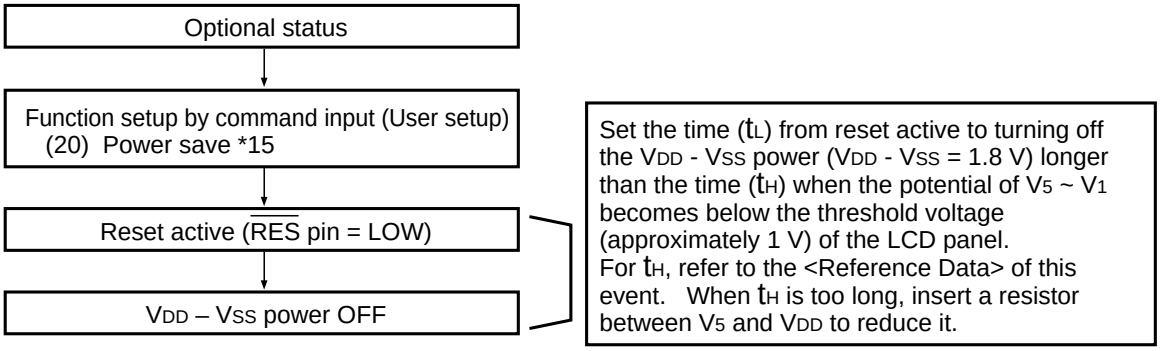
(2) Data Display



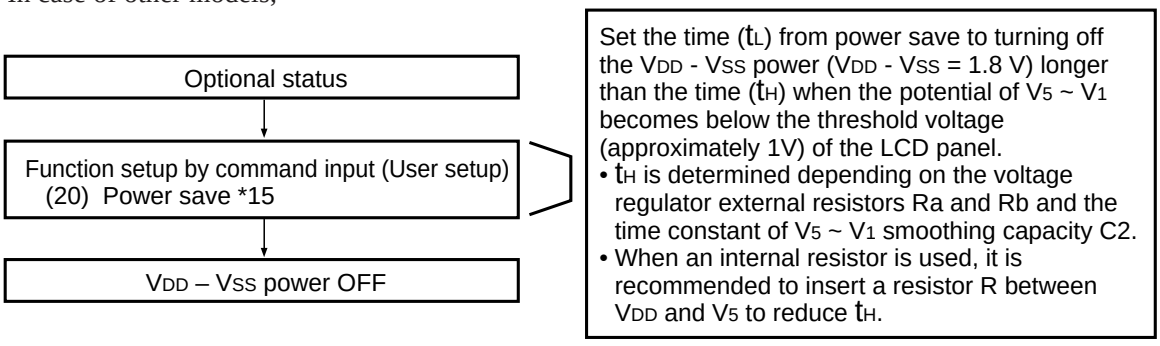
Notes: Reference items
- *9: Command Description; Display start line set
- *10: Command Description; Page address set
- *11: Command Description; Column address set
- *12: Command Description; Display data write
- *13: Command Description; Display ON/OFF
  Avoid displaying all the data at the data display start (when the display is ON) in white.

(3) Power OFF *14

• In case of S1D15605D11B∗, S1D15606D11B∗, S1D15607D11B∗, S1D15608D11B∗ and S1D15609D11B∗,



• In case of other models,



Notes: Reference items

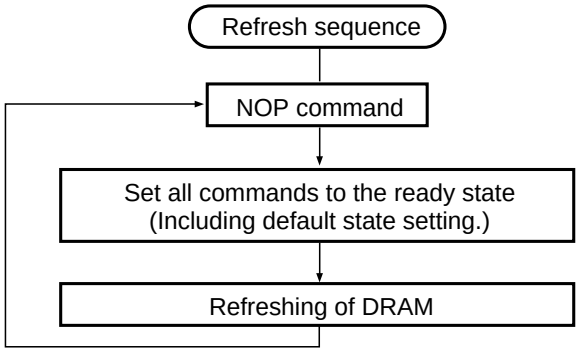
*14: The logic circuit of this IC's power supply VDD - VSS controls the driver of the LCD power supply VDD - V5. So, if the power supply VDD - VSS is cut off when the LCD power supply VDD - V5 has still any residual voltage, the driver (COM. SEG) may output any uncontrolled voltage. When turning off the power, observe the following basic procedures:
- After turning off the internal power supply, make sure that the potential V5 ~ V1 has become below the threshold voltage of the LCD panel, and then turn off this IC's power supply (VDD - VSS). 6. Description of Function, 6.7 Power Circuit

*15: After inputting the power save command, be sure to reset the function using the $\overline{RES}$ terminal until the power supply VDD - VSS is turned off. 7. Command Description (20) Power Save

*16: After inputting the power save command, do not reset the function using the RES terminal until the power supply VDD - VSS is turned off. 7. Command Description (20) Power Save

(4) Refresh

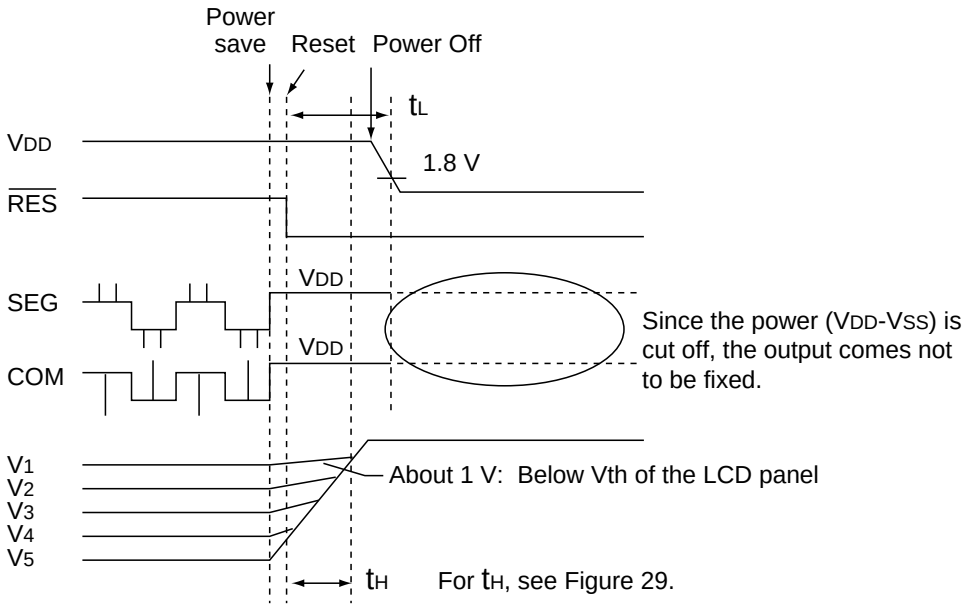
It is recommended that the operating modes and display contents be refreshed periodically to prevent the effect of unexpected noise.



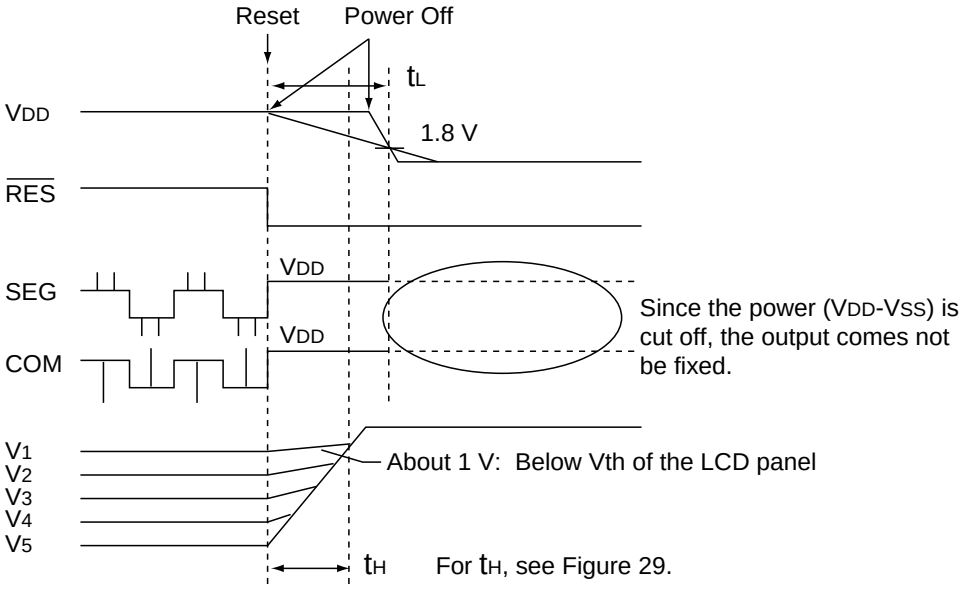
Precautions on Turning off the power

- In case of S1D15605D11B∗, S1D15606D11B∗, S1D15607D11B∗, S1D15608D11B∗ and S1D15609D11B∗, Observe Paragraph 1) as the basic rule.

  <Turning the power (V_{DD} - V_{SS}) off>
  1) Power Save (The LCD powers (V_{DD} - V_5) are off.) → Reset input → Power (V_{DD} - V_{SS}) OFF
     - Observe $t_L > t_H$.
     - When $t_L < t_H$, an irregular display may occur.
       Set t_L on the MPU according to the software. t_H is determined according to the external capacity C_2 (smoothing capacity of V_5 ~ V_1) and the driver's discharging capacity.



<Turning the power (V_{DD} - V_{SS}) off : When command control is not possible.>
2) Reset (The LCD powers (V_{DD} - V_{SS}) are off.) → Power (V_{DD} - V_{SS}) OFF
- Observe $t_L > t_H$.
- When $t_L < t_H$, an irregular display may occur.
  For t_L, make the power (V_{DD} - V_{SS}) falling characteristics longer or consider any other method. t_H is determined according to the external capacity C_2 (smoothing capacity of V_5 to V_1) and the driver's discharging capacity.



<Reference Data>
V_5 voltage falling (discharge) time (t_H) after the process of operation → power save → reset.
V_5 voltage falling (discharge) time (t_H) after the process of operation → reset.

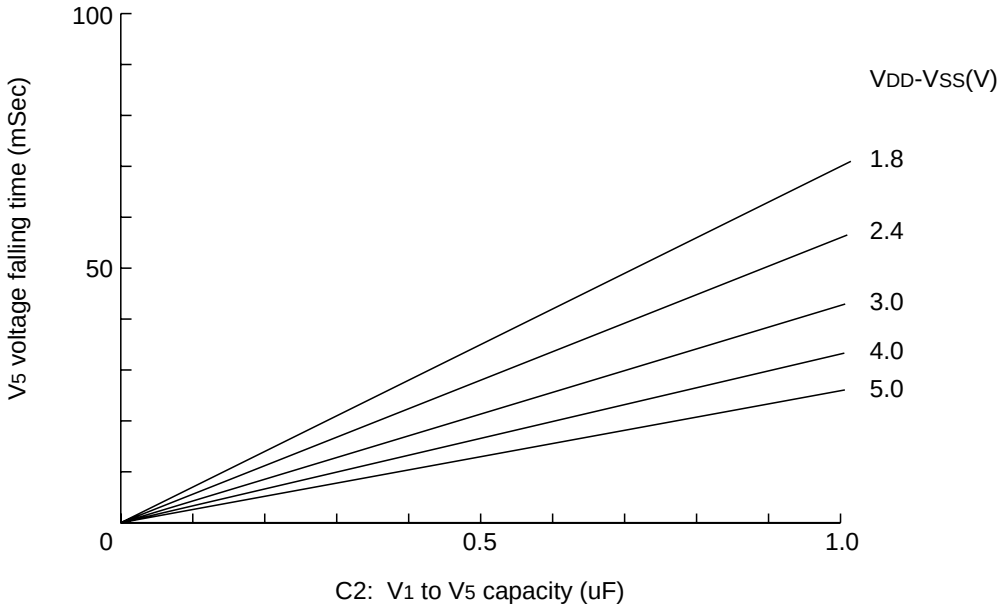
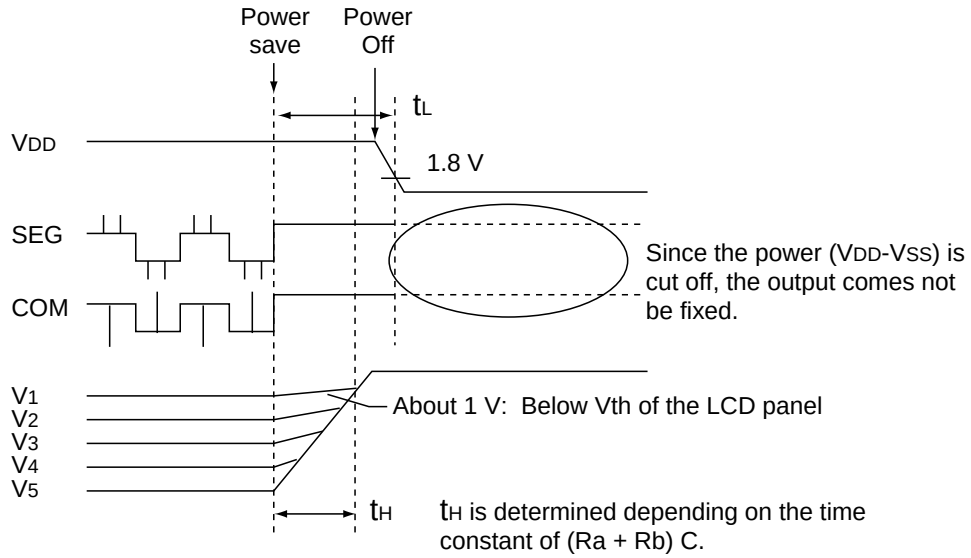


Figure 29

- In case of other models than the above
  <Turning the power (V_{DD} - V_{SS}) off>
  Power save (The LCD powers (V_{DD} - V_{SS}) are off.) -> Power (V_{DD} - V_{SS}) OFF
  - Observe $t_L > t_H$.
  - When $t_L < t_H$, an irregular display may occur.
    Set t_L on the MPU according to the software. t_H is determined according to the external capacity C (smoothing capacity of V_5 to V_1) and the external resisters Ra + Rb (for V_5 voltage regulation)



9. ABSOLUTE MAXIMUM RATINGS

Unless otherwise noted, V_{SS} = 0 V

Table 17

Parameter		Symbol	Conditions	Unit
Power Supply Voltage		V_{DD}	–0.3 to +7.0	V
Power supply voltage (2) (V_{DD} standard)	With Triple step-up With Quad step-up	V_{SS2}	–7.0 to +0.3 –6.0 to +0.3 –4.5 to +0.3	V
Power supply voltage (3) (V_{DD} standard)		V_5, V_{OUT}	–18.0 to +0.3	V
Power supply voltage (4) (V_{DD} standard)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage		V_{IN}	–0.3 to V_{DD} + 0.3	V
Output voltage		V_O	–0.3 to V_{DD} + 0.3	V
Operating temperature		T_{OPR}	–40 to +85	°C
Storage temperature	TCP Bare chip	T_{STR}	–55 to +100 –55 to +125	°C

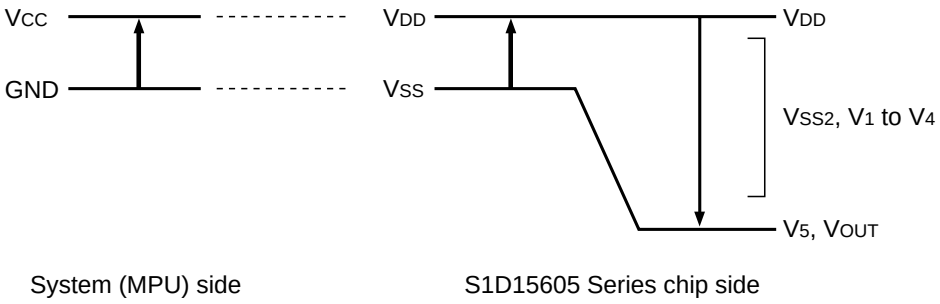


Figure 30

Notes and Cautions
1. The V_{SS2}, V_1 to V_5 and V_{OUT} are relative to the V_{DD} = 0V reference.
2. Insure that the voltage levels of V_1, V_2, V_3, and V_4 are always such that $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$.
3. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

10. DC CHARACTERISTICS

Unless otherwise specified, V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%, Ta = –40 to 85°C

Table 18

Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Operating Voltage (1)	Recommended Voltage	V_{DD}		2.7	—	3.3	V	V_{DD}*1
	Possible Operating Voltage			1.8	—	5.5	V	V_{DD}*1
Operating Voltage (2)	Recommended Voltage	V_{SS2}	(Relative to V_{DD})	–3.3	—	–2.7	V	V_{SS2}
	Possible Operating Voltage	V_{SS2}	(Relative to V_{DD})	–6.0	—	–1.8	V	V_{SS2}
Operating Voltage (3)	Possible Operating Voltage	V_5	(Relative to V_{DD})	–16.0	—	–4.5	V	V_5 *2
	Possible Operating Voltage	V_1, V_2	(Relative to V_{DD})	0.4 × V_5	—	V_{DD}	V	V_1, V_2
	Possible Operating Voltage	V_3, V_4	(Relative to V_{DD})	V_5	—	0.6 × V_5	V	V_3, V_4
High-level Input Voltage		V_{IHC}		0.8 × V_{DD}	—	V_{DD}	V	*3
Low-level Input Voltage		V_{ILC}		V_{SS}	—	0.2 × V_{DD}	V	*3
High-level Output Voltage		V_{OHC}	I_{OH} = –0.5 mA	0.8 × V_{DD}	—	V_{DD}	V	*4
Low-level Output Voltage		V_{OLC}	I_{OL} = 0.5 mA	V_{SS}	—	0.2 × V_{DD}	V	*4
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}	–1.0	—	1.0	µA	*5
Output leakage current		I_{LO}		–3.0	—	3.0	µA	*6
Liquid Crystal Driver ON Resistance		R_{ON}	Ta = 25°C (Relative To V_{DD}) V_5 = –14.0 V	—	2.0	3.5	kΩ	SEGn
			V_5 = –8.0 V	—	3.2	5.4	kΩ	COMn *7
Static Consumption Current		I_{SSQ}		—	0.01	5	µA	V_{SS}, V_{SS2}
Output Leakage Current		I_{5Q}	V_5 = –18.0 V (Relative To V_{DD})	—	0.01	15	µA	V_5
Input Terminal Capacitance		C_{IN}	Ta = 25°C f = 1 MHz	—	5.0	8.0	pF	
Oscillator Frequency	Internal Oscillator	f_{OSC}	Ta = 25°C	18	22	26	kHz	*8
	External Input	f_{CL}	S1D15605★★★★★/15607★★★★★	18	22	26	kHz	CL
	Internal Oscillator	f_{OSC}	Ta = 25°C	27	33	39	kHz	*8
	External Input	f_{CL}	S1D15606★★★★★/15608★★★★★/15609★★★★★	14	17	20	kHz	CL

Table 19

Item		Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Units	Applicable Pin
Internal Power	Input voltage	V_{SS2}	With Triple (Relative To V_{DD})		–6.0	—	–1.8	V	V_{SS2}
		V_{SS2}	With Quad (Relative To V_{DD})		–4.5	—	–1.8	V	V_{SS2}
	Supply Step-up output voltage Circuit	V_{OUT}	(Relative to V_{DD})		–18.0	—	—	V	V_{OUT}
	Voltage regulator Circuit Operating Voltage	V_{OUT}	(Relative to V_{DD})		–18.0	—	–6.0	V	V_{OUT}
	Voltage Follower Circuit Operating Voltage	V_5	(Relative to V_{DD})		–16.0	—	–4.5	V	V_5 *9
	Base Voltage	V_{REG0}	Ta = 25°C	–0.05%/°C	–2.04	–2.10	–2.16	V	*10
		V_{REG1}	(Relative to V_{DD})	–0.2%/°C	–4.65	–4.9	–5.15	V	*10

- Dynamic Consumption Current (1), During Display, with the Internal Power Supply OFF
  Current consumed by total ICs when an external power supply is used.

Table 20 Display Pattern OFF

Ta = 25°C

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
S1D15605*****	I_{DD} (1)	V_{DD} = 5.0 V, V_5 – V_{DD} = –11.0 V	—	18	30	µA	*11
		V_{DD} = 3.0 V, V_5 – V_{DD} = –11.0 V	—	16	27		
S1D15606*****		V_{DD} = 3.0 V, V_5 – V_{DD} = –11.0 V	—	13	22		
		V_{DD} = 5.0 V, V_5 – V_{DD} = –8.0 V	—	11	19		
		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	9	15		
S1D15607*****		V_{DD} = 5.0 V, V_5 – V_{DD} = –8.0 V	—	8	13		
		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	7	12		
S1D15608*****/		V_{DD} = 5.0 V, V_5 – V_{DD} = –8.0 V	—	12	20		
S1D15609*****		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	10	17		

Table 21 Display Pattern Checker

Ta = 25°C

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
S1D15605*****	I_{DD} (1)	V_{DD} = 5.0 V, V_5 – V_{DD} = –11.0 V	—	23	38	µA	*11
		V_{DD} = 3.0 V, V_5 – V_{DD} = –11.0 V	—	21	35		
S1D15606*****		V_{DD} = 3.0 V, V_5 – V_{DD} = –11.0 V	—	17	29		
		V_{DD} = 5.0 V, V_5 – V_{DD} = –8.0 V	—	14	24		
		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	12	20		
S1D15607*****		V_{DD} = 5.0 V, V_5 – V_{DD} = –8.0 V	—	11	18		
		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	10	17		
S1D15608*****/		V_{DD} = 5.0 V, V_5 – V_{DD} = –8.0 V	—	15	25		
S1D15609*****		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	13	22		

- Dynamic Consumption Current (2), During Display, with the Internal Power Supply ON
  The values of curret consumed in all the IC including internal power supply circuit.

Table 22 Display Pattern OFF

Ta = 25°C

Item	Symbol	Condition		Rating			Units	Notes
				Min.	Typ.	Max.		
S1D15605*****	I_{DD} (2)	V_{DD} = 5.0 V, Triple step-up voltage. V_5 – V_{DD} = –11.0 V	Normal Mode	—	67	112	µA	*12
			High-Power Mode	—	114	190		
		V_{DD} = 3.0 V, Quad step-up voltage. V_5 – V_{DD} = –11.0 V	Normal Mode	—	81	135		
			High-Power Mode	—	138	230		
S1D15606*****		V_{DD} = 5.0 V, Double step-up voltage. V_5 – V_{DD} = –8.0 V	Normal Mode	—	35	59		
			High-Power Mode	—	64	107		
		V_{DD} = 3.0 V, Triple step-up voltage. V_5 – V_{DD} = –8.0 V	Normal Mode	—	43	72		
			High-Power Mode	—	84	140		
		V_{DD} = 3.0 V, Quad step-up voltage. V_5 – V_{DD} = –11.0 V	Normal Mode	—	72	121		
			High-Power Mode	—	128	214		
S1D15607*****		V_{DD} = 5.0 V, Double step-up voltage. V_5 – V_{DD} = –8.0 V	Normal Mode	—	26	44		
			High-Power Mode	—	60	100		
		V_{DD} = 3.0 V, Triple step-up voltage. V_5 – V_{DD} = –8.0 V	Normal Mode	—	29	49		
			High-Power Mode	—	73	122		
S1D15608*****/ S1D15609*****		V_{DD} = 5.0 V, Double step-up voltage. V_5 – V_{DD} = –8.0 V	Normal Mode	—	37	62		
			High-Power Mode	—	67	112		
		V_{DD} = 3.0 V, Triple step-up voltage. V_5 – V_{DD} = –8.0 V	Normal Mode	—	46	77		
			High-Power Mode	—	87	145		

Table 23 Display Pattern Checker

Ta = 25°C

Item	Symbol	Condition		Rating			Units	Notes
				Min.	Typ.	Max.		
S1D15605*****	I_{DD} (2)	V_{DD} = 5.0 V, Triple step-up voltage. $V_5 - V_{DD}$ = –11.0 V	Normal Mode	—	81	135	µA	*12
			High-Power Mode	—	127	212		
		V_{DD} = 3.0 V, Quad step-up voltage. $V_5 - V_{DD}$ = –11.0 V	Normal Mode	—	96	160		
			High-Power Mode	—	153	255		
S1D15606*****		V_{DD} = 5.0 V, Double step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	41	69		
			High-Power Mode	—	71	119		
		V_{DD} = 3.0 V, Triple step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	51	85		
			High-Power Mode	—	92	154		
		V_{DD} = 3.0 V, Quad step-up voltage. $V_5 - V_{DD}$ = –11.0 V	Normal Mode	—	85	142		
			High-Power Mode	—	142	237		
S1D15607*****		V_{DD} = 5.0 V, Double step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	32	53		
			High-Power Mode	—	62	103		
		V_{DD} = 3.0 V, Triple step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	44	73		
			High-Power Mode	—	89	148		
S1D15608*****/ S1D15609*****		V_{DD} = 5.0 V, Double step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	44	74		
			High-Power Mode	—	74	127		
		V_{DD} = 3.0 V, Triple step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	54	90		
			High-Power Mode	—	95	159		

- Consumption Current at Time of Power Saver Mode, V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%

Table 24

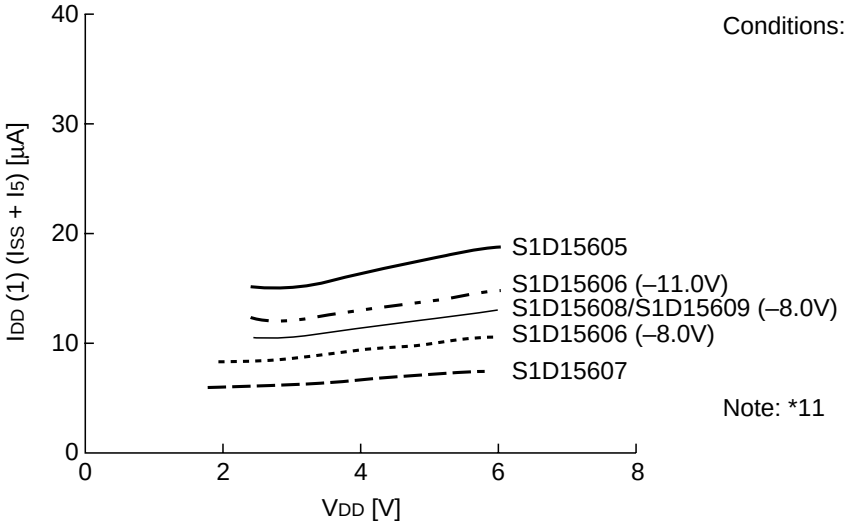
Ta = 25°C

Item		Symbol	Condition	Rating			Units	Notes
				Min.	Typ.	Max.		
Sleep mode	S1D15605*****	I_{DDS1}	—		0.01	5	µA	
Standby Mode	S1D15605*****	I_{DDS2}	—		4	8	µA	
Sleep mode	S1D15606*****	I_{DDS1}	—		0.01	5	µA	
Standby Mode	S1D15606*****	I_{DDS2}	—		4	8	µA	
Sleep mode	S1D15607*****	I_{DDS1}	—		0.01	5	µA	
Standby Mode	S1D15607*****	I_{DDS2}	—		3	6	µA	
Sleep mode	S1D15608*****/ S1D15609*****	I_{DDS1}	—		0.01	5	µA	
Standby Mode	S1D15608*****/ S1D15609*****	I_{DDS2}	—		4	8	µA	

TBD: To Be Determined

Reference Data 1

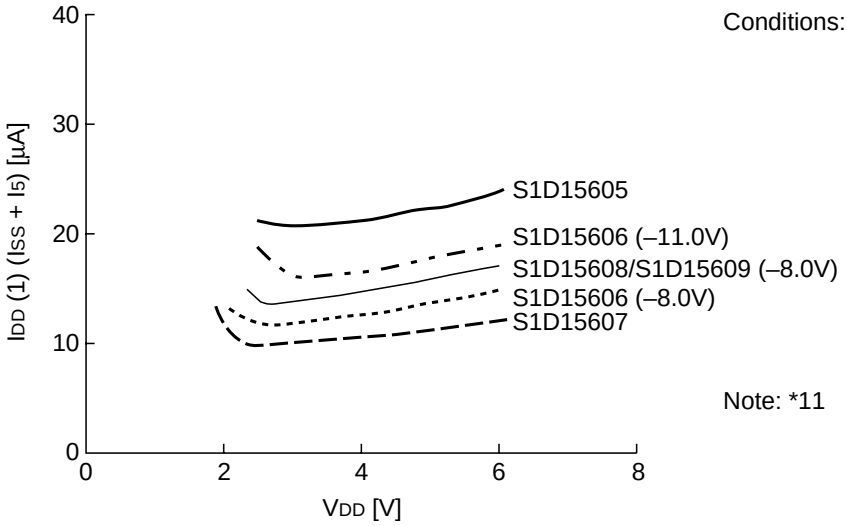
- Dynamic Consumption Current (1) During LCD Display Using an External Power Supply



Conditions: Internal power supply OFF
External power supply in use
S1D15605/S1D15606 (–11.0V):
$V_5 – V_{DD}$ = –11.0 V
S1D15606 (–8.0V)/S1D15607/
S1D15608/S1D15609:
$V_5 – V_{DD}$ = –8.0 V
Display pattern: OFF
Ta = 25°C

Note: *11

Figure 31



Conditions: Internal power supply OFF
External power supply in use
S1D15605/S1D15606 (–11.0V):
$V_5 – V_{DD}$ = –11.0 V
S1D15606 (–8.0V)/S1D15607/
S1D15608/S1D15609:
$V_5 – V_{DD}$ = –8.0 V
Display pattern: Checker
Ta = 25°C

Note: *11

Figure 32

Reference Data 2

- Dynamic Consumption Current (2) During LCD display using the internal power supply

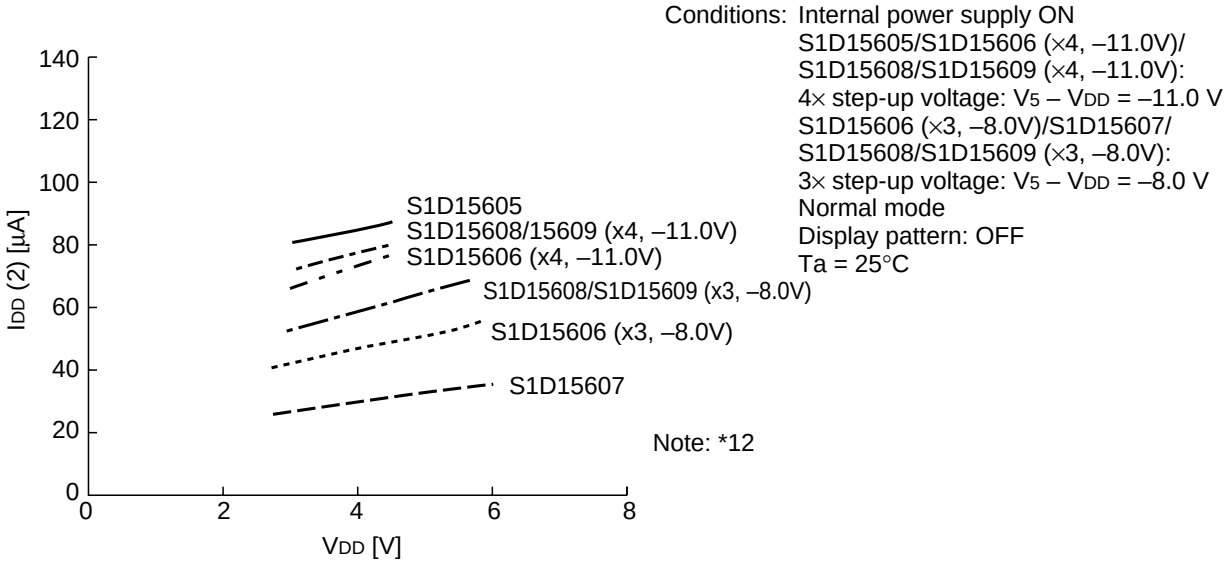


Figure 33

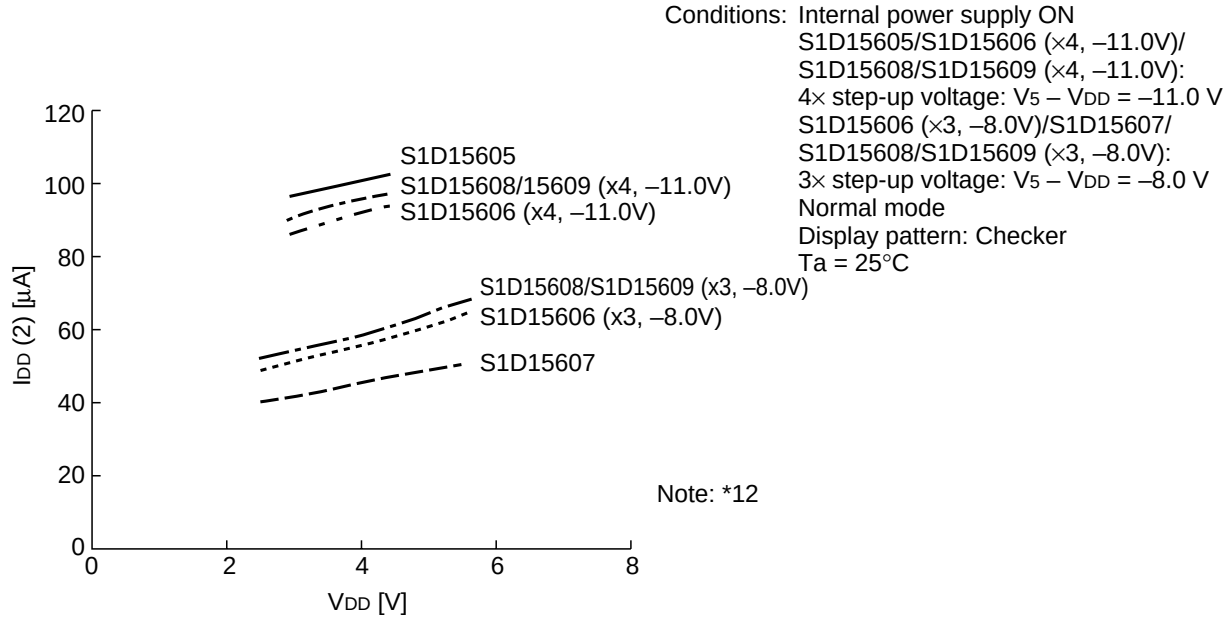
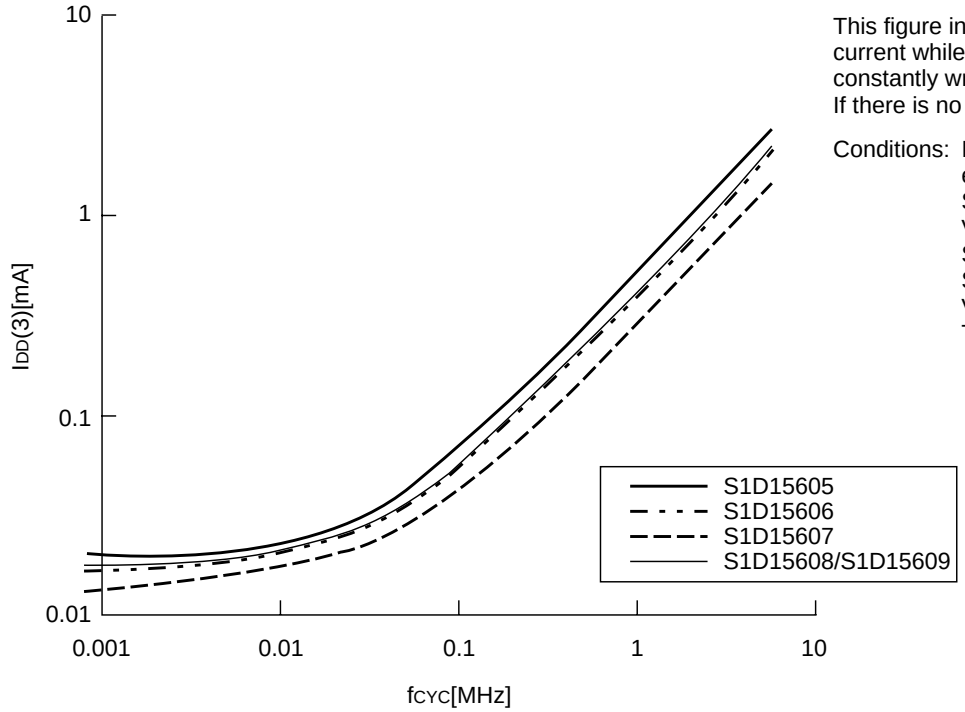


Figure 34

Reference Data 3

- Dynamic Consumption Current (3) During access



This figure indicates the consumption current while the checker pattern is constantly written through f_{CYC}.
If there is no access, then only (1) remains.

Conditions: Internal power supply OFF, external power supply used
S1D15605:
$V_{DD} - V_{SS}$ = 3.0 V, V_5=–11.0 V
S1D15606/S1D15607/
S1D15608/S1D15609:
$V_{DD} - V_{SS}$ = 3.0 V, V_5=–8.0 V
Ta = 25°C

Figure 35

Reference Data 4

- Operating voltage range of V_{SS} and V_5 systems

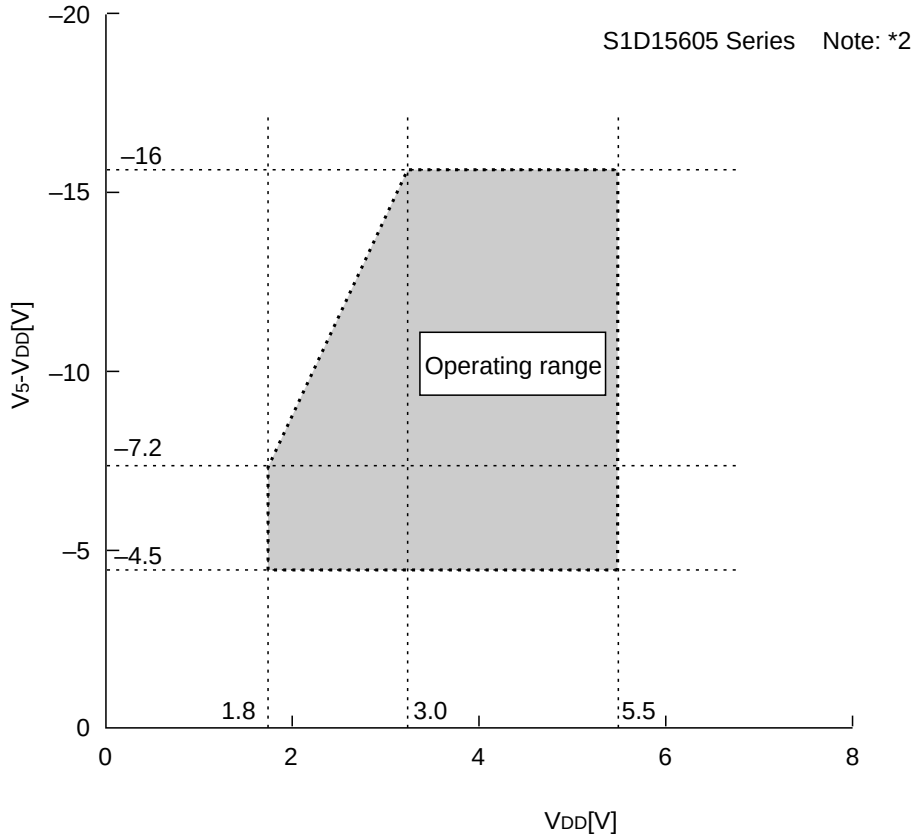


Figure 36

- The Relationship Between Oscillator Frequency f_{OSC}, Display Clock Frequency f_{CL} and the Liquid Crystal Frame Rate Frequency f_{FR}

Table 25

Item		f_{CL}	f_{FR}
S1D15605*****	When the internal oscillator circuit is used	$\frac{f_{OSC}}{4}$	$\frac{f_{OSC}}{4 \times 65}$
	When the internal oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{260}$
S1D15606*****	When the internal oscillator circuit is used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{8 \times 49}$
	When the internal oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{196}$
S1D15607*****	When the internal oscillator circuit is used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{8 \times 33}$
	When the internal oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{264}$
S1D15608*****	When the internal oscillator circuit is used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{8 \times 55}$
	When the internal oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{220}$
S1D15609*****	When the internal oscillator circuit is used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{8 \times 53}$
	When the internal oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{212}$

(f_{FR} is the liquid crystal alternating current period, and not the FR signal period.)

References for items market with *

*1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

*2 The operating voltage range for the V_{DD} system and the V_5 system is as shown in Figure 36. This applies when the external power supply is being used.

*3 The A0, D0 to D5, D6 (SCL), D7 (SI), $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, CL, FR, M/S, C86, P/S, $\overline{DOF}$, $\overline{RES}$, IRS, and $\overline{HPM}$ terminals.

*4 The D0 to D7, FR, FRS, $\overline{DOF}$, and CL terminals.

*5 The A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, M/S, C86, P/S, $\overline{RES}$, IRS, and $\overline{HPM}$ terminals.

*6 Applies when the D0 to D5, D6 (SCL), D7 (SI), CL, FR, and $\overline{DOF}$ terminals are in a high impedance state.

*7 These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V_1, V_2, V_3, and V_4). These are specified for the operating voltage (3) range.
R_{ON} = 0.1 V/Δ I (Where Δ I is the current that flows when 0.1 V is applied while the power supply is ON.)

*8 See Table 9-7 for the relationship between the oscillator frequency and the frame rate frequency.

*9 The V_5 voltage regulator circuit regulates within the operating voltage range of the voltage follower.

*10 This is the internal voltage reference supply for the V_5 voltage regulator circuit. In the S1D15605/S1D15606/S1D15607 chips, the temperature range can come in three types as V_{REG} options: (1) approximately–0.05%/°C, (2) –0.2%/°C, and (3) external input.

*11, 12 It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on.
The S1D15605 is 1/9 biased, S1D15606/S1D15608/S1D15609 is 1/8 biased and S1D15607 is 1/6 biased.
Does not include the current due to the LCD panel capacity and wiring capacity.
Applicable only when there is no access from the MPU.

*12 It is the value on a model having the V_{REG} option temperature gradient is –0.05%/°C when the V_5 voltage regulator internal resistor is used.

11. TIMING CHARACTERISTICS

(1) System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

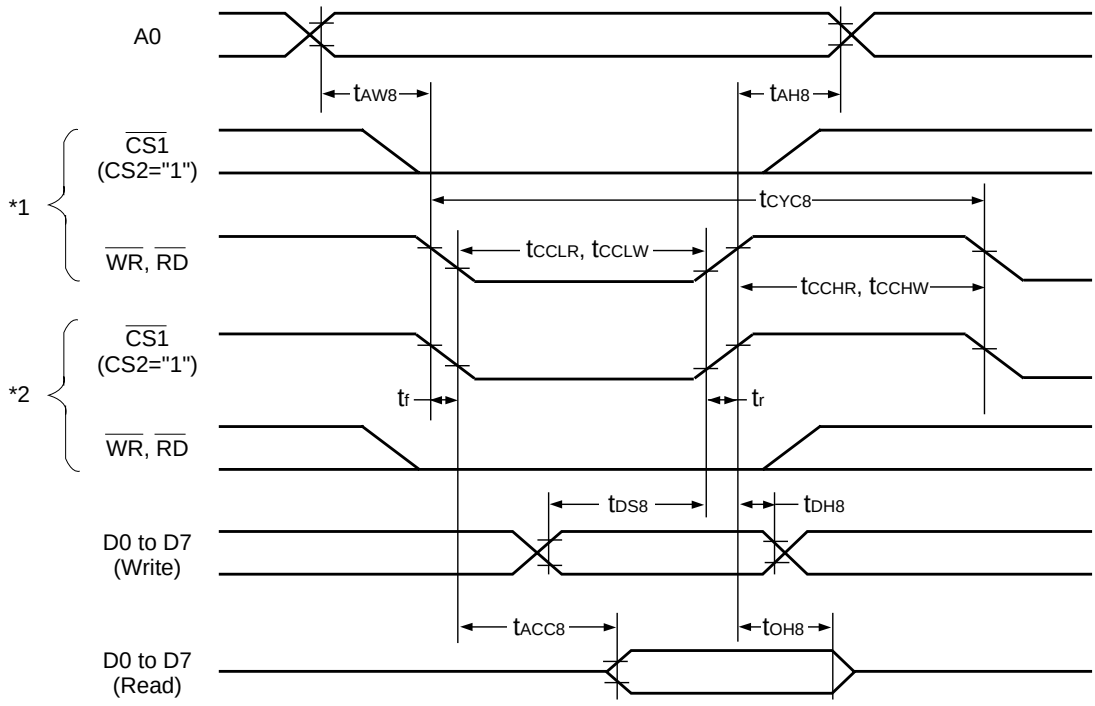


Figure 37

Table 26

(V_{DD} = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	ns
System cycle time	A0	t_{CYC8}		166	—	ns
Control LOW pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		30	—	ns
Control LOW pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		70	—	ns
Control HIGH pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		30	—	ns
Control HIGH pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		30	—	ns
Data setup time	D0 to D7	t_{DS8}		30	—	ns
Address hold time		t_{DH8}		10	—	ns
$\overline{RD}$ access time		t_{ACC8}	CL = 100 pF	—	70	ns
Output disable time		t_{OH8}		5	50	ns

Table 27

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	ns
System cycle time	A0	t_{CYC8}		300	—	ns
Control LOW pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		60	—	ns
Control LOW pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		120	—	ns
Control HIGH pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		60	—	ns
Control HIGH pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		60	—	ns
Data setup time	D0 to D7	t_{DS8}		40	—	ns
Address hold time		t_{DH8}		15	—	ns
$\overline{RD}$ access time		t_{ACC8}	CL = 100 pF	—	140	ns
Output disable time		t_{OH8}		10	100	ns

Table 28

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	ns
System cycle time	A0	t_{CYC8}		1000	—	ns
Control LOW pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		120	—	ns
Control LOW pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		240	—	ns
Control HIGH pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		120	—	ns
Control HIGH pulse width (RD)	$\overline{RD}$	t_{CCHR}		120	—	ns
Data setup time	D0 to D7	t_{DS8}		80	—	ns
Address hold time		t_{DH8}		30	—	ns
$\overline{RD}$ access time		t_{ACC8}	CL = 100 pF	—	280	ns
Output disable time		t_{OH8}		10	200	ns

*1 This is in the case of making the access by $\overline{WR}$ and $\overline{RD}$,setting the $\overline{CS1}$=LOW.
*2 This is the case of making the accese by $\overline{CS1}$,setting the WR,$\overline{RD}$=LOW.
*3 The rise and fall times (t_r and t_f) of the input signal are specified for less than 15 ns.When using the system cycle time at high speed, they are specified for ($t_r + t_f$) ≤ (t_{CYC8}-t_{CCLR}-t_{CCHR}).
*4 All timings are specified based on the 20 and 80% of V_{DD}.
*5 t_{CCLW} and t_{CCLR} are specified for the overlap period when $\overline{CS1}$ is at LOW (CS2=HIGH) level and $\overline{WR}$,$\overline{RD}$ are at the LOW level.

(2) System Bus Read/Write Characteristics 2 (6800 Series MPU)

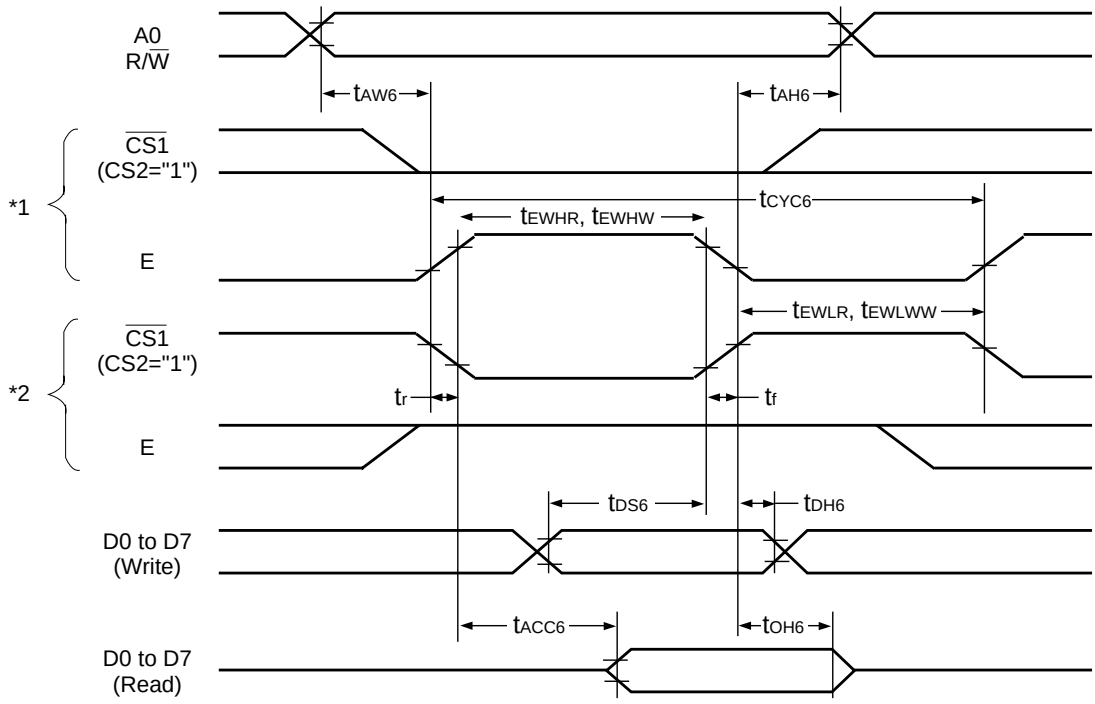


Figure 38

Table 29

(V_{DD} = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min.	Max.	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}		0 0	— —	ns ns
System cycle time		A0	t_{CYC6}		166	—	ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		30 10	— —	ns ns
Access time Output disable time			t_{ACC6} t_{OH6}	CL = 100 pF	— 10	70 50	ns ns
Enable HIGH pulse time	Read Write	E	t_{EWHR} t_{EWHW}		70 30	— —	ns ns
Enable LOW pulse time	Read Write	E	t_{EWLR} t_{EWLW}		30 30	— —	ns ns

Table 30

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min.	Max.	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}		0 0	— —	ns ns
System cycle time		A0	t_{CYC6}		300	—	ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		40 15	— —	ns ns
Access time Output disable time			t_{ACC6} t_{OH6}	CL = 100 pF	— 10	140 100	ns ns
Enable HIGH pulse time	Read Write	E	t_{EWHR} t_{EWHW}		120 60	— —	ns ns
Enable LOW pulse time	Read Write	E	t_{EWLR} t_{EWLW}		60 60	— —	ns ns

Table 31

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min.	Max.	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}		0 0	— —	ns ns
System cycle time		A0	t_{CYC6}		1000	—	ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		80 30	— —	ns ns
Access time Output disable time			t_{ACC6} t_{OH6}	CL = 100 pF	— 10	280 200	ns ns
Enable HIGH pulse time	Read Write	E	t_{EWHR} t_{EWHW}		240 120	— —	ns ns
Enable LOW pulse time	Read Write	E	t_{EWLR} t_{EWLW}		120 120	— —	ns ns

*1 This is in the case of making the access by E, setting the $\overline{CS1}$=LOW.
*2 This is the case of making the accese by $\overline{CS1}$,setting the E=HIGH.
*3 The rise and fall times ((t_r and t_f) of the input signal are specified for less than 15 ns.When using the system cycle time at high speed, they are specified for ($t_r + t_f$) ≤ (t_{CYC6}-t_{EWLW}-t_{EWHW}) or ($t_r + t_f$) ≤ (t_{CYC6}-t_{EWLR}-t_{EWHR}).
*4 All timings are specified based on the 20 and 80% of V_{DD}.
*5 t_{EWLW} and t_{EWLR} are specified for the overlap period when $\overline{CS1}$ is at LOW (CS2=HIGH) level and E is at the HIGH level.

(3) The Serial Interface

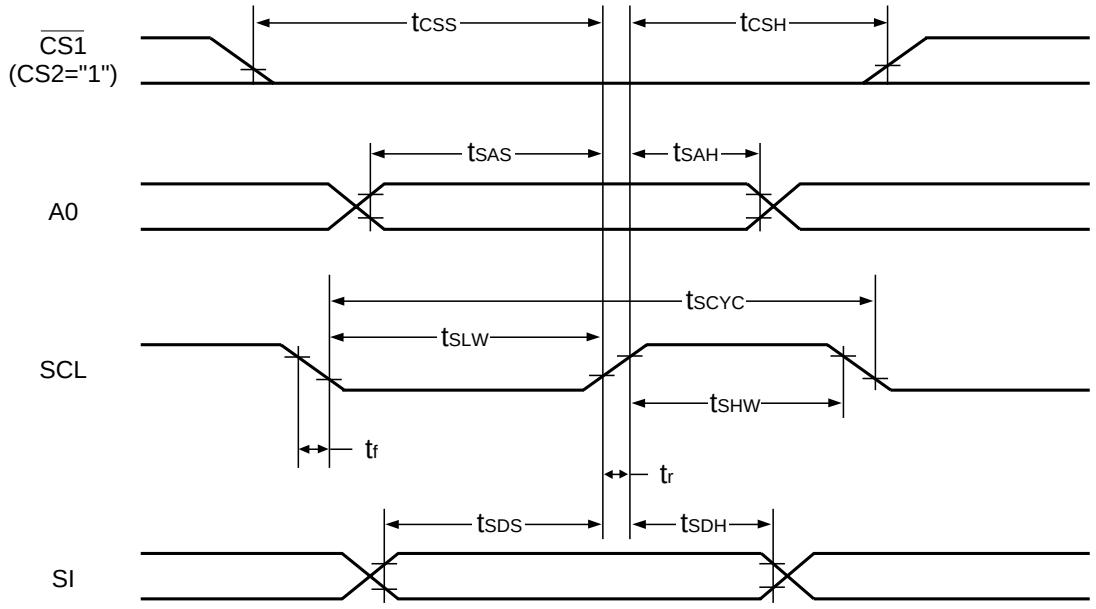


Figure 39

Table 32

(V_{DD} = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		200	—	ns
SCL HIGH pulse width		t_{SHW}		75	—	ns
SCL LOW pulse width		t_{SLW}		75	—	ns
Address setup time	A0	t_{SAS}		50	—	ns
Address hold time		t_{SAH}		100	—	ns
Data setup time	SI	t_{SDS}		50	—	ns
Data hold time		t_{SDH}		50	—	ns
CS-SCL time	CS	t_{CSS}		100	—	ns
		t_{CSH}		100	—	ns

Table 33

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		250	—	ns
SCL HIGH pulse width		t_{SHW}		100	—	ns
SCL LOW pulse width		t_{SLW}		100	—	ns
Address setup time	A0	t_{SAS}		150	—	ns
Address hold time		t_{SAH}		150	—	ns
Data setup time	SI	t_{SDS}		100	—	ns
Data hold time		t_{SDH}		100	—	ns
CS-SCL time	CS	t_{CSS}		150	—	ns
		t_{CSH}		150	—	ns

Table 34

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		400	—	ns
SCL HIGH pulse width		t_{SHW}		150	—	ns
SCL LOW pulse width		t_{SLW}		150	—	ns
Address setup time	A0	t_{SAS}		250	—	ns
Address hold time		t_{SAH}		250	—	ns
Data setup time	SI	t_{SDS}		150	—	ns
Data hold time		t_{SDH}		150	—	ns
CS-SCL time	CS	t_{CSS}		250	—	ns
		t_{CSH}		250	—	ns

*1 The input signal rise and fall time (t_r, t_f) are specified at 15 ns or less.
*2 All timing is specified using 20% and 80% of V_{DD} as the standard.

(4) Display Control Output Timing

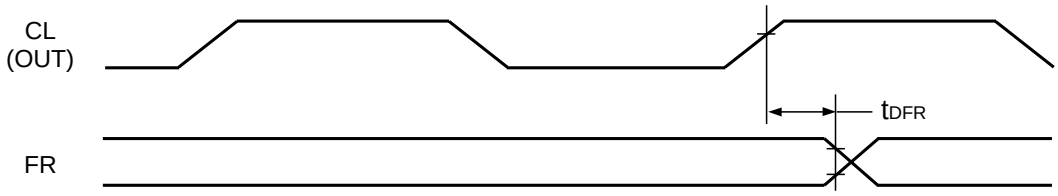


Figure 40

Table 35

(V_{DD} = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL = 50 pF	—	10	40	ns

Table 36

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL = 50 pF	—	20	80	ns

Table 37

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL = 50 pF	—	50	200	ns

*1 Valid only when the master mode is selected.
*2 All timing is based on 20% and 80% of V_{DD}.

Reset Timing

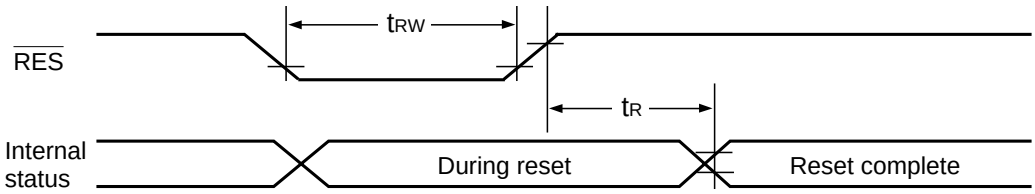


Figure 41

Table 38

(V_{DD} = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		—	—	0.5	µs
Reset LOW pulse width	RES	t_{RW}		0.5	—	—	µs

Table 39

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1	µs
Reset LOW pulse width	RES	t_{RW}		1	—	—	µs

Table 40

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1.5	µs
Reset LOW pulse width	RES	t_{RW}		1.5	—	—	µs

*1 All timing is specified with 20% and 80% of V_{DD} as the standard.

12. THE MPU INTERFACE (REFERENCE EXAMPLES)

The S1D15605 Series can be connected to either 80 × 86 Series MPUs or to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the S1D15605 series chips with fewer signal lines.
The display area can be enlarged by using multiple S1D15605 Series chips. When this is done, the chip select signal can be used to select the individual ICs to access.

(1) 8080 Series MPUs

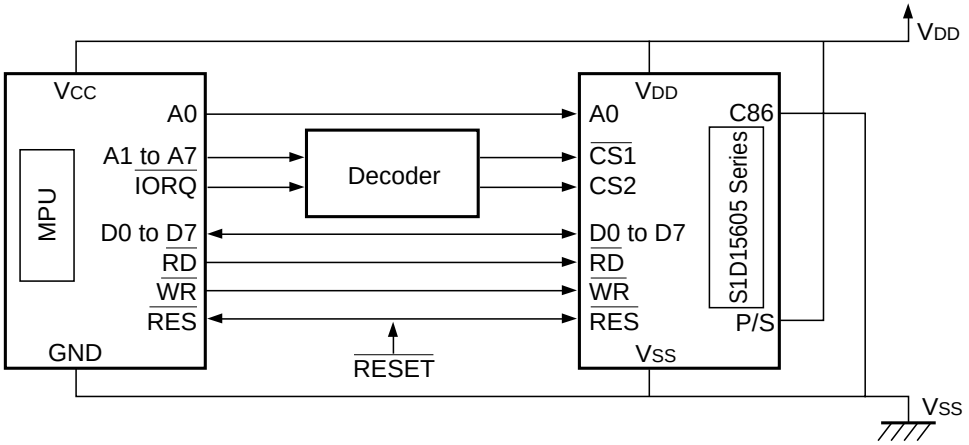


Figure 42-1

(2) 6800 Series MPUs

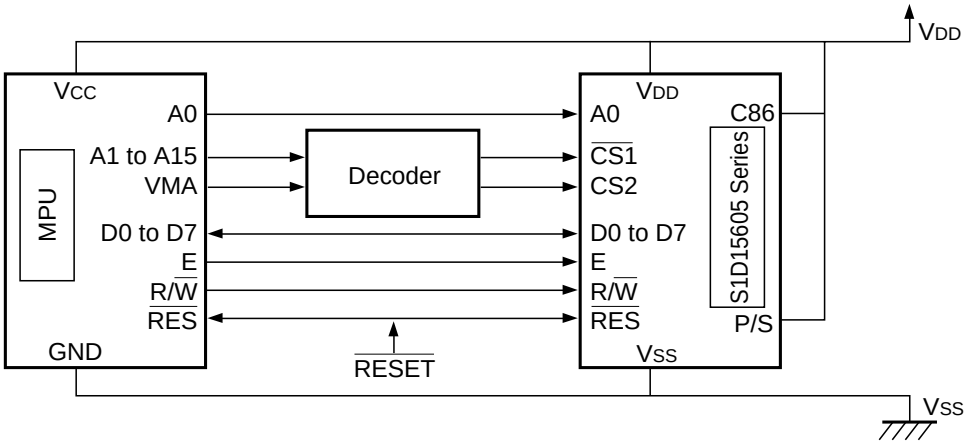


Figure 42-2

(3) Using the Serial Interface

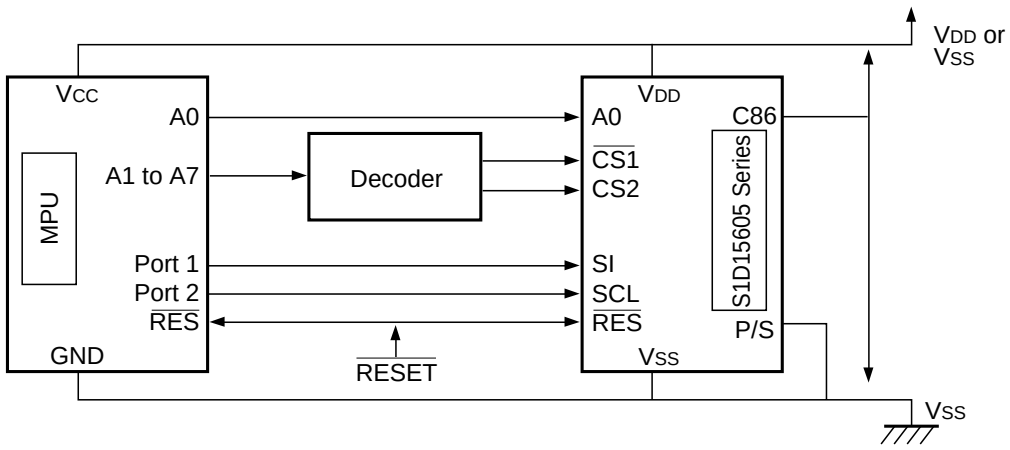


Figure 42-3

13. CONNECTIONS BETWEEN LCD DRIVERS (REFERENCE EXAMPLE)

The liquid crystal display area can be enlarged with ease through the use of multiple S1D15605 Series chips. Use a same equipment type.

(1) S1D15605 (master) ↔ S1D15605 (slave)

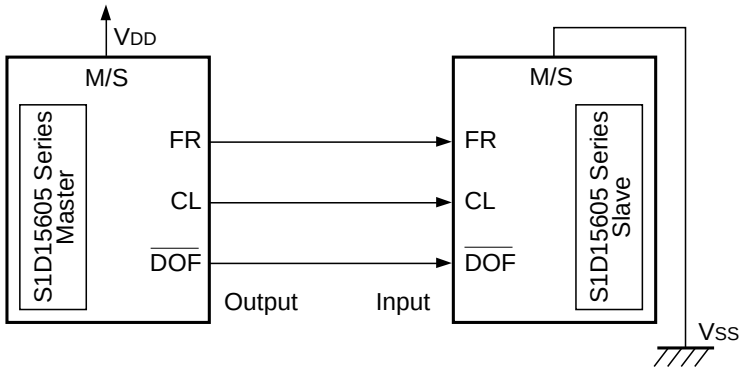


Figure 43

14. CONNECTIONS BETWEEN LCD DRIVERS (REFERENCE EXAMPLES)

The liquid crystal display area can be enlarged with ease through the use of multiple S1D15605 Series chips. Use a same equipment type, in the composition of these chips.

(1) Single-chip Structure

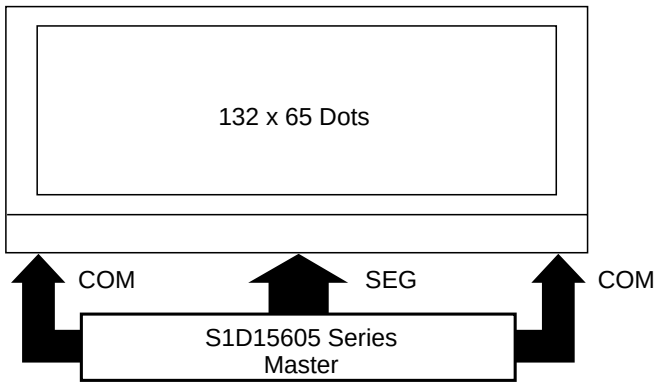


Figure 44-1

(2) Double-chip Structure, #1

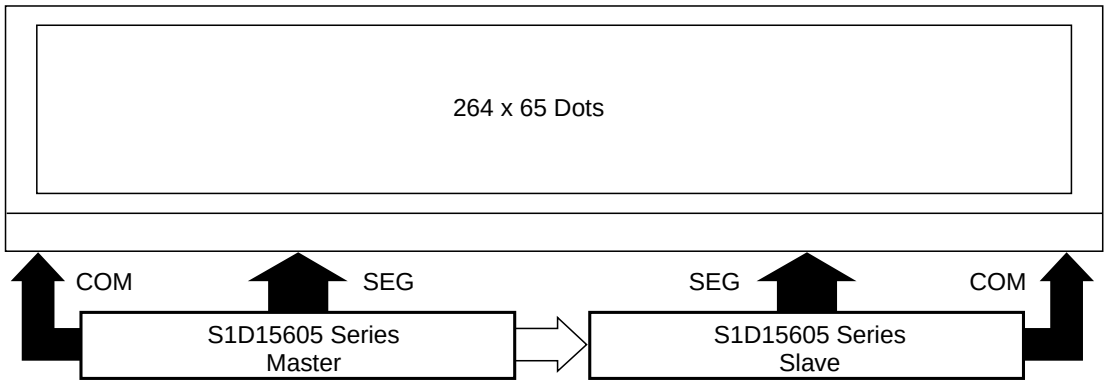


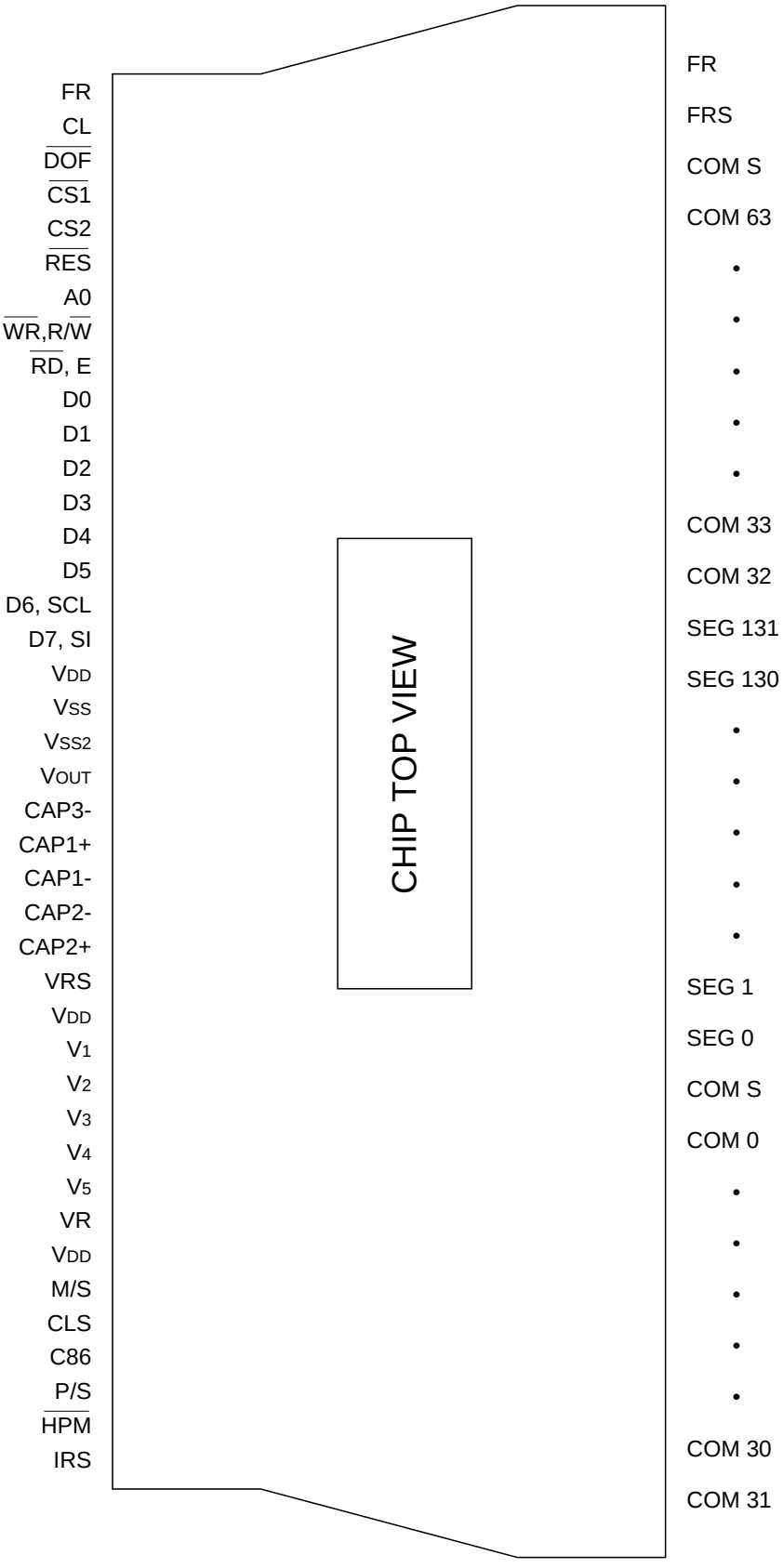
Figure 44-2

15. A SAMPLE TCP PIN ASSIGNMENT

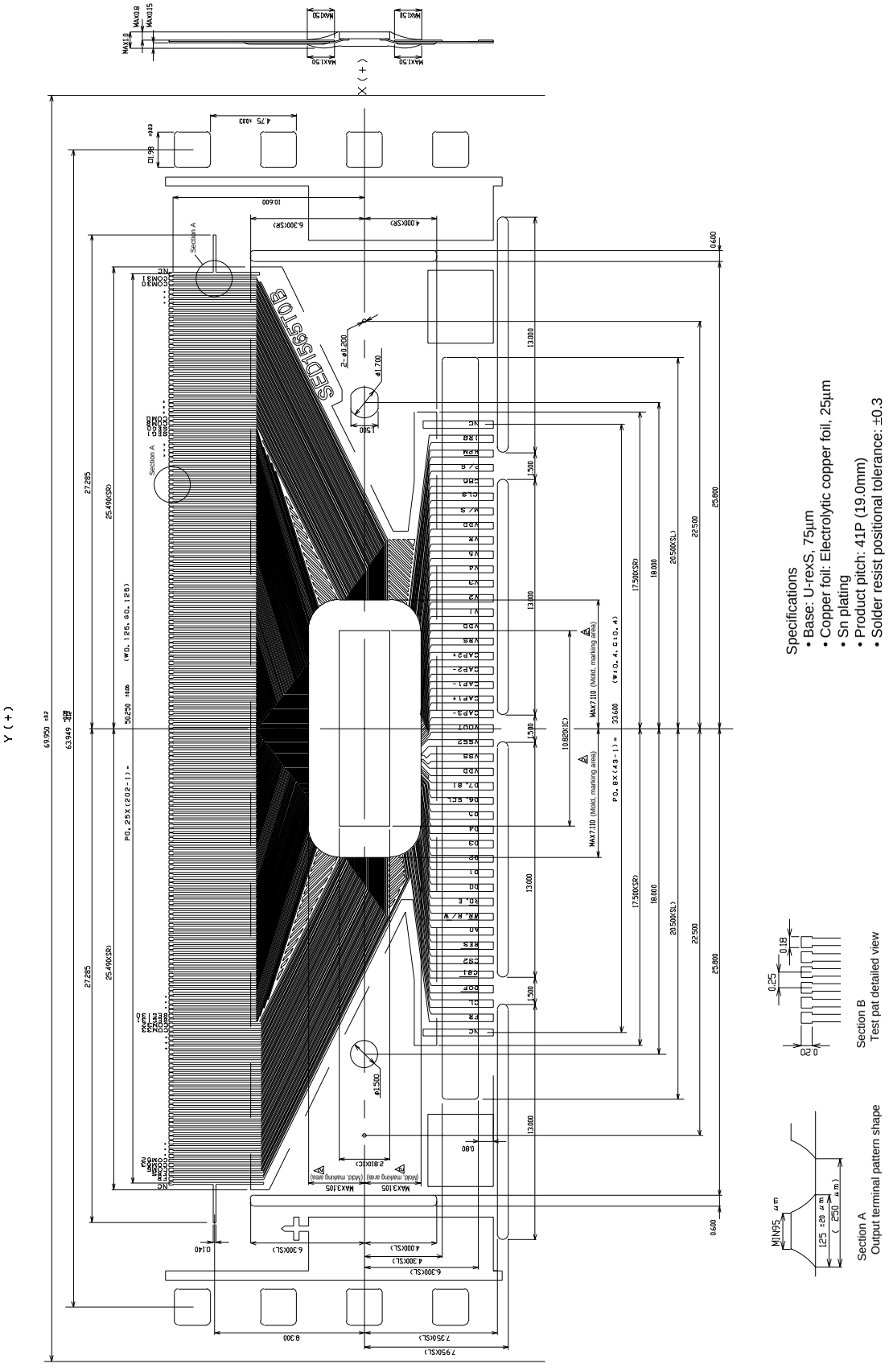
S1D15605T00B* TCP Pin Layout

Note: The following does not specify dimensions of the TCP pins.

An example



16. EXTERNAL VIEW OF TCP PINS



9. S1D15700 Series

Contents

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1. DESCRIPTION

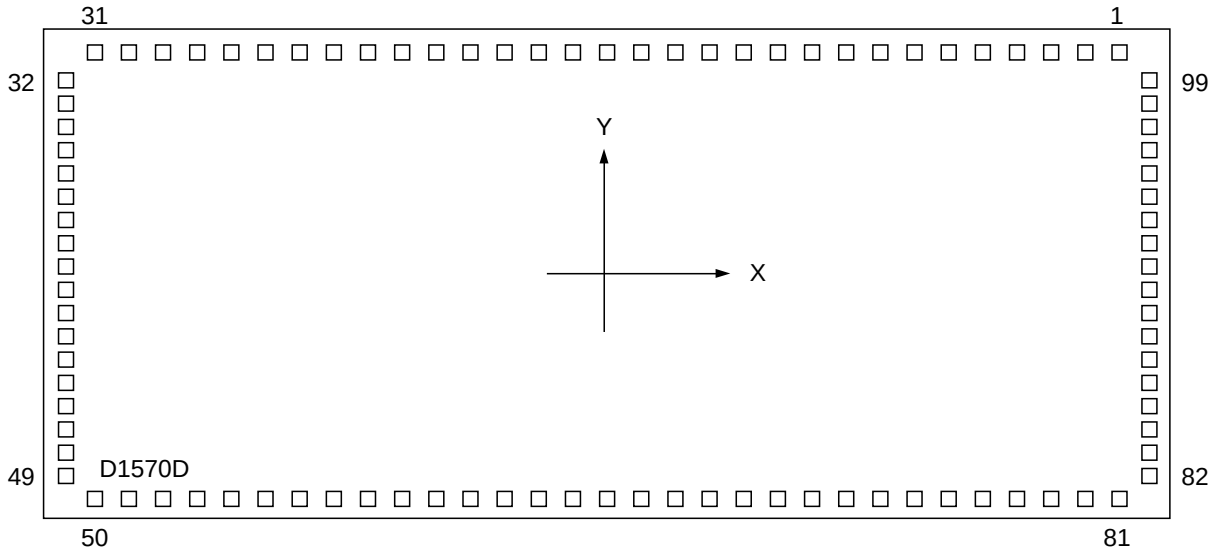
The S1D15700 is an 80 output segment (column) driver with an internal display RAM. This drive is suitable for driving a dot matrix LCD panel; from a mid-range capacity dot matrix LCD panel to a CGA class dot matrix LCD panel. This device is used with the S1D16305.
The display data is stored in the internal display RAM and an LCD panel drive signal is generated. As a result, this device allows configuration of an ultra low power display system since the display data is not transferred unless the display is changed.
In addition, the logic power is low voltage; a wide range of applications is possible.

2. FEATURES

- Display duty cycle: 1/64 – 1/200
- LCD driver output: 80 out
- Internal display RAM: 200 × 80 bits
- Slim chip
- Ultra low power consumption
- Power $V_{DD} - V_{SS}$ 2.7 V to 5.5 V
  $V_{DD} - V_{EE}$ 8.0 V to 20 V
- High speed and low power date transfer by the 4-bit bus enables chain method
- Non-bias display off function
- Output shift direction-pin selection
- Adjustable LCD power offset bias for V_{DD} level
- Package Chip S1D15700D00A∗ (Al-pad chip)
  S1D15700D00B∗ (Au-bump chip)

3. PAD

Pad Layout



S1D15700D00A∗	(Al-pad chip)
Chip Size	8.04 mm × 3.51 mm
Pad Center Size	100 μm × 100 μm
Pad Pitch	170 μm (Min.)
Chip Thickness	400 μm ±25 μm (Al Pad)

S1D15700D00B∗	(Al-bump chip)
Bump Size	92 μm × 82 μm
Pump Pitch	170 μm (Min.)
Chip Thickness	525 μm
Bump Height	17~28 μm (reference)

S1D15700 Pad Center Coordinates (Al-pad)

Unit: μm

PAD No	PIN Name	X	Y
1	X 75	3640	1595
2	X 76	3432	
3	X 77	3224	
4	X 78	3016	
5	X 79	2808	
6	X 80	2600	
7	EIO2	2340	
8	V_{DD}	2080	
9	SHL	1820	
10	D_0	1560	
11	D_1	1300	
12	D_2	1040	
13	D_3	780	
14	YD	520	
15	V_{EE}	260	
16	V_5	0	
17	V_3	–260	
18	V_2	–520	
19	V_0	–780	
20	FR	–1040	
21	XSCL	–1300	
22	$\overline{DOFF}$	–1560	
23	LP	–1820	
24	V_{SS}	–2080	
25	EIO1	–2340	
26	X 1	–2600	
27	X 2	–2808	
28	X 3	–3016	
29	X 4	–3224	
30	X 5	–3432	
31	X 6	–3640	
32	X 7	–3862	1452
33	X 8		1282
34	X 9		1112
35	X 10		942
36	X 11		772
37	X 12		602
38	X 13		432
39	X 14		262
40	X 15		92

PAD No	PIN Name	X	Y
41	X 16	–3862	–78
42	X 17		–248
43	X 18		–418
44	X 19		–588
45	X 20		–758
46	X 21		–928
47	X 22		–1098
48	X 23		–1268
49	X 24		–1438
50	X 25	–3641	–1595
51	X 26	–3406	
52	X 27	–3171	
53	X 28	–2936	
54	X 29	–2701	
55	X 30	–2466	
56	X 31	–2231	
57	X 32	–1996	
58	X 33	–1761	
59	X 34	–1526	
60	X 35	–1291	
61	X 36	–1056	
62	X 37	–821	
63	X 38	–586	
64	X 39	–351	
65	X 40	–116	
66	X 41	119	
67	X 42	354	
68	X 43	589	
69	X 44	824	
70	X 45	1059	
71	X 46	1294	
72	X 47	1530	
73	X 48	1765	
74	X 49	2000	
75	X 50	2235	
76	X 51	2470	
77	X 52	2705	
78	X 53	2940	
79	X 54	3175	
80	X 55	3410	

PAD No	PIN Name	X	Y
81	X 56	3645	–1595
82	X 57	3862	–1438
83	X 58		–1268
84	X 59		–1098
85	X 60		–928
86	X 61		–758
87	X 62		–588
88	X 63		–418
89	X 64		–248
90	X 65		–78
91	X 66		92
92	X 67		262
93	X 68		432
94	X 69		602
95	X 70		772
96	X 71		942
97	X 72		1112
98	X 73		1282
99	X 74		1452

(Au-bump) Unit: μm

Unit: μm

PAD No	PIN Name	X	Y
1	X 75	3640	1601
2	X 76	3432	↑
3	X 77	3224	↑
4	X 78	3016	↑
5	X 79	2808	↑
6	X 80	2600	↑
7	EIO2	2340	↑
8	V_{DD}	2080	↑
9	SHL	1820	↑
10	D_0	1560	↑
11	D_1	1300	↑
12	D_2	1040	↑
13	D_3	780	↑
14	YD	520	↑
15	V_{EE}	260	↑
16	V_5	0	↑
17	V_3	–260	↑
18	V_2	–520	↑
19	V_0	–780	↑
20	FR	–1040	↑
21	XSCL	–1300	↑
22	$\overline{DOFF}$	–1560	↑
23	LP	–1820	↑
24	V_{SS}	–2080	↑
25	EIO1	–2340	↑
26	X 1	–2600	↑
27	X 2	–2808	↑
28	X 3	–3016	↑
29	X 4	–3224	↑
30	X 5	–3432	↑
31	X 6	–3640	↑
32	X 7	–3868	1452
33	X 8	↑	1282
34	X 9	↑	1112
35	X 10	↑	942
36	X 11	↑	772
37	X 12	↑	602
38	X 13	↑	432
39	X 14	↑	262
40	X 15	↑	92

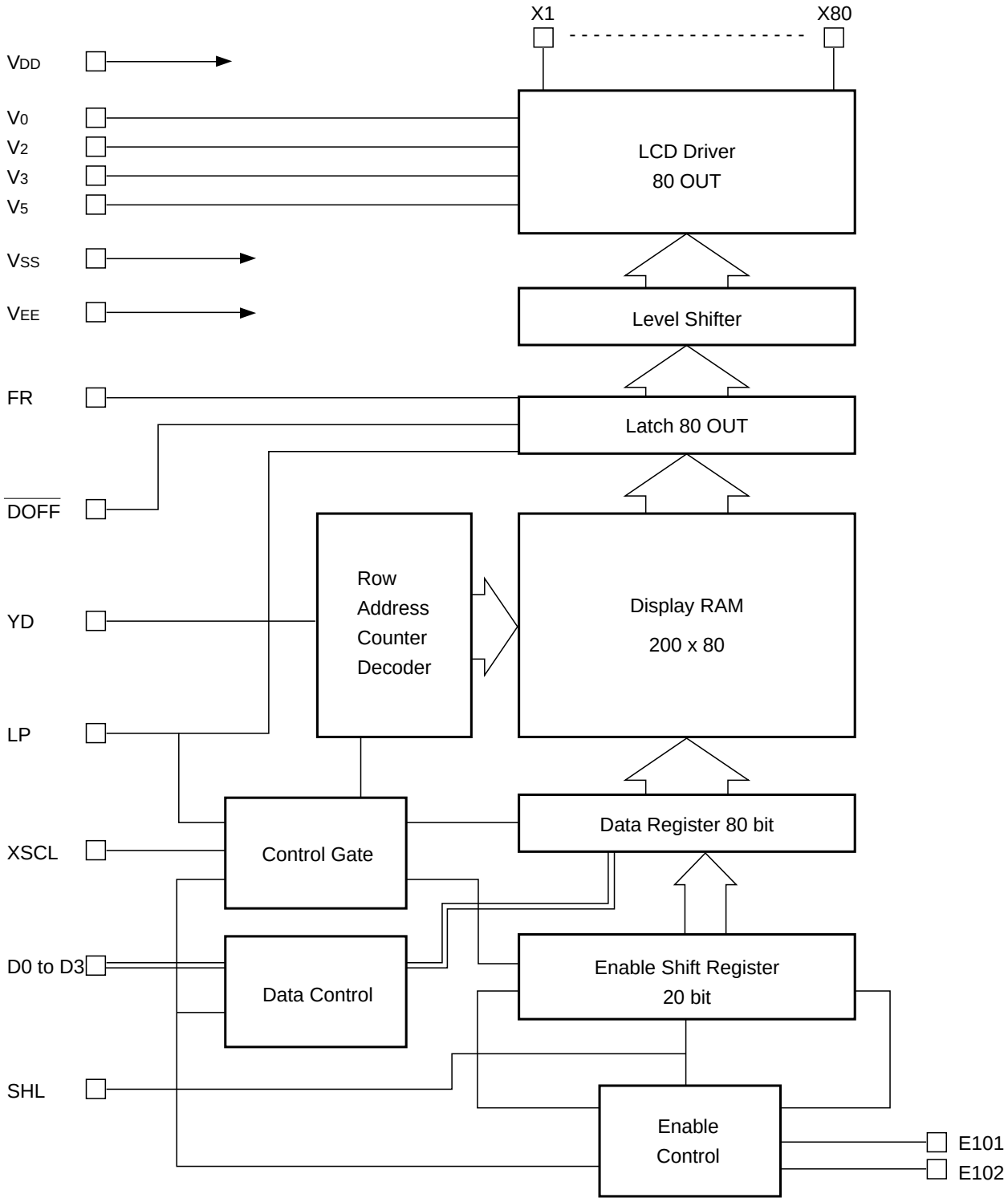
PAD No	PIN Name	X	Y
41	X 16	–3868	–78
42	X 17	↑	–248
43	X 18	↑	–418
44	X 19	↑	–588
45	X 20	↑	–758
46	X 21	↑	–928
47	X 22	↑	–1098
48	X 23	↑	–1268
49	X 24	↑	–1438
50	X 25	–3641	–1601
51	X 26	–3406	↑
52	X 27	–3171	↑
53	X 28	–2936	↑
54	X 29	–2701	↑
55	X 30	–2466	↑
56	X 31	–2231	↑
57	X 32	–1996	↑
58	X 33	–1761	↑
59	X 34	–1526	↑
60	X 35	–1291	↑
61	X 36	–1056	↑
62	X 37	–821	↑
63	X 38	–586	↑
64	X 39	–351	↑
65	X 40	–116	↑
66	X 41	119	↑
67	X 42	354	↑
68	X 43	589	↑
69	X 44	824	↑
70	X 45	1059	↑
71	X 46	1294	↑
72	X 47	1530	↑
73	X 48	1765	↑
74	X 49	2000	↑
75	X 50	2235	↑
76	X 51	2470	↑
77	X 52	2705	↑
78	X 53	2940	↑
79	X 54	3175	↑
80	X 55	3410	↑

PAD No	PIN Name	X	Y
81	X 56	3645	–1601
82	X 57	3868	–1438
83	X 58	↑	–1268
84	X 59	↑	–1098
85	X 60	↑	–928
86	X 61	↑	–758
87	X 62	↑	–588
88	X 63	↑	–418
89	X 64	↑	–248
90	X 65	↑	–78
91	X 66	↑	92
92	X 67	↑	262
93	X 68	↑	432
94	X 69	↑	602
95	X 70	↑	772
96	X 71	↑	942
97	X 72	↑	1112
98	X 73	↑	1282
99	X 74	↑	1452

4. PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>X1 – X80</td><td>O</td><td>LCD drive segment (column) output
The output changes with the LP's trailing edge.</td><td>80</td></tr>
<tr><td>D_0 – D_3</td><td>I</td><td>Display data input</td><td>4</td></tr>
<tr><td>XSCL</td><td>I</td><td>Display data shift clock input
Reads the display data (D_0 – D_3) into the data register with a trailing edge.</td><td>1</td></tr>
<tr><td>LP</td><td>I/O</td><td>Display data latch clock input
• The display RAM data (specified by the low address shift register) is read into the latch with a leading edge, and the LCD display data is output.
• For a specified low address, the contents of the write register are written in the display RAM. (At Data transfer mode)
• Resets the enable control circuit.</td><td>1</td></tr>
<tr><td>EIO1
EIO2</td><td>I/O</td><td>Enable I/O
• Configured by SHL.
• Output is reset to HIGH by LP input. When the 80 bit display data is read, the output falls to LOW automatically.
• To connect in cascade format, connect these pins to the next level EIO.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction and input/output select input
• If the display data is entered in the input (D_3, D_2, D_1, D_0) in the order of (a1, a2, a3, a4) (b1, b2, b3, b4) … (t1, t2, t3, t4), the relationship of the display data and the segment output is as given in the table below.
<table>
<tr><th rowspan="2">SHL</th><th colspan="14">Xn (SEG output)</th><th colspan="2">EIO</th></tr>
<tr><th>80</th><th>79</th><th>78</th><th>77</th><th>76</th><th>75</th><th>…</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>1</th><th>2</th></tr>
<tr><td>LOW</td><td>a1</td><td>a2</td><td>a3</td><td>a4</td><td>b1</td><td>b2</td><td>…</td><td>s3</td><td>s4</td><td>t1</td><td>t2</td><td>t3</td><td>t4</td><td>O</td><td>I</td></tr>
<tr><td>HIGH</td><td>t4</td><td>t3</td><td>t2</td><td>t1</td><td>s4</td><td>s3</td><td>…</td><td>b2</td><td>b1</td><td>a4</td><td>a3</td><td>a2</td><td>a1</td><td>I</td><td>O</td></tr>
</table></td><td>1</td></tr>
<tr><td>$\overline{DOFF}$</td><td>I</td><td>Forced blank input
In the LOW level, the segment output is forced to the V_0 level.
The display RAM data is maintained.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LCD AC drive signal input</td><td>1</td></tr>
<tr><td>YD</td><td>I</td><td>Scan start input
• Rests the low address counter decoder.
• The number of scanned lines (number of low addresses) for the display RAM is determined by the number of LP pulses, which are input in one YD cycle.</td><td>1</td></tr>
<tr><td>V_0, V_2, V_3, V_5</td><td>Power supply</td><td>LCD drive power input
$V_{DD} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq V_{EE}$</td><td>4</td></tr>
<tr><td>V_{EE}</td><td>Power supply</td><td>LCD drive power input V_{DD} – V_{EE}</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power supply</td><td>Logic power input
V_{DD}: connect to the system V_{CC} pin.
V_{SS}: connect to the system GND.</td><td>2</td></tr>
</table>

5. BLOCK DIAGRAM



6. FUNCTION DESCRIPTION

Enable Shift Register

The order of the display data latched is reversed by the SHL input.

Enable Control and Data Control

If the enable signal is disabled (EIO = HIGH), the internal clock signal and the data bus are fixed to LOW. This is a power-save mode.
To use multiple segment drivers, connect in cascade format the EIO pin of each driver, and connect the EIO pin of the first driver to the "V_{SS}" pin.
The enable control circuit automatically detects when the 80 bit data has been read and automatically transfers the enable signal. As a result, a control signal by a control LSI is not necessary.

Display RAM

This is a static RAM (200 × 80 bits) that stores the LCD data.
The display RAM data (80 bit) for the low address is read out to the latch with the trailing edge of the LP signal. In addition, with the trailing edge of the LP signal, the contents of the data register is moved to the write register. The contents of the write register are then written in the display RAM area for the low address. The low address is then incremented.
If the XSCL signal does not come in after the trailing edge of the LP signal, the mode is changed to the self-refresh mode. The write register does not write data in the display RAM and the low address is incremented. The mode is then changed to the read out mode to read the next line.

Low Address Counter Decoder

This selects a line of the display RAM in sequence. This decoder catches the HIGH of the YD signal at the trailing edge of the LP signal, and resets the low address counter. It then initialize the selected address of the display RAM. In a normal operation, the decoder is incremented after the writing operation into the display RAM. (The writing operation is caused by the trailing edge of the LP signal.) In the self-refresh mode, the decoder is incremented without the writing operation into the display RAM.

Data Register

This 80 bit register controls the write operation into the display RAM. The data is written in the display RAM with the trailing edge of the LP signal. In the self-refresh mode, the data is not written in the display RAM.

Control Circuit

The control circuit detects the self-refresh mode, allows the write register to write the data into the display RAM, and controls and low address count signal.

Latch

This reads the 80 bit data for the low address of the display RAM with the trailing edge of the LP signal, and sends the output signal to the level shifter.

Level Shifter

This is the level interface circuit that converts the signal voltage level from $V_{DD} – V_{SS}$ to $V_{DD} – V_{EE}$ (LCD driver power).

LCD Driver

The LCD driver outputs the LCD driver voltage.
The table below shows the relationship between the display signals ($D_3 – D_0$), LCD AC-drive wave form (FR) and the segment output voltage.

$\overline{DOFF}$	$D_0 – D_3$	FR	X Output Voltage
HIGH	HIGH	HIGH	V_0
		LOW	V_5
	LOW	HIGH	V_2
		LOW	V_3
LOW	—	—	V_0

Self-Refresh Function

Setting self-refresh mode

The self-refresh mode functions as follows: if the displayed contents do not change, there is no transfer of the display data from the display controller to the S1D15700. The S1D15700 automatically detects this and power-down is displayed.

The S1D15700 is set to the self-refresh mode by maintaining the shift clock (XSCLK) in the "L" level for 1 horizontal display period (LP signal cycle) after the row data for 1 line has been input. The S1D15700 checks the mode (whether or not the mode is changed to the self-refresh mode) every 1 horizontal display period. During 1 horizontal display period in which XSCL stops working, the display data is not written into the S1D15700 display RAM.

To stop XSCL, terminate display data (D0 – D3) transfer from the display controller (because of the power down), and set XSCL to HIGH or LOW. At this time, the display control must periodically send the LP, YD, and FR signals to the S1D15700 the same way as when data is transferred. The S1D15700 inputs these signals, reads the display data periodically from the internal display RAM and refreshes the display.

The display-off function is available in the self-refresh mode.

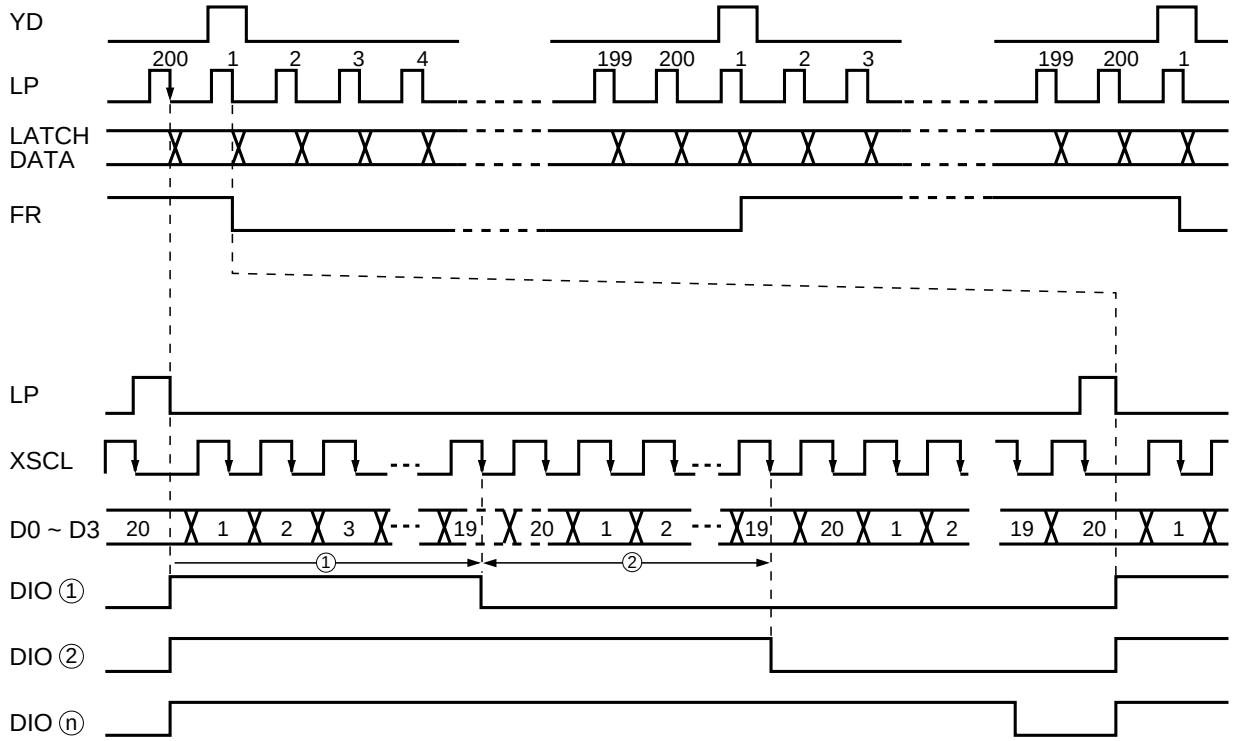
Canceling self-refresh mode

The self-refresh mode is canceled as follows: The display controller inputs the shift clock (XSCL) into the S1D15700 for one horizontal display period or longer. This should be down with the trailing edge of the LP signal and in the data transfer timing. After the mode is canceled, the line data, which has been sent in the horizontal display period, is written in the display RAM at the time of the next trailing edge of the LP signal.

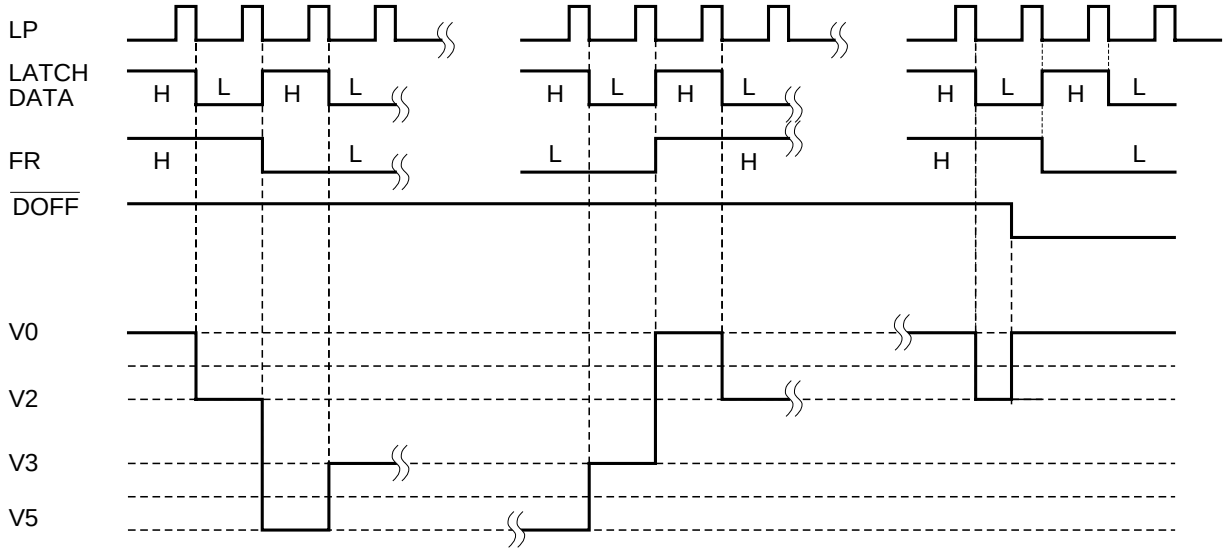
If the S1D15700s are connected in cascade format, the self-refresh modes of all S1D15700s are not canceled unless the appropriate number of the XSCL clocks for the cascaded S1D15700s are entered.

Timing Diagram

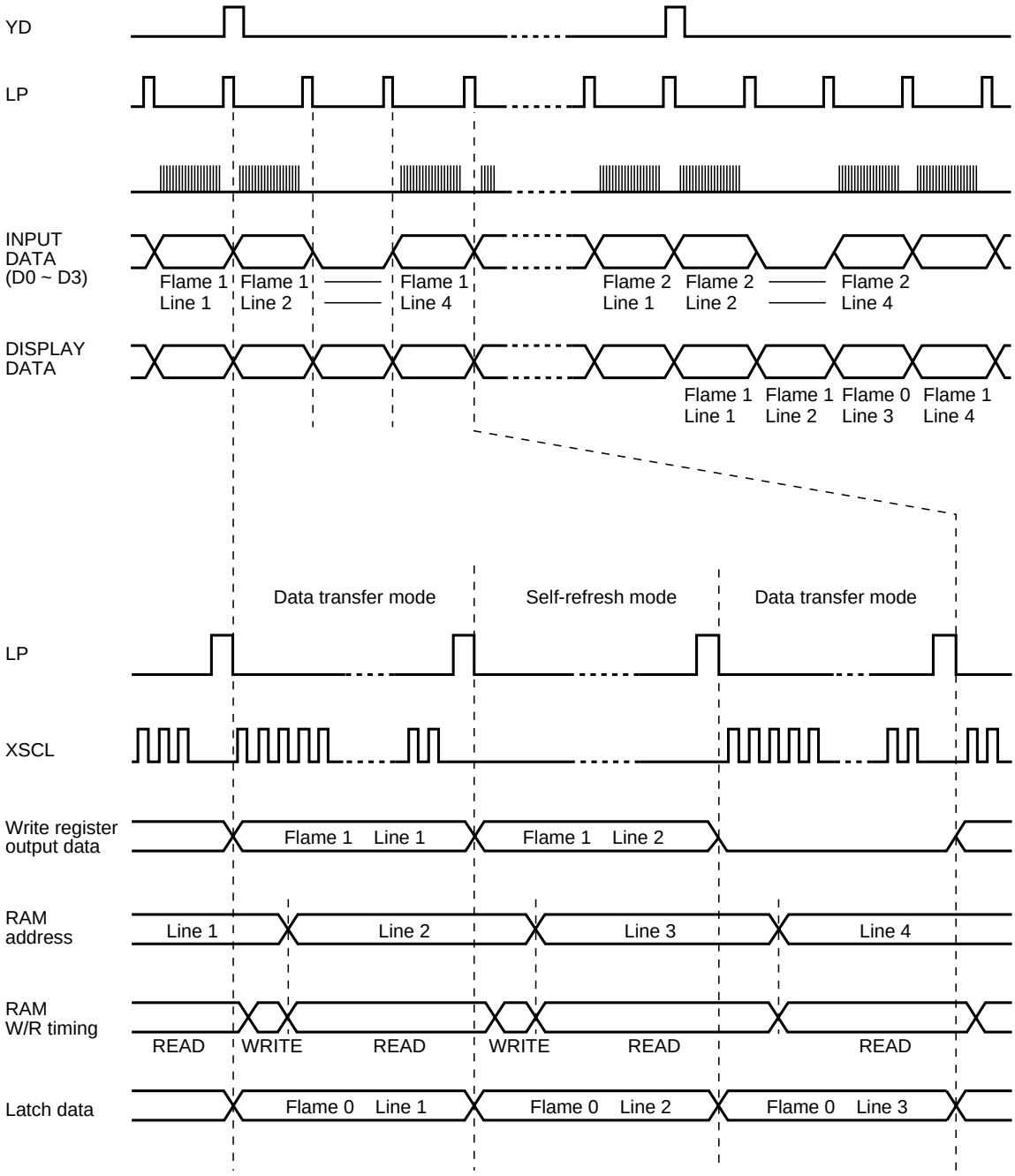
Sample of 1/200 duty



① ~ ⓝ serial conection number of Driver IC



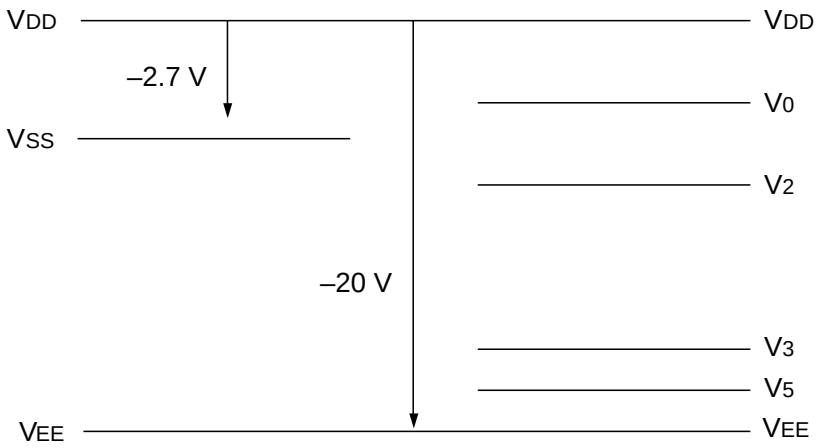
Self-refresh mode timing



7. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Unit
Supply voltage 1	V_{SS}	–7.0 to +0.3	V
Supply voltage 2	V_{EE}	–22.0 to +0.3	V
Supply voltage 3	V_0, V_2, V_3, V_5	V_{EE} –0.3 to V_{DD} +0.3	V
Input voltage	V_I	V_{SS} –0.3 to V_{DD} +0.3	V
Output voltage	V_O	V_{SS} –0.3 to V_{DD} +0.3	V
EIO output current	I01	20	mA
Operating temperature	Topr	–40 to +85	°C
Storage temperature 1	Tstg1	–65 to +150	°C
Storage temperature 2	Tstg2	–55 to +100	°C

Notes: 1. All voltages are given relative to V_{DD} = 0 V.
2. For storage temperature 1 – Plastic package
For storage temperature 2 – TAB mounted
3. V_0, V_2, V_3, and V_5 must satisfy the condition
$V_{DD} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq V_{EE}$



4. If the logic power is being floated or if the Vss voltage exceeds -2.5 Vdc during LCD power-on, the LSI chips may be damaged permanently. Take care not to damage the chips especially in the system power on/off sequence.

8. ELECTRICAL CHARACTERISTICS

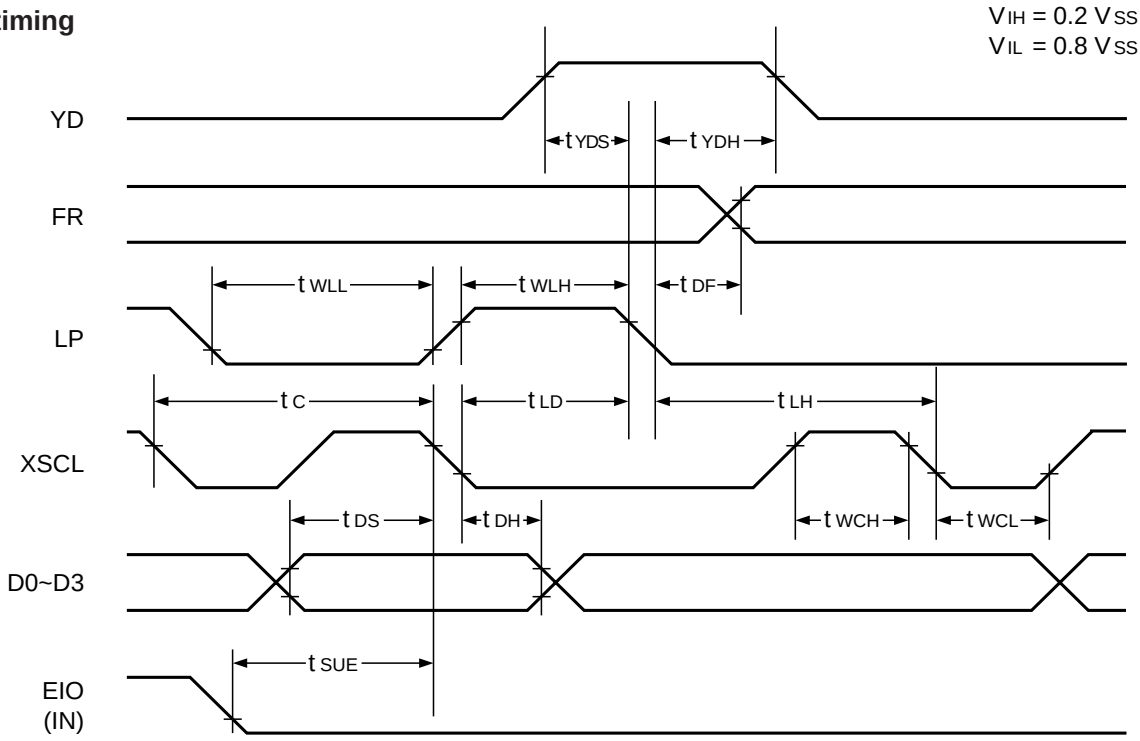
DC Characteristics

V_{DD} = V_0 = 0 V, V_{SS} = –5.0 V ±10%, Ta = –40 to 85°C

Item		Symbol	Condition		Min.	Typ.	Max.	Unit	Pin
Supply voltage (1)		V_{SS}			–5.5	–5.0	–2.7	V	V_{SS}
Recommended operation voltage		V_{EE}	V_{SS} = –2.7 to –5.5V		–20.0		–8.0	V	V_{EE}
Supply voltage (2)		V_0	Recommended value		V_{DD} –2.5		V_{DD}	V	V_0
Supply voltage (3)		V_2	Recommended value		2/9 V_{EE}			V	V_2
Supply voltage (4)		V_3	Recommended value				7/9 V_{EE}	V	V_3
Supply voltage (5)		V_5	Recommended value		V_{EE}		V_{EE} +2.5	V	V_5
Input high voltage		V_{IH}	V_{SS} = –2.7 to –5.5V		0.2•V_{SS}			V	EIO1, EIO2, FR, D0 to D3, YD, LP, SHL, DOFF, XSCL
Input low voltage		V_{IL}					0.8•V_{SS}	V	
Output high voltage		V_{OH}	V_{SS} = –2.7	I_{OH} = –0.6mA	V_{DD} –0.4			V	EIO1, EIO2
Output low voltage		V_{OL}	to –5.5 V	I_{OL} = 0.6mA			V_{DD} +0.4	V	
Input leakage current		I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$				2.0	µA	D_0 to D_3, LP, FR, YD, XSCL, SHL, DOFF
I/O leakage current		$I_{LI/O}$	$V_{SS} \le V_{IN} \le V_{DD}$				5.0	µA	EIO1, EIO2
Static current		I_{SS}	V_5 = –20.0 to –10.0 V V_{IH} = V_{DD}, V_{IL} = V_{SS}				25	µA	V_{SS}
On resistance		R_{SEG}	ΔV_{ON} = 0.5 V, V_0 = V_{DD}, V_3 = 7/9•V_{EE}, V_2 = 2/9•V_{EE} V_{EE} = V_5 = –14.0 V			1.0	1.4	kΩ	X1 to X80
Average current consumption (1)	Data transfer mode	I_{DDT}	V_{SS} = –5.0 V, V_{IH} = V_{DD} V_{IL} = V_{SS}, f_{XSCL} = 4.0 MHz f_{LP} = 14 kHz, f_{FR} = 70 Hz Checkered pattern, non-burden V_{DD} = V_0 = 0V V_2 = –4 V V_3 = –16 V, V_{EE} = V_5 = –20 V			0.3	0.8	mA	V_{DD}
	Self-refresh mode	I_{DDS}	f_{XSCL} = 0 Hz = V_{SS} Another place is same as I_{DDT} item			70	200	µA	
Average current consumption (2)		I_{EE}	V_{SS} = –5.0 V, V_0 = 0.0 V V_2 = –4 V, V_3 = –16 V I_{EE} = V_5 = –20.0 V Another place is same as I_{DDT} item			25	70	µA	V_{EE}
Input capacitance		C_I	Freq. = 1 MHz, Ta = 25°C Simple substance of CHIP				8	pF	D_0 to D_3, LP, FR, YD, XSCL, SHL, DOFF
I/O capacitance		$C_{I/O}$					15	pF	EIO1, EIO2

AC Timing

Input timing



VSS = –5.0 V ±10%, Ta = –40 to 85°C

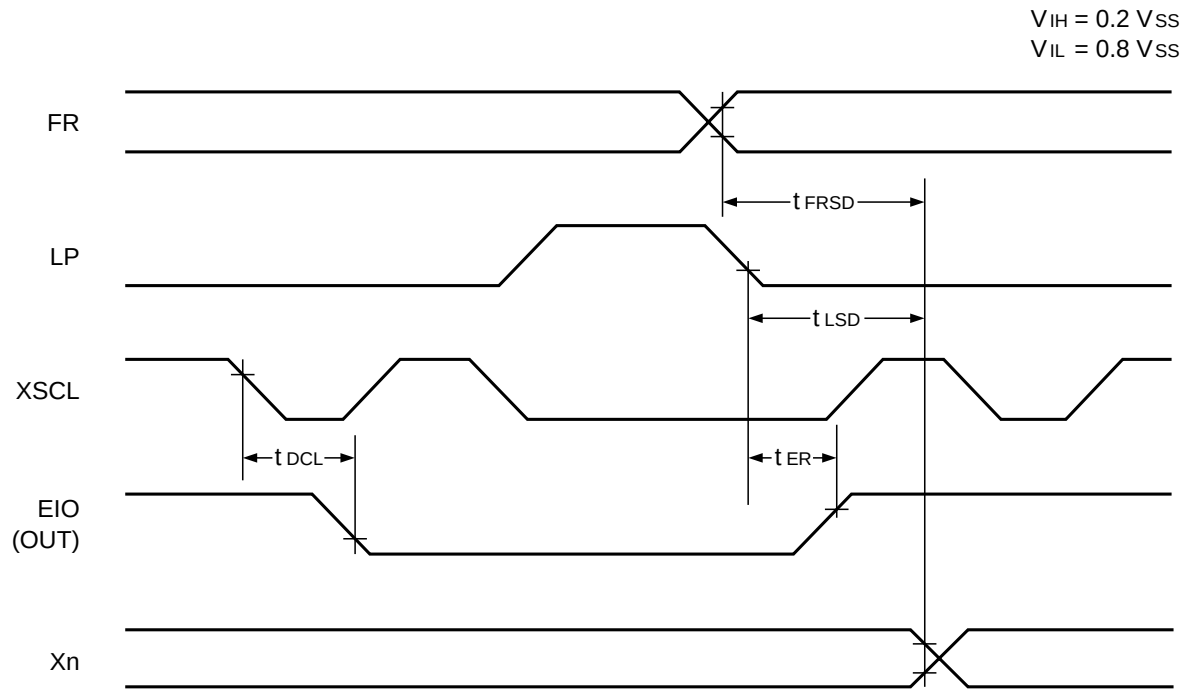
Item	Symbol	Condition	Min.	Max.	Unit
XSCL cycle time	t_C		150		ns
XSCL high level pulse width	t_{WCH}		30		ns
XSCL low level pulse width	t_{WCL}		30		ns
Data setup time	t_{DS}		20		ns
Data hold time	t_{DH}		15		ns
XSCL ↓ → LP ↓	t_{LD}		10		ns
LP ↓ → XSCL ↓	t_{LH}		70		ns
LP high level pulse width	t_{WLH}	*	40		ns
LP low level pulse width	t_{WLL}		600		ns
FR phase difference	t_{DF}		–300	+300	ns
EIO setup time	t_{SUE}		35		ns
YD setup time	t_{YDS}		40		ns
YD hold time	t_{YDH}		40		ns
Rise/fall time	t_r, t_f			30	ns

VSS = –4.5 V to –2.7 V, Ta = –40 to 85°C

Item	Symbol	Condition	Min.	Max.	Unit
XSCL cycle time	t_C		250		ns
XSCL high level pulse width	t_{WCH}		70		ns
XSCL low level pulse width	t_{WCL}		70		ns
Data setup time	t_{DS}		50		ns
Data hold time	t_{DH}		50		ns
XSCL ↓ → LP ↓	t_{LD}		80		ns
LP ↓ → XSCL ↓	t_{LH}		140		ns
LP high level pulse width	t_{WLH}	*	75		ns
LP low level pulse width	t_{WLL}		1200		ns
FR phase difference	t_{DF}		–300	+300	ns
EIO setup time	t_{SUE}		50		ns
YD setup time	t_{YDS}		80		ns
YD hold time	t_{YDH}		80		ns
Rise/fall time	t_r, t_f			30	ns

*: Recommended t_{WLH} value = t_C

Output Timing



VDD = –5.0 ±10%, VEE = –8.0 to –20.0 V, Ta = –40 to 85°C

Item	Symbol	Condition		Min.	Max.	Unit
EIO reset time	t_{ER}	CL = 15 pF			90	ns
EIO output delay time	t_{DCL}	(EIO)	VSS = –2.7 V		55	ns
LP → Xn output delay time	t_{LSD}	CL = 100 pF			400	ns
FR → Xn output delay time	t_{FRSD}				400	ns

VDD = –4.5 V to –2.7 V, VEE = –8.0 to –20.0 V, Ta = –40 to 85°C

Item	Symbol	Condition		Min.	Max.	Unit
EIO reset time	t_{ER}	CL = 15 pF			150	ns
EIO output delay time	t_{DCL}	(EIO)	VSS = –2.7 V		95	ns
LP → Xn output delay time	t_{LSD}	CL = 100 pF			800	ns
FR → Xn output delay time	t_{FRSD}				800	ns

9. LCD DRIVER POWER SUPPLY

Generating LCD Drive Voltages

To obtain individual voltage levels for LCD driver, register-split the potential between V_{EE} – V_{DD} and drive the LCD with the voltage follower using the operation amplifier. When using an operation amplifier, V_0 and V_{DD}, V_5 and V_{EE} are separated.

However, if the potential of V_0 is lower than V_{DD} potential or V_5 is higher than V_{EE} and the potential difference increases, the LCD driver capability decreases. To avoid this, set V_{DD} and V_0 or V_5 and V_{EE} within 0 V to 2.5 V. If an operation amplifier is not used, connect V_0 and V_{DD}, V_5 and V_{EE}.

If there are direct resistors on the V_{EE} (V_{DD}) power line, voltage falls in V_{EE} (V_{DD}) at the LSI power pins. This is caused by I_{DD} (I_{EE}) at the time of signal change. As a result, the relationship ($V_{DD} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq V_{EE}$) for intermediate potential of LCD can not be maintained and the LSI may be damaged.

To insert a protective resistor, the voltage must be stabilized according to the capacity.

System Power-up

This LSI has high LCD drive voltage. As a result, if the logic power is being floated or if the V_{SS} voltage is kept above –2.5Vdc and high voltage is applied in the LCD driver, the LSI may be damaged because of the excess current.

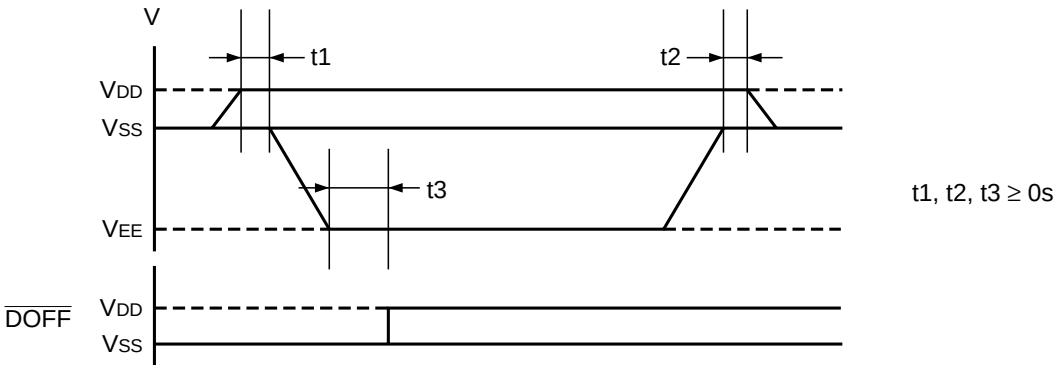
Until the LCD drive voltage is stabilized, use the display off function ($\overline{DOFF}$) to set the potential of the LCD drive output to V0 level.

Follow the sequence given below when turning the power on/off.

To turn on the power – Turn on the logic power
→ Turn the LCD driver on.
(On turn them on simultaneously.)

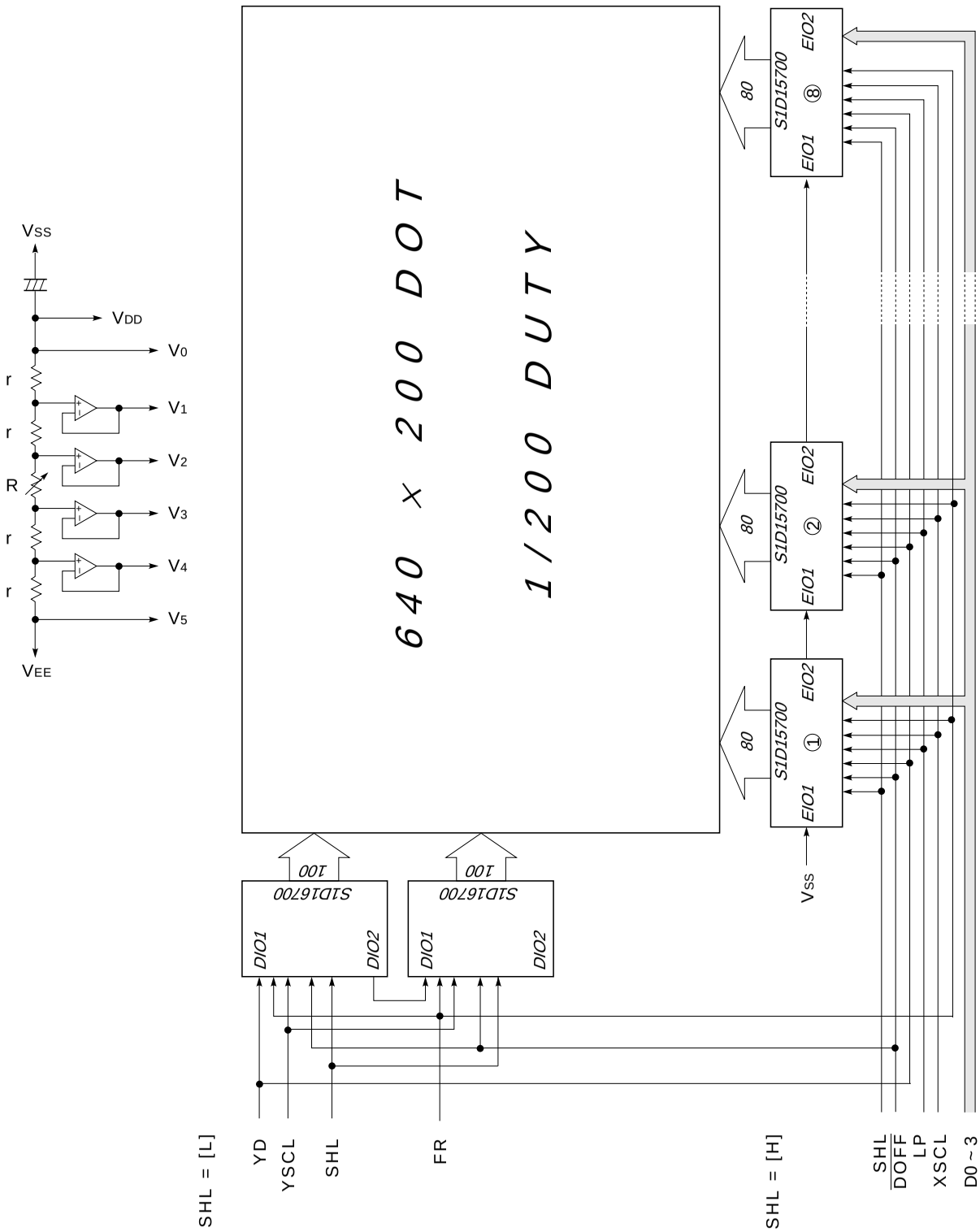
To turn off the power – Turn off the LCD driver
→ Turn off the logic power.
(Or turn them off simultaneously.)

To avoid excess current, insert the high-speed fuse in series with the LCD power. Select the appropriate value for a protective resistor according to the capacity of a LCD cell.



10. EXAMPLE OF APPLICATION

Constitution of LCD



10. S1D15705 Series

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1. DESCRIPTION

The S1D15705 series is a 1-chip dot matrix liquid crystal driver that can be connected to the bus of a microcomputer. It stores the 8-bit parallel or serial display data sent from the microcomputer in the built-in display data RAM and generates liquid crystal drive signals independently of the microcomputer. Since it incorporates 65 × 200 bits of the display data RAM and the one-dot pixel of the liquid crystal panel and one bit of the built-in RAM have a one-to-one correspondence, it enables display with the high degree of freedom.

The S1D15705 series incorporates 65 circuits of the common output and 168 circuits of the segment output and can display 65 × 168 dots (capable of displaying 10 columns × 4 rows of a 16 × 16 dot kanji font) using the single chip. The S1D15707 Series incorporates 33 circuits of the common output and 200 circuits of the segment output and can display 33 × 200 dots (capable of displaying 12 columns × 2 rows of a 16 × 16 dot kanji font). The S1D15708 series incorporates 17 circuits of the common output and 200 circuits of the segment output and can display 17 × 200 dots (capable of displaying 12 columns × 1 rows of a 16 × 16 dot kanji font). It can also expand the display capacity by using the two chips for the master and slave configuration.

Incorporating an analog temperature sensor circuit, the S1D15705∗10∗∗ can be used to constitute a system to provide optimum LCD contrast throughout a wide temperature range without need for use of supplementary parts such as the thermistor, under controls of a microcomputer.

Since the read/write operation of the display data RAM does not require external operation clocks, the S1D15705 series can be operated with the minimum current consumption. Since it also incorporates a liquid crystal drive power supply with low current consumption, liquid crystal drive power supply voltage adjusting resistor, and display clock CR oscillator circuit, it can provide a display system for high performance handy equipment with the minimum current consumption and the minimum parts configuration.

2. FEATURES

- Direct display of RAM data using the display data RAM
  RAM bit data "1" .... goes on.
  "0" .... goes off (at display normal rotation).
- RAM capacity
  65 × 200 = 13,000 bits
- Liquid crystal drive circuit
  The S1D15705 Series
  65 circuits for the common output and 168 circuits for the segment output
  The S1D15707 Series
  33 circuits for the common output and 200 circuits for the segment output
  The S1D15708 Series
  17 circuits for the common output and 200 circuits for the segment output
- High-speed 8-bit MPU interface (Both the 80 and 68 series MUPs can directly be connected.)/serial interface enabled
- Abundant command functions
  Display Data Read/Write, Display ON/OFF, Display Normal Rotation/Reversal, Page Address Set, Display Start Line Set, column address set, Status Read, Power Supply Save Display All Lighting ON/OFF, LCD Bias Set, Read Modify Write, Segment Driver Direction Select, Electronic Control, V_5 Voltage Adjusting Built-in Resistance Ratio Set, Static Indicator, n Line Alternating Current Reversal Drive, Common Output State Selection, and Built-in Oscillator Circuit ON
- Built-in static drive circuit for indicators (One set, blinking speed variable)
- Built-in power supply circuit for low power supply liquid crystal drive
  Booster circuit (Boosting magnification - double, triple, quadruple, boosting reference power supply external input enabled)
- 3% high accuracy alternating current voltage adjusting circuit (Temperature gradient: –0.05%/°C)
  Built-in V_5 voltage adjusting resistor, built-in V_1 to V4 voltage generation split resistors, built-in electronic control function, and voltage follower
- Built-in CR oscillator circuit (external clock input enabled)
- Ultra-low power consumption
- Built-in temperature sensor circuit (S1D15705D10B∗)
- Power supplies
  Logic power supply: $V_{DD} – V_{SS}$ = 2.4 to 3.6 V
  (S1D15705∗03∗∗, S1D15707∗03∗∗)
  $V_{DD} – V_{SS}$ = 3.6 to 5.5 V
  (S1D15705∗00∗∗, S1D15707∗00∗∗, S1D15708∗00∗∗)
  Boosting reference power supply: $V_{DD} – V_{SS}$ = 1.8 to 6.0 V
  Liquid crystal drive power supply: $V_5 – V_{DD}$ = –4.5 to –18.0 V (S1D15705∗∗∗∗∗) /–4.5 V to –16.0 V (S1D15707∗∗∗∗∗)/–4.5 V to –10.0 (S1D15708∗∗∗∗∗)
- Wide operating temperature range –40 to 85°C
- CMOS process
- Shipping form Bare chip, TCP
- No light-resistant and radiation-resistant design are provided.

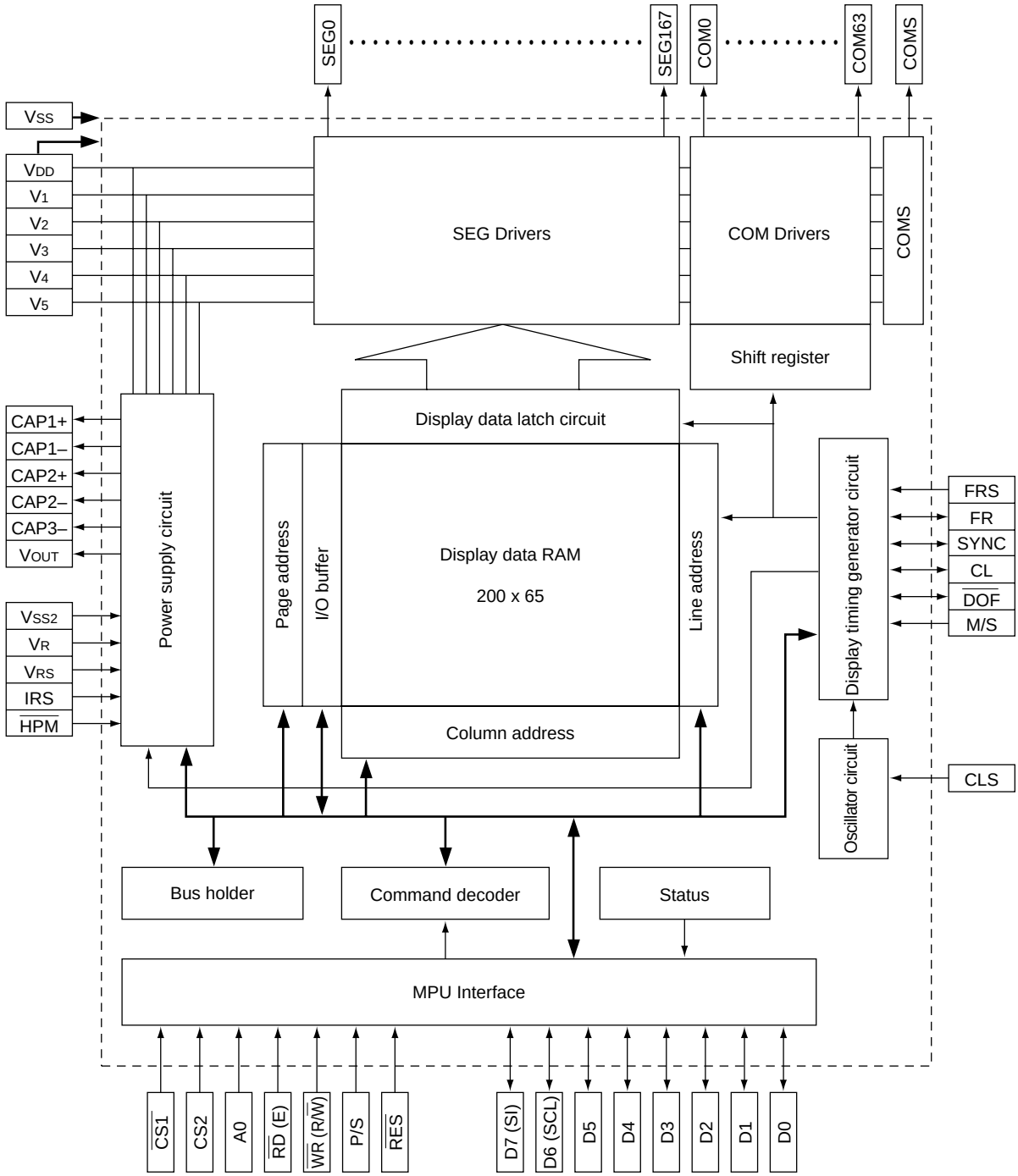
Series specification

Product name	Voltage [V]	Duty	Bias	SEG Dr	COM Dr	V_{REG} temperature gradient	Shipping form
S1D15705D00B*	–3.6 to –5.5	1/65	1/9, 1/7	168	65	–0.05%/°C	Bare chip
S1D15705D10B*	–3.6 to –5.5	1/65	1/9, 1/7	168	65	–0.05%/°C	Bare chip
S1D15705D03B*	–2.4 to –3.6	1/65	1/9, 1/7	168	65	–0.05%/°C	Bare chip
S1D15705T00A*	–3.6 to –5.5	1/65	1/9, 1/7	168	65	–0.05%/°C	TCP
S1D15705T03A*	–2.4 to –3.6	1/65	1/9, 1/7	168	65	–0.05%/°C	TCP
S1D15707D00B*	–3.6 to –5.5	1/33	1/6, 1/5	200	33	–0.05%/°C	Bare chip
S1D15707D03B*	–2.4 to –3.6	1/33	1/6, 1/5	200	33	–0.05%/°C	Bare chip
S1D15707T00**	–3.6 to –5.5	1/33	1/6, 1/5	200	33	–0.05%/°C	TCP
S1D15707T03**	–2.4 to –3.6	1/33	1/6, 1/5	200	33	–0.05%/°C	TCP
S1D15708D00B*	–3.6 to –5.5	1/17	1/6, 1/5	200	17	–0.05%/°C	Bare chip

Specifications for circuits other than the temperature sensor circuit are the same as those of the S1D15705D00B.

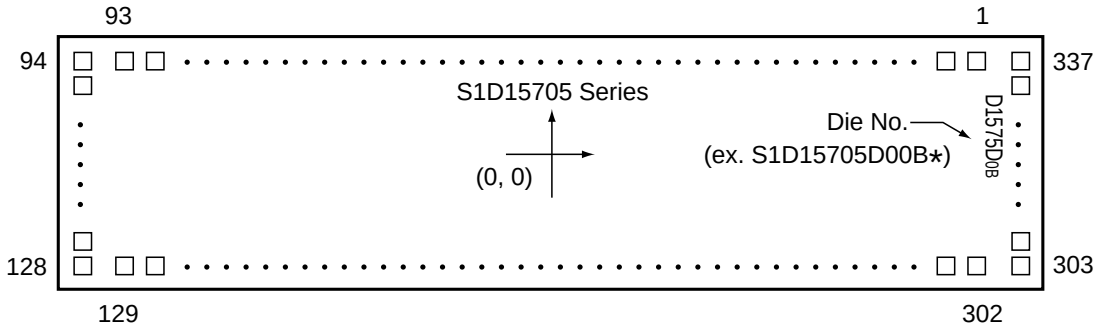
3. BLOCK DIAGRAM

Example : S1D15705*****



4. PAD

Pad layout



Item		Size X		Size Y	Unit
Chip size		13.30	×	2.81	mm
Chip thickness		0.625			mm
Bump pitch		71 (Min.)			µm
Bump size	PAD No.1 to 93	85	×	85	µm
	PAD No.94	85	×	73	µm
	PAD No.95 to 127	85	×	47	µm
	PAD No.128	85	×	73	µm
	PAD No.129	73	×	85	µm
	PAD No.130 to 301	47	×	85	µm
	PAD No.302	73	×	85	µm
	PAD No.303	86	×	73	µm
	PAD No.304 to 336	85	×	47	µm
	PAD No.337	85	×	73	µm
Bump height		17 (Typ.)			µm

S1D15705***** Pad Central Coordinates

Unit: μm

PAD No.	PIN Name	X	Y
1	(NC)	6195	1246
2	(NC)	6059	
3	SYNC	5922	
4	FRS	5786	
5	FR	5649	
6	CL	5513	
7	DOF	5376	
8	SYNC	5240	
9	VSS	5103	
10	CS1	4967	
11	CS2	4830	
12	VDD	4694	
13	RES	4557	
14	A0	4421	
15	VSS	4284	
16	WR, R/W	4148	
17	RD, E	4011	
18	VDD	3875	
19	D0	3738	
20	D1	3602	
21	D2	3465	
22	D3	3329	
23	D4	3192	
24	D5	3056	
25	D6 (SCL)	2919	
26	D7 (SI)	2783	
27	VDD	2646	
28	VDD	2512	
29	VDD	2378	
30	VDD	2245	
31	VDD	2111	
32	VSS	1977	
33	VSS	1843	
34	VSS	1709	
35	VSS2	1575	
36	VSS2	1441	
37	VSS2	1307	
38	VSS2	1173	
39	VSS2	1039	
40	(NC)	906	
41	VOUT	772	
42	VOUT	638	
43	CAP3–	504	
44	CAP3–	370	
45	(NC)	236	
46	CAP1+	102	
47	CAP1+	–32	
48	CAP1–	–166	
49	CAP1–	–300	
50	CAP2–	–433	
51	CAP2–	–567	1246
52	CAP2+	–701	
53	CAP2+	–835	
54	VSS	–969	
55	VSS	–1103	
56	VRS	–1237	
57	VRS	–1371	
58	VDD	–1505	
59	VDD	–1639	
60	V1	–1772	
61	V1	–1906	
62	V2	–2040	
63	V2	–2174	
64	(NC)	–2308	
65	V3	–2442	
66	V3	–2576	
67	V4	–2710	
68	V4	–2844	
69	V5	–2978	
70	V5	–3111	
71	(NC)	–3245	
72	VR	–3379	
73	TEST1	–3513	
74	TEST2	–3647	
75	TEST3	–3781	
76	TEST4	–3915	
77	VDD	–4049	
78	M/S	–4185	
79	CLS	–4322	
80	VSS	–4458	
81	C86	–4595	
82	P/S	–4731	
83	VDD	–4868	
84	HPM	–5004	
85	VSS	–5141	
86	IRS	–5277	
87	VDD	–5414	
88	TEST5	–5550	
89	TEST6	–5687	
90	TEST7	–5836	
91	TEST8	–5956	
92	TEST9	–6076	
93	(NC)	–6195	
94	(NC)	–6474	1248
95	COM31		1163
96	COM30		1090
97	COM29		1017
98	COM28		945
99	COM27		872
100	COM26		799
101	COM25	–6474	727
102	COM24		654
103	COM23		581
104	COM22		509
105	COM21		436
106	COM20		363
107	COM19		291
108	COM18		218
109	COM17		145
110	COM16		73
111	COM15		0
112	COM14		–73
113	COM13		–145
114	COM12		–218
115	COM11		–291
116	COM10		–363
117	COM9		–436
118	COM8		–509
119	COM7		–581
120	COM6		–654
121	COM5		–727
122	COM4		–800
123	COM3		–872
124	COM2		–945
125	COM1		–1018
126	COM0		–1090
127	COMS		–1163
128	(NC)		–1248
129	(NC)	–6232	–1246
130	(NC)	–6147	
131	(NC)	–6075	
132	SEG0	–6002	
133	SEG1	–5930	
134	SEG2	–5859	
135	SEG3	–5787	
136	SEG4	–5715	
137	SEG5	–5643	
138	SEG6	–5571	
139	SEG7	–5499	
140	SEG8	–5427	
141	SEG9	–5355	
142	SEG10	–5283	
143	SEG11	–5212	
144	SEG12	–5140	
145	SEG13	–5068	
146	SEG14	–4996	
147	SEG15	–4924	
148	SEG16	–4852	
149	SEG17	–4780	
150	SEG18	–4708	

Unit: μm

PAD No.	PIN Name	X	Y
151	SEG19	–4636	–1246
152	SEG20	–4564	
153	SEG21	–4493	
154	SEG22	–4421	
155	SEG23	–4349	
156	SEG24	–4277	
157	SEG25	–4205	
158	SEG26	–4133	
159	SEG27	–4061	
160	SEG28	–3989	
161	SEG29	–3917	
162	SEG30	–3846	
163	SEG31	–3774	
164	SEG32	–3702	
165	SEG33	–3630	
166	SEG34	–3558	
167	SEG35	–3486	
168	SEG36	–3414	
169	SEG37	–3342	
170	SEG38	–3270	
171	SEG39	–3199	
172	SEG40	–3127	
173	SEG41	–3055	
174	SEG42	–2983	
175	SEG43	–2911	
176	SEG44	–2839	
177	SEG45	–2767	
178	SEG46	–2695	
179	SEG47	–2623	
180	SEG48	–2552	
181	SEG49	–2480	
182	SEG50	–2408	
183	SEG51	–2336	
184	SEG52	–2264	
185	SEG53	–2192	
186	SEG54	–2120	
187	SEG55	–2048	
188	SEG56	–1976	
189	SEG57	–1905	
190	SEG58	–1833	
191	SEG59	–1761	
192	SEG60	–1689	
193	SEG61	–1617	
194	SEG62	–1545	
195	SEG63	–1473	
196	SEG64	–1401	
197	SEG65	–1329	
198	SEG66	–1258	
199	SEG67	–1186	
200	SEG68	–1114	

PAD No.	PIN Name	X	Y
201	SEG69	–1042	–1246
202	SEG70	–970	
203	SEG71	–898	
204	SEG72	–826	
205	SEG73	–754	
206	SEG74	–682	
207	SEG75	–611	
208	SEG76	–539	
209	SEG77	–467	
210	SEG78	–395	
211	SEG79	–323	
212	SEG80	–251	
213	SEG81	–179	
214	SEG82	–107	
215	SEG83	–35	
216	SEG84	36	
217	SEG85	108	
218	SEG86	180	
219	SEG87	252	
220	SEG88	324	
221	SEG89	396	
222	SEG90	468	
223	SEG91	540	
224	SEG92	612	
225	SEG93	683	
226	SEG94	755	
227	SEG95	827	
228	SEG96	899	
229	SEG97	971	
230	SEG98	1043	
231	SEG99	1115	
232	SEG100	1187	
233	SEG101	1259	
234	SEG102	1330	
235	SEG103	1402	
236	SEG104	1474	
237	SEG105	1546	
238	SEG106	1618	
239	SEG107	1690	
240	SEG108	1762	
241	SEG109	1834	
242	SEG110	1906	
243	SEG111	1977	
244	SEG112	2049	
245	SEG113	2121	
246	SEG114	2193	
247	SEG115	2265	
248	SEG116	2337	
249	SEG117	2409	
250	SEG118	2481	

PAD No.	PIN Name	X	Y
251	SEG119	2553	–1246
252	SEG120	2625	
253	SEG121	2696	
254	SEG122	2768	
255	SEG123	2840	
256	SEG124	2912	
257	SEG125	2984	
258	SEG126	3056	
259	SEG127	3128	
260	SEG128	3200	
261	SEG129	3272	
262	SEG130	3343	
263	SEG131	3415	
264	SEG132	3487	
265	SEG133	3559	
266	SEG134	3631	
267	SEG135	3703	
268	SEG136	3775	
269	SEG137	3847	
270	SEG138	3919	
271	SEG139	3990	
272	SEG140	4062	
273	SEG141	4134	
274	SEG142	4206	
275	SEG143	4278	
276	SEG144	4350	
277	SEG145	4422	
278	SEG146	4494	
279	SEG147	4566	
280	SEG148	4637	
281	SEG149	4709	
282	SEG150	4781	
283	SEG151	4853	
284	SEG152	4925	
285	SEG153	4997	
286	SEG154	5069	
287	SEG155	5141	
288	SEG156	5213	
289	SEG157	5284	
290	SEG158	5356	
291	SEG159	5428	
292	SEG160	5500	
293	SEG161	5572	
294	SEG162	5644	
295	SEG163	5716	
296	SEG164	5788	
297	SEG165	5860	
298	SEG166	5931	
299	SEG167	6003	
300	(NC)	6075	

Unit: μm

PAD No.	PIN Name	X	Y
301	(NC)	6147	–1246
302	(NC)	6232	↓
303	(NC)	6474	–1248
304	COM32		–1163
305	COM33		–1090
306	COM34		–1018
307	COM35		–945
308	COM36		–872
309	COM37		–800
310	COM38		–727
311	COM39		–654
312	COM40		–581
313	COM41		–509
314	COM42		–436
315	COM43		–363
316	COM44		–291
317	COM45		–218
318	COM46		–145
319	COM47		–73
320	COM48		0
321	COM49		73
322	COM50		145
323	COM51		218
324	COM52		291
325	COM53		363
326	COM54		436
327	COM55		509
328	COM56		581
329	COM57		654
330	COM58		727
331	COM59		799
332	COM60		872
333	COM61		945
334	COM62		1017
335	COM63		1090
336	COMS		1163
337	(NC)		1248

S1D15707***** Pad Central Coordinates

Unit: μm

PAD No.	PIN Name	X	Y
1	(NC)	6195	1246
2	(NC)	6059	
3	SYNC	5922	
4	FRS	5786	
5	FR	5649	
6	CL	5513	
7	DOF	5376	
8	SYNC	5240	
9	VSS	5103	
10	CS1	4967	
11	CS2	4830	
12	VDD	4694	
13	RES	4557	
14	A0	4421	
15	VSS	4284	
16	WR, R/W	4148	
17	RD, E	4011	
18	VDD	3875	
19	D0	3738	
20	D1	3602	
21	D2	3465	
22	D3	3329	
23	D4	3192	
24	D5	3056	
25	D6 (SCL)	2919	
26	D7 (SI)	2783	
27	VDD	2646	
28	VDD	2512	
29	VDD	2378	
30	VDD	2245	
31	VDD	2111	
32	VSS	1977	
33	VSS	1843	
34	VSS	1709	
35	VSS2	1575	
36	VSS2	1441	
37	VSS2	1307	
38	VSS2	1173	
39	VSS2	1039	
40	(NC)	906	
41	VOUT	772	
42	VOUT	638	
43	CAP3–	504	
44	CAP3–	370	
45	(NC)	236	
46	CAP1+	102	
47	CAP1+	–32	
48	CAP1–	–166	
49	CAP1–	–300	
50	CAP2–	–433	
51	CAP2–	–567	1246
52	CAP2+	–701	
53	CAP2+	–835	
54	VSS	–969	
55	VSS	–1103	
56	VRS	–1237	
57	VRS	–1371	
58	VDD	–1505	
59	VDD	–1639	
60	V1	–1772	
61	V1	–1906	
62	V2	–2040	
63	V2	–2174	
64	(NC)	–2308	
65	V3	–2442	
66	V3	–2576	
67	V4	–2710	
68	V4	–2844	
69	V5	–2978	
70	V5	–3111	
71	(NC)	–3245	
72	VR	–3379	
73	TEST1	–3513	
74	TEST2	–3647	
75	TEST3	–3781	
76	TEST4	–3915	
77	VDD	–4049	
78	M/S	–4185	
79	CLS	–4322	
80	VSS	–4458	
81	C86	–4595	
82	P/S	–4731	
83	VDD	–4868	
84	HPM	–5004	
85	VSS	–5141	
86	IRS	–5277	
87	VDD	–5414	
88	TEST5	–5550	
89	TEST6	–5687	
90	TEST7	–5836	
91	TEST8	–5956	
92	TEST9	–6076	
93	(NC)	–6195	
94	(NC)	–6474	1248
95	COM31		1163
96	COM30		1090
97	COM29		1017
98	COM28		945
99	COM27		872
100	COM26		799
101	COM25	–6474	727
102	COM24		654
103	COM23		581
104	COM22		509
105	COM21		436
106	COM20		363
107	COM19		291
108	COM18		218
109	COM17		145
110	COM16		73
111	COM15		0
112	COM14		–73
113	COM13		–145
114	COM12		–218
115	COM11		–291
116	COM10		–363
117	COM9		–436
118	COM8		–509
119	COM7		–581
120	COM6		–654
121	COM5		–727
122	COM4		–800
123	COM3		–872
124	COM2		–945
125	COM1		–1018
126	COM0		–1090
127	COMS		–1163
128	(NC)		–1248
129	(NC)	–6232	–1246
130	(NC)	–6147	
131	(NC)	–6075	
132	SEG0	–6002	
133	SEG1	–5930	
134	SEG2	–5859	
135	SEG3	–5787	
136	SEG4	–5715	
137	SEG5	–5643	
138	SEG6	–5571	
139	SEG7	–5499	
140	SEG8	–5427	
141	SEG9	–5355	
142	SEG10	–5283	
143	SEG11	–5212	
144	SEG12	–5140	
145	SEG13	–5068	
146	SEG14	–4996	
147	SEG15	–4924	
148	SEG16	–4852	
149	SEG17	–4780	
150	SEG18	–4708	

Unit: μm

PAD No.	PIN Name	X	Y
151	SEG19	–4636	–1246
152	SEG20	–4564	
153	SEG21	–4493	
154	SEG22	–4421	
155	SEG23	–4349	
156	SEG24	–4277	
157	SEG25	–4205	
158	SEG26	–4133	
159	SEG27	–4061	
160	SEG28	–3989	
161	SEG29	–3917	
162	SEG30	–3846	
163	SEG31	–3774	
164	SEG32	–3702	
165	SEG33	–3630	
166	SEG34	–3558	
167	SEG35	–3486	
168	SEG36	–3414	
169	SEG37	–3342	
170	SEG38	–3270	
171	SEG39	–3199	
172	SEG40	–3127	
173	SEG41	–3055	
174	SEG42	–2983	
175	SEG43	–2911	
176	SEG44	–2839	
177	SEG45	–2767	
178	SEG46	–2695	
179	SEG47	–2623	
180	SEG48	–2552	
181	SEG49	–2480	
182	SEG50	–2408	
183	SEG51	–2336	
184	SEG52	–2264	
185	SEG53	–2192	
186	SEG54	–2120	
187	SEG55	–2048	
188	SEG56	–1976	
189	SEG57	–1905	
190	SEG58	–1833	
191	SEG59	–1761	
192	SEG60	–1689	
193	SEG61	–1617	
194	SEG62	–1545	
195	SEG63	–1473	
196	SEG64	–1401	
197	SEG65	–1329	
198	SEG66	–1258	
199	SEG67	–1186	
200	SEG68	–1114	

PAD No.	PIN Name	X	Y
201	SEG69	–1042	–1246
202	SEG70	–970	
203	SEG71	–898	
204	SEG72	–826	
205	SEG73	–754	
206	SEG74	–682	
207	SEG75	–611	
208	SEG76	–539	
209	SEG77	–467	
210	SEG78	–395	
211	SEG79	–323	
212	SEG80	–251	
213	SEG81	–179	
214	SEG82	–107	
215	SEG83	–35	
216	SEG84	36	
217	SEG85	108	
218	SEG86	180	
219	SEG87	252	
220	SEG88	324	
221	SEG89	396	
222	SEG90	468	
223	SEG91	540	
224	SEG92	612	
225	SEG93	683	
226	SEG94	755	
227	SEG95	827	
228	SEG96	899	
229	SEG97	971	
230	SEG98	1043	
231	SEG99	1115	
232	SEG100	1187	
233	SEG101	1259	
234	SEG102	1330	
235	SEG103	1402	
236	SEG104	1474	
237	SEG105	1546	
238	SEG106	1618	
239	SEG107	1690	
240	SEG108	1762	
241	SEG109	1834	
242	SEG110	1906	
243	SEG111	1977	
244	SEG112	2049	
245	SEG113	2121	
246	SEG114	2193	
247	SEG115	2265	
248	SEG116	2337	
249	SEG117	2409	
250	SEG118	2481	

PAD No.	PIN Name	X	Y
251	SEG119	2553	–1246
252	SEG120	2625	
253	SEG121	2696	
254	SEG122	2768	
255	SEG123	2840	
256	SEG124	2912	
257	SEG125	2984	
258	SEG126	3056	
259	SEG127	3128	
260	SEG128	3200	
261	SEG129	3272	
262	SEG130	3343	
263	SEG131	3415	
264	SEG132	3487	
265	SEG133	3559	
266	SEG134	3631	
267	SEG135	3703	
268	SEG136	3775	
269	SEG137	3847	
270	SEG138	3919	
271	SEG139	3990	
272	SEG140	4062	
273	SEG141	4134	
274	SEG142	4206	
275	SEG143	4278	
276	SEG144	4350	
277	SEG145	4422	
278	SEG146	4494	
279	SEG147	4566	
280	SEG148	4637	
281	SEG149	4709	
282	SEG150	4781	
283	SEG151	4853	
284	SEG152	4925	
285	SEG153	4997	
286	SEG154	5069	
287	SEG155	5141	
288	SEG156	5213	
289	SEG157	5284	
290	SEG158	5356	
291	SEG159	5428	
292	SEG160	5500	
293	SEG161	5572	
294	SEG162	5644	
295	SEG163	5716	
296	SEG164	5788	
297	SEG165	5860	
298	SEG166	5931	
299	SEG167	6003	
300	(NC)	6075	

Unit: μm

PAD No.	PIN Name	X	Y
301	(NC)	6147	–1246
302	(NC)	6232	↓
303	(NC)	6474	–1248
304	SEG168		–1163
305	SEG169		–1090
306	SEG170		–1018
307	SEG171		–945
308	SEG172		–872
309	SEG173		–800
310	SEG174		–727
311	SEG175		–654
312	SEG176		–581
313	SEG177		–509
314	SEG178		–436
315	SEG179		–363
316	SEG180		–291
317	SEG181		–218
318	SEG182		–145
319	SEG183		–73
320	SEG184		0
321	SEG185		73
322	SEG186		145
323	SEG187		218
324	SEG188		291
325	SEG189		363
326	SEG190		436
327	SEG191		509
328	SEG192		581
329	SEG193		654
330	SEG194		727
331	SEG195		799
332	SEG196		872
333	SEG197		945
334	SEG198		1017
335	SEG199		1090
336	COMS		1163
337	(NC)		1248

S1D15708***** Pad Central Coordinates

Unit: μm

PAD No.	PIN Name	X	Y
1	(NC)	6159	1246
2	(NC)	6059	
3	SYNC	5922	
4	FRS	5786	
5	FR	5649	
6	CL	5513	
7	DOF	5376	
8	SYNC	5240	
9	VSS	5103	
10	CS1	4967	
11	CS2	4830	
12	VDD	4694	
13	RES	4557	
14	A0	4421	
15	VSS	4284	
16	WR,R/W	4148	
17	RD, E	4011	
18	VDD	3875	
19	D0	3738	
20	D1	3602	
21	D2	3465	
22	D3	3329	
23	D4	3192	
24	D5	3056	
25	D6 (SCL)	2919	
26	D7 (SI)	2783	
27	VDD	2646	
28	VDD	2512	
29	VDD	2378	
30	VDD	2245	
31	VDD	2111	
32	VSS	1977	
33	VSS	1843	
34	VSS	1709	
35	VSS2	1575	
36	VSS2	1441	
37	VSS2	1307	
38	VSS2	1173	
39	VSS2	1039	
40	(NC)	906	
41	VOUT	772	
42	VOUT	638	
43	CAP3–	504	
44	CAP3–	370	
45	(NC)	236	
46	CAP1+	102	
47	CAP1+	–32	
48	CAP1–	–166	
49	CAP1–	–300	
50	CAP2–	–433	
51	CAP2–	–567	1246
52	CAP2+	–701	
53	CAP2+	–835	
54	VSS	–969	
55	VSS	–1103	
56	VRS	–1237	
57	VRS	–1371	
58	VDD	–1505	
59	VDD	–1639	
60	V1	–1772	
61	V1	–1906	
62	V2	–2040	
63	V2	–2174	
64	(NC)	–2308	
65	V3	–2442	
66	V3	–2576	
67	V4	–2710	
68	V4	–2844	
69	V5	–2978	
70	V5	–3111	
71	(NC)	–3245	
72	VR	–3379	
73	TEST1	–3513	
74	TEST2	–3647	
75	TEST3	–3781	
76	TEST4	–3915	
77	VDD	–4049	
78	M/S	–4185	
79	CLS	–4322	
80	VSS	–4458	
81	C86	–4595	
82	P/S	–4731	
83	VDD	–4868	
84	HPM	–5004	
85	VSS	–5141	
86	IRS	–5277	
87	VDD	–5414	
88	TEST5	–5550	
89	TEST6	–5687	
90	TEST7	–5836	
91	TEST8	–5956	
92	TEST9	–6076	
93	(NC)	–6195	
94	(NC)	–6474	1248
95	COM15		1163
96	COM15		1090
97	COM14		1017
98	COM14		945
99	COM13		872
100	COM13		799
101	COM12	–6474	727
102	COM12		654
103	COM11		581
104	COM11		509
105	COM10		436
106	COM10		363
107	COM9		291
108	COM9		218
109	COM8		145
110	COM8		73
111	COM7		0
112	COM7		–73
113	COM6		–145
114	COM6		–218
115	COM5		–291
116	COM5		–363
117	COM4		–436
118	COM4		–509
119	COM3		–581
120	COM3		–654
121	COM2		–727
122	COM2		–800
123	COM1		–872
124	COM1		–945
125	COM0		–1018
126	COM0		–1090
127	COMS		–1163
128	(NC)		–1248
129	(NC)	–6232	–1246
130	(NC)	–6147	
131	(NC)	–6075	
132	SEG0	–6002	
133	SEG1	–5930	
134	SEG2	–5859	
135	SEG3	–5787	
136	SEG4	–5715	
137	SEG5	–5643	
138	SEG6	–5571	
139	SEG7	–5499	
140	SEG8	–5427	
141	SEG9	–5355	
142	SEG10	–5283	
143	SEG11	–5212	
144	SEG12	–5140	
145	SEG13	–5068	
146	SEG14	–4996	
147	SEG15	–4924	
148	SEG16	–4852	
149	SEG17	–4780	
150	SEG18	–4708	

Unit: μm

PAD No.	PIN Name	X	Y
151	SEG19	–4636	–1246
152	SEG20	–4564	
153	SEG21	–4493	
154	SEG22	–4421	
155	SEG23	–4349	
156	SEG24	–4277	
157	SEG25	–4205	
158	SEG26	–4133	
159	SEG27	–4061	
160	SEG28	–3989	
161	SEG29	–3917	
162	SEG30	–3846	
163	SEG31	–3774	
164	SEG32	–3702	
165	SEG33	–3630	
166	SEG34	–3558	
167	SEG35	–3486	
168	SEG36	–3414	
169	SEG37	–3342	
170	SEG38	–3270	
171	SEG39	–3199	
172	SEG40	–3127	
173	SEG41	–3055	
174	SEG42	–2983	
175	SEG43	–2911	
176	SEG44	–2839	
177	SEG45	–2767	
178	SEG46	–2695	
179	SEG47	–2623	
180	SEG48	–2552	
181	SEG49	–2480	
182	SEG50	–2408	
183	SEG51	–2336	
184	SEG52	–2264	
185	SEG53	–2192	
186	SEG54	–2120	
187	SEG55	–2048	
188	SEG56	–1976	
189	SEG57	–1905	
190	SEG58	–1833	
191	SEG59	–1761	
192	SEG60	–1689	
193	SEG61	–1617	
194	SEG62	–1545	
195	SEG63	–1473	
196	SEG64	–1401	
197	SEG65	–1329	
198	SEG66	–1258	
199	SEG67	–1186	
200	SEG68	–1114	

PAD No.	PIN Name	X	Y
201	SEG69	–1042	–1246
202	SEG70	–970	
203	SEG71	–898	
204	SEG72	–826	
205	SEG73	–754	
206	SEG74	–682	
207	SEG75	–611	
208	SEG76	–539	
209	SEG77	–467	
210	SEG78	–395	
211	SEG79	–323	
212	SEG80	–251	
213	SEG81	–179	
214	SEG82	–107	
215	SEG83	–35	
216	SEG84	36	
217	SEG85	108	
218	SEG86	180	
219	SEG87	252	
220	SEG88	324	
221	SEG89	396	
222	SEG90	468	
223	SEG91	540	
224	SEG92	612	
225	SEG93	683	
226	SEG94	755	
227	SEG95	827	
228	SEG96	899	
229	SEG97	971	
230	SEG98	1043	
231	SEG99	1115	
232	SEG100	1187	
233	SEG101	1259	
234	SEG102	1330	
235	SEG103	1402	
236	SEG104	1474	
237	SEG105	1546	
238	SEG106	1618	
239	SEG107	1690	
240	SEG108	1762	
241	SEG109	1834	
242	SEG110	1906	
243	SEG111	1977	
244	SEG112	2049	
245	SEG113	2121	
246	SEG114	2193	
247	SEG115	2265	
248	SEG116	2337	
249	SEG117	2409	
250	SEG118	2481	

PAD No.	PIN Name	X	Y
251	SEG119	2553	–1246
252	SEG120	2625	
253	SEG121	2696	
254	SEG122	2768	
255	SEG123	2840	
256	SEG124	2912	
257	SEG125	2984	
258	SEG126	3056	
259	SEG127	3128	
260	SEG128	3200	
261	SEG129	3272	
262	SEG130	3343	
263	SEG131	3415	
264	SEG132	3487	
265	SEG133	3559	
266	SEG134	3631	
267	SEG135	3703	
268	SEG136	3775	
269	SEG137	3847	
270	SEG138	3919	
271	SEG139	3990	
272	SEG140	4062	
273	SEG141	4134	
274	SEG142	4206	
275	SEG143	4278	
276	SEG144	4350	
277	SEG145	4422	
278	SEG146	4494	
279	SEG147	4566	
280	SEG148	4637	
281	SEG149	4709	
282	SEG150	4781	
283	SEG151	4853	
284	SEG152	4925	
285	SEG153	4997	
286	SEG154	5069	
287	SEG155	5141	
288	SEG156	5213	
289	SEG157	5284	
290	SEG158	5356	
291	SEG159	5428	
292	SEG160	5500	
293	SEG161	5572	
294	SEG162	5644	
295	SEG163	5716	
296	SEG164	5788	
297	SEG165	5860	
298	SEG166	5931	
299	SEG167	6003	
300	(NC)	6075	

Unit: µm

PAD No.	PIN Name	X	Y
301	(NC)	6147	–1246
302	(NC)	6232	↓
303	(NC)	6474	–1248
304	SEG168		–1163
305	SEG169		–1090
306	SEG170		–1018
307	SEG171		–945
308	SEG172		–872
309	SEG173		–800
310	SEG174		–727
311	SEG175		–654
312	SEG176		–581
313	SEG177		–509
314	SEG178		–436
315	SEG179		–363
316	SEG180		–291
317	SEG181		–218
318	SEG182		–145
319	SEG183		–73
320	SEG184		0
321	SEG185		73
322	SEG186		145
323	SEG187		218
324	SEG188		291
325	SEG189		363
326	SEG190		436
327	SEG191		509
328	SEG192		581
329	SEG193		654
330	SEG194		727
331	SEG195		799
332	SEG196		872
333	SEG197		945
334	SEG198		1017
335	SEG199		1090
336	COMS		1163
337	(NC)		1248

5. PIN DESCRIPTION

Power Supply Pin

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>V_{DD}</td><td>Power supply</td><td>Commonly used with the MPU power supply pin V_{CC}.</td><td>12</td></tr>
<tr><td>V_{SS}</td><td>Power supply</td><td>0 V pin connected to the system ground (GND).</td><td>9</td></tr>
<tr><td>V_{SS2}</td><td>Power supply</td><td>Boosting circuit reference power supply for liquid crystal drive.</td><td>5</td></tr>
<tr><td>V_{RS}</td><td>Power supply</td><td>External input pin for liquid crystal power supply voltage adjusting circuit.
They are set to OPEN.</td><td>2</td></tr>
<tr><td>V_1, V_2
V_3, V_4
V_5</td><td>Power supply</td><td>Multi-level power supply for liquid crystal drive. The voltage specified according to liquid crystal cells is impedance-converted by a split resistor or operation amplifier (OP amp) and applied. The potential needs to be specified based on V_{DD} to establish the relationship of dimensions shown below:
V_{DD} (=V_0) ≥ V_1 ≥ V_2 ≥ V_3 ≥ V_4 ≥ V_5
Master operation When the power supply is ON, the following voltages are applied to V_1 to V_4 from the built-in power supply circuit. The selection of the voltages is determined using the LCD bias set command.
<table>
<tr><th></th><th colspan="2">S1D15705***</th><th colspan="2">S1D15707***, S1D15708***</th></tr>
<tr><td>V_1</td><td>1/9•V_5</td><td>1/7•V_5</td><td>1/6•V_5</td><td>1/5•V_5</td></tr>
<tr><td>V_2</td><td>2/9•V_5</td><td>2/7•V_5</td><td>2/6•V_5</td><td>2/5•V_5</td></tr>
<tr><td>V_3</td><td>7/9•V_5</td><td>5/7•V_5</td><td>4/6•V_5</td><td>3/5•V_5</td></tr>
<tr><td>V_4</td><td>8/9•V_5</td><td>6/7•V_5</td><td>5/6•V_5</td><td>4/5•V_5</td></tr>
</table></td><td>10</td></tr>
</table>

LCD Power Supply Circuit Pin

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>CAP1+</td><td>O</td><td>Boosting capacitor positive side connecting pin. Connects a capacitor between the pin and CAP1– pin.</td><td>2</td></tr>
<tr><td>CAP1–</td><td>O</td><td>Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP1+ pin.</td><td>2</td></tr>
<tr><td>CAP2+</td><td>O</td><td>Boosting capacitor positive side connecting pin. Connects a capacitor between the pin and CAP2– pin.</td><td>2</td></tr>
<tr><td>CAP2–</td><td>O</td><td>Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP2+ pin.</td><td>2</td></tr>
<tr><td>CAP3–</td><td>O</td><td>Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP1+ pin.</td><td>2</td></tr>
<tr><td>V_{OUT}</td><td>O</td><td>Boosting output pin. Connects a capacitor between the pin and V_{SS2}.</td><td>2</td></tr>
<tr><td>V_R</td><td>I</td><td>Voltage adjusting pin. Applies voltage between V_{DD} and V_5 using a split resistor.
Valid only when the V_5 voltage adjusting built-in resistor is not used (IRS=LOW)
Do not use VR when the V_5 voltage adjusting built-in resistor is used (IRS=HIGH)</td><td>1</td></tr>
</table>

System Bus Connecting Pins

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>D7 to D0
(SI)
(SCL)</td><td>I/O</td><td>An 8-bit bidirectional data bus is used to connect an 8-bit or 16-bit standard MPU data bus.
When the serial interface is selected (P/S=LOW),
D7: Serial data entry pin (SI)
D6: Serial clock input pin (SCL)
In this case, D0 to D5 are set to high impedance.
When Chip Select is in the non-active state, D0 to D7 are set to high impedance.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Normally the lowest order bit of the MPU address bus is connected to discriminate data / commands.
A0=HIGH: Indicates that D0 to D7 are display data.
A0=LOW: Indicates that D0 to D7 are control data.</td><td>1</td></tr>
<tr><td>RES</td><td>I</td><td>Initialized by setting $\overline{RES}$ to LOW.
Reset operation is performed at the $\overline{RES}$ signal level.</td><td>1</td></tr>
<tr><td>$\overline{CS1}$
CS2</td><td>I</td><td>Chip Select signal. When $\overline{CS1}$=LOW and CS2=HIGH, this signal becomes active and the input/output of data/commands is enabled.</td><td>2</td></tr>
<tr><td>$\overline{RD}$
(E)</td><td>I</td><td>• When the 80 series MPU is connected, active LOW is set.
Pin that connects the $\overline{RD}$ signal of the 80 series MPU. When this signal is LOW, the S1D15705 series data bus is set in the output state.
• When the 68 series MPU is connected, active HIGH is set.
68 series MPU enable clock input pin</td><td>1</td></tr>
<tr><td>WR
(R/$\overline{W}$)</td><td>I</td><td>• When the 80 series MPU is connected, active LOW is set.
Pin that connects the $\overline{WR}$ signal of the 80 series MPU. The data bus signal is latched on the leading edge of the $\overline{WR}$ signal.
• When the 68 series MPU is connected,
Read/write control signal input pin
R/$\overline{W}$=HIGH: Read operation
R/$\overline{W}$=LOW: Write operation</td><td>1</td></tr>
<tr><td>FRS</td><td>O</td><td>Output pin for static drive
Used together with the SYNC pin</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>MPU interface switching pin
C86=HIGH: 68 series MPU interface
C86=LOW: 80 series MPU interface</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>Switching pin for parallel data entry/serial data entry
P/S=HIGH: Parallel data entry
P/S=LOW: Serial data entry
According to the P/S state, the following table is given.
<table>
<tr><th>P/S</th><th>Data/ command</th><th>Data</th><th>Read/write</th><th>Serial clock</th></tr>
<tr><td>HIGH</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$, $\overline{WR}$</td><td></td></tr>
<tr><td>LOW</td><td>A0</td><td>SI (D7)</td><td>Write-only</td><td>SCL (D6)</td></tr>
</table>
When P/S=LOW, D0 to D5 are set to high impedance. D0 to D5 can be HIGH, LOW, or “OPEN”.
RD(E) and WR (R/W) are fixed to HIGH or LOW.
For the serial data entry, RAM display data cannot be read.</td><td>1</td></tr>
</table>

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>CLS</td><td>I</td><td>Pin that selects the validity/invalidity of the built-in oscillator circuit for display clocks.
CLS=HIGH: Built-in oscillator circuit valid
CLS=LOW: Built-in oscillator circuit invalid (external input)
When CLS=LOW, display clocks are input from the CL pin.
When the S1D15705 series is used for the master/slave configuration, each of the CLS pins is set to the same level together.
<table>
<tr><th>Display clock</th><th>Master</th><th>Slave</th></tr>
<tr><td>Built-in oscillator circuit used
External input</td><td>HIGH
LOW</td><td>HIGH
LOW</td></tr>
</table></td><td>1</td></tr>
<tr><td>M/S</td><td>I</td><td>Pin that selects the master/slave operation for the S1D15705 series. The liquid crystal display system is synchronized by outputting the timing signal required for the liquid crystal display for the master operation and inputting the timing signal required for the liquid crystal display for the slave operation.
M/S=HIGH : Master operation
M/S=LOW : Slave operation
According to the M/S and CLS states, the following table is given.
<table>
<tr><th>M/S</th><th>CLS</th><th>Oscillator circuit</th><th>Power supply circuit</th><th>CL</th><th>FR</th><th>SYNC</th><th>FRS</th><th>DOF</th></tr>
<tr><td>HIGH</td><td>HIGH
LOW</td><td>Valid
Invalid</td><td>Valid
Valid</td><td>Output
Input</td><td>Output
Output</td><td>Output
Output</td><td>Output
Output</td><td>Output
Output</td></tr>
<tr><td>LOW</td><td>HIGH
LOW</td><td>Invalid
Invalid</td><td>Invalid
Invalid</td><td>Input
Input</td><td>Input
Input</td><td>Input
Input</td><td>Output
Output</td><td>Input
Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock I/O pin
According to the M/S and CLS states, the following table is given.
<table>
<tr><th>M/S</th><th>CLS</th><th>CL</th></tr>
<tr><td>HIGH</td><td>HIGH
LOW</td><td>Output
Input</td></tr>
<tr><td>LOW</td><td>HIGH
LOW</td><td>Input
Input</td></tr>
</table>
When the S1D15705 series is used for the master/slave configuration, each CL pin is connected.</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>Liquid crystal alternating current signal I/O pin
M/S=HIGH : Output
M/S=LOW : Input
When the SED15705 series is used for the master/slave configuration, each FR pin is connected.</td><td>1</td></tr>
<tr><td>SYNC</td><td>I/O</td><td>Liquid crystal synchronizing current signal I/O pin
M/S=HIGH : Output
M/S=LOW : Input
When the S1D15705 series is used for the master/slave configuration, each SYNC pin is connected.</td><td>2</td></tr>
<tr><td>$\overline{DOF}$</td><td>I/O</td><td>Liquid crystal display blanking control pin
M/S=HIGH : Output
M/S=LOW : Input
When the S1D15705 series is used for the master/slave configuration, each $\overline{DOF}$ pin is connected.</td><td>1</td></tr>
<tr><td>IRS</td><td>I</td><td>V_5 voltage adjusting resistor selection pin
IRS=HIGH: Built-in resistor used
IRS=LOW: Built-in resistor not used. The V_5 voltage is adjusted by the VR pin and stand-alone split resistor.
Valid only at master operation. The pin is fixed to HIGH or LOW at slave operation.</td><td>1</td></tr>
<tr><td>$\overline{HPM}$</td><td>I</td><td>Power supply control pin of the power supply circuit for liquid crystal drive
$\overline{HPM}$=HIGH : Normal mode
$\overline{HPM}$=LOW : High power supply mode
Valid only at master operation. The pin is fixed to HIGH or LOW at slave operation.</td><td>1</td></tr>
</table>

Liquid Crystal Drive Pin

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>SEG0
to
SEGn</td><td>O</td><td>Output pins for the LCD segment drive.
For the pin assignment by model, refer to the table below.
<table>
<tr><th>Product name</th><th>SEG</th><th>Number of pins</th></tr>
<tr><td>S1D15705*****</td><td>SEG0 to SEG167</td><td>168</td></tr>
<tr><td>S1D15707*****/S1D15708*****</td><td>SEG0 to SEG199</td><td>200</td></tr>
</table>
Contents of the display RAM and FR signal are combined to select a desired level among V_{DD}, V_2, V_3 and V_5.
<table>
<tr><th rowspan="2">RAM data</th><th rowspan="2">FR</th><th colspan="2">Output voltage</th></tr>
<tr><th>Display normal operation</th><th>Display reversal</th></tr>
<tr><td>HIGH</td><td>HIGH</td><td>V_{DD}</td><td>V_2</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>V_5</td><td>V_3</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td>LOW</td><td>LOW</td><td>V_3</td><td>V_5</td></tr>
<tr><td>Power save</td><td>—</td><td colspan="2">V_{DD}</td></tr>
</table></td><td>168 or 200</td></tr>
<tr><td>COM0
to
COMn</td><td></td><td>Output pins for the LCD common drive.
For the pin assignment by model, refer to the table below.
<table>
<tr><th>Product name</th><th>SEG</th><th>Number of pins</th></tr>
<tr><td>S1D15705*****</td><td>COM0 to COM63</td><td>64</td></tr>
<tr><td>S1D15707*****</td><td>COM0 to COM31</td><td>32</td></tr>
<tr><td>S1D15708*****</td><td>COM0 to COM15</td><td>16</td></tr>
</table>
Scan data and FR signal are combined to select a desired level among V_{DD}, V_1, V_4 and V_5.
<table>
<tr><th>Scanning data</th><th>FR</th><th>Output voltage</th></tr>
<tr><td>HIGH</td><td>HIGH</td><td>V_5</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>V_{DD}</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>V_1</td></tr>
<tr><td>LOW</td><td>LOW</td><td>V_4</td></tr>
<tr><td>Power save</td><td>—</td><td>V_{DD}</td></tr>
</table></td><td>64 or 32
or 16</td></tr>
<tr><td>COMS</td><td>O</td><td>Indicator dedicated COM output pin. Set to OPEN when not used.
When COMS is used for the master/slave configuration, the same signal is output to both the master and slave.</td><td>2</td></tr>
</table>

Test Pin

Pin name	I/O	Description	Number of pins
TEST1 to 6	I/O	IC chip test pin. Fix the pin to HIGH. When using the temperature sensor with the S1D15705⋆10⋆⋆, refer to “Section 17. Temperature Sensor Circuit”.	6
TEST7 to 9	I/O	IC chip test pin. Take into consideration so that the capacity of lines cannot be exhausted by setting the pin to OPEN.	3

6. FUNCTION DESCRIPTION

MPU Interface

Selection of interface type

The S1D15705 series transfers data through 8-bit bidirectional data buses (D7 to D0) or serial data input (SI). By setting the polarity of the P/S pin to either HIGH or LOW, the 8-bit parallel data entry or serial data entry can be selected as listed in Table 1.

Table 1

P/S	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
HIGH: Parallel data entry	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
LOW: Serial data entry	$\overline{CS1}$	CS2	A0	—	—	—	SI	SCL	(HZ)

Fix — to HIGH or LOW. HZ indicates the high impedance state.

Parallel interface

When the parallel interface is selected (P/S=HIGH), the S1D15705 series can directly be connected to the MPU bus of either the 80 or 68 series MPU by setting the C86 pin to HIGH or LOW as listed in Table 2.

Table 2

C86	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0
H: 68 series MPU bus	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D7 to D0
L: 80 series MPU bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0

In addition, the data bus signal can be identified according to the combinations of the A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$) signals as listed in Table 3.

Table 3

Common	68 series	80 series		
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	Function
1	1	0	1	Display data read
1	0	1	0	Display data write
0	1	0	1	Status read
0	0	1	0	Control data write (command)

Serial interface

When the serial interface is selected (P/S=LOW), the serial data entry (SI) and serial clock input(SCL) can be accepted with the chip in the non-active state ($\overline{CS1}$=LOW or CS2=HIGH. The serial interface consists of an 8-bit shift register and a 3-bit counter. Serial data is fetched from the serial data entry pin in the order of D7, D6, ..., and D0 on the leading edge of the serial clock and converted into 8-bit parallel data on the leading edge of the 8th serial clock, then processed.
Whether to identify that the serial data entry is display data or command is judged by the A0 input, and A0=HIGH indicates display data and A0=LOW indicates the command. After the chip is set to the non-active state, the A0 input is read and identified at the timing on the 8 × n-th leading edge of the serial clock. Fig. 1 shows the signal chart of the serial interface.

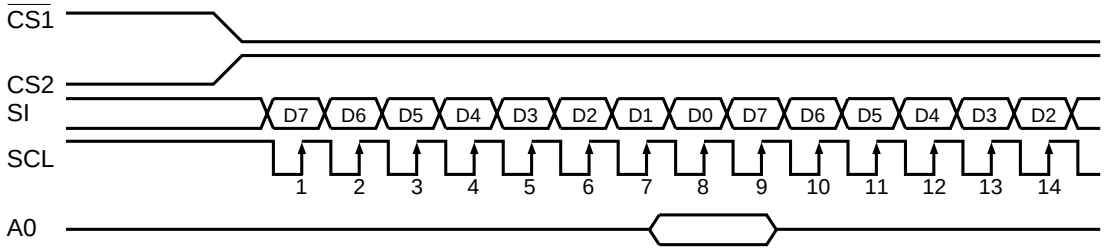


Fig. 1

- When the chip is in the non-active state, both the shift register and counter are reset to the initial state.
- Cannot be read for the serial interface.
- For the SCL signal, pay careful attention to the terminating reflection of lines and external noise. The operation confirmation using actual equipment is recommended.

Chip select

The S1D15705 series has two chip select pins $\overline{CS1}$ and CS2 and enables the MPU interface or serial interface only when $\overline{CS1}$=LOW and CS2=HIGH.
When Chip Select is in the non-active state, D0 to D7 are in the high impedance state and the A0, $\overline{RD}$, and $\overline{WR}$ inputs become invalid. When the serial interface is selected, the shift register and counter are reset.

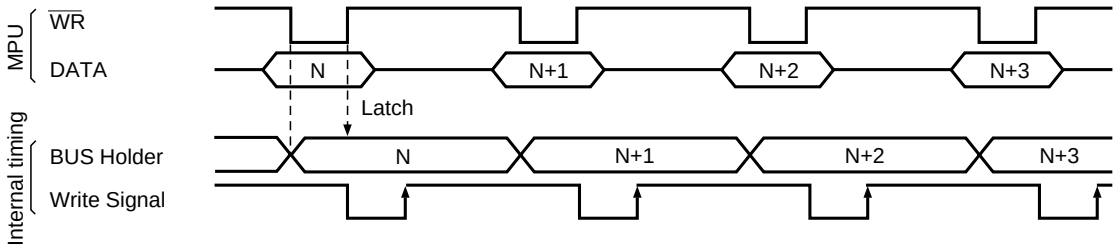
Display data RAM and internal register access

Since the S1D15705 series access viewed from the MUP side satisfies the cycle time and does not require the wait time, high-speed data transfer is enabled.
The S1D15705 series performs a kind of inter-LSI pipeline processing through the bus holder attached to the internal data bus when it performs the data transfer with the MPU.
For example, when data is written on the display data RAM, the data is first held in the bus holder and written on the display data RAM up to the next data write cycle. Further, when the MPU reads the contents of display data RAM, the read data at the first data read cycle (dummy) is held in the bus holder and read on the system bus from the bus holder up to the next data read cycle. The read sequence of the display data RAM is restricted. When the address is set, note that the specified address data is not output to the subsequent read instruction and output at the second data read. Therefore single dummy read is required after the address set and write cycle. Fig. 2 shows this relationship.

Busy flag

When the busy flag is "1", it indicates that the S1D15705 series is performing an internal operation, and only the status read instruction can be accepted. The busy flag is output to the D7 pin using the status read command. If the cycle time (t_{CYC}) is ensured, the MPU throughput can be improved greatly since this flag needs not be checked before each command.

• Write



• Read

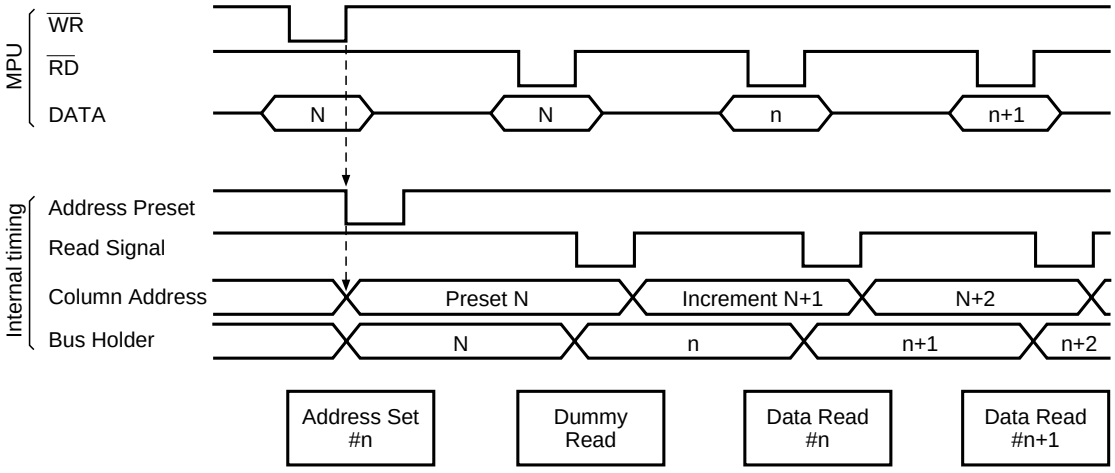


Fig. 2

Display Data RAM

Display data RAM

This display data RAM stores display dot data and consists of 65 (8 pages × one 8 bit + 1) × 200 bits. Desired bits can be accessed by specifying page and column addresses.
Since the MPU display data D7 to D0 correspond to the common direction of the liquid crystal display, the restrictions at display data transfer is reduced and the display configuration with the high degree of freedom can easily be obtained when the S1D15705 series is used for the multiple chip configuration.
Besides, the read/write operation to the display data RAM is performed through the I/O buffer from the MPU side independently of the liquid crystal drive signal read. Therefore even when the display data RAM is asynchronously accessed during liquid crystal display, the access will not have any adverse effect on the display such as flickering.

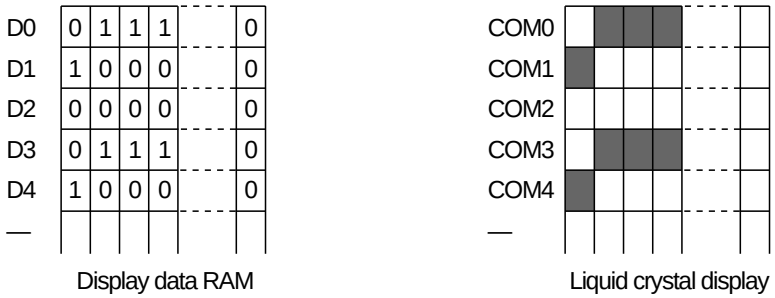


Fig. 3

Page address circuit

As shown in Fig. 4, the page address of the display data RAM is specified using the page address set command. To access the data using a new page, the page address is respecified.
The page address 8 (D3,D2,D1,D0=1,0,0,0) is an indicator dedicated RAM area and only the display data D0 is valid.

Column address circuit

As shown in Fig. 4, an address on the column side of the display data RAM is specified using the column address set command. Since the specified address is incremented by 1 whenever the display data read/write command is input, the MPU can successively access the display data.
Besides, the column address stops the increment at the column C7H. Since the column and page addresses are independent each other, for example, the page and column addresses need to be respecified respectively to move from the column C7H of page 0 and column 00H.
Further, as shown in Fig. 4, the correspondence relationship between the column address of the display data RAM and the segment address can be reversed using the ADC command (segment driver direction select command). Therefore the IC assignment restrictions at LCD module assembly are reduced.

Table 4

	S1D15705*****	S1D15707***** / S1D15708*****
SEG output	SEG0 SEG167	SEG0 SEG199
ADC "0"	0 (H)→ Column Address→ A7 (H)	0 (H)→ Column Address→ C7 (H)
(D0) "1"	C7 (H)←Column Address← 20 (H)	C7 (H)←Column Address ← 0 (H)

Line address circuit

When displaying contents of the display data RAM, the line address circuit is used for specifying the corresponding addresses. See Figure 4. Using the display start line address set command, the top line is normally selected (when the common output state is normal, COM0 is output. And, when reversed, the S1D15705***** outputs COM63, S1D15707***** outputs COM31 and S1D15708*****outputs COM15). For the S1D15705*****, the display area of 65 lines is secured starting from the specified display start line address in the address incrementing direction. And, 33 lines are provided for the S1D15707*****, 17 lines are provided for the S1D15708*****.
Dynamically changing the line address using the display start line address set command enables screen scrolling and page change.

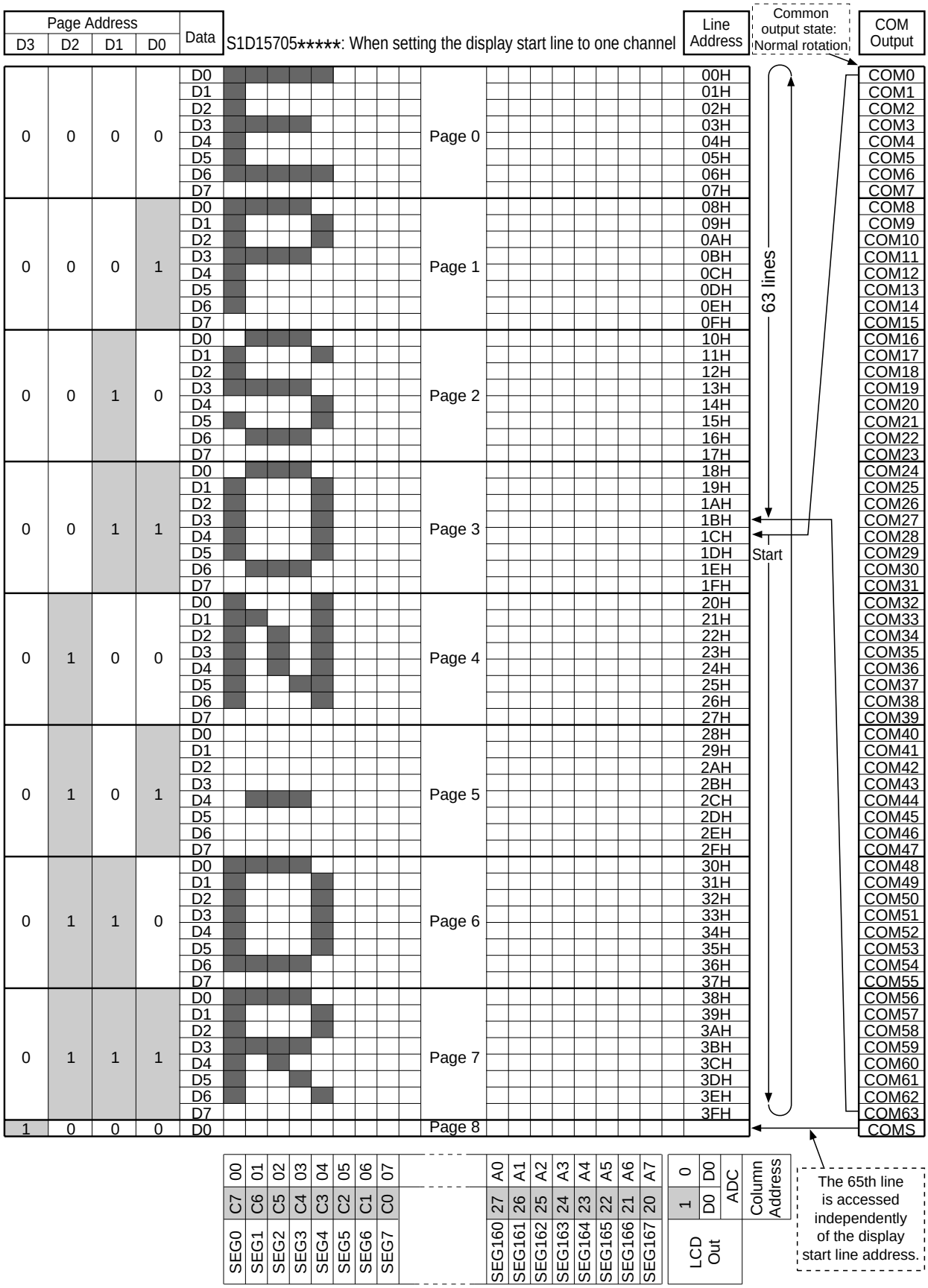

Page Address
D3 D2 D1 D0
Data
S1D15705*****: When setting the display start line to one channel
Line Address
Common output state: Normal rotation
COM Output
Page 0
Page 1
Page 2
Page 3
Page 4
Page 5
Page 6
Page 7
Page 8
63 lines
Start
The 65th line is accessed independently of the display start line address.
Column Address
ADC
LCD Out

Fig. 4

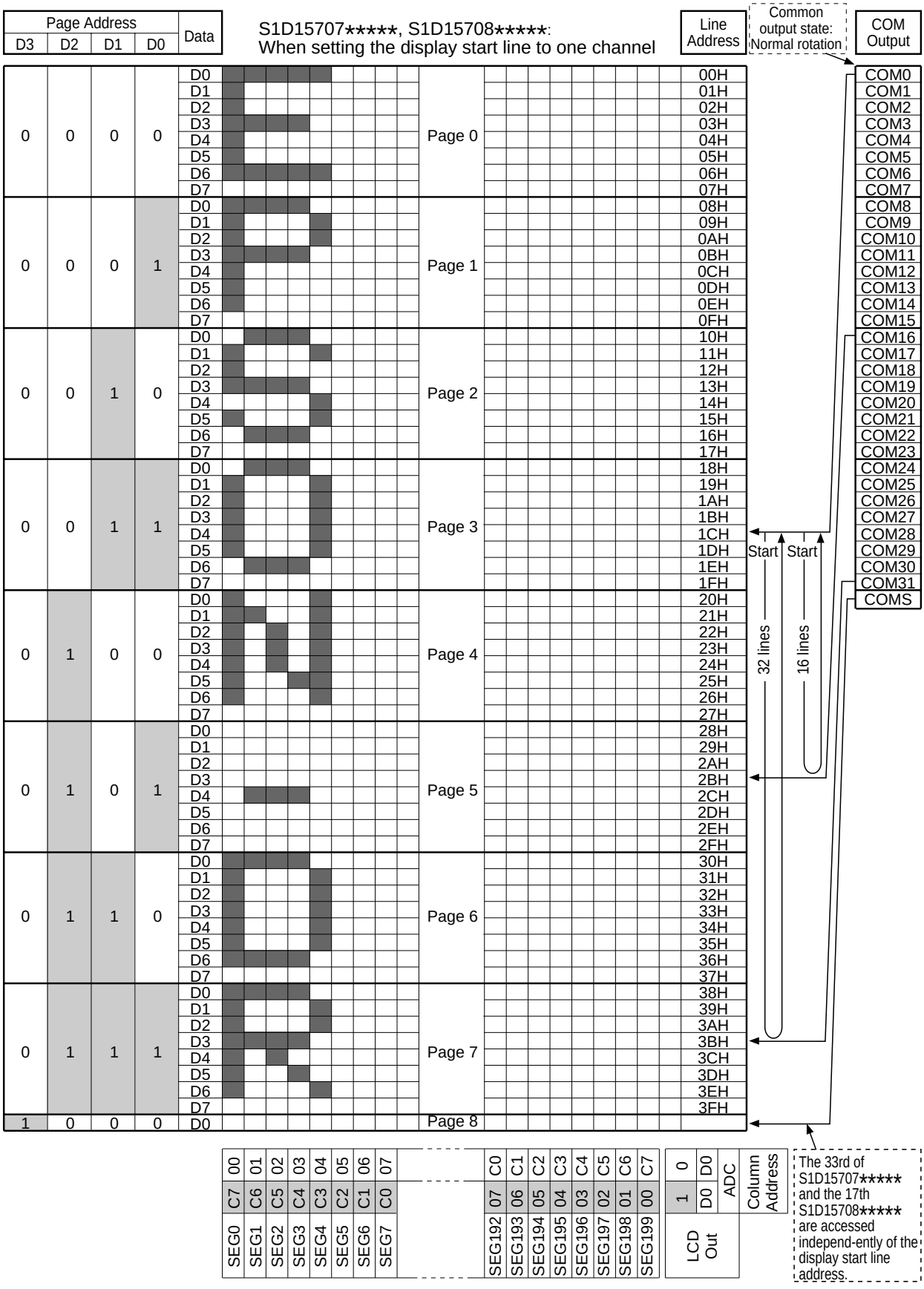

Page Address
D3 D2 D1 D0
Data
S1D15707*****, S1D15708*****:
When setting the display start line to one channel
Line Address
Common output state: Normal rotation
COM Output
Page 0
Page 1
Page 2
Page 3
Page 4
Page 5
Page 6
Page 7
Page 8
Start
Start
32 lines
16 lines
SEG0 SEG1 SEG2 SEG3 SEG4 SEG5 SEG6 SEG7
SEG192 SEG193 SEG194 SEG195 SEG196 SEG197 SEG198 SEG199
LCD Out
ADC
Column Address
The 33rd of S1D15707***** and the 17th S1D15708***** are accessed independ-ently of the display start line address.

Fig. 4-2

Display data latch circuit

The display data latch circuit is a latch that temporarily stores the display data output from the display data RAM to the liquid crystal drive circuit.
Since the Display Normal Rotation/Reversal, Display ON/OFF, and Display All Lighting ON/OFF commands control the data in this latch, the data within the display data RAM is not changed.

Oscillator Circuit

This oscillator circuit is a CR type oscillator and generates display clocks. The oscillator circuit is valid only when M/S=HIGH and CLS=HIGH and starts oscillation after the Built-in Oscillator Circuit ON command is entered. When CLS=LOW, the oscillation is stopped and the display clocks are entered from the CL pin.

Display Timing Generator Circuit

This display timing generator circuit generates timing signals from the display clocks to the line address circuit and the display latch circuit. It latches the display data to the display data latch circuit and outputs it to the segment drive output pin by synchronizing to the display clocks. The read operation of display data to the liquid crystal drive circuit is completely independent of the access to the display data RAM from the MPU. Therefore even when the display data RAM is asynchronously accessed during liquid crystal display, the access will not have any adverse effect on the display such as flickering.
The circuit also generates the internal common timing, liquid crystal alternating current signal (FR), and synchronous signal (SYNC) from the display clocks.
As shown in Fig. 5, the FR normally generates the drive waveforms in the 2-frame alternating current drive system to the liquid crystal drive circuit. It can generate n-line reversal alternating current drive waveforms by setting data (n-1) to the n-line reversal drive register. If a display quality problem such as crosstalk occurs, it can be improved by using the n-line reversal alternating current drive waveforms. Determine the number of lines (n) to which alternating current is applied by actually displaying the liquid crystal.
SNYC is a signal that synchronizes the line counter and common timing generator circuit to the SYNC signal output side IC. Therefore the SYNC signal becomes a waveform at a duty ratio of 50% that synchronizes to the frame synchronization.
When the S1D15705 series is used for the multiple chip configuration, the slave side needs to supply the display timing signals (FR, SYNC, CL, and $\overline{DOF}$) from the master side.
Table 5 shows the state of FR, SYNC, CL, or $\overline{DOF}$.

Table 5

Operation mode		FR	SYNC	CL	DOF
Master (M/S=HIGH)	Built-in oscillator circuit valid (CLS=HIGH)	Output	Output	Output	Output
	Built-in oscillator circuit invalid (CLS=LOW)	Output	Output	Input	Output
Slave (M/S=LOW)	Built-in oscillator circuit valid (CLS=HIGH)	Input	Input	Input	Input
	Built-in oscillator circuit invalid (CLS=LOW)	Input	Input	Input	Input

2-frame alternating current drive waveforms

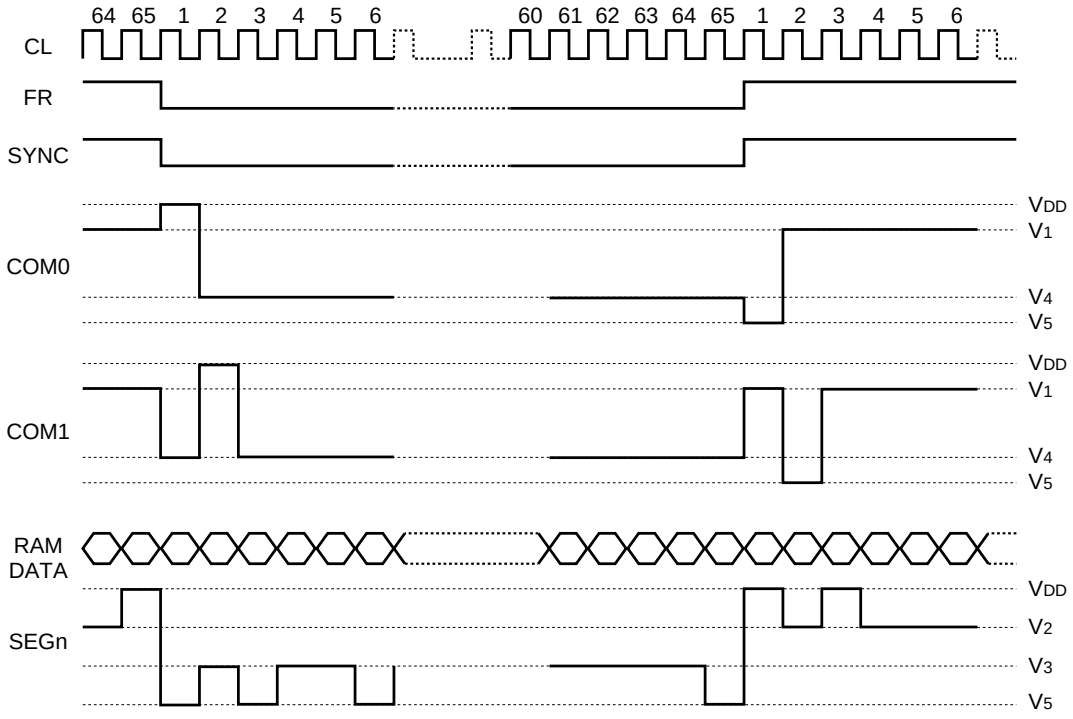


Fig. 5

n-line reversal alternating current drive waveforms (Example of n=5: when the line reversal register is set to 4)

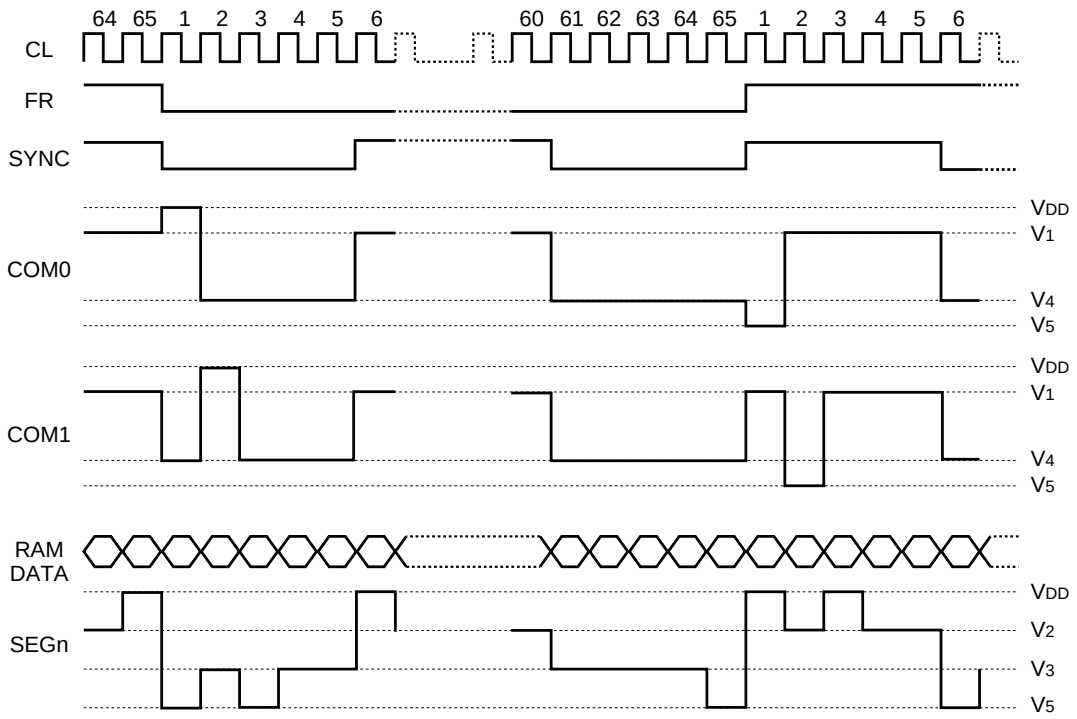


Fig. 6

Common Output State Selection Circuit

The S1D15705 series can set the scanning direction of the COM output using the common output state selection command (see Fig. 6). Therefore the IC assignment restrictions at LCD module assembly are reduced.

Table 6

State	COM scanning direction		
	S1D15705*****	S1D15707*****	S1D15708*****
Normal rotation	COM 0 → COM 63	COM 0 → COM 31	COM 0 → COM 15
Reversal	COM 63 → COM 0	COM 31 → COM 0	COM 15 → COM 0

Liquid Crystal Drive Circuit

These are a 233-channel (S1D15705***** and S1D15707*****), a 217-channel (S1D15708*****) multiplexers that generate four voltage levels for liquid crystal drive. It outputs the liquid crystal drive voltage that corresponds to the combinations of the display data, COM scanning signal, and FR signal.
Fig. 7 shows examples of the SEG and COM output waveforms.

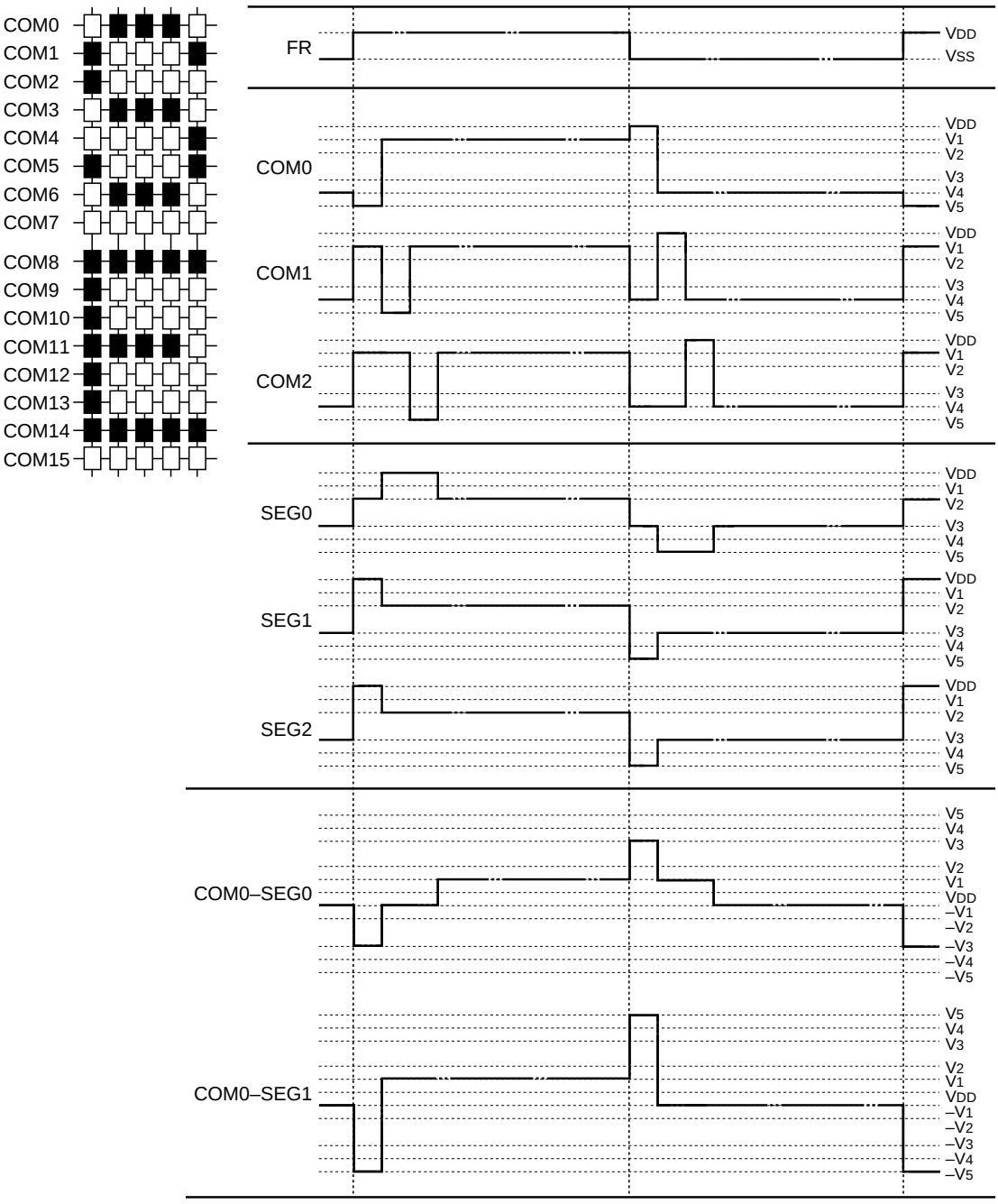

COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15
FR
VDD
VSS
COM0
COM1
COM2
V1
V2
V3
V4
V5
SEG0
SEG1
SEG2
COM0–SEG0
COM0–SEG1
–V1
–V2
–V3
–V4
–V5

Fig. 7

Power Supply Circuit

This power supply circuit is a low power supply consumption one that generates the voltage required for the liquid crystal drive and consists of a boosting circuit, voltage adjusting circuit, and voltage follower circuit. It is valid only at master operation.
The power supply circuit ON/OFF controls the boosting circuit, voltage adjusting circuit, and voltage follower circuit using the power supply control set command, respectively.
Therefore, it can also use the partial functions of the external power supply and built-in power supply together. Table 7 lists the functions that control 3-bit data using the power control set command and Table 8 lists the reference combinations.

Table 7 Description of controlling bits using the power control set command

Item		State "1"	State "0"
D2	Boosting circuit control bit	ON	OFF
D1	Voltage adjusting circuit (V adjusting circuit) control bit	ON	OFF
D0	Voltage follower circuit (V/F circuit) control bit	ON	OFF

Table 8 Reference combinations

Status of use	D2	D1	D0	Boosting circuit	V adjusting circuit	V/F circuit	External voltage input	Boosting system pin
① Built-in power supply used	1	1	1	O	O	O	V_{SS2}	Used
② V adjusting circuit and V/F circuit only	0	1	1	X	O	O	V_{OUT}, V_{SS2}	OPEN
③ V/F circuit only	0	0	1	X	X	O	V_5, V_{SS2}	OPEN
④ External power supply only	0	0	0	X	X	X	V_1 to V_5	OPEN

- The boosting system pin indicates the CAP1+, CAP1–, CAP2+, CAP2–, or CAP3– pin.
- Although the combinations other than those listed in the above table are also possible, they cannot be recommended because they are not actual use methods.

Boosting circuit

The boosting circuit incorporated in the S1D15705 series enables the quadruple boosting, triple boosting, and double boosting of the V_{DD} – V_{SS2} potential.
For the quadruple boosting, the $V_{DD} \leftrightarrow V_{SS2}$ potential is quadruple-boosted to the negative side and output to the V_{OUT} pin by connecting the capacitor C1 between CAP1+↔and CAP1–, between CAP2+↔ and CAP2–, between CAP1+↔ and CAP3–, and between V_{SS2}↔ and V_{OUT}.
For the triple boosting, the $V_{DD} \leftrightarrow V_{SS2}$ potential is triple-boosted to the negative side and output to the V_{OUT} pin by connecting the capacitor C1 between CAP1+↔ and CAP1–, between CAP2+↔ and CAP2–, and between V_{SS2}↔ and V_{OUT} and strapping both CAP3– and V_{OUT} pins.
For the double boosting, the $V_{DD} \leftrightarrow V_{SS2}$ potential is doubly boosted to the negative side and output to the V_{OUT} pin by connecting the capacitor C1 between CAP1+↔ and CAP1–, and between V_{SS2}↔, setting CAP2+ to OPEN, and V_{OUT} and strapping CAP2–, CAP3–, and V_{OUT} pins.
Fig. 8 shows the relationships of boosting potential.

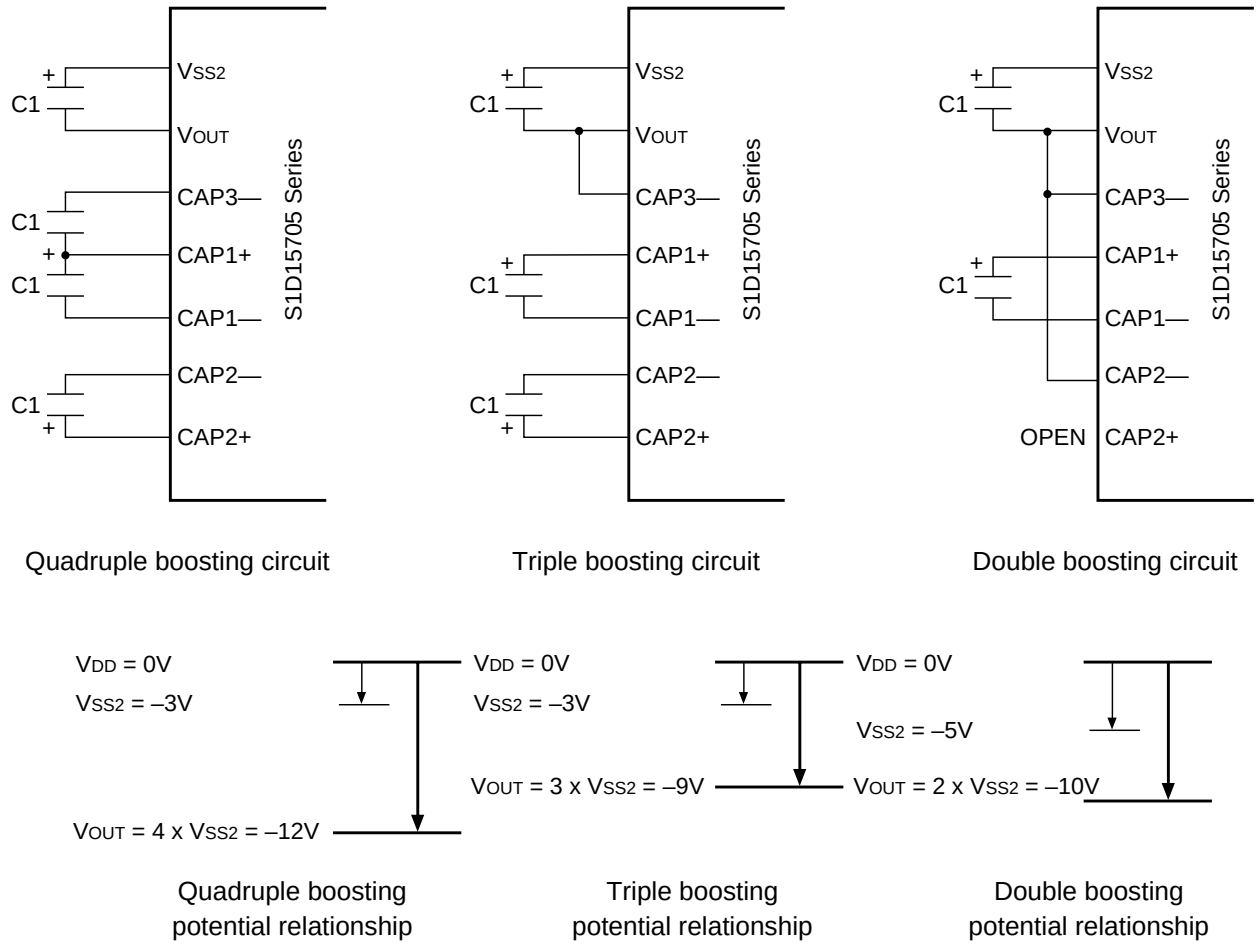


Fig. 8

- Set the VSS2" voltage range so that the voltage of the VOUT pin cannot exceed the absolute maximum ratings.

Voltage adjusting circuit

The boosting voltage generated in VOUT outputs the liquid crystal drive voltage V5 through the voltage adjusting circuit.
Since the S1D15705 series incorporates a high-accuracy constant power supply, 64-step electronic control function, and V5 voltage adjusting resistor, a high-accuracy voltage adjusting circuit can eliminate and save parts.

(A) When using the V5 voltage adjusting built-in resistor
The liquid crystal power supply voltage V5 can be controlled only using the command without an external resistor and the light and shade of liquid crystal display be adjusted by using the V5 voltage adjusting built-in resistor and the electronic control function.
The V5 voltage can be obtained according to Expression A-1 within the range of |V5|<|VOUT|.

$$V_5 = \left(1+\frac{Rb}{Ra}\right)\cdot V_{EV} = \left(1+\frac{Rb}{Ra}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG} \quad \left[\because V_{EV} = \left(1-\alpha/162\right)\cdot V_{REG}\right] \qquad \text{(Expression A-1)}$$

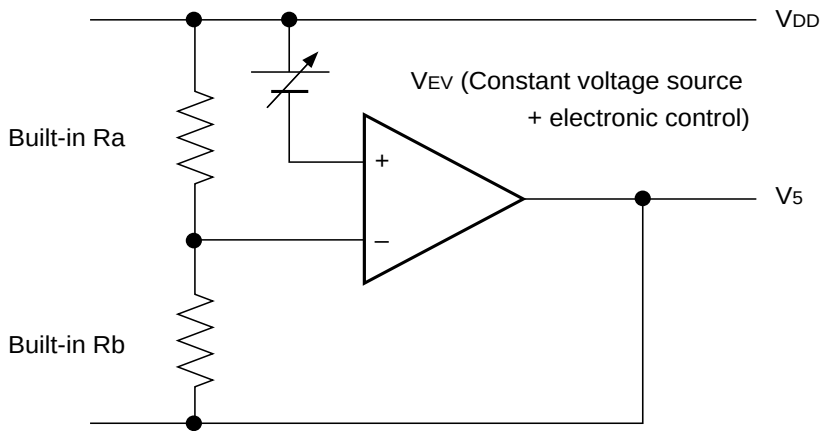


Fig. 9

VREG is a constant voltage source within an IC, and the value at Ta=25°C is constant as listed in Table 9.

Table 9

Device	Temperature gradient	Unit	VREG	Unit
Internal power supply	–0.05	[%/°C]	–2.1	[V]

α indicates an electronic control command value. Setting data in a 6-bit electronic control register enters one state among 64 states. Table 10 lists the values of α based on the setup of the electronic control register.

Table 10

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
			⋮			⋮
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

Rb/Ra indicates the V5 voltage adjusting built-in resistance ratio and can be adjusted into eight steps using the V5 voltage adjusting built-in resistance ratio set command. The reference values of the (1+Rb/Ra) ratio are obtained as listed in Table 11 by setting 3-bit data in the V5 voltage adjusting built-in resistance ratio register.

Table 11 (Reference values)

Register			S1D15705*****	S1D15707***** / S1D15708*****
			Device per temperature gradient [Unit: %/°C]	Device per temperature gradient [Unit: %/°C]
D2	D1	D0	–0.05	–0.05
0	0	0	4.5	3.0
0	0	1	5.0	3.5
0	1	0	5.5	4.0
0	1	1	6.0	4.5
1	0	0	6.5	5.0
1	0	1	7.0	5.5
1	1	0	7.6	6.0
1	1	1	8.1	6.5

It is necessary to take a manufacturing deviation of upto ±7% of the built-in resistance ratio into consideration. When this is not permissible, supplement external Ra and Rb to ajdust the V5 voltage.
Figs. 10 show the V5 voltage reference values per temperature gradient device based on the values of the V5 voltage adjusting built-in resistance ratio register and electronic control register at Ta=25°C.

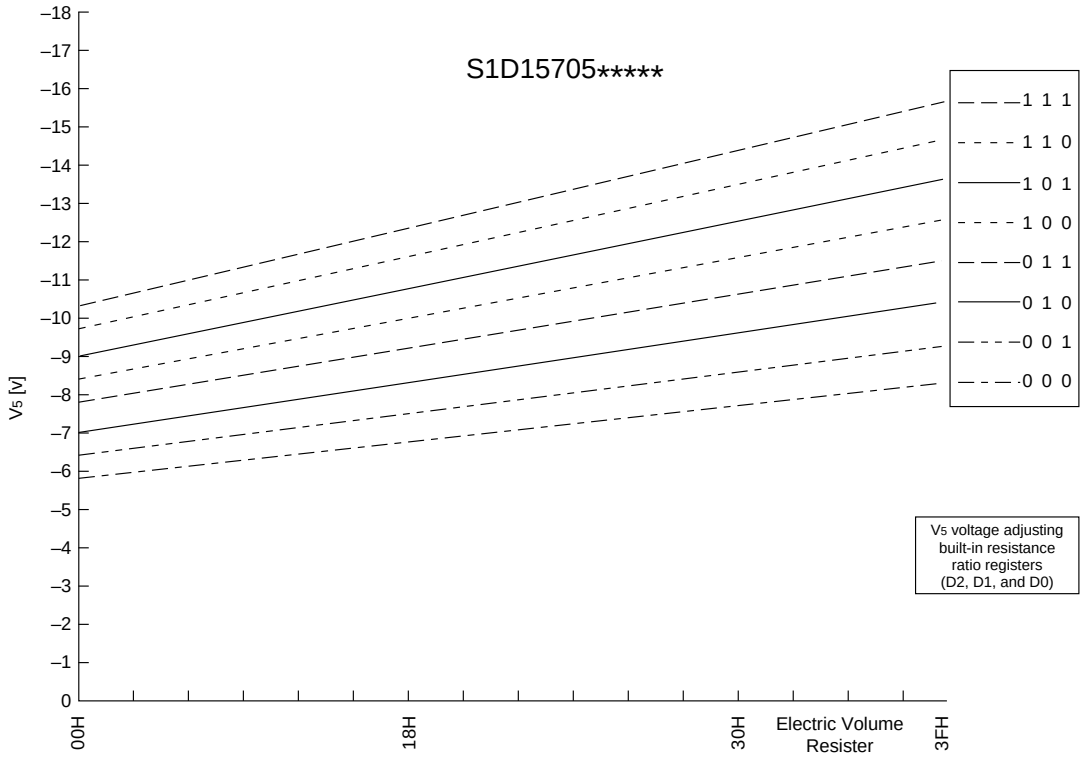


Fig. 10-1 S1D15705***** Temperature gradient = –0.05%/°C device

V_5 voltage based on the values of V_5 voltage adjusting built-in resistance ratio register and electronic control register

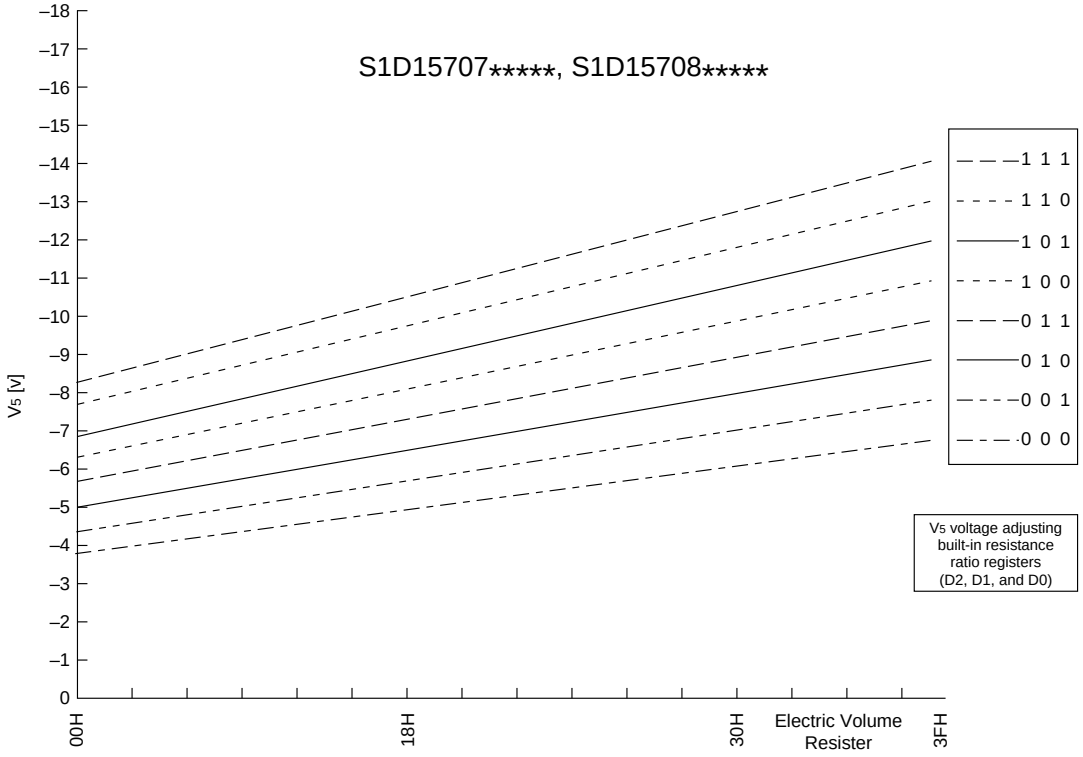


Fig. 10-2 S1D15707*****, S1D15708***** Temperature gradient = –0.05%/°C device

V_5 voltage based on the values of V_5 voltage adjusting built-in resistance ratio register and electronic control register

*S1D15708 should be used in system operating voltage ranges. (V_5–V_{DD} = –10V or V_5–V_{DD}=less than –10V)

<Setting example: S1D15705★★★★★ When setting V_5 = –9 V at Ta=25°C>
From Fig. 8 and Expression A-1.

Table 12

Description	Register					
	D5	D4	D3	D2	D1	D0
V_5 voltage adjusting	–	–	–	0	1	0
electronic control	0	1	1	0	0	1

In this case, Table 13 lists the V_5 voltage variable range and pitch width using the electronic control function.

Table 13

V_5	Min.		Typ.		Max.	Unit
Variable range	–11.6	to	–9.3	to	–7.1	[V]
Pitch width			67			[mV]

(B) When using the external resistor (not using the V_5 voltage adjusting built-in resistor) ①
The liquid crystal power supply voltage V_5 can also be set by adding the resistors (Ra' and Rb') between V_{DD} and V_R and between V_R and V_5 without the V5 voltage adjusting built-in resistor (IRS pin=LOW). Also in this case, the liquid crystal power supply voltage V_5 can be controlled using the command and the light and shade of liquid crystal display can be adjusted by using the electronic control function.

The V_5 voltage can be obtained from Expression B-1 by setting the external resistors Ra' and Rb' within the range of $|V_5| < |V_{OUT}|$.

$$V_5 = \left(1+\frac{Rb'}{Ra'}\right)\cdot V_{EV} = \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG} \quad \left[\because V_{EV} = \left(1-\alpha/162\right)\cdot V_{REG}\right] \qquad \text{(Expression B-1)}$$

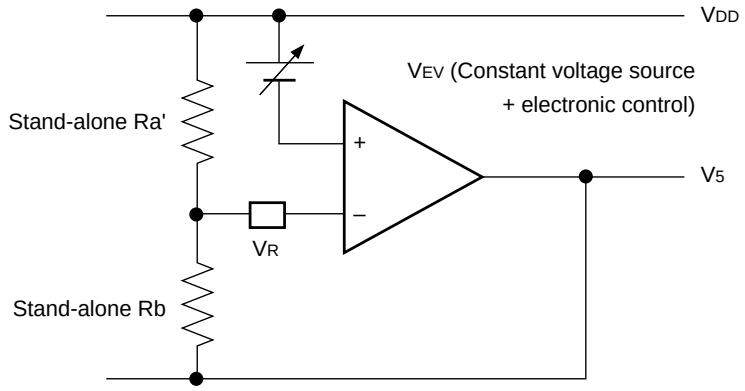


Fig. 11

<Setting example: S1D15705★★★★★ When setting V_5=–7 V at Ta=25°C>

Set the value of the electronic control register as the intermediate value (D5, D4, D3, D2, D1, D0) = (1,0,0,0,0,0). From the foregoing we can establish the expression:

$$\alpha = 31$$
$$V_{REG} = -2.1V$$

From Expression B-1, it follows that

$$V_5 = \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG} \qquad \text{(Expression B-2)}$$
$$-7V = \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{31}{162}\right)\cdot(-2.1)$$

Also, suppose the current applied to Ra' and Rb' is 5μA.

$$Ra' + Rb' = 1.4M\Omega \qquad \text{(Expression B-2)}$$

It follows that
Therefore from Expressions B-2 and B-3, we have

$$\frac{Rb'}{Ra'} = 3.12$$
$$Ra' = 340k\Omega$$
$$Rb' = 1060k\Omega$$

In this case, Table 14 lists the V_5 voltage variable range and pitch width using the electronic control function.

Table 14

V_5	Min.		Typ.		Max.	Unit
Variable range	–8.6	to	–7.0	to	–5.3	[V]
Pitch width			52			[mV]

(C) When using the external resistor (not using the V_5 voltage adjusting built-in resistor) ②
In the use of the above-mentioned external resistor, the liquid crystal power supply voltage V_5 can also be set by adding the resistors to finely adjust Ra' and Rb'. Also in this case, the liquid crystal power supply voltage V_5 can be controlled using the command and the light and shade of liquid crystal display can be adjusted by using the electronic control function.

The V_5 voltage can be obtained from the following expression C-1 by setting the external resistors R_1, R_2 (variable resistors), and R_3 within the range of $|V_5| < |V_{OUT}|$ and finely adjusting R_2 (ΔR_2).

$$V_5 = \left(1+\frac{R_3+R_2-\Delta R_2}{R_1+\Delta R_2}\right)\cdot V_{EV}$$
$$= \left(1+\frac{R_3+R_2-\Delta R_2}{R_1+\Delta R_2}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG}$$
$$\left[\because V_{EV} = \left(1-\alpha/162\right)\cdot V_{REG}\right] \quad \text{(Expression C-1)}$$

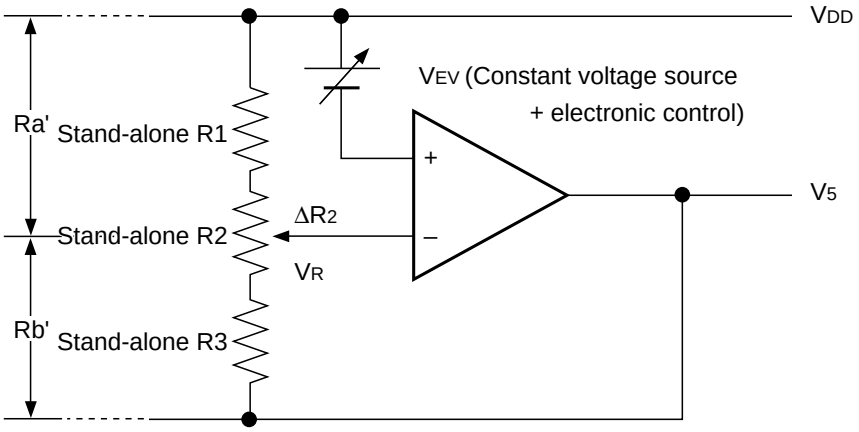


Fig. 12

<Setting example: S1D15705★★★★★ When setting V_5=–5 to –9 V at Ta=25°C>

Set the value of the electronic control register as the intermediate value (D5, D4, D3, D2, D1, D0) = (1,0,0,0,0,0). From the foregoing we can establish the expression:

$$\alpha = 31$$
$$V_{REG} = -2.1V$$

When ΔR_2=0Ω, to obtain V_5=–9 V from Expression C-1, it follows that

$$-9V = \left(1+\frac{R_3+R_2}{R_1}\right)\cdot\left(1-\frac{31}{162}\right)\cdot(-2.1)$$

(Expression C-2)

When ΔR2=R2, to obtain V_5=-5V, it follows that

$$-5V = \left(1+\frac{R_3}{R_1+R_2}\right)\cdot\left(1-\frac{31}{162}\right)\cdot(-2.1)$$

(Expression C-3)

Also, suppose the current applied between V_{DD} and V_5 is 5μA.

$$R_1 + R_2 + R_3 = 1.4M\Omega$$

(Expression C-4)

It follows that
Therefore from Expressions C-2, C-3, and C-4, we have

$$R_1 = 264k\Omega$$
$$R_2 = 211k\Omega$$
$$R_3 = 925k\Omega$$

In this case, Table 6-15 lists the V_5 voltage variable range and pitch width using the electronic control function.

Table 15

V_5	Min.		Typ.		Max.	Unit
Variable range	–8.7	to	–7.0	to	–5.3	[V]
Pitch width			53			[mV]

- When using the V_5 voltage adjusting built-in resistor or electronic control function, the state where at least the voltage adjusting circuit and voltage follower circuit are operated together needs to be set using the power control set command. Also when the boosting circuit is OFF, the voltage needs to be applied from V_{OUT}.
- The V_R pin is valid only when the V_5 voltage adjusting built-in resistor (IRS pin=LOW). Set the V_R pin to OPEN when using the V_5 voltage adjusting built-in resistor (IRS pin=HIGH).
- Since the V_R pin has high input impedance, noise must be taken into consideration such as for short and shielded lines.

Liquid crystal voltage generator circuit

The V_5 voltage is resistor-split within an IC and generates the V_1, V_2, V_3, and V_4 potentials required for the liquid crystal drive.
Further, the V_1, V_2, V_3, and V_4 potentials are impedance-converted by the voltage follower and supplied to the liquid crystal drive circuit.
Using the bias set command allows you to select a desired bias ratio from 1/9 or 1/7 for the S1D15705***** and 1/6 or 1/5 for the S1D15707***** and S1D15708***** .

High power mode

The power supply circuit incorporated in the S1D15705 series has the ultra-low power consumption (normal mode: $\overline{HPM}$=HIGH). Therefore the display quality may be deteriorated in large load liquid crystal or panels. In this case, the display quality can be improved by setting $\overline{HPM}$ pin=LOW (high power mode). Whether to use the power supply circuit in this mode should need the display confirmation by actual equipment.
Besides, if the improvement is insufficient even for the high power mode setting, the crystal liquid drive power needs to be supplied externally.

Command sequence when the built-in power supply is turned off

To turn off the built-in power supply, set it in the power save state and then turn off the power supply according to the command sequence shown in Fig. 13 (procedure).

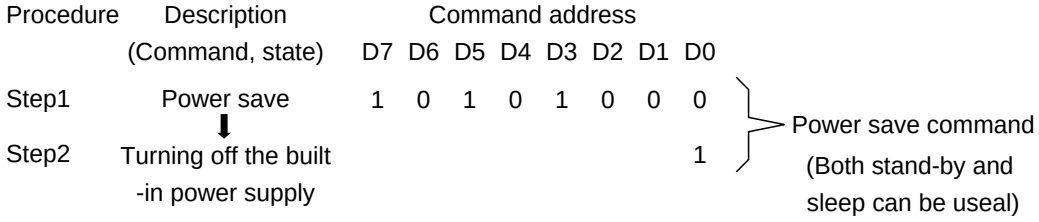
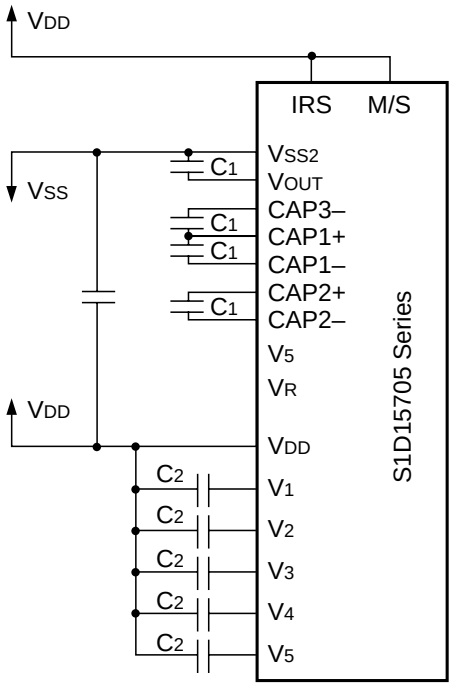


Fig. 13

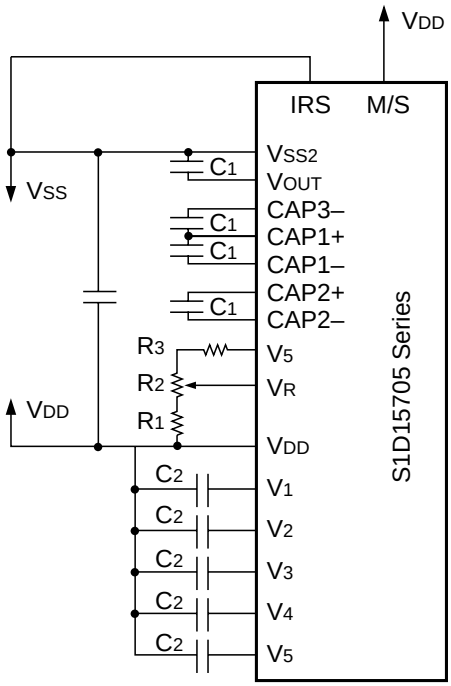
Reference circuit examples

① Built-in power supply used

(1) When using the V_5 voltage adjusting built-in resistor
(Example of V_{SS2}=V_{SS}, quadruple boosting)

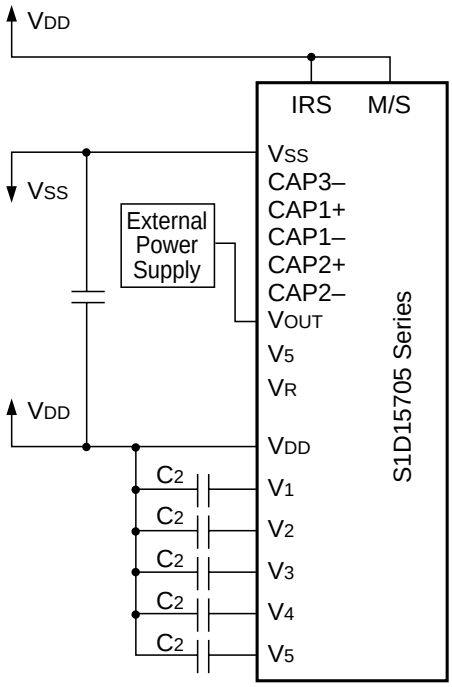


(2) When not using the V_5 voltage adjusting built-in resistor
(Example of V_{SS2}=V_{SS}, quadruple boosting)

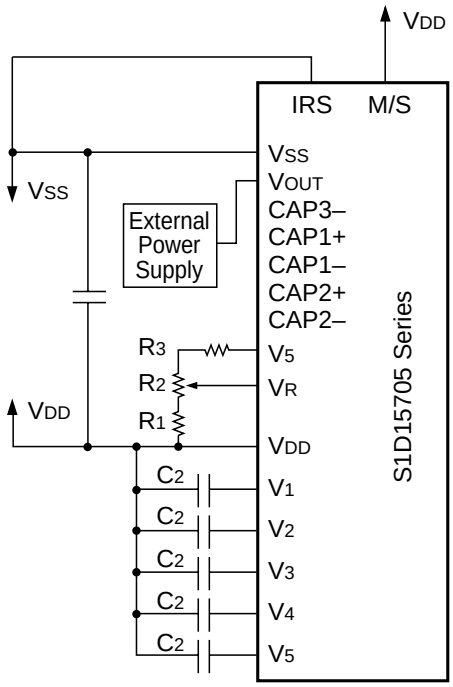


② Only the voltage adjusting circuit and V/F circuit used

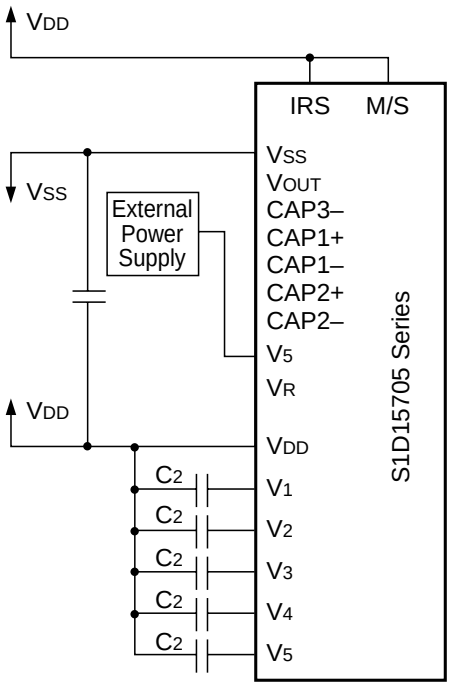
(1) When using the V_5 voltage adjusting built-in resistor



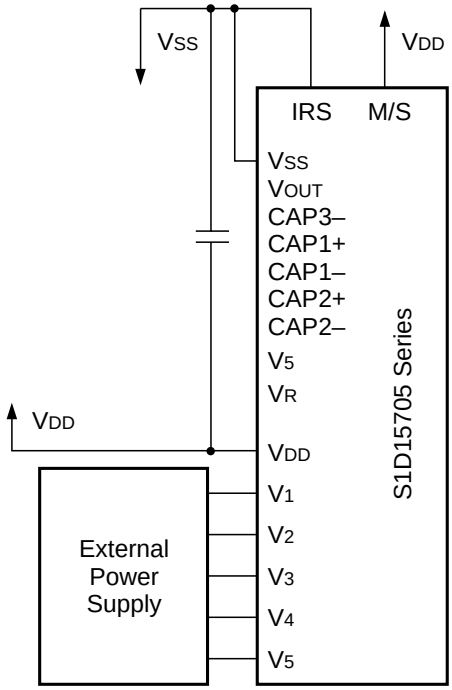
(2) When not using the V_5 voltage adjusting built-in resistor



③ Only the V/F circuit used



④ Only the external power supply used
Depending on all external power supplies



Common reference setting example
At V_5=–8 to –12 V variable

Item	Setting value	Unit
C_1	1.0 to 4.7	µF
C_2	0.01 to 1.0	µF

Fig. 14

*1 Since the V_R pin has high input impedance, it uses short and shielded wires.
*2 C_1 and C_2 are determined according to the size of the LCD panel. Set a value so that the liquid crystal drive voltage can be stable.
[Setting example] • Turn on the V adjusting circuit and the V/F circuit and apply external voltage.
• Display LCD heavy load patterns like lateral stripes and determine C_2 so that the liquid crystal drive voltages (V_1 to V_5) can be stable.
• Then turn on all built-in power supplies and determine C_1.
*3 Capacity is connected in order to stabilize voltage between V_{DD} and V_{SS} power supplies.

*4 When the built-in V/F circuit is used to drive an LCD panel with heavy alternating or direct current load, we recommend that external resistance be connected in order to stabilize V/F outputs, or electric potentials, V_1, V_2, V_3 and V_4.

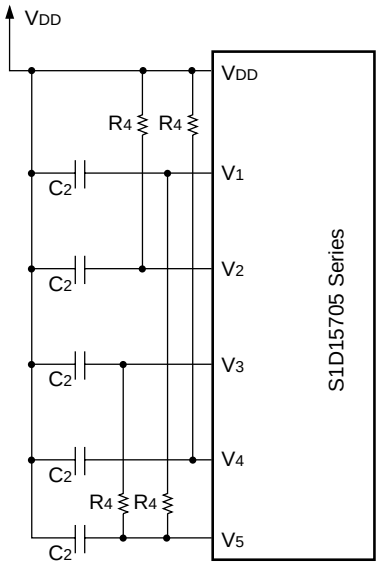


Fig. 15

Adjust resistance value R_4 to the optimal level by checking driving waveform displayed on the LCD.

Reference setting: R_4 = 0.1 to 1.0 [MΩ]

*5 Precautions when installing the COG

When installing the COG, it is necessary to duly consider the fact that there exists a resistance of the ITO wiring occurring between the driver chip and the externally connected parts (such as capacitors and resistors). By the influence of this resistance, non-conformity may occur with the indications on the liquid crystal display.
Therefore, when installing the COG design the module paying sufficient considerations to the following three points.

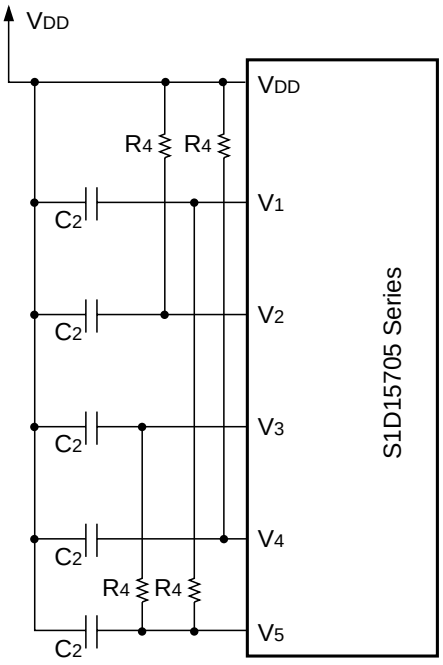
1. Suppress the resistance occurring between the driver chip pin to the externally connected parts as much as possible.
2. Suppress the resistance connecting to the power supply pin of the driver chip.
3. Make various COG module samples with different ITO sheet resistance to select the module with the sheet resistance with sufficient operation margin.

Also, as for this driver IC, pay sufficient attention to the following points when connecting to external parts for the characteristics of the circuit.

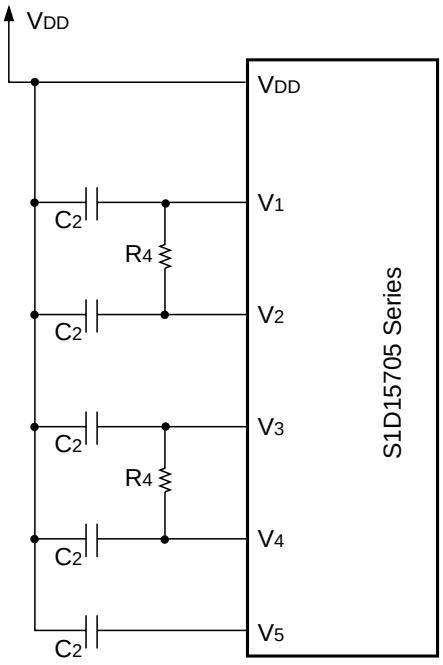
1. Connection to the boosting capacitors The boosting capacitors (the capacitors connecting to respective CAP pins and capacitor being inserted between V_{OUT} and V_{SS2}) of this IC are being switched over by use of the transistor with very low ON-resistance of about 10Ω. However, when installing the COG, the resistance of ITO wiring is being inserted in series with the switching transistor, thus dominating the boosting ability.
   Consequently, the boosting ability will be hindered as a result and pay sufficient attention to the wiring to respective boosting capacitors.
2. Connection of the smoothing capacitors for the liquid crystal drive
   The smoothing capacitors for the liquid crystal driving potentials (V_1. V_2, V_3 and V_4) are indispensable for liquid crystal drives not only for the purpose of mere stabilization of the voltage levels. If the ITO wiring resistance which occurs pursuant to installation of the COG is supplemented to these smoothing capacitors, the liquid crystal driving potentials become unstable to cause non-conformity with the indications of the liquid crystal display. Therefore, when using the COG module, we definitely recommend to connect reinforcing resistors externally.
   Reference value of the resistance is 100kΩ to 1MΩ. Meanwhile, because of the existence of these reinforcing resistors, current consumption will increase.

Indicated below is an exemplary connection diagram of external resistors.
Please make sufficient evaluation work for the display statuses with any connection tests.

Exemplary connection diagram 1.



Exemplary connection diagram 2.



Reset Circuit

When the $\overline{RES}$ input is set to the LOW level, this LSI enters each of the initial setting states

1. Display OFF
2. Display Normal Rotation
3. ADC Select: Normal rotation (ADC command D0=0)
4. Power Control Register: (D2,D1,D0)=(0,0,0)
5. Register Data Clear within Serial Interface
6. LCD Power Supply Bias Ratio:
   S1D15705: 1/9 bias
   S1D15707/S1D15708: 1/6 bias
7. n-Line Alternating Current Reversal Drive Reset
8. Sleeve mode cancel (standby mode is not canceled)
9. Display All Lighting OFF: (Display All Lighting ON/OFF command D0=LOW)
10. Built-in Oscillator Circuit stopped
11. Static Indicator OFF
    Static Indicator Register: (D1,D2)=(0,0)
12. Read Modify Write OFF
13. Display start line set to the first line
14. Column address set to address 0
15. Page address set to page 0
16. Common Output State Normal rotation
17. V_5 Voltage Adjusting Built-in Resistance Ratio Register: (D2,D1,D0)=(0,0,0)
18. Electronic Control Register Set Mode Reset
    Electronic Control Register* (D5, D4, D3, D2, D1, D0) = (1,0,0,0,0,0)
19. n-Line Alternating Current Reversal Register: (D3, D2, D1, D0) = (0, 0, 0, 0)
20. Test Mode Reset

On the other hand, when using the reset command, only the items 11 to 20 of the above-mentioned initial setting are executed.

When the power is turned on, the initialization using the $\overline{RES}$ pin is required. After the initialization using the $\overline{RES}$ pin, each input pin needs to be controlled normally. Besides, when the MPU control signal has high impedance, overcurrent may be applied to an IC. After turning on the power, take action so that the input pin cannot have high impedance.
The S1D15705 Series discharge electric charges of V_5 and V_{OUT} at $\overline{RES}$ pin is set to the LOW level. If external power supplies for driving LCD are used, do not input external power while the $\overline{RES}$ pin is set to the LOW level to prevent short-circuiting between the external power supplies and V_{DD}.

7. COMMAND

The S1D15705 series identifies data bus signals according to the combinations of A0, $\overline{RD}$(E), and $\overline{WR}$(R/$\overline{W}$). Since the interpretation and execution of commands are performed only by the internal timing independently of external clocks, the S1D15705 performs high-speed processing that does not require busy check normally.
The 80 series MPU interface starts commands by inputting low pulses to the $\overline{RD}$ pin at read and to the $\overline{WR}$ pin at write operation. The 68 series MPU interface enters the read state when HIGH is input to the R/$\overline{W}$ pin. It enters the write state when LOW is input to the same pin. It starts commands by inputting high pulses to the E pin (for the timing, see the Timing Characteristics of Chapter 10). Therefore the 68 series MPU interface differs from the 80 series MPU interface in that $\overline{RD}$(E) is set to "1 (H)" at status read and display data read in the Command Description and Command Table. The command description is given below by taking the 80 series MPU interface as an example.
When selecting the serial interface, enter sequential data from D_7.

Command description

(1) Display ON/OFF

This command specifies display ON/OFF.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

For display OFF, the segment and common drivers output the V_{DD} level.

(2) Display Start Line Set

This command specifies the display start line address of the display data RAM shown in Fig. 4. The display area is displayed for 65 lines for the S1D15705*****, 33 lines for the S1D15707***** and 17 lines for the S1D15708***** from the specified line address to the line address increment direction. When this command is used to dynamically change the line address, the vertical smooth scroll and page change are enabled. For details, see the Line address circuit of "Function Description".

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	0	0	1	0	2
							↓				↓
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

(3) Page Address Set

This command specifies the page address that corresponds to the low address when accessing the display data RAM shown in Fig. 4 from the MPU side. The display data RAM can access desired bits when the page address and column address are specified. Even when the page address is changed, the display state will not be changed. For details, see the Page address circuit of "Function Description".

A0	$\overline{E}$ / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
								↓			↓
							0	1	1	1	7
							1	0	0	0	8

(4) Column Address Set

This command specifies the column address of the display data RAM shown in Fig. 4. The column address is set (basically successively) by dividing it into high-order four bits and low-order four bits. Since the column address is automatically incremented by 1 whenever the display data RAM is accessed. The MPU can successively read/write the display data. The column address stops the increment at C7H. In this case, the page address is not changed successively. For details, see the Column address circuit of "Function Description".

	A0	$\overline{E}$ / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
High-order bit →	0	1	0	0	0	0	1	A7	A6	A5	A4
Low-order bit →							0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
				↓				↓
1	0	1	0	0	1	1	0	166
1	0	1	0	0	1	1	1	167
				↓				↓
1	1	0	0	0	1	1	0	198
1	1	0	0	0	1	1	1	199

(5) Status Read

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	When BUSY=1, indicates an internal operation being done or reset. The command cannot be accepted until BUSY=0 is reached. However, if the cycle time is satisfied, the command needs not be checked.
ADC	Indicates the correspondence relationship between the column address and segment driver. 0: Reversal (column address 199–n ↔ SEG n) 1: Normal rotation (column address n ↔ SEG n) (Reverses the polarity of ADC command.)
ON/OFF	ON/OFF: Specifies display ON/OFF 0: Display ON 1: Display OFF (Reverses the polarity of display ON/OFF command.)
RESET	Indicates the $\overline{RES}$ signal or that initial setting is being done using the reset command. 0: Operating state 1: Resetting

(6) Display Data Write

This command writes 8-bit data to the specified address of the display data RAM. Since the column address is automatically incremented by 1 after the data is written, the MPU can successively write the display data.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

(7) Display Data Read

This command reads the 8-bit data in the specified address of the display data RAM. Since the column address is automatically incremented by 1 after the data is written, the MPU can successively read the data consisting of multiple words.
Besides, immediately after the column address is set, dummy read is required one time. For details, see the description of the Display data RAM and internal register access of “Function Description”.
When using the serial interface, the display cannot be read.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

(8) ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence relationship between the column address of the display RAM data shown in Fig. 4 and the segment driver output. Therefore the order of the segment driver output pin can be reversed using the command. After the display data is written and read, the column address is incremented by 1 according to the column address of Fig. 4. For details, see the Column address circuit of "Function Description".

A0	$\overline{E}$ RD	R/$\overline{W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Clockwise (normal rotation)
										1	Counterclockwise (reversal)

(9) Display Normal Rotation/Reversal

This command can reversal display lighting and non-lighting without overwriting the contents of display data RAM. In this case, the contents of display data RAM are held.

A0	$\overline{E}$ RD	R/$\overline{W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	LCD on potential (normal rotation) RAM data HIGH
										1	LCD on potential (reversal) RAM data LOW

(10) Display All Lighting ON/OFF

This command can forcedly make all display set in the lighting state irrespective of the contents of display data RAM. In this case, the contents of display data RAM are held.
This command has priority over the display normal rotation/reversal command.

A0	$\overline{E}$ RD	R/$\overline{W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display state
										1	Display all lighting

(11) LCD Bias Set

This command selects the bias ratio of the voltage required for liquid crystal drive. The command is valid when the V/F circuit of the power supply circuit is operated.

A0	$\overline{E}$ RD	R/$\overline{W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected state	
											S1D15705*****	S1D15707***** / S1D15708*****
0	1	0	1	0	1	0	0	0	1	0	1/9 bias	1/6 bias
										1	1/7 bias	1/5 bias

(12) Read Modify Write

This command is used together with the end command. Once this command is entered, the column address can be incremented by 1 only using the display data write command instead of being changed using the display read command. This state is held until the end command is entered. When the end command is entered, the column address returns to the address when the read modify write command is entered. This function can reduce the load of the MPU when repeatedly changing data for a specific display area such as a blinking cursor.

A0	$\overline{E}$ RD	R/$\overline{W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

* The commands other than Display Data Read/Write can be used even in Read Modify Write mode. However, the column address set command cannot be used.

• Sequence for cursor display

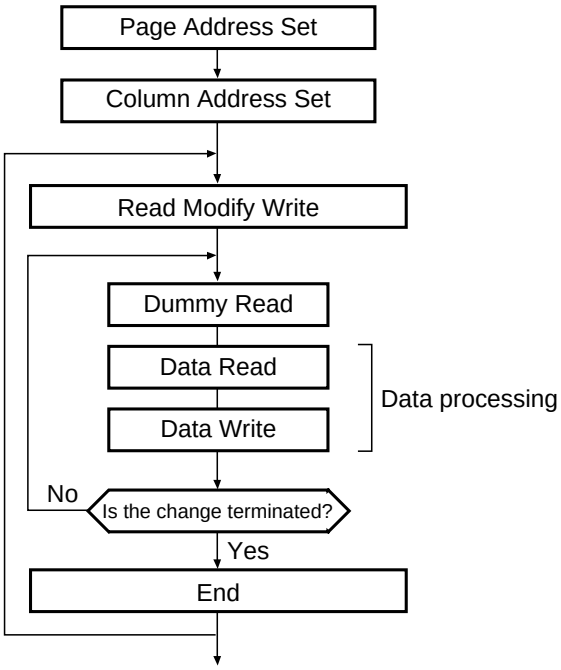


Fig. 16

(13) End

This command resets the Read Modify Write mode and returns the column address to the mode initial address.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

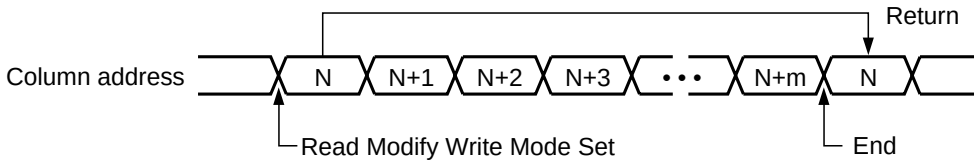


Fig. 17

(14) Reset

This command initializes Display Start Line, Column Address, Page Address, Common Output State, V_5 Voltage Adjusting Built-in Resistance Ratio, Electronic Control, and Static Indicator and resets the Read Modify Write mode and Test mode. This will not have any effect on the display data RAM. For details, see the Reset of " Function Description".
Reset operation is performed after the reset command is entered.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The initialization when the power is applied is performed using the reset signal to the $\overline{RES}$ pin. The reset command cannot be substituted for the signal.

(15) Common Output State Selection

This command can select the scanning direction of the COM output pin. For details, see the Common Output State Selection Circuit of "Function Description".

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Selected state	S1D15705*****	S1D15707*****	S1D15708*****
0	1	0	1	1	0	0	0	*	*	*	Normal rotation	COM0 → COM63	COM0 → COM31	C OM0 → COM15
							1				Reversal	COM63 → COM0	COM31 → COM0	COM15→ COM0

*: Invalid bit

(16) Power Control Set

This command sets the function of the power supply circuit. For details, see the Power Supply Circuit of "Function Description".

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected state
0	1	0	0	0	1	0	1	0			Boosting circuit: OFF
								1			Boosting circuit: ON
									0		V adjusting circuit: OFF
									1		V adjusting circuit: ON
										0	V/F circuit: OFF
										1	V/F circuit: ON

(V/F circuit: Voltage follower circuit, V adjusting circuit: voltage adjusting circuit)

(17) V_5 Voltage Adjusting Built-in Resistance Ratio Set

This command sets the V_5 voltage adjusting built-in resistance ratio. For details, see the Power Supply Circuit of "Function Description".

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0	Rb to Ra ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									↓		↓
								1	1	0	
								1	1	1	Large

(18) Electronic Control (2-Byte Command)

This command controls the liquid crystal drive voltage V_5 output from the voltage adjusting circuit of the built-in liquid crystal power supply and can adjust the light and shade of liquid crystal display.
Since this command is a 2-byte command that is used together with the electronic control mode set command and electronic control register set command, always use both the commands consecutively.

• Electronic Control Mode Set

Entering this command validates the electronic control register set command. Once the electronic control mode is set, the commands other than the electronic control register set command cannot be used. This state is reset after data is set in the register using the electronic control register set command.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

• Electronic Control Register Set
This command is used to set 6-bit data in the electronic volume register to allow the liquid crystal drive voltage V_5 to enter one-state voltage value among 64-state voltage values.
After this command is entered and the electronic control register is set, the electronic control mode is reset.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	| V5 |
0	1	0	*	*	0	0	0	0	0	0	Small
0	1	0	*	*	0	0	0	0	0	1	
0	1	0	*	*	0	0	0	0	1	0	
							↓				↓
0	1	0	*	*	1	1	1	1	1	0	
0	1	0	*	*	1	1	1	1	1	1	Large

*: Invalid bit

When not using the electronic control function, set (1,0,0,0,0,0).

• Sequence of the electronic control register set

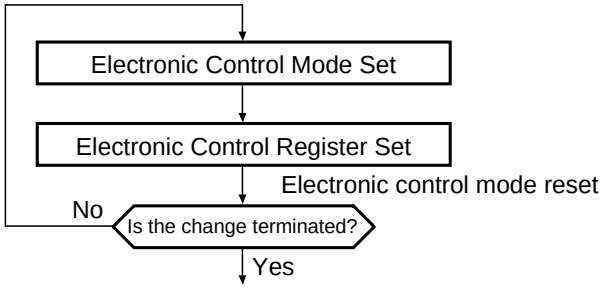


Fig. 18

(19) Static Indicator (2-Byte Command)

This command controls the indicator display of the static drive system. The static indicator display is controlled only using this command, and this command is independent of other display control commands.
The static indicator is used to connect the SYNC pin to one of its liquid crystal drive electrodes and the FRS pin to the other. For the electrodes used for the static indicator, the pattern separated from the electrodes for dynamic drive are recommended. When this pattern is too adjacent, the deterioration of liquid crystal and electrodes may be caused.
Since the static indicator ON command is a 2-byte command that is used together with the static indicator register set command, always use both the commands consecutively. (The static indicator OFF command is a 1-byte command.)

• Static Indicator ON/OFF

Entering the static indicator ON command validates the static indicator register set command. Once the static indicator ON command is entered, the commands other than the static indicator register set command cannot be used. This state is reset after the data is set in the register using the static indicator register set command.

A0	$\overline{E}$ $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Static indicator
0	1	0	1	0	1	0	1	1	0	0	OFF
										1	ON

• Static Indicator Register Set

This command sets data in the 2-bit static indicator register and sets the blinking state of the static indicator.

A0	$\overline{E}$ $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Indicator display state
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON (blinks at an interval of approximately 0.5 second.)
									1	0	ON (blinks at an interval of approximately one second.)
									1	1	ON (goes on at all times.)

*: Invalid bit

• Sequence of Static Indicator Register Set

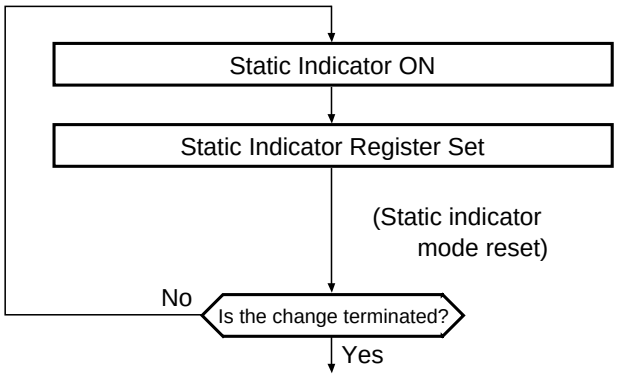


Fig. 19

(20) Power Save

This command makes the static indicator enter the power save state and can greatly reduce the power consumption. The power save state consists of the sleep state and stand-by state.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Power save state
0	1	0	1	0	1	0	1	0	0	0	Stand-by state
										1	Sleep state

The operating state before the display data and power save activation is held in the sleep and stand-by states, and the display data RAM can also be accessed from the MPU.

• Sleep State

This command stops all the operations of LCD display systems, and can reduce the power consumption approximate to the static current when they are not accessed from the MPU. The internal state in the sleep state is as follows:

(1) The oscillator circuit and the LCD power supply circuit are stopped.
(2) All liquid crystal drive circuit is stopped and the segment and common drivers output the V_{DD} level.

• Stand-by State

This command stops the operation of the duty LCD display system and operates only the static drive system for indicators. Consequently the minimum current consumption required for the static drive is obtained. The internal state in the stand-by state is as follows:

(1) The LCD power supply circuit is stopped. The oscillator circuit is operated.
(2) The duty drive system liquid crystal drive circuit is stopped and the segment and common drivers output the V_{DD} level. The static drive system is operated.
    * When using external power supplies, it is recommended that the function of the external power supply circuit should be stopped at power save activation. For example, when providing each level of the liquid crystal drive voltage using a stand-alone split resistor circuit, it is recommended that the circuit which cuts off the current applied to the split resistor circuit should be added at power save activation. The S1D15705 series has the liquid crystal display blanking control pin $\overline{DOF}$ and is set to LOW at power save activation. The function of the external power supply circuit can be stopped using the $\overline{DOF}$ output.

(21) Power Save Reset

This command resets the power save state and returns the state before power save activation.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	1

(22) n-Line Reversal Drive Register Set

This command sets the number of reversal lines of the liquid crystal drive in the register. 2 to 16 lines can be set. For details, see the Display Timing Generator Circuit of “Function Description”.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Line of reversal lines
0	1	0	0	0	1	1	0	0	0	0	—
							0	0	0	1	2
							0	0	1	0	3
									↓		↓
							1	1	1	0	15
							1	1	1	1	16

(23) n-Line Reversal Drive Reset

This command resets the n-line reversal alternating current drive and returns to the normal 2-frame reversal alternating current drive system. The value of the n-line reversal alternating current drive register is not changed.

A0	$\overline{E}$ $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	1	0	0

(24) Built-in Oscillator Circuit ON

This command starts the operation of the built-in CR oscillator circuit. This command is valid only for the master operation (M/S=HIGH) and built-in oscillator circuit valid (CLS=HIGH).

A0	$\overline{E}$ $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	1	1

(25) NOP

Non-OPeration

A0	$\overline{E}$ $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

(26) Test

IC chip test command. Do not use this command. If the test command is used incorrectly, it can be reset by setting the RES input to LOW or by using the reset command or NOP.

A0	$\overline{E}$ $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

*: Invalid bit

(Note) Although the S1D15705 series holds the command operating state, it may change the internal state if excessive foreign noise is entered. Such action that suppresses the generation of noise and prevents the effect of noise needs to be taken on installation and systems. Besides, to prevent sudden noise, it is recommended that the operating state should periodically be refreshed.

Table 16 S1D15705 Series Commands

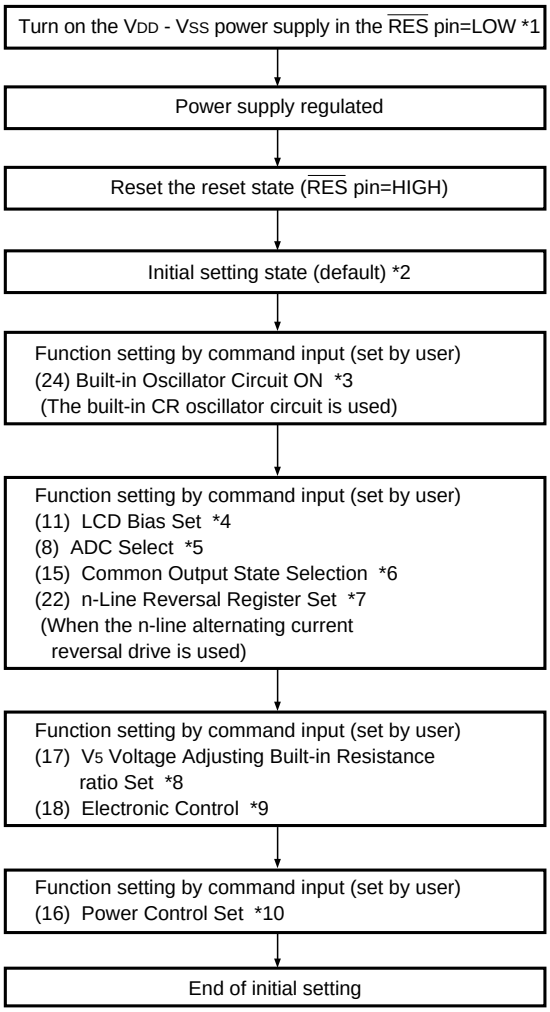
Command	Command code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display Start Line Set	0	1	0	0	1	Display start address						Sets the display start line address of the display RAM.
(3) Page Address Set	0	1	0	1	0	1	1	Page Address				Sets the page address of the display RAM.
(4) Column Address Set High-Order Bit	0	1	0	0	0	0	1	High order Column address				Sets the high-order four bits of the column address of the display RAM.
Column Address Set Low-Order Bit	0	1	0	0	0	0	0	Low order Column address				Sets the low-order four bits of the column address of the display RAM.
(5) Status Read	0	0	1	Status				0	0	0	0	Reads the status information.
(6) Display Data Read	1	1	0	Write data								Writes data on the display RAM.
(7) Display Data Write	1	0	1	Read data								Reads data from the display RAM.
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Supports the SEG output of the display RAM address. 0: normal rotation, 1: Reversal
(9) Display Normal Rotation/Reversal	0	1	0	1	0	1	0	0	1	1	0 1	LCD display normal rotation/ reversal 0: normal rotation, 1: Reversal
(10) Display All Lighting ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all lighting 0: normal display, 1: All ON
(11) LCD Bias Set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio. S1D15705★★★★★ 0: 1/9, 1: 1/7, S1D15707★★★★★ 0: 1/6, 1: 1/5
(12) Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increments the column address. At write operation: By 1, at read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Resets Read Modify Write.
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal resetting
(15) Common Output State Selection	0	1	0	1	1	0	0	0 1	*	*	*	Selects the scanning direction of the COM output. 0: Normal rotation, 1: Reversal
(16) Power Control Set	0	1	0	0	0	1	0	1	Operating state			Selects the state of the built-in power supply
(17) V_5 Voltage Adjusting Internal Resistance Ratio Set	0	1	0	0	0	1	0	0	Resistance ratio setting			Selects the state of the built-in resistance ratio (Rb/Ra).
(18) Electronic Control Mode Set	0	1	0	1	0	0	0	0	0	0	1	
Electronic Control Register Set	0	1	0	*	*	Electronic control value						Sets the V_5 output voltage in the electronic register.
(19) Static Indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1	0: OFF, 1: ON
Static Indicator Register Set	0	1	0	*	*	*	*	*	*	State		Sets the blinking state.
(20) Power Save	0	1	0	1	0	1	0	1	0	0	0 1	Moves to the power save state. 0: Stand-by, 1: Sleep
(21) Power Save Reset	0	1	0	1	1	1	0	0	0	0	1	Resets power save.
(22) n-Line Reversal Drive Register Set	0	1	0	0	0	1	1	Number of reversal Line				Sets the number of line reversal drive lines.
(23) n-Line Reversal Drive Reset	0	1	0	1	1	1	0	0	1	0	0	Resets the line reversal drive.
(24) Built-in Oscillator Circuit ON	0	1	0	1	0	1	0	1	0	1	1	Starts the operation of the built-in CR oscillator circuit.
(25) NOP	0	1	0	1	1	1	0	0	0	1	1	Non-Operation command
(26) Test	0	1	0	1	1	1	1	*	*	*	*	Do not use the IC chip test command.

*: Invalid bit

8. COMMAND SETTING

Instruction Setup: Reference

(1) Initial Setting



Notes: Reference items

*1: If external power supplies for driving LCD are used, do not supply voltage on VOUT or V5 pin during the period when RES = LOW. Instead, input voltage after releasing the reset state.
6. Function Description "Reset Circuit"

*2: The contents of DDRAM are not defined even in the initial setting state after resetting.
6. Function Description Section "Reset Circuit"

*3: 7. Command Description Item (24) Built-in oscillator circuit ON

*4: 7. Command Description Item (11) LCD bias set

*5: 7. Command Description Item (8) ADC select

*6: 7. Command Description Item (15) Common output state selection

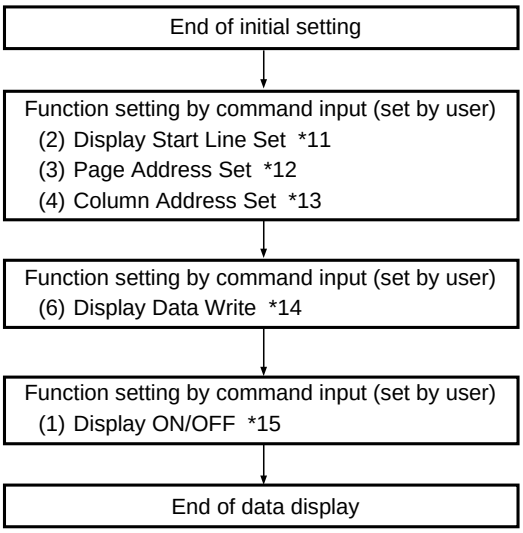
*7: 6. Function Description Section "Display Timing Generator Circuit", 7. Command Description Item (22) n-Line Reversal Register Set

*8: 6. Function Description Section "Power Supply Circuit" and 7. Command Description Item (17) V5 Voltage Adjusting Built-in Resistance ratio Set

*9: 6. Function Description Section "Power Supply Circuit" and 7. Command Description Item (18) Electronic Control

*10: 6. Function Description Section "Power Supply Circuit" and 7. Command Description Item (16) Power Control Set

(2) Data Display



Notes: Reference items

*11: 7. Command Description Item (2) Display Start Line Set

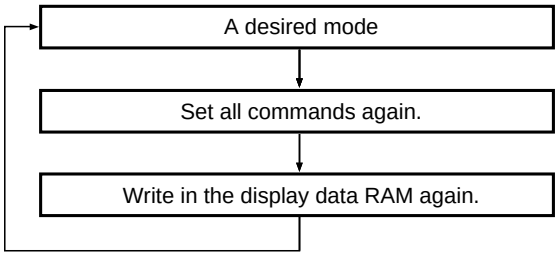
*12: 7. Command Description Item (3) Page Address Set

*13: 7. Command Description Item (4) Column Address Set

*14: The contents of DDRAM is not defined after completing initial setting. Enter data in each DDRAM to be used for display.
7. Command Description Item (6) Display Data Write

*15: Avoid activating the display function with entering space characters as the data if possible.
7. Command Description Item (1) Display ON/OFF

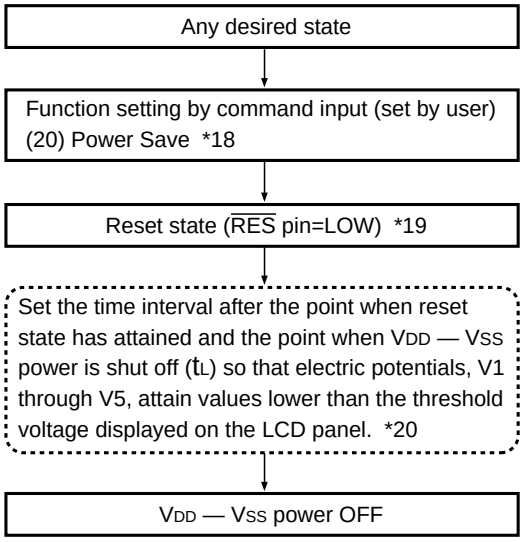
(3) Refresh *16



Notes: Reference items

*16: It is recommended that the operating modes and display contents be refreshed periodically to prevent the effect of unexpected noise.

(4) Power OFF *17



Notes: Reference items

*17: This IC is a V_{DD} – V_{SS} power system circuit controlling the LCD driving circuit for the V_{DD} – V_5 power system. Shutting of power with voltage remaining in the V_{DD} – V_5 power system may cause uncontrolling voltage to be output from the SEG and COM pins. Follow the Power OFF sequence.

*18: 7. Command Description Item Power Saving

*19: When external power supplies for driving LCD are used, turn all external power supplies off before entering reset state.
6. Function Description Item Reset Circuit

*20: The reference value for the threshold voltage of the LCD panel is 1 [V].
When the built-in power circuit is used, the discharge time, t_H, or the time interval between the point when the reset state has started and the point when voltage between V_{DD} and V_5 becomes 1 [V] depends on the V_{DD} – V_{SS} power voltage and the capacity C2 connected between V_1 – V_5 and V_{DD}.

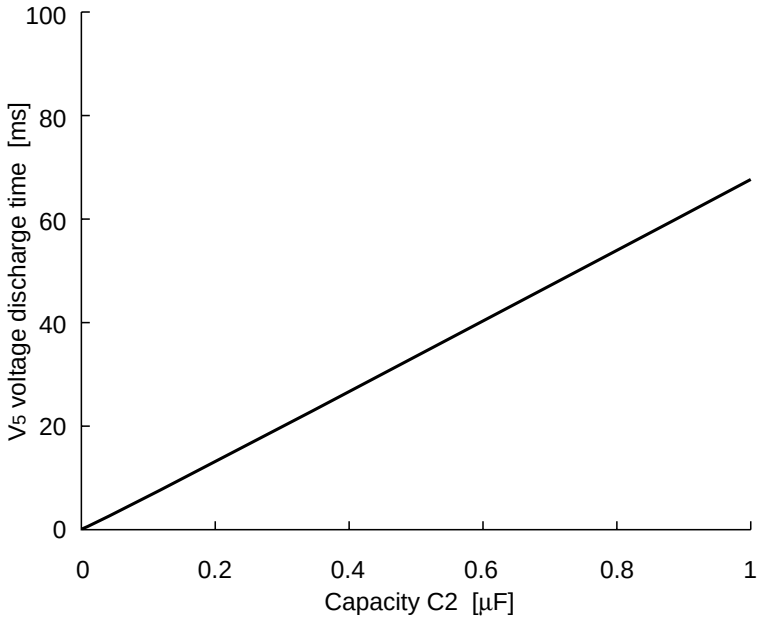


Fig. 20

Set up t_L so that the relationship, $t_L > t_H$, is maintained. A state of $t_L < t_H$ may cause faulty display.

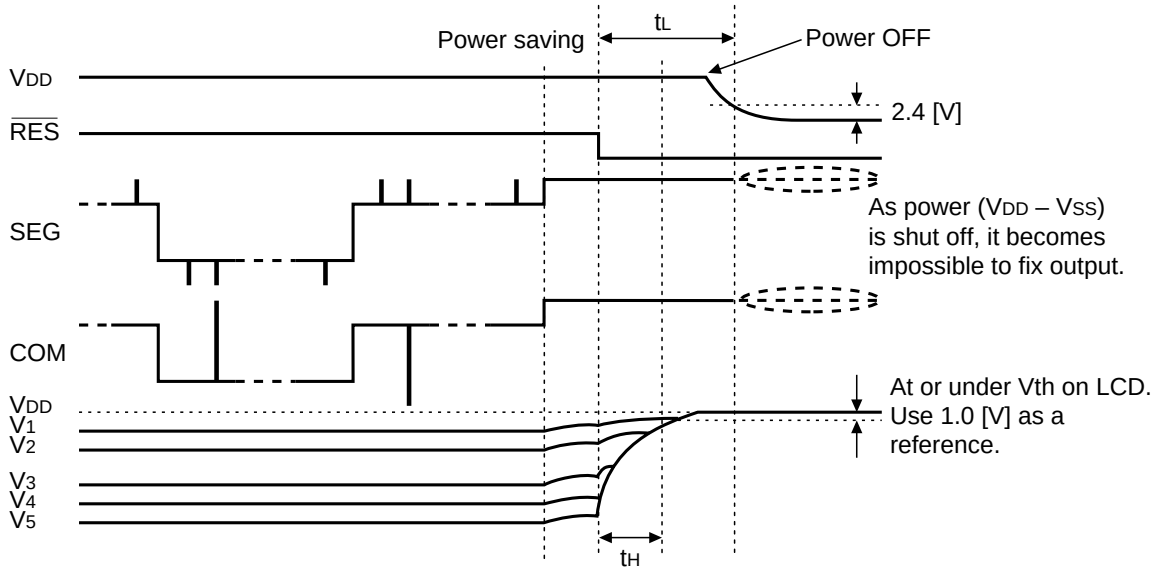
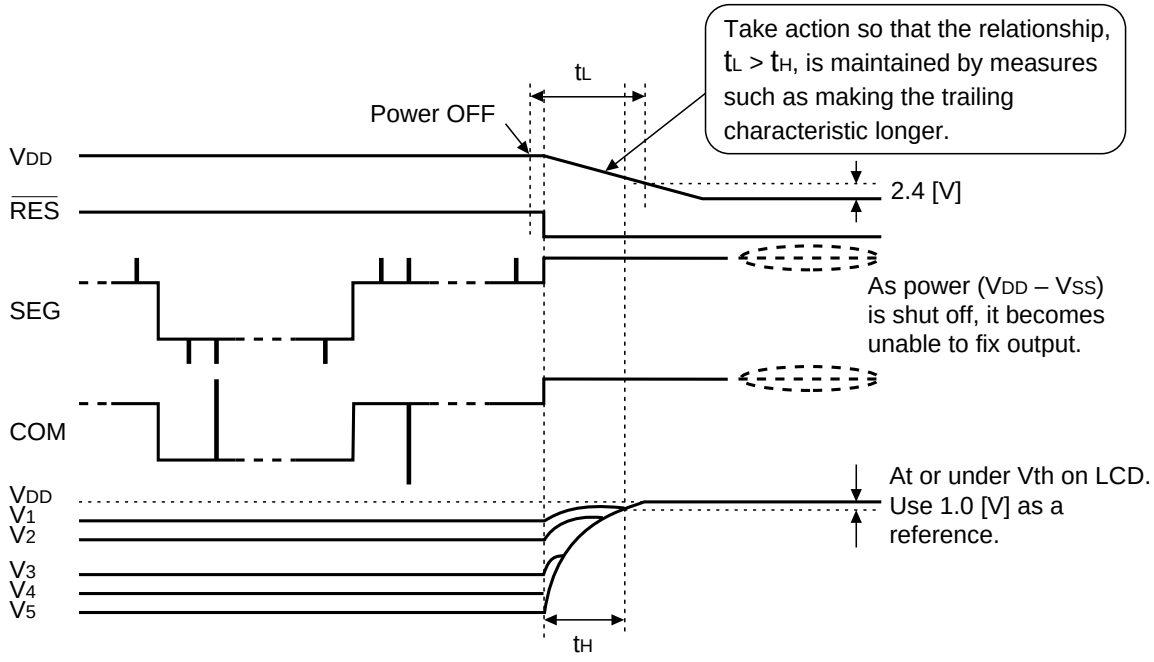


Fig. 21



If command control is disabled when power is OFF, take action so that the relationship, $t_L > t_H$, is maintained by measures such as making the trailing characteristic of power ($V_{DD} – V_{SS}$) longer.

Fig. 22

9. ABSOLUTE MAXIMUM RATINGS

Table 17

V_{SS}=0 V unless specified otherwise

Item		Symbol	Specification value			Unit
Power supply voltage		V_{DD}	–0.3	to	+7.0	V
Power supply voltage (2) (Based on V_{DD})		V_{SS2}	–7.0	to	+0.3	
	At triple boosting		–6.0	to	+0.3	
	At quadruple boosting		–4.5	to	+0.3	
Power supply voltage (3) (Based on V_{DD})		V_5, V_{OUT}	–20.0	to	+0.3	
Power supply voltage (4) (Based on V_{DD})		V_1, V_2, V_3, V_4	V_5	to	+0.3	
Input voltage		V_{IN}	–0.3	to	V_{DD}+0.3	
Output voltage		V_O	–0.3	to	V_{DD}+0.3	
Operating temperature		T_{OPR}	–40	to	+85	°C
Storage temperature	TCP	T_{STR}	–55	to	+100	
	Bare chip		–55	to	+125	

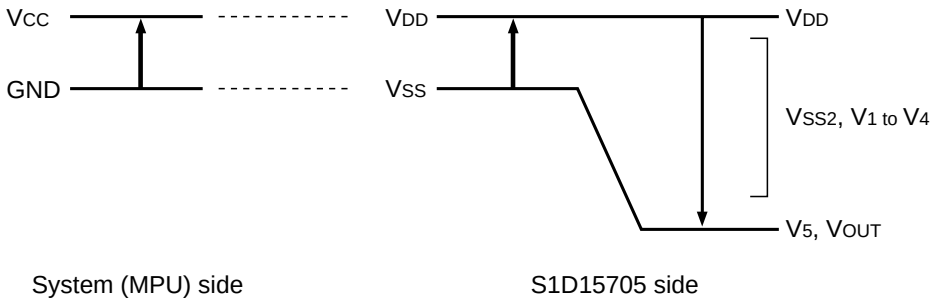


Fig. 23

(Notes) 1. The values of the V_{SS2}, V_1 to V_5, and V_{OUT} voltages are based on V_{DD}=0 V.
2. The V_1, V_2, V_3, and V_4 voltages must always satisfy the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$.
3. The V_{SS2} and V_{OUT} voltages must always satisfy the condition of $V_{DD} \geq V_{SS} \geq V_{SS2} \geq V_{OUT}$.
4. When LSI is used exceeding the absolute maximum ratings, the LSI may be damaged permanently. Besides, it is desirable that the LSI should be used in the electrical characteristics condition for normal operation. If this condition is exceeded, the LSI may malfunction and have an adverse effect on the reliability of the LSI.

10. DC CHARACTERISTICS

Table 18

Unless otherwise specified, V_{SS}=0 V, Ta=–40 to 85°C

Item	Symbol	Condition	Specification value Min.	Typ.	Max.	Unit	Applicable pin
Operating voltage (1)	V_{DD}	S1D15705⋆03⋆⋆/S1D15707⋆03⋆⋆	2.4	—	3.6	V	V_{DD} *1
	V_{DD}	S1D15705⋆00⋆⋆/S1D15707⋆00⋆⋆ /S1D15708⋆00⋆⋆	3.6	—	5.5		V_{DD} *1
Operating voltage (2)	V_{SS2}	(Based on VDD)	–6.0	—	–1.8		V_{SS2}
Operating voltage (3)	V_5	S1D15705⋆⋆⋆⋆⋆ (Based on V_{DD})	–18.0	—	–4.5		V_5 *2
	V_5	S1D15707⋆⋆⋆⋆⋆ (Based on V_{DD})	–16.0	—	–4.5		V_5 *2
	V_5	S1D15708⋆⋆⋆⋆⋆ (Based on V_{DD})	–10.0	—	–4.5		V_5 *2
	V_1, V_2	(Based on VDD)	0.4×V_5	—	V_{DD}		V_1, V_2
	V_3, V_4	(Based on V_{DD})	V_5	—	0.6×V_5		V_3, V_4
High level input voltage	V_{IHC}		0.8×V_{DD}	—	V_{DD}		*3
Low level input voltage	V_{ILC}		V_{SS}	—	0.2×V_{DD}		*3
High level output voltage	V_{OHC}	I_{OH}=–0.5mA	0.8×V_{DD}	—	V_{DD}		*4
Low level output voltage	V_{OLC}	I_{OL}=0.5mA	V_{SS}	—	0.2×V_{DD}		*4
Input leak current	I_{LI}	V_{IN}=V_{DD} or V_{SS}	–1.0	—	1.0	µA	*5
Output leak current	I_{LO}		–3.0	—	3.0		*6
Liquid crystal driver On resistance	R_{ON}	Ta=25°C, V_5=–14.0V	—	2.0	3.5	kΩ	SEGn
		(Based on V_{DD}) V_5=–8.0V	—	3.2	5.4		COMn *7
Static current consumption	I_{SSQ}		—	0.01	5	µA	V_{SS}, V_{SS2}
Output leak current	I_{5Q}	V_5=–18.0V (Based on V_{DD})	—	0.01	15		V_5
Input pin capacity	C_{IN}	Ta=25°C, f=1MHz	—	5.0	8.0	pF	
Oscillating frequency: Built-in oscillation	f_{OSC}	Ta=25°C	18	22	26		*8
Oscillating frequency: External input	f_{CL}	Ta=25°C, S1D15705⋆⋆⋆⋆⋆	4.5	5.5	6.5	kHz	CL *8
		Ta=25°C, S1D15707⋆⋆⋆⋆⋆	2.25	2.75	3.25		CL *8
		Ta=25°C, S1D15708⋆⋆⋆⋆⋆	1.13	1.38	1.63		CL *8

Table 19

	Item	Symbol	Condition	Specification value Min.	Typ.	Max.	Unit	Applicable pin
Built-in power supply circuit	Input voltage	V_{SS2}	At triple boosting (Based on V_{DD})	–6.0	—	–1.8	V	V_{SS2}
		V_{SS2}	At quadruple boosting (Based on V_{DD})	–4.5	—	–1.8		V_{SS2}
	Boosting output voltage	V_{OUT}	(Based on V_{DD}) –20.0	—	—		V_{OUT}	
	Voltage adjusting circuit operating voltage	V_{OUT}	(Based on V_{DD}) –20.0	—	–6.0		V_{OUT}	
	V/F circuit operating voltage	V_5	S1D15705⋆⋆⋆⋆⋆ (Based on V_{DD})	–18.0	—	–4.5		V_5 *9
		V_5	S1D15707⋆⋆⋆⋆⋆ (Based on V_{DD})	–16.0	—	–4.5		V_5 *9
		V_5	S1D15708⋆⋆⋆⋆⋆ (Based on V_{DD})	–10.0	—	–4.5		V_5 *9
	Reference voltage	V_{REG0}	Ta=25°C, –0.05%/°C	–2.04	–2.10	–2.16		*10

[*: see Page 61.]

Dynamic current consumption value (1) During display operation and built-in power supply OFF
Current values dissipated by the whole IC when the external power supply is used

Table 20-1 Display All White Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
S1D15705⋆00⋆⋆	I_{DD} (1)	V_{DD}=5.0V, V_5–V_{DD}=–11.0V	—	22	37	µA	*11
S1D15705⋆03⋆⋆		V_{DD}=3.0V, V_5–V_{DD}=–11.0V	—	22	37		
S1D15707⋆00⋆⋆		V_{DD}=5.0V, V_5–V_{DD}=–8.0V		8	14		
S1D15707⋆03⋆⋆		V_{DD}=3.0V, V_5–V_{DD}=–8.0V		8	14		
S1D15708⋆00⋆⋆		V_{DD}=5.0V, V_5–V_{DD}=–6.0V		4	7		

Table 20-2 Display Checker Pattern Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
S1D15705⋆00⋆⋆	I_{DD} (1)	V_{DD}=5.0V, V_5–V_{DD}=–11.0V	—	33	55	µA	*11
S1D15705⋆03⋆⋆		V_{DD}=3.0V, V_5–V_{DD}=–11.0V	—	32	54		
S1D15707⋆00⋆⋆		V_{DD}=5.0V, V_5–V_{DD}=–8.0V		14	24		
S1D15707⋆03⋆⋆		V_{DD}=3.0V, V_5–V_{DD}=–8.0V		14	24		
S1D15708⋆00⋆⋆		V_{DD}=5.0V, V_5–V_{DD}=–6.0V		5	9		

Dynamic current consumption value (2) During display operation and built-in power supply ON
Current values dissipated by the whole IC containing the built-in power supply circuit

Table 21-1 Display Checker Pattern Ta=25°C

Item	Symbol	Condition		Specification value			Unit	Remarks
				Min.	Typ.	Max.		
S1D15705⋆00⋆⋆	I_{DD} (2)	V_{DD}=5.0V, Triple boosting	Normal mode	—	73	122	µA	*12
		V_5–V_{DD}=–11.0V	High power mode	—	216	360		
S1D15705⋆03⋆⋆		V_{DD}=3.0V, Quadruple boosting	Normal mode	—	92	154		
		V_5–V_{DD}=–11.0V	High power mode	—	272	454		
S1D15707⋆00⋆⋆		V_{DD}=5.0V, Triple boosting	Normal mode	—	40	67		
		V_5–V_{DD}=–8.0V	High power mode	—	171	285		
S1D15707⋆03⋆⋆		V_{DD}=3.0V, Quadruple boosting	Normal mode	—	51	85		
		V_5–V_{DD}=–8.0V	High power mode	—	228	380		
S1D15708⋆00⋆⋆		V_{DD}=5.0V, Double boosting	Normal mode	—	28	47		
		V_5–V_{DD}=–6.0V	High power mode	—	137	229		

[*: see Page 61.]

Table 21-2 Display Checker Pattern Ta=25°C

Item	Symbol	Condition		Specification value			Unit	Remarks
				Min.	Typ.	Max.		
S1D15705∗00∗∗	I_{DD} (2)	V_{DD}=5.0V, Triple boosting	Normal mode	—	97	162	μA	*12
		V_5–V_{DD}=–11.0V	High power mode	—	254	424		
S1D15705∗03∗∗		V_{DD}=3.0V, Quadruple boosting	Normal mode	—	130	217		
		V_5–V_{DD}=–11.0V	High power mode	—	308	514		
S1D15707∗00∗∗		V_{DD}=5.0V, Triple boosting	Normal mode	—	54	90		
		V_5–V_{DD}=–8.0V	High power mode	—	185	309		
S1D15707∗03∗∗		V_{DD}=3.0V, Quadruple boosting	Normal mode	—	71	119		
		V_5–V_{DD}=–8.0V	High power mode	—	248	414		
S1D15708∗00∗∗		V_{DD}=3.0V, Double boosting	Normal mode	—	35	59		
		V_5–V_{DD}=–6.0V	High power mode	—	144	240		

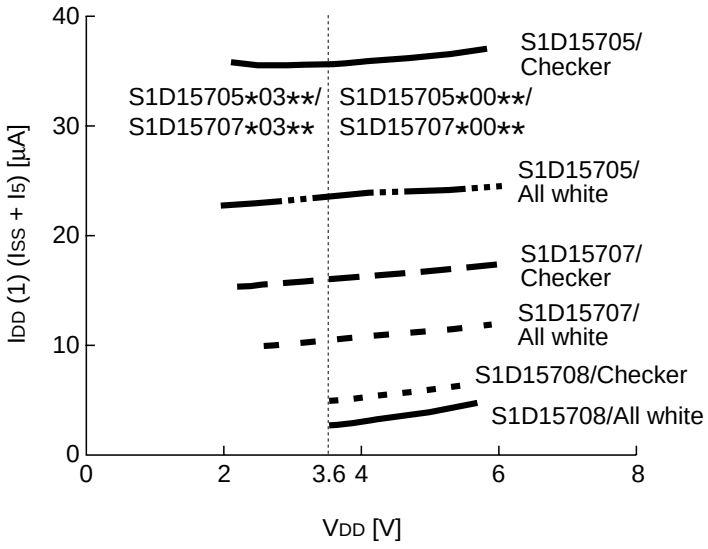
Current consumption at power save V_{SS}=0 V and V_{DD}= 3.0 V ±10% (S1D15705∗03∗∗, S1D15707∗03∗∗)
5.0V ± 10% (S1D15705∗00∗∗, S1D15707∗00∗∗,
S1D15708∗00∗∗)

Table 22 Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
Sleep state	I_{DDS1}	Ta=25°C	—	0.01	5	μA	
Stand-by state	I_{DDS2}	Ta=25°C	—	4	8		

[*: see Page 61.]

[Reference data 1]
• Dynamic current consumption (1) External power supply used and LCD being displayed

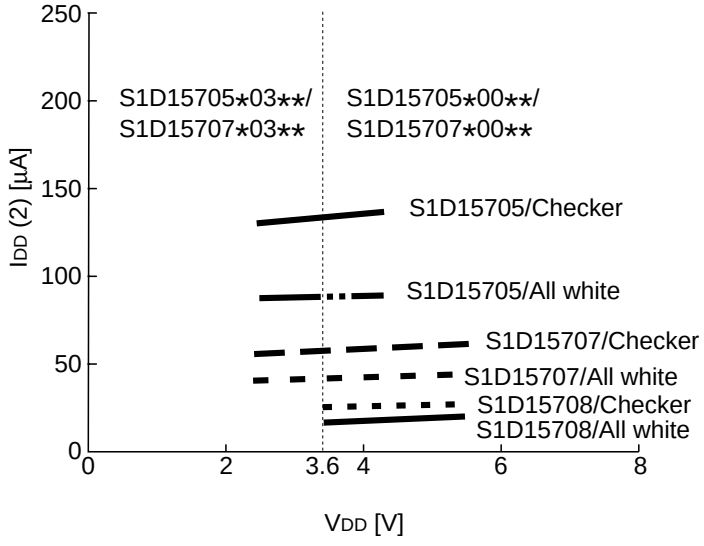


Condition: Built-in power supply OFF
External power supply used
S1D15705: $V_5 - V_{DD} = -11.0$ V
S1D15707: $V_5 - V_{DD} = -8.0$ V
S1D15708: $V_5 - V_{DD} = -6.0$ V
Display pattern: All white/checker
Ta = 25°C

Remarks: *11

Fig. 24

[Reference data 2]
• Dynamic current consumption (2) Built-in power supply used and LCD being displayed



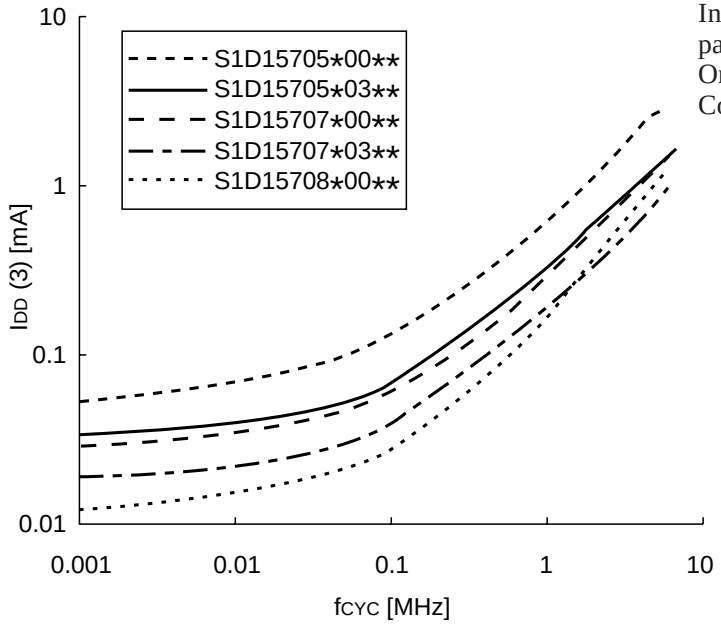
Condition: Built-in power supply ON
Normal mode
Quadruple boosting
S1D15705: $V_5 - V_{DD} = -11.0$ V
Triple boosting
S1D15707: $V_5 - V_{DD} = -8.0$ V
Double boosting
S1D15708: $V_5 - V_{DD} = -6.0$ V
Display pattern: All white/checker
Ta = 25°C

Remarks: *12

Fig. 25

[*: see page 61.]

[Reference data 3]
• Dynamic current consumption (3) During access



Indicates the current consumption when the checker pattern is always written at f_{CYC}.
Only I_{DD} (1) when not accessed
Condition: Built-in power supply OFF and external power supply used
S1D15705:
$V_5 - V_{DD} = -11.0$ V
S1D15707:
$V_5 - V_{DD} = -11.0$ V
S1D15705∗03∗∗/S1D15707∗03∗∗:
$V_{DD} - V_{SS} = 3.0$ V
S1D15705∗00∗∗/S1D15707∗00∗∗
/S1D15708∗00∗∗:
$V_{DD} - V_{SS} = 5.0$ V
Ta = 25°C

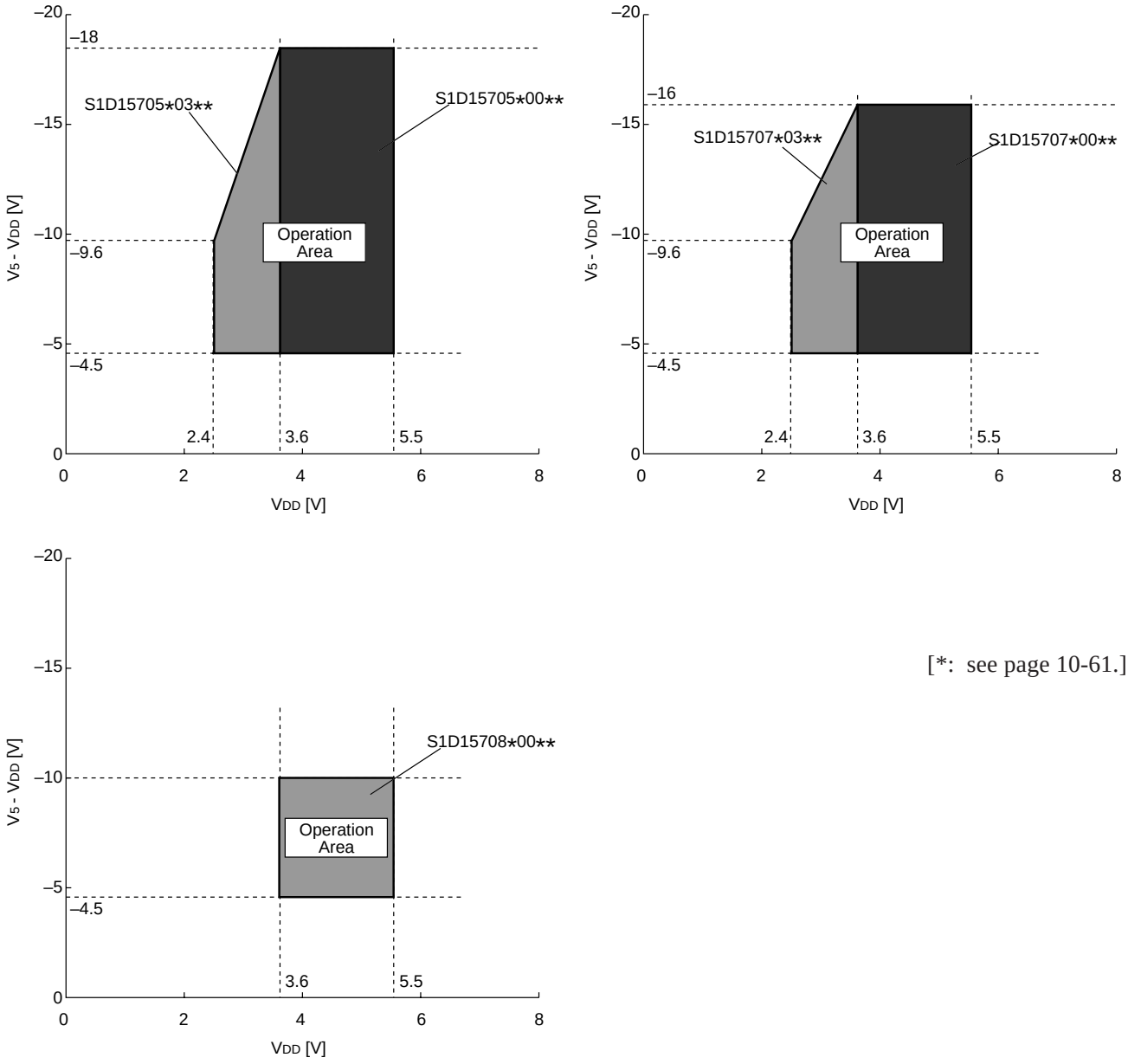
[*: see page 61.]

Fig. 26

[Reference data 4]

VSS and V5 system operating voltage ranges

Remarks: *2



[*: see page 10-61.]

Fig. 27

Relationships between the oscillating frequency fOSC, display clock frequency fCL, and liquid crystal frame frequency fFR

Table 23

Item		fCL	fFR
S1D15705*****	When built-in oscillator circuit used	$\frac{f_{OSC}}{4}$	$\frac{f_{OSC}}{4*65}$
	When built-in oscillator circuit not used	External input (fCL)	$\frac{f_{CL}}{65}$
S1D15707*****	When built-in oscillator circuit used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{8*33}$
	When built-in oscillator circuit not used	External input (fCL)	$\frac{f_{CL}}{33}$
S1D15708*****	When built-in oscillator circuit used	$\frac{f_{OSC}}{16}$	$\frac{f_{OSC}}{16*17}$
	When built-in oscillator circuit not used	External input (fCL)	$\frac{f_{CL}}{17}$

(fFR indicates the alternating current cycle of the liquid crystal and does not indicate that of the FR signal.)

[Reference items marked by *]

*1 The wide operating voltage range is not warranted. However, when there is a sudden voltage change during MPU access, it cannot be warranted.

*2 For the VDD and V5 operating voltage ranges, see Fig. 27. These ranges are applied when using the external power supply.

*3 A0, D0 to D5, D6 (SCL), D7 (SI), $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, CL, FR, M/S, C86, P/S, $\overline{DOF}$, $\overline{RES}$, $\overline{IRS}$ and HPM pins

*4 D0 to D7, FR, FRS, $\overline{DOF}$ and CL pins

*5 A0, $\overline{RD}$ (E), $\overline{WR}$ (R/W), $\overline{CS1}$, CS2, CLS, M/S, C86, P/S, $\overline{RES}$, IRS and $\overline{HPM}$ pins

*6 Applied when D0 to D5, D6 (SCL), D7 (SI), CL, FR, and $\overline{DOF}$ pins are in the high impedance state

*7 Resistance value when the 0.1 V voltage is applied between the output pin SEGn or COMn and power supply pins (V1, V2, V3, and V4). Specified within the range of operating voltage (3)
RON = 0.1 V/ΔI (ΔI indicates the current applied when 0.1 V is applied between the power ON.)

*8 For the relationship between the oscillating frequency and frame frequency, see Table 23. The specification value of the external input item is a recommended value.

*9 The V5 voltage adjusting circuit is adjusted within the voltage follower operating voltage range.

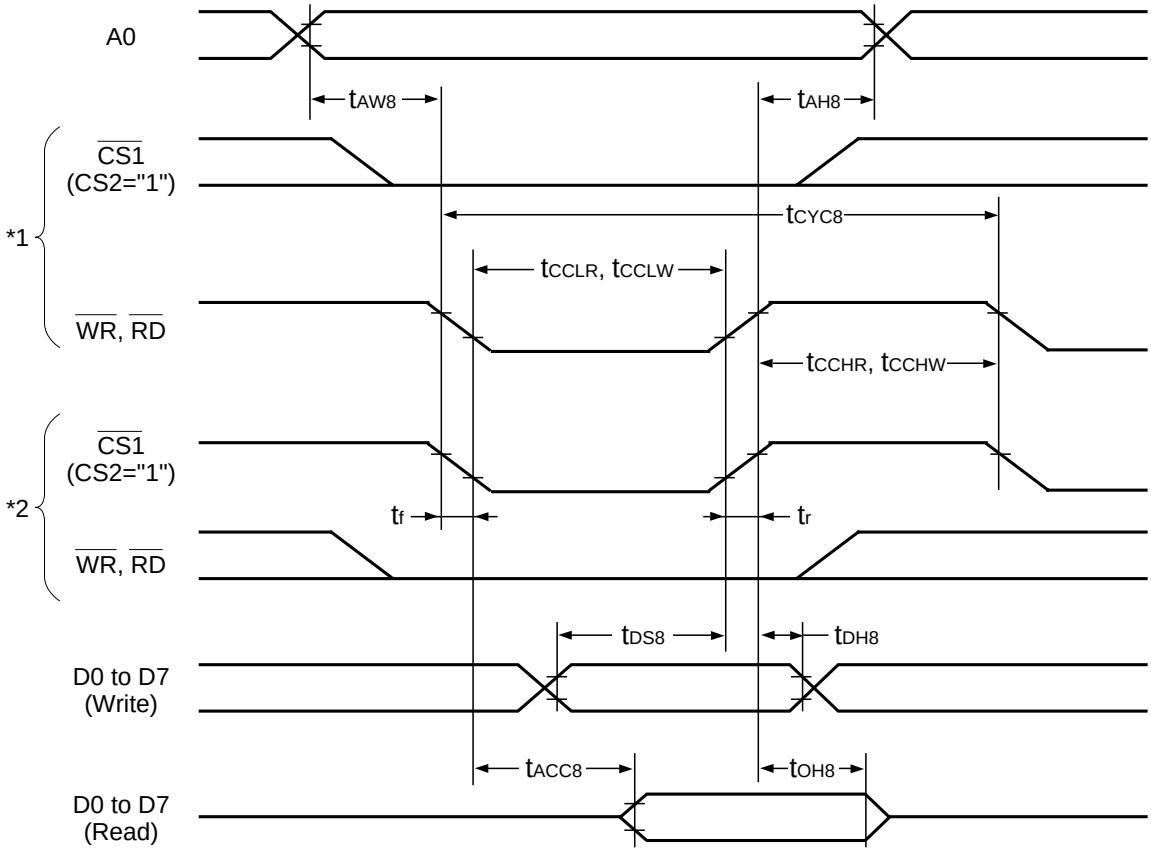
*10 Built-in reference voltage source of the V5 voltage adjusting circuit.

*11 and *12 Indicate the current dissipated by a single IC at built-in oscillator circuit used, 1/9 bias (S1D15705*****), 1/6 bias (S1D15707*****/S1D15708*****), and display ON. Does not include the current due to the LCD panel capacity and wireing capacity. Applicable only when there is no access from the MPU.

*12 When the V5 voltage adjusting built-in resistor is used

Timing Characteristics

System bus read/write characteristics 1 (80 series MPU)



[S1D15705∗00∗∗, S1D15707∗00∗∗, S1D15708∗00∗∗: V_{DD}=4.5V to 5.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		250	—	
Control LOW pulse width (Write)	$\overline{WR}$	t_{CCLW}		30	—	
Control LOW pulse width (Read)	$\overline{RD}$	t_{CCLR}		70	—	
Control HIGH pulse width (Write)	$\overline{WR}$	t_{CCHW}		30	—	
Control HIGH pulse width (Read)	$\overline{RD}$	t_{CCHR}		30	—	
Data setup time	D0 to D7	t_{DS8}		30	—	
Data hold time		t_{DH8}		10	—	
$\overline{RD}$ access time		t_{ACC8}	CL=100pF	—	70	
Output disable time		t_{OH8}		5	50	

[S1D15705⋆00⋆⋆, S1D15707⋆00⋆⋆, S1D15708⋆00⋆⋆: V_{DD}=3.6V to 4.5V, Ta=–40 to 85°C]

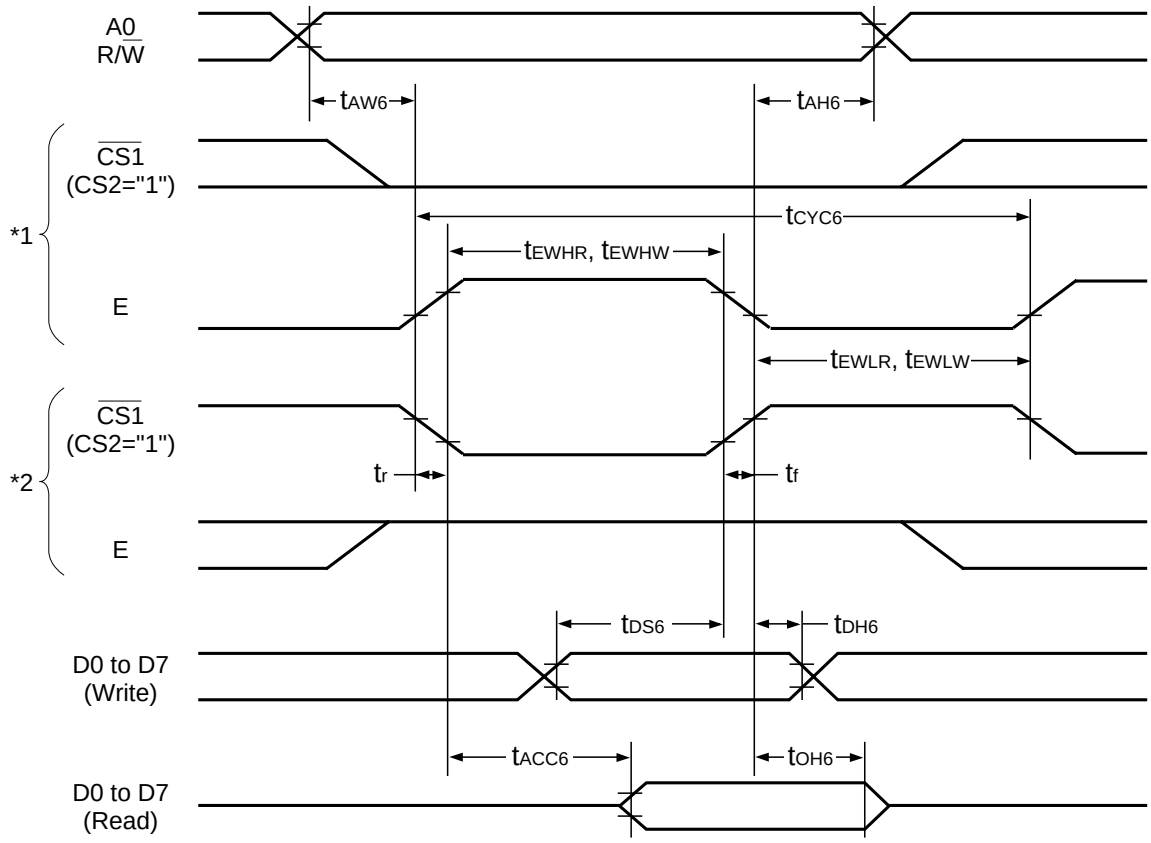
Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		300	—	
Control LOW pulse width (Write)	$\overline{WR}$	t_{CCLW}		60	—	
Control LOW pulse width (Read)	$\overline{RD}$	t_{CCLR}		120	—	
Control HIGH pulse width (Write)	$\overline{WR}$	t_{CCHW}		60	—	
Control HIGH pulse width (Read)	$\overline{RD}$	t_{CCHR}		60	—	
Data setup time	D0 to D7	t_{DS8}		40	—	
Data hold time		t_{DH8}		15	—	
$\overline{RD}$ access time		t_{ACC8}	CL=100pF	—	280	
Output disable time		t_{OH8}		10	100	

[S1D15705⋆03⋆⋆, S1D15707⋆03⋆⋆: V_{DD}=2.4V to3.6V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		800	—	
Control LOW pulse width (Write)	$\overline{WR}$	t_{CCLW}		120	—	
Control LOW pulse width (Read)	$\overline{RD}$	t_{CCLR}		240	—	
Control HIGH pulse width (Write)	$\overline{WR}$	t_{CCHW}		120	—	
Control HIGH pulse width (Read)	$\overline{RD}$	t_{CCHR}		120	—	
Data setup time	D0 to D7	t_{DS8}		80	—	
Data hold time		t_{DH8}		30	—	
$\overline{RD}$ access time		t_{ACC8}	CL=100pF	—	280	
Output disable time		t_{OH8}		10	200	

*1 This is in the case of making the access by $\overline{WR}$ and $\overline{RD}$, setting the $\overline{CS1}$=LOW.
*2 This is in the case of making the access by $\overline{CS1}$, setting the $\overline{WR}$, $\overline{RD}$=LOW.
*3 The rise and fall times (tr and tf) of the input signal are specified for less than 15 ns. When using the system cycle time at high speed, they are specified for $(t_r+t_f) \leq (t_{CYC8}-t_{CCLW}-t_{CCHW})$ or $(t_r+t_f) \leq (t_{CYC8}-t_{CCLR}-t_{CCHR})$.
*4 All timings are specified based on the 20 and 80% of V_{DD}.
*5 t_{CCLW} and t_{CCLR} are specified for the overlap period when $\overline{CS1}$ is at LOW (CS2= HIGH) level and $\overline{WR}$, $\overline{RD}$ are at the LOW level.

System bus read/write characteristics 2 (68 series MPU)



[S1D15705⋆00⋆⋆, S1D15707⋆00⋆⋆, S1D15708⋆00⋆⋆: V_{DD}=4.5V to 5.5V, Ta=–40 to 85°C]

Item		Signal	Symbol	Condition	Specification value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		0	—	ns
Address setup time			t_{AW6}		0	—	
System cycle time			t_{CYC6}		250	—	
Data setup time		D0 to D7	t_{DS6}		30	—	
Data hold time			t_{DH6}		10	—	
Access time			t_{ACC6}	CL=100pF	—	70	
Output disable time			t_{OH6}		5	50	
Enable HIGH pulse width	Read	E	t_{EWHR}		70	—	
	Write		t_{EWHW}		30	—	
Enable LOW pulse width	Read	E	t_{EWLR}		30	—	
	Write		t_{EWLW}		30	—	

[S1D15705⋆00⋆⋆, S1D15707⋆00⋆⋆, S1D15708⋆00⋆⋆: V_{DD}=3.6V to 4.5V, Ta=–40 to 85°C]

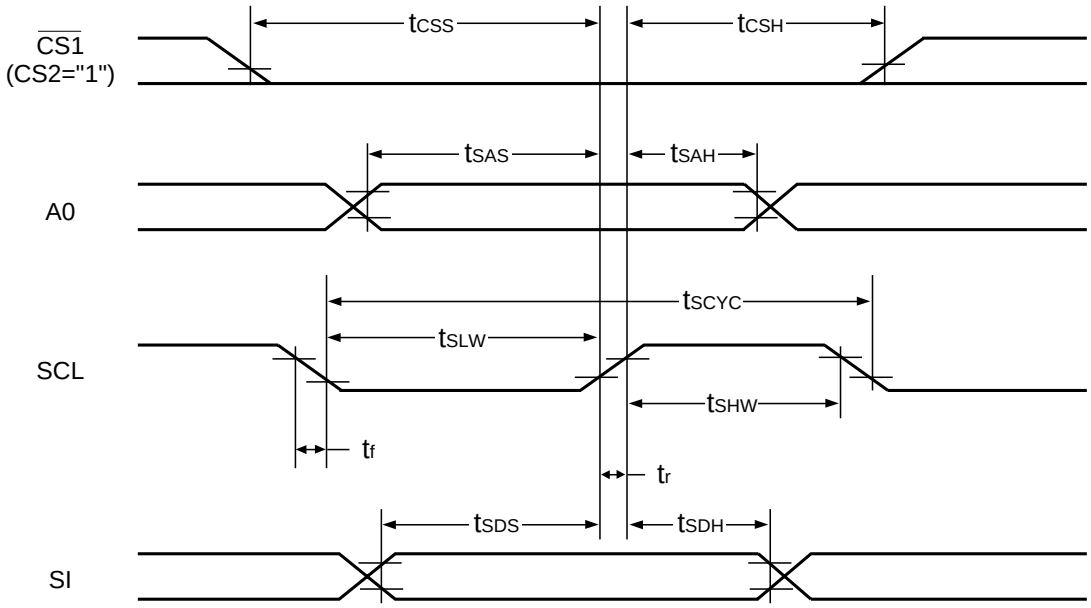
Item		Signal	Symbol	Condition	Specification value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		0	—	ns
Address setup time			t_{AW6}		0	—	
System cycle time			t_{CYC6}		300	—	
Data setup time		D0 to D7	t_{DS6}		40	—	
Data hold time			t_{DH6}		15	—	
Access time			t_{ACC6}	CL=100pF	—	140	
Output disable time			t_{OH6}		10	100	
Enable HIGH pulse width	Read	E	t_{EWHR}		120	—	
	Write		t_{EWHW}		60	—	
Enable LOW pulse width	Read	E	t_{EWLR}		60	—	
	Write		t_{EWLW}		60	—	

[S1D15705⋆03⋆⋆, S1D15707⋆03⋆⋆: V_{DD}=2.4V to 3.6V, Ta=–40 to 85°C]

Item		Signal	Symbol	Condition	Specification value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		0	—	ns
Address setup time			t_{AW6}		0	—	
System cycle time			t_{CYC6}		800	—	
Data setup time		D0 to D7	t_{DS6}		80	—	
Data hold time			t_{DH6}		30	—	
Access time			t_{ACC6}	CL=100pF	—	280	
Output disable time			t_{OH6}		10	200	
Enable HIGH pulse width	Read	E	t_{EWHR}		240	—	
	Write		t_{EWHW}		120	—	
Enable LOW pulse width	Read	E	t_{EWLR}		120	—	
	Write		t_{EWLW}		120	—	

*1 This is in the case of making the access by E, setting the $\overline{CS1}$=LOW.
*2 This is in the case of making the access by $\overline{CS1}$, setting the E=HIGH.
*3 The rise and fall times (tr and tf) of the input signal are specified for less than 15 ns. When using the system cycle time at high speed, they are specified for $(t_r+t_f) \leq (t_{CYC6}-t_{EWLW}-t_{EWHW})$ or $(t_r+t_f) \leq (t_{CYC6}-t_{EWLR}-t_{EWHR})$.
*4 All timings are specified based on the 20 and 80% of V_{DD}.
*5 t_{EWLW} and t_{EWLR} are specified for the overlap period when $\overline{CS1}$ is at LOW (CS2= HIGH) level and E is at the HIGH level.

Serial interface



[S1D15705⋆00⋆⋆, S1D15707⋆00⋆⋆, S1D15708⋆00⋆⋆: V_{DD}=4.5V to 5.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	t_{SCYC}		200	—	ns
SCL HIGH pulse width		t_{SHW}		75	—	
SCL LOW pulse width		t_{SLW}		75	—	
Address setup time	A0	t_{SAS}		50	—	
Address hold time		t_{SAH}		100	—	
Data setup time	SI	t_{SDS}		50	—	
Data hold time		t_{SDH}		50	—	
CS-SCL time	CS	t_{CSS}		100	—	
		t_{CSH}		100	—	

[S1D15705⋆00⋆⋆, S1D15707⋆00⋆⋆, S1D15708⋆00⋆⋆: V_{DD}=3.6V to 4.5V, Ta=–40 to 85°C]

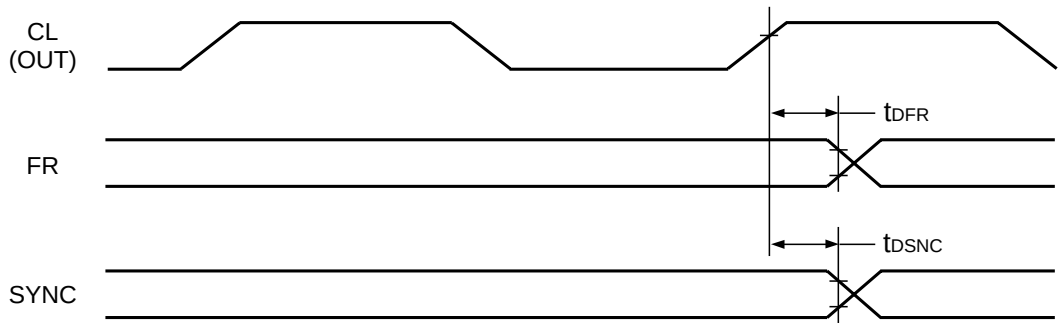
Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	t_{SCYC}		250	—	ns
SCL HIGH pulse width		t_{SHW}		100	—	
SCL LOW pulse width		t_{SLW}		100	—	
Address setup time	A0	t_{SAS}		150	—	
Address hold time		t_{SAH}		150	—	
Data setup time	SI	t_{SDS}		100	—	
Data hold time		t_{SDH}		100	—	
CS-SCL time	CS	t_{CSS}		150	—	
		t_{CSH}		150	—	

[S1D15705⋆03⋆⋆, S1D15707⋆03⋆⋆: V_{DD}=2.4V to 3.6V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	t_{SCYC}		400	—	ns
SCL HIGH pulse width		t_{SHW}		150	—	
SCL LOW pulse width		t_{SLW}		150	—	
Address setup time	A0	t_{SAS}		250	—	
Address hold time		t_{SAH}		250	—	
Data setup time	SI	t_{SDS}		150	—	
Data hold time		t_{SDH}		150	—	
CS-SCL time	CS	t_{CSS}		250	—	
		t_{CSH}		250	—	

*1 The rise and fall times (tr and tf) of the input signal are specified for less than 15 ns.
*2 All timings are specified based on the 20 and 80% of V_{DD}.

Display control output timing



[S1D15705⋆00⋆⋆, S1D15707⋆00⋆⋆, S1D15708⋆00⋆⋆: V_{DD}=4.5V to 5.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL=50pF	—	10	40	ns
SYNC delay time	SYNC	t_{DSNC}	CL=50pF	—	10	40	ns

[S1D15705⋆00⋆⋆, S1D15707⋆00⋆⋆, S1D15708⋆00⋆⋆: V_{DD}=3.6V to 4.5V, Ta=–40 to 85°C]

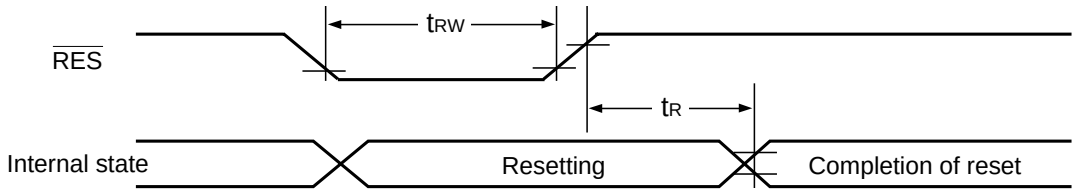
Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL=50pF	—	20	80	ns
SYNC delay time	SYNC	t_{DSNC}	CL=50pF	—	20	80	ns

[S1D15705⋆03⋆⋆, S1D15707⋆03⋆⋆: V_{DD}=2.4V to 3.6V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL=50pF	—	50	200	ns
SYNC delay time	SYNC	t_{DSNC}	CL=50pF	—	50	200	ns

*1 Valid only when the master mode is selected.
*2 All timings are specified based on the 20 and 80% of V_{DD}.
*3 Pay attention not to cause delays of the timing signals CL, FR and SYNC to the salve side by wiring resistance, etc., while master/slave operations are in progress. If these delays occur, indication failures such as flickering may occur.

Reset input timing



[S1D15705⋆00⋆⋆, S1D15707⋆00⋆⋆, S1D15708⋆00⋆⋆: V_{DD}=4.5V to 5.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		t_R		—	—	0.5	µs
Reset LOW pulse width	RES	t_{RW}		0.5	—	—	

[S1D15705⋆00⋆⋆, S1D15707⋆00⋆⋆, S1D15708⋆00⋆⋆: V_{DD}=3.6V to 4.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1	µs
Reset LOW pulse width	RES	t_{RW}		1	—	—	

[S1D15705⋆03⋆⋆, S1D15707⋆03⋆⋆: V_{DD}=2.4V to 3.6V, Ta=–40 to 85°C]

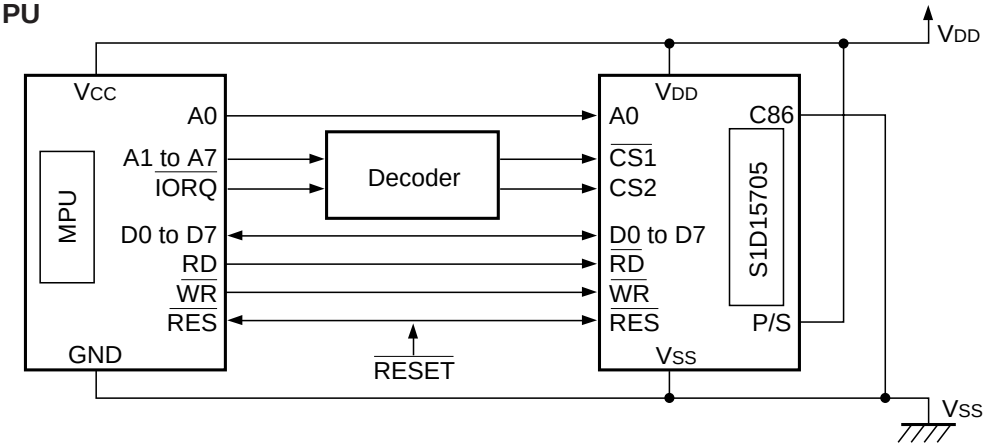
Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1.5	µs
Reset LOW pulse width	RES	t_{RW}		1.5	—	—	

*1 All timings are specified based on the 20 and 80% of V_{DD}.

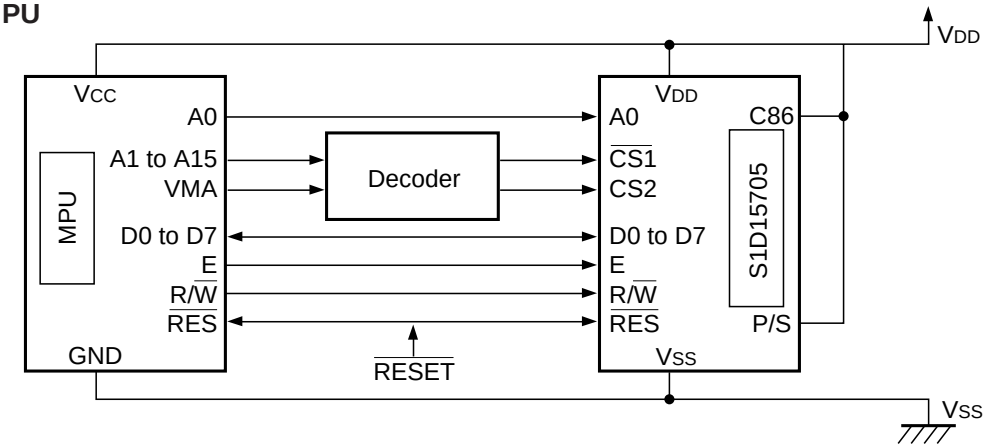
11. MICROPROCESSOR (MPU) INTERFACE: REFERENCE

The S1D15705 series can directly be connected to the 80 system MPU and 68 series MUP. It can also be operated with a fewer signal lines by using the serial interface.
The S1D15705 series is used for the multiple chip configuration to expand the display area. In this case, it can select the ICs that are accessed individually using the Chip Select signal.
After the initialization using the $\overline{RES}$ pin, the respective input pins of the S1D15705 series need to be controlled normally.

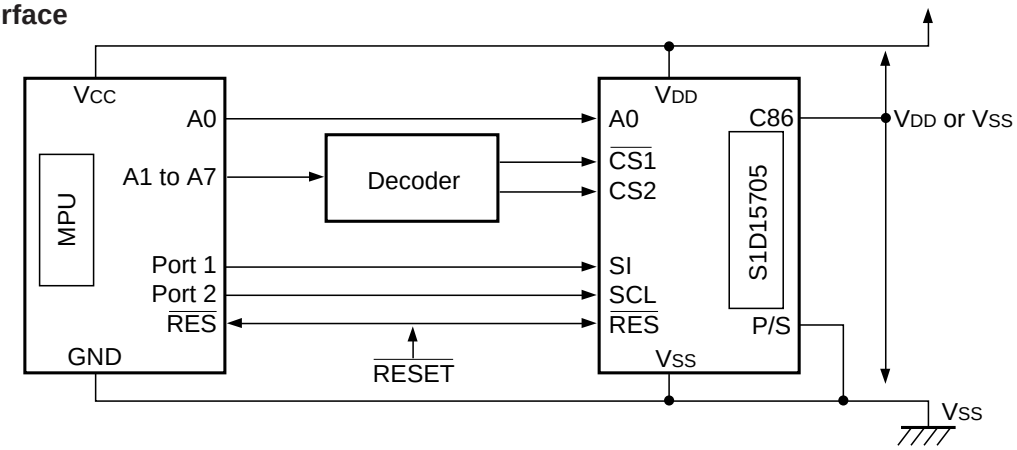
80 series MPU



68 series MPU



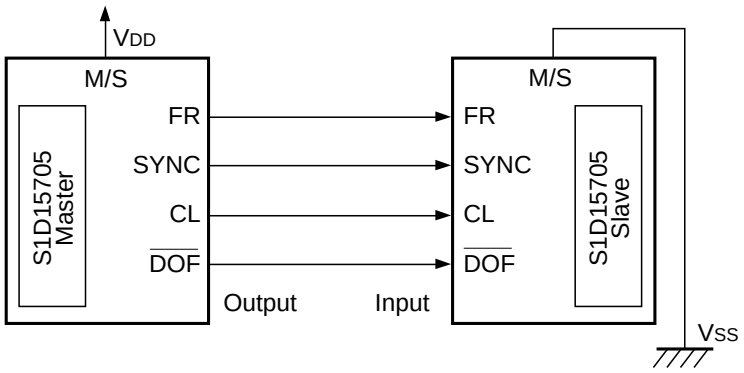
Serial interface



12. CONNECTION BETWEEN LCD DRIVERS: REFERENCE

The S1D15705 series is used for the multiple chip configuration to easily expand the liquid crystal display area. Use the same device (S1D15705*****/S1D15705*****, S1D15707*****/S1D15707***** or S1D15708*****/S1D15708*****) for the master/slave.

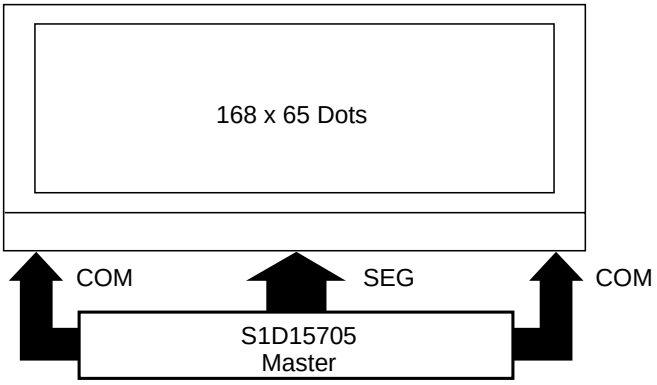
S1D15705 (master) ↔ S1D15705 (slave)



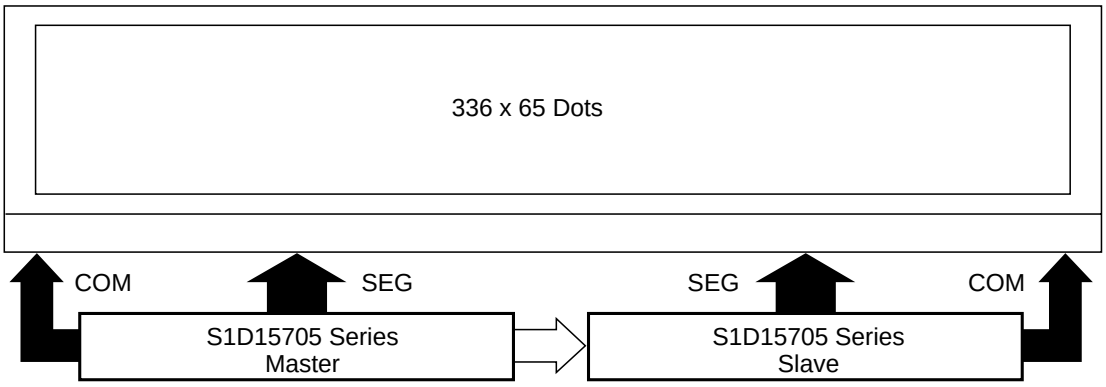
13. LCD PANEL WIRING: REFERENCE

The S1D15705 series is used for the multiple chip configuration to easily expand the liquid crystal display area. Use the same device (S1D15705*****/S1D15705*****, S1D15707*****/S1D15707***** or S1D15708*****/S1D15708*****) for the multiple chip configuration.

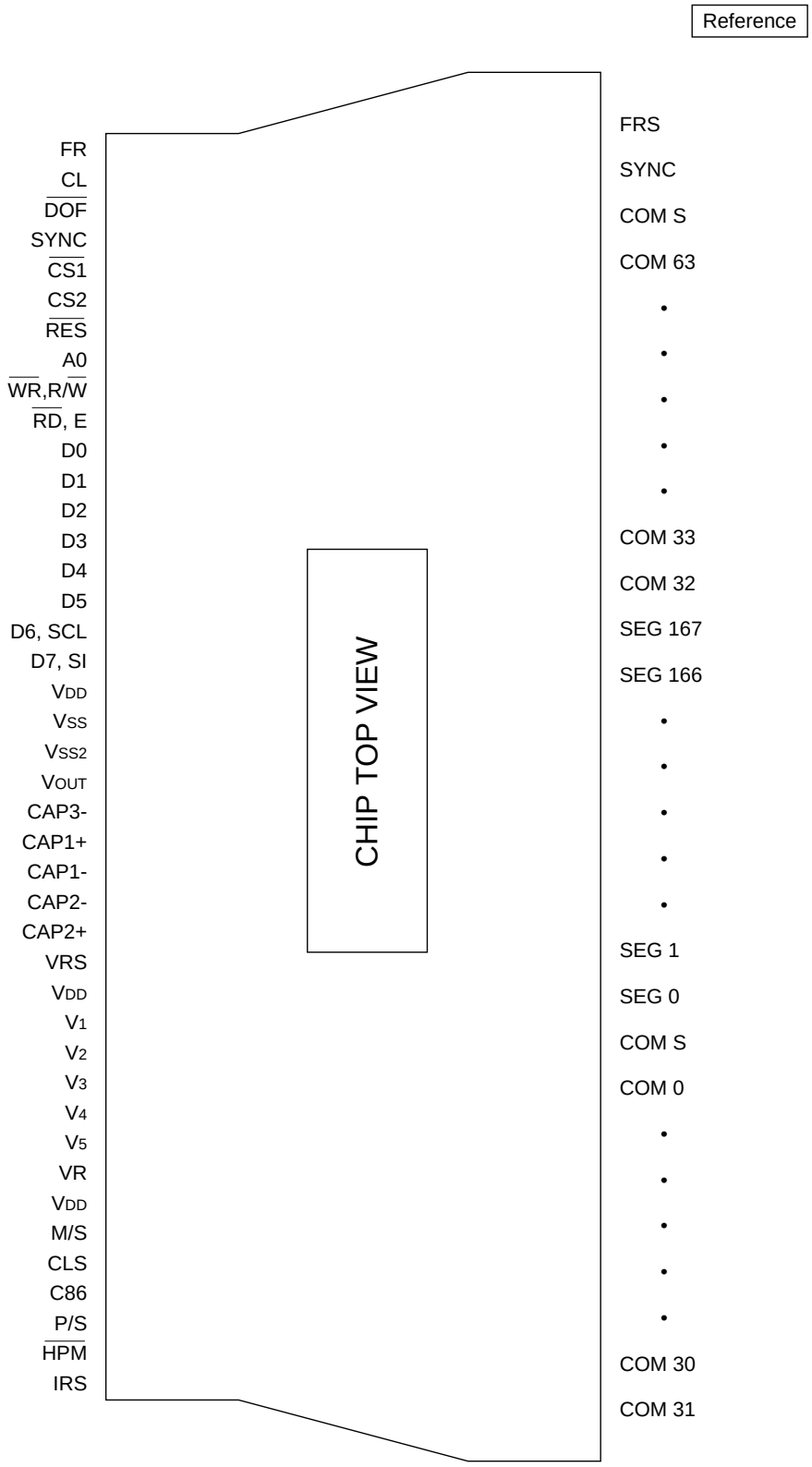
1-chip configuration



2-chip configuration

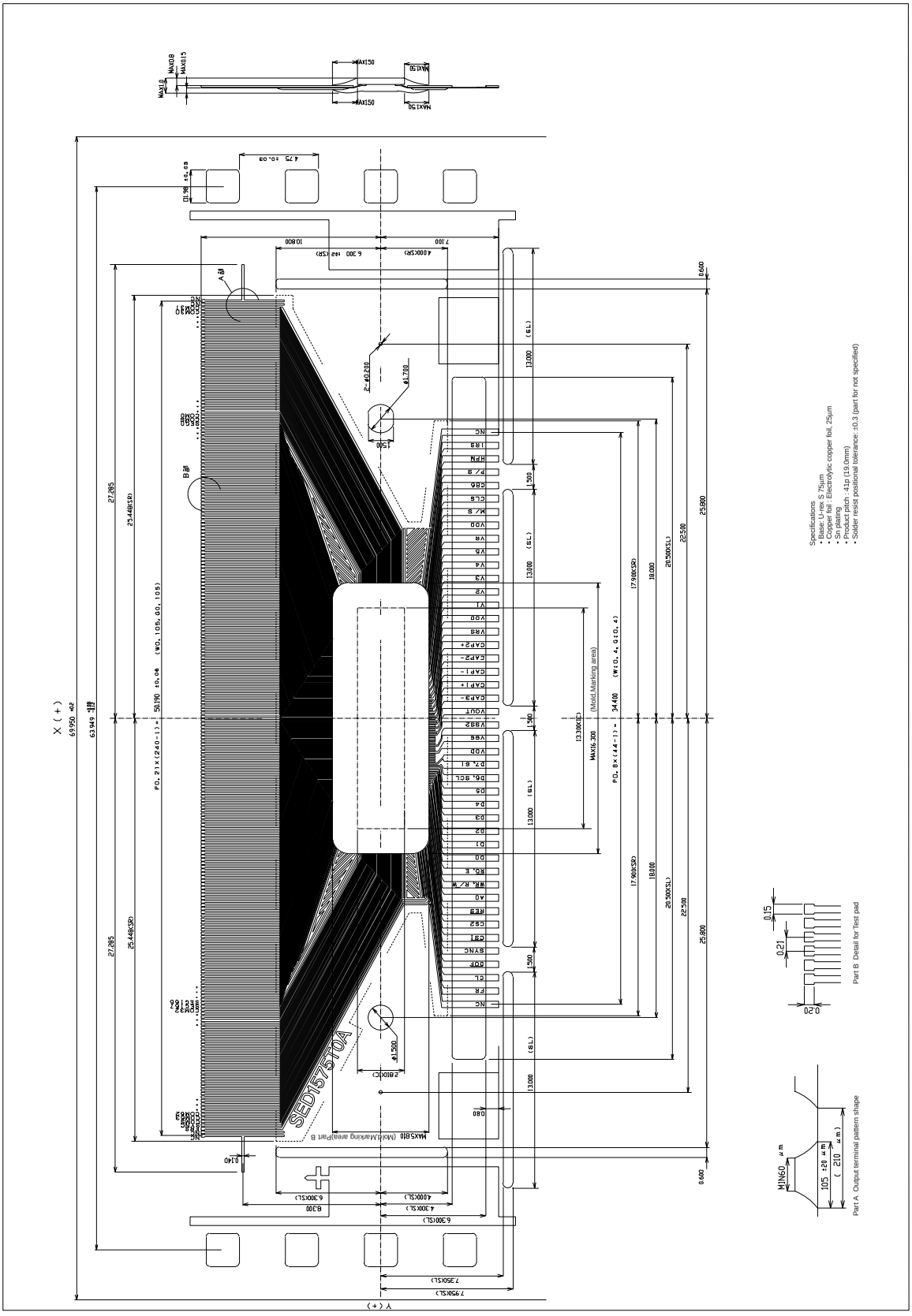


14. TCP PIN LAYOUT



Note) This TCP pin layout does not specify the TCP dimensions.

15. TCP DIMENSIONS



16. TEMPERATURE SENSOR CIRCUIT

S1D15705∗10∗∗ incorporates a temperatujre sensor circuit with a 11.4mV/°C (typ.) temperature gradient carrying analog voltage output pins. The S1D15705∗10∗∗ makes it possible to provide LCD indications with optimum contrast throughout a wide temperature range without need for use of supplementary parts by inputting electronic volume control registration value equivalent signals corresponding to the outputs of the temperature sensor through the MPU to control the LCD drive voltage V_5.
For LCD drive voltage controls of higher precision, we recommend you to constitute a system which can absorb deviations of the output voltage by, such as, feeding back sampled output voltages under a certain temperature environment to the MPU to let it memorize as the reference voltages.
Regarding the specifications of other items than the temperature sensor circuit, such as of the absolute maximum ratings, DC characteristics, AC characteristics, etc., refer to the specifications for S1D15705∗00∗∗.

Pin Definitions

Temperature sensor circuit related pins are allocated to TEST1, 2, 3 and 4 and the pin names are TEST1, SVS, V_{SEN}, SEN and SENSEL in the given sequence. The temperature sensor should be used under the pin statuses indicated in the Table below. When the temperature sensor is not being used, fix respective pins to HIGH.

Pin names	I/O	Pin definitions	Number of pins
SVS	Power supply	This is the power supply pin for the temperature sensor. Apply prescribed operating voltage between the V_{DD}.	1
V_{SEN}	O	This is the analog voltage output pin for the temperature sensor. Monitor the output voltage between the V_{DD}.	1
SEN	O	Consider to keep this pin open in order not to apply the load capacitance of wires, etc.	1
SENSEL	I	Fix this pin to HIGH.	1

Electric Characteristics

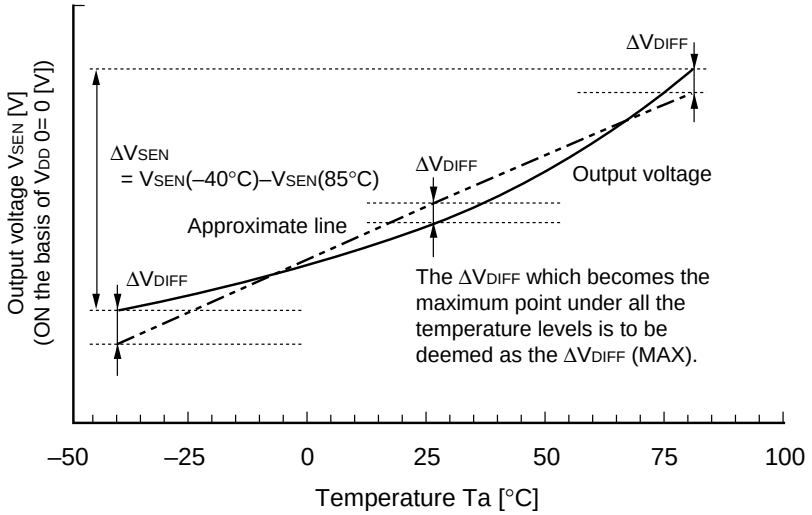
Items	Codes	Conditions	Specifications			Units	Applicable pins
			Min.	Typ.	Max.		
Operating voltage	SVS	(On the basis of V_{DD})	–5.5	–5.0	–4.5	V	SVS
Output voltage	V_{SEN}	(On the basis of V_{DD}) Ta = 40°C	–4.35	–3.62	–2.89	V	V_{SEN}
		(On the basis of V_{DD}) Ta = 25°C	–3.48	–2.88	–2.28		
		(On the basis of V_{DD}) Ta = 85°C	–2.92	–2.20	–1.47		
Output voltage temperature gradient	V_{GRA}	*1	9.4	11.4	13.4	mV/°C	V_{SEN}
Output voltage linearity	ΔV_L	*2	–1.5	—	1.5	%	V_{SEN}
Output voltage setup time	t_{SEN}	*3	100	—	—	mS	V_{SEN}
Operating current	I_{SEN}	Ta = 25°C	—	40	150	µA	SVS

[* Notes]

*1: Represents the gradient of the approximate line of the Typ. output voltages.

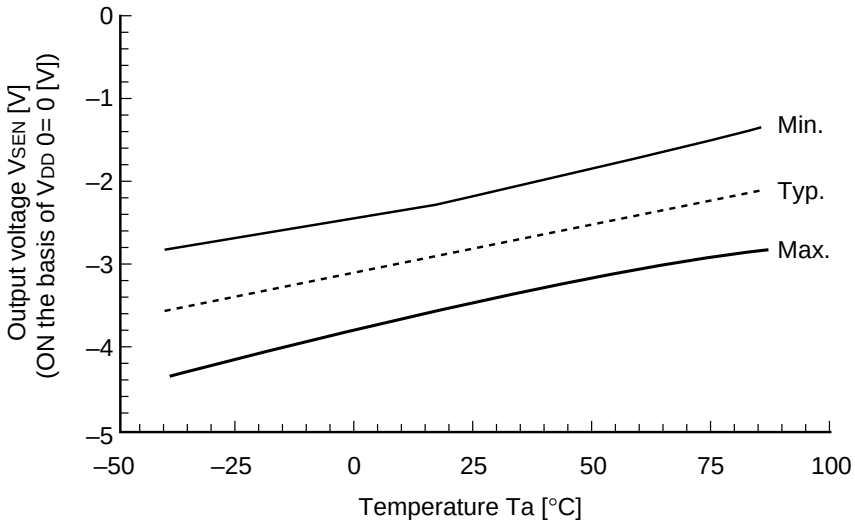
*2: Represents the maximum deviation between the output voltage curve and the approximate line. Assuming that the difference of output voltages at –40°C and at 80°C as ΔV_{SEN}, assuming that the difference between the approximate line and the output voltage values as ΔDIFF and assuming that the maximum value thereof as ΔDIFF (MAX), the output voltages linearity ΔV_L can be calculated by use of the following equation.

$$\Delta V_L = \frac{\Delta DIFF\ (MAX)}{\Delta V_{SEN}} \times 100$$



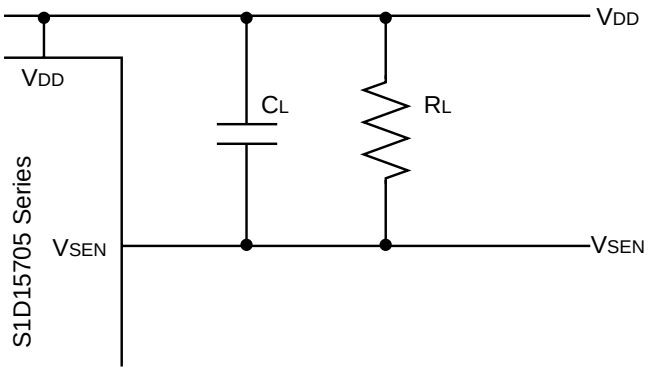
*3: Represents the queuing time after the supply voltage SVS is applied to the SVS pin until the output voltage is stabilized and monitoring thereof becomes feasible. Be sure to sample the output voltage after the prescribed queuing time has elapsed.

Output voltage characteristics



Output Pin Load

Maintain the load capacity C_L for the V_{SEN} output pin V_{SEN} at 100pF or less and keep the load resistance R_L for the V_{SEN} output pin V_{SEN} at 1MΩ or more.
In order to obtain accurate output voltage values, be careful not to insert a current flowing channel between the V_{SS}.



11. S1D15710 Series

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1. DESCRIPTION

The S1D15710 Series is a single-chip dot matrix liquid crystal display driver that can be connected directly to a microprocessor bus. Eight-bit parallel or serial display data transmitted from the microprocessor is stored in the internal display data RAM, and the chip generates liquid crystal drive signals, independently of the microprocessor.
It has a on-chip 65 × 256-bit display data RAM, and there is a one-to-one correspondence between the dot pixel on the liquid crystal panel pixels and internal RAM bit. This feature ensures implementation of highly free display.
The S1D15710 Series incorporate 65 common output circuits and 224 segment output circuits. A single chip can drive a 65 × 224 dot display (capable of displaying 14 columns × 4 rows with 16 × 16-dot kanji font). Further, display capacity can be extended by designing two chips in a master/display configuration.
Since both the S1D15710∗10∗∗ and S1D15710∗11∗∗ have built-in analog temperature sensor circuits, systems can be build that can maintain appropriate liquid crystal contrast over a wide temperature range with microcomputer control without requiring such parts as thermostats.
The S1D15710 Series can read and write RAM data with the minimum current consumption because it does not require any external operation clock. Also it incorporates a LCD power supply featuring a very low current consumption, a LCD drive power voltage regulator resistor and a display clock CR oscillator circuit. This allows the display system of a high-performance for handy equipment to be realized at the minimum power consumption and minimum component configuration.

2. FEATURES

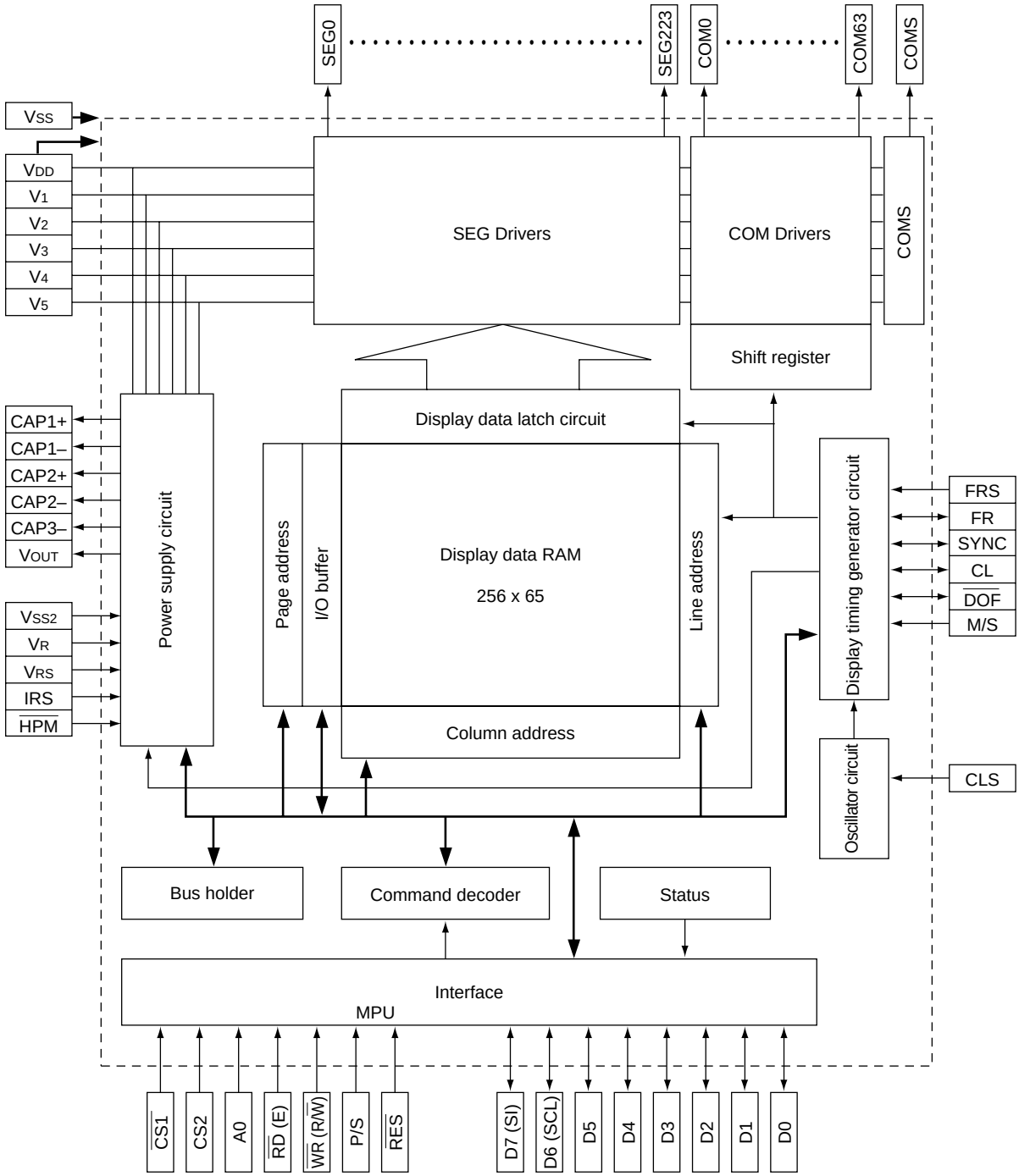
- Direct display of RAM data using the display data RAM
  RAM bit data "1" .... goes on.
  "0" .... goes off (at display normal rotation).
- RAM capacity
  65 × 256 = 16,640 bits
- Liquid crystal drive circuit
  65 circuits for the common output and 224 circuits for the segment output
- High-speed 8-bit MPU interface (Both the 80 and 68 series MUPs can directly be connected.)/serial interface enabled
- Abundant command functions
  Display Data Read/Write, Display ON/OFF, Display Normal Rotation/Reversal, Page Address Set, Display Start Line Set, column address set, Status Read, Power Supply Save Display All Lighting ON/OFF, LCD Bias Set, Read Modify Write, Segment Driver Direction Select, Electronic Control, V_5 Voltage Adjusting Built-in Resistance Ratio Set, Static Indicator, n Line Alternating Current Reversal Drive, Common Output State Selection, and Built-in Oscillator Circuit ON
- Built-in static drive circuit for indicators (One set, blinking speed variable)
- Built-in power supply circuit for low power supply liquid crystal drive
  Booster circuit (Boosting magnification - double, triple, quadruple, boosting reference power supply external input enabled)
- 3% high accuracy alternating current voltage adjusting circuit (Temperature gradient: –0.05%/°C)
  Built-in V_5 voltage adjusting resistor, built-in V_1 to V4 voltage generation split resistors, built-in electronic control function, and voltage follower
- Built-in CR oscillator circuit (external clock input enabled)
- Low power consumption
- Built-in temperature sensor circuit (S1D15710D10B∗ and S1D15710D11B∗)
- Power supplies
  Logic power supply: $V_{DD} – V_{SS}$ = 1.8 to 5.5 V
  Boosting reference power supply: $V_{DD} – V_{SS}$ = 1.8 to 6.0 V
  Liquid crystal drive power supply: $V_5 – V_{DD}$ = –4.5 to –18.0 V
- Wide operating temperature range –40 to 85°C
- CMOS process
- Shipping form Bare chip, TCP
- No light-resistant and radiation-resistant design are provided.

Series specification

Product name	Duty	Bias	SEG Dr	COM Dr	V_{REG} temperature gradient	Shipping form
S1D15710D00B∗	1/65	1/9, 1/7	224	65	–0.05%/°C	Bare chip
S1D15710D10B∗(*1)	1/65	1/9, 1/7	224	65	–0.05%/°C	Bare chip
S1D15710D11B∗(*2)	1/65	1/9, 1/7	224	65	–0.05%/°C	Bare chip
S1D15710T00∗∗	1/65	1/9, 1/7	224	65	–0.05%/°C	TCP

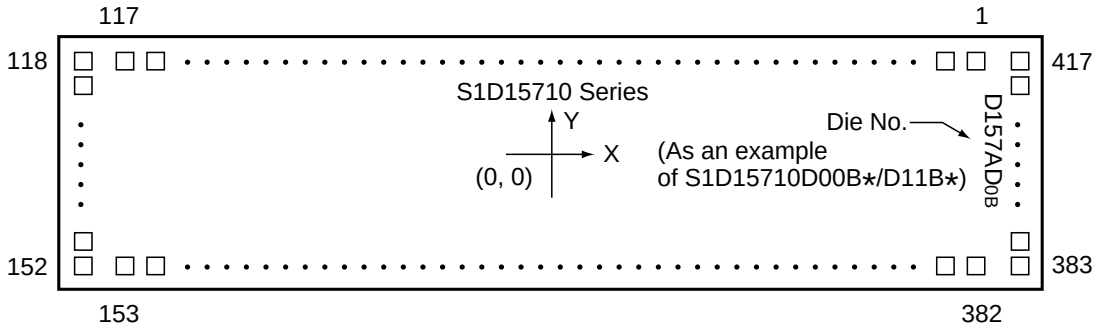
*1: The built-in power circuit has been upgraded so that liquid crystal displays having big load capacities can be driven. Check the display and select if the display quality is inadequate even in high power mode of S1D15710D00B∗. There are no methods for supplying liquid crystal drive power externally without using the built-in power circuit. In that case, select either the S1D15710D10B∗ or the S1D15710D11B∗.
*2: All specificationa are same as those of the S1D15710D11B∗ except for the temperature sensor circuit.

3. BLOCK DIAGRAM



4. PIN LAYOUT

Chip Specification



Item		Size X		Size Y	Unit
Chip size		16.65	×	2.90	mm
Chip thickness		0.625			mm
Bump pitch		69 (Min.)			μm
Bump size	PAD No.1 to 117	85	×	85	μm
	PAD No.118	85	×	73	μm
	PAD No.119 to 151	85	×	47	μm
	PAD No.152	85	×	73	μm
	PAD No.153	73	×	85	μm
	PAD No.154 to 381	47	×	85	μm
	PAD No.382	73	×	85	μm
	PAD No.383	86	×	73	μm
	PAD No.384 to 416	85	×	47	μm
	PAD No.417	85	×	73	μm
Bump height		17 (Typ.)			μm

PAD Central Coordinates

Unit: μm

PAD No.	PIN Name	X	Y
1	(NC)	7814	1293
2	SYNC	7677	
3	FRS	7541	
4	TEST1	7404	
5	V_{DD}	7268	
6	TEST2	7131	
7	V_{SS}	6995	
8	TEST3	6855	
9	V_{DD}	6718	
10	TEST4	6582	
11	V_{SS}	6445	
12	V_{SS}	6309	
13	V_{SS}	6169	
14	V_{DD}	6033	
15	V_{DD}	5896	
16	V_{DD}	5760	
17	V_{DD}	5623	
18	TEST5	5483	
19	TEST5	5347	
20	TEST6	5210	
21	TEST6	5074	
22	TEST7	4937	
23	TEST7	4798	
24	TEST8	4661	
25	TEST8	4525	
26	TEST9	4388	
27	TEST9	4252	
28	SYNC	4112	
29	FRS	3975	
30	FR	3839	
31	$\overline{CL}$	3702	
32	$\overline{DOF}$	3566	
33	$\overline{V_{SS}}$	3429	
34	$\overline{CS1}$	3293	
35	CS2	3156	
36	$\overline{V_{DD}}$	3020	
37	$\overline{RES}$	2883	
38	A0	2747	
39	V_{SS}	2610	
40	$\overline{WR}$, R/$\overline{W}$	2474	
41	$\overline{RD}$,E	2337	
42	V_{DD}	2201	
43	D0	2064	
44	D1	1928	
45	D2	1791	
46	D3	1655	
47	D4	1518	
48	D5	1382	
49	D6 (SCL)	1245	
50	D7 (SI)	1109	

PAD No.	PIN Name	X	Y
51	V_{DD}	972	1293
52	V_{DD}	838	
53	V_{DD}	704	
54	V_{DD}	571	
55	V_{DD}	437	
56	V_{SS}	303	
57	V_{SS}	169	
58	V_{SS}	35	
59	V_{SS2}	–99	
60	V_{SS2}	–233	
61	V_{SS2}	–367	
62	V_{SS2}	–501	
63	V_{SS2}	–635	
64	(NC)	–768	
65	V_{OUT}	–902	
66	V_{OUT}	–1036	
67	CAP3–	–1170	
68	CAP3–	–1304	
69	(NC)	–1438	
70	CAP1+	–1572	
71	CAP1+	–1706	
72	CAP1–	–1840	
73	CAP1–	–1974	
74	CAP2–	–2107	
75	CAP2–	–2241	
76	CAP2+	–2375	
77	CAP2+	–2509	
78	V_{SS}	–2643	
79	V_{SS}	–2777	
80	V_{RS}	–2911	
81	V_{RS}	–3045	
82	V_{DD}	–3179	
83	V_{DD}	–3313	
84	V_1	–3446	
85	V_1	–3580	
86	V_2	–3714	
87	V_2	–3848	
88	(NC)	–3982	
89	V_3	–4116	
90	V_3	–4250	
91	V_4	–4384	
92	V_4	–4518	
93	V_5	–4652	
94	V_5	–4785	
95	(NC)	–4919	
96	V_R	–5053	
97	V_{DD}	–5187	
98	TEST10	–5321	
99	V_{SS}	–5455	
100	TEST11	–5589	

PAD No.	PIN Name	X	Y
101	V_{DD}	–5723	1293
102	M/S	–5859	
103	CLS	–5996	
104	V_{SS}	–6132	
105	C86	–6269	
106	P/S	–6405	
107	$\overline{V_{DD}}$	–6542	
108	HPM	–6678	
109	V_{SS}	–6815	
110	IRS	–6951	
111	V_{DD}	–7088	
112	TEST12	–7224	
113	TEST13	–7361	
114	TEST14	–7510	
115	TEST15	–7630	
116	TEST16	–7750	
117	(NC)	–7869	
118	(NC)	–8148	1295
119	COM31		1209
120	COM30		1137
121	COM29		1064
122	COM28		991
123	COM27		919
124	COM26		846
125	COM25		773
126	COM24		701
127	COM23		628
128	COM22		555
129	COM21		483
130	COM20		410
131	COM19		337
132	COM18		265
133	COM17		192
134	COM16		119
135	COM15		47
136	COM14		–26
137	COM13		–99
138	COM12		–171
139	COM11		–244
140	COM10		–317
141	COM9		–389
142	COM8		–462
143	COM7		–535
144	COM6		–607
145	COM5		–680
146	COM4		–753
147	COM3		–825
148	COM2		–898
149	COM1		–971
150	COM0		–1043

Unit: μm

PAD No.	PIN Name	X	Y
151	COMS	–8148	–1116
152	(NC)	↓	–1201
153	(NC)	–7906	–1293
154	(NC)	–7823	↓
155	(NC)	–7754	
156	SEG0	–7685	
157	SEG1	–7616	
158	SEG2	–7547	
159	SEG3	–7478	
160	SEG4	–7409	
161	SEG5	–7340	
162	SEG6	–7271	
163	SEG7	–7202	
164	SEG8	–7133	
165	SEG9	–7064	
166	SEG10	–6995	
167	SEG11	–6926	
168	SEG12	–6857	
169	SEG13	–6788	
170	SEG14	–6719	
171	SEG15	–6650	
172	SEG16	–6581	
173	SEG17	–6512	
174	SEG18	–6442	
175	SEG19	–6373	
176	SEG20	–6304	
177	SEG21	–6235	
178	SEG22	–6166	
179	SEG23	–6097	
180	SEG24	–6028	
181	SEG25	–5959	
182	SEG26	–5890	
183	SEG27	–5821	
184	SEG28	–5752	
185	SEG29	–5683	
186	SEG30	–5614	
187	SEG31	–5545	
188	SEG32	–5476	
189	SEG33	–5407	
190	SEG34	–5338	
191	SEG35	–5269	
192	SEG36	–5200	
193	SEG37	–5131	
194	SEG38	–5062	
195	SEG39	–4993	
196	SEG40	–4924	
197	SEG41	–4855	
198	SEG42	–4786	
199	SEG43	–4717	
200	SEG44	–4648	↓

PAD No.	PIN Name	X	Y
201	SEG45	–4579	–1293
202	SEG46	–4510	↓
203	SEG47	–4441	
204	SEG48	–4372	
205	SEG49	–4303	
206	SEG50	–4234	
207	SEG51	–4164	
208	SEG52	–4095	
209	SEG53	–4026	
210	SEG54	–3957	
211	SEG55	–3888	
212	SEG56	–3819	
213	SEG57	–3750	
214	SEG58	–3681	
215	SEG59	–3612	
216	SEG60	–3543	
217	SEG61	–3474	
218	SEG62	–3405	
219	SEG63	–3336	
220	SEG64	–3267	
221	SEG65	–3198	
222	SEG66	–3129	
223	SEG67	–3060	
224	SEG68	–2991	
225	SEG69	–2922	
226	SEG70	–2853	
227	SEG71	–2784	
228	SEG72	–2715	
229	SEG73	–2646	
230	SEG74	–2577	
231	SEG75	–2508	
232	SEG76	–2439	
233	SEG77	–2370	
234	SEG78	–2301	
235	SEG79	–2232	
236	SEG80	–2163	
237	SEG81	–2094	
238	SEG82	–2025	
239	SEG83	–1956	
240	SEG84	–1886	
241	SEG85	–1817	
242	SEG86	–1748	
243	SEG87	–1679	
244	SEG88	–1610	
245	SEG89	–1541	
246	SEG90	–1472	
247	SEG91	–1403	
248	SEG92	–1334	
249	SEG93	–1265	
250	SEG94	–1196	↓

PAD No.	PIN Name	X	Y
251	SEG95	–1127	–1293
252	SEG96	–1058	↓
253	SEG97	–989	
254	SEG98	–920	
255	SEG99	–851	
256	SEG100	–782	
257	SEG101	–713	
258	SEG102	–644	
259	SEG103	–575	
260	SEG104	–506	
261	SEG105	–437	
262	SEG106	–368	
263	SEG107	–299	
264	SEG108	–230	
265	SEG109	–161	
266	SEG110	–92	
267	SEG111	–23	
268	SEG112	46	
269	SEG113	115	
270	SEG114	184	
271	SEG115	253	
272	SEG116	322	
273	SEG117	391	
274	SEG118	461	
275	SEG119	530	
276	SEG120	599	
277	SEG121	668	
278	SEG122	737	
279	SEG123	806	
280	SEG124	875	
281	SEG125	944	
282	SEG126	1013	
283	SEG127	1082	
284	SEG128	1151	
285	SEG129	1220	
286	SEG130	1289	
287	SEG131	1358	
288	SEG132	1427	
289	SEG133	1496	
290	SEG134	1565	
291	SEG135	1634	
292	SEG136	1703	
293	SEG137	1772	
294	SEG138	1841	
295	SEG139	1910	
296	SEG140	1979	
297	SEG141	2048	
298	SEG142	2117	
299	SEG143	2186	
300	SEG144	2255	↓

Unit: µm

PAD No.	PIN Name	X	Y
301	SEG145	2324	–1293
302	SEG146	2393	
303	SEG147	2462	
304	SEG148	2531	
305	SEG149	2600	
306	SEG150	2669	
307	SEG151	2739	
308	SEG152	2808	
309	SEG153	2877	
310	SEG154	2946	
311	SEG155	3015	
312	SEG156	3084	
313	SEG157	3153	
314	SEG158	3222	
315	SEG159	3291	
316	SEG160	3360	
317	SEG161	3429	
318	SEG162	3498	
319	SEG163	3567	
320	SEG164	3636	
321	SEG165	3705	
322	SEG166	3774	
323	SEG167	3843	
324	SEG168	3912	
325	SEG169	3981	
326	SEG170	4050	
327	SEG171	4119	
328	SEG172	4188	
329	SEG173	4257	
330	SEG174	4326	
331	SEG175	4395	
332	SEG176	4464	
333	SEG177	4533	
334	SEG178	4602	
335	SEG179	4671	
336	SEG180	4740	
337	SEG181	4809	
338	SEG182	4878	
339	SEG183	4947	
340	SEG184	5017	
341	SEG185	5086	
342	SEG186	5155	
343	SEG187	5224	
344	SEG188	5293	
345	SEG189	5362	
346	SEG190	5431	
347	SEG191	5500	
348	SEG192	5569	
349	SEG193	5638	
350	SEG194	5707	

PAD No.	PIN Name	X	Y
351	SEG195	5776	–1293
352	SEG196	5845	
353	SEG197	5914	
354	SEG198	5983	
355	SEG199	6052	
356	SEG200	6121	
357	SEG201	6190	
358	SEG202	6259	
359	SEG203	6328	
360	SEG204	6397	
361	SEG205	6466	
362	SEG206	6535	
363	SEG207	6604	
364	SEG208	6673	
365	SEG209	6742	
366	SEG210	6811	
367	SEG211	6880	
368	SEG212	6949	
369	SEG213	7018	
370	SEG214	7087	
371	SEG215	7156	
372	SEG216	7225	
373	SEG217	7294	
374	SEG218	7364	
375	SEG219	7433	
376	SEG220	7502	
377	SEG221	7571	
378	SEG222	7640	
379	SEG223	7709	
380	(NC)	7778	
381	(NC)	7847	
382	(NC)	7930	
383	(NC)	8148	–1201
384	COM32		–1116
385	COM33		–1043
386	COM34		–971
387	COM35		–898
388	COM36		–825
389	COM37		–753
390	COM38		–680
391	COM39		–607
392	COM40		–535
393	COM41		–462
394	COM42		–389
395	COM43		–317
396	COM44		–244
397	COM45		–171
398	COM46		–99
399	COM47		–26
400	COM48		47

PAD No.	PIN Name	X	Y
401	COM49	8148	119
402	COM50		192
403	COM51		265
404	COM52		337
405	COM53		410
406	COM54		483
407	COM55		555
408	COM56		628
409	COM57		701
410	COM58		773
411	COM59		846
412	COM60		919
413	COM61		991
414	COM62		1064
415	COM63		1137
416	COMS		1209
417	(NC)		1295

5. PIN DESCRIPTION

Power Supply Pin

Pin name	I/O	Description	Number of pins
V_{DD}	Power supply	Commonly used with the MPU power supply pin V_{CC}.	12
V_{SS}	Power supply	0 V pin connected to the system ground (GND)	9
V_{SS2}	Power supply	Boosting circuit reference power supply for liquid crystal drive	5
V_{RS}	Power supply	External input pin for liquid crystal power supply voltage adjusting circuit They are set to OPEN	2
V_1, V_2 V_3, V_4 V_5	Power supply	Multi-level power supply for liquid crystal drive. The voltage specified according to liquid crystal cells is impedance-converted by a split resistor or operation amplifier (OP amp) and applied. The potential needs to be specified based on V_{DD} to establish the relationship of dimensions shown below: V_{DD} (=V_0) ≥ V_1 ≥ V_2 ≥ V_3 ≥ V_4 ≥ V_5 Master operation When the power supply is ON, the following voltages are applied to V_1 ~ V_4 from the built-in power supply circuit. The selection of the voltages is determined using the LCD bias set command. V_1 1/9•V_5 1/7•V_5 V_2 2/9•V_5 2/7•V_5 V_3 7/9•V_5 5/7•V_5 V_4 8/9•V_5 6/7•V_5	10

LCD Power Supply Circuit Pin

Pin name	I/O	Description	Number of pins
CAP1+	O	Boosting capacitor positive side connecting pin. Connects a capacitor between the pin and CAP1– pin.	2
CAP1–	O	Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP1+ pin.	2
CAP2+	O	Boosting capacitor positive side connecting pin. Connects a capacitor between the pin and CAP2– pin.	2
CAP2–	O	Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP2+ pin.	2
CAP3–	O	Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP1+ pin.	2
V_{OUT}	I/O	Boosting output pin. Connects a capacitor between the pin and V_{SS2}.	2
V_R	I	Voltage adjusting pin. Applies voltage between V_{DD} and V_5 using a split resistor. Valid only when the V_5 voltage adjusting built-in resistor is not used (IRS=LOW) Do not use VR when the V_5 voltage adjusting built-in resistor is used (IRS=HIGH)	1

System Bus Connecting Pins

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>D7 to D0
(SI)
(SCL)</td><td>I/O</td><td>An 8-bit bidirectional data bus is used to connect an 8-bit or 16-bit standard MPU data bus.
When the serial interface is selected (P/S=LOW),
D7: Serial data entry pin (SI)
D6: Serial clock input pin (SCL)
In this case, D0 to D5 are set to high impedance.
When Chip Select is in the non-active state, D0 to D7 are set to high impedance.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Normally the lowest order bit of the MPU address bus is connected to discriminate data / commands.
A0=HIGH: Indicates that D0 to D7 are display data.
A0=LOW: Indicates that D0 to D7 are control data.</td><td>1</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>Initialized by setting $\overline{RES}$ to LOW.
Reset operation is performed at the $\overline{RES}$ signal level.</td><td>1</td></tr>
<tr><td>$\overline{CS1}$
CS2</td><td>I</td><td>Chip Select signal. When $\overline{CS1}$=LOW and CS2=HIGH, this signal becomes active and the input/output of data/commands is enabled.</td><td>2</td></tr>
<tr><td>$\overline{RD}$
(E)</td><td>I</td><td>• When the 80 series MPU is connected, active LOW is set.
Pin that connects the $\overline{RD}$ signal of the 80 series MPU. When this signal is LOW, the S1D15710 series data bus is set in the output state.
• When the 68 series MPU is connected, active HIGH is set.
68 series MPU enable clock input pin</td><td>1</td></tr>
<tr><td>$\overline{WR}$
(R/$\overline{W}$)</td><td>I</td><td>• When the 80 series MPU is connected, active LOW is set.
Pin that connects the $\overline{WR}$ signal of the 80 series MPU. The data bus signal is latched on the leading edge of the $\overline{WR}$ signal.
• When the 68 series MPU is connected,
Read/write control signal input pin
R/$\overline{W}$=HIGH: Read operation
R/$\overline{W}$=LOW: Write operation</td><td>1</td></tr>
<tr><td>FRS</td><td>O</td><td>Output pin for static drive
Used together with the SYNC pin</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>MPU interface switching pin
C86=HIGH: 68 series MPU interface
C86=LOW: 80 series MPU interface</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>Switching pin for parallel data entry/serial data entry
P/S=HIGH: Parallel data entry
P/S=LOW: Serial data entry
According to the P/S state, the following table is given.
<table>
<tr><th>P/S</th><th>Data/ command</th><th>Data</th><th>Read/write</th><th>Serial clock</th></tr>
<tr><td>HIGH</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$, $\overline{WR}$</td><td></td></tr>
<tr><td>LOW</td><td>A0</td><td>SI (D7)</td><td>Write-only</td><td>SCL (D6)</td></tr>
</table>
When P/S=LOW, D0 to D5 are set to high impedance. D0 to D5 can be HIGH, LOW, or “OPEN”.
$\overline{RD}$(E) and $\overline{WR}$ (R/$\overline{W}$) are fixed to HIGH or LOW.
For the serial data entry, RAM display data cannot be read.</td><td>1</td></tr>
</table>

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>CLS</td><td>I</td><td>Pin that selects the validity/invalidity of the built-in oscillator circuit for display clocks.
CLS=HIGH: Built-in oscillator circuit valid
CLS=LOW: Built-in oscillator circuit invalid (external input)
When CLS=LOW, display clocks are input from the CL pin.
When the S1D15710 series is used for the master/slave configuration, each of the CLS pins is set to the same level together.
<table>
<tr><th>Display clock</th><th>Master</th><th>Slave</th></tr>
<tr><td>Built-in oscillator circuit used
External input</td><td>HIGH
LOW</td><td>HIGH
LOW</td></tr>
</table></td><td>1</td></tr>
<tr><td>M/S</td><td>I</td><td>Pin that selects the master/slave operation for the S1D15710 series. The liquid crystal display system is synchronized by outputting the timing signal required for the liquid crystal display for the master operation and inputting the timing signal required for the liquid crystal display for the slave operation.
M/S=HIGH: Master operation
M/S=LOW: Slave operation
According to the M/S and CLS states, the following table is given.
<table>
<tr><th>M/S</th><th>CLS</th><th>Oscillator circuit</th><th>Power supply circuit</th><th>CL</th><th>FR</th><th>SYNC</th><th>FRS</th><th>DOF</th></tr>
<tr><td>HIGH</td><td>HIGH</td><td>Valid</td><td>Valid</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td></td><td>LOW</td><td>Invalid</td><td>Valid</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>Invalid</td><td>Invalid</td><td>Input</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
<tr><td></td><td>LOW</td><td>Invalid</td><td>Invalid</td><td>Input</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock I/O pin
According to the M/S and CLS states, the following table is given.
<table>
<tr><th>M/S</th><th>CLS</th><th>CL</th></tr>
<tr><td>HIGH</td><td>HIGH</td><td>Output</td></tr>
<tr><td></td><td>LOW</td><td>Input</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>Input</td></tr>
<tr><td></td><td>LOW</td><td>Input</td></tr>
</table>
When the S1D15710 series is used for the master/slave configuration, each CL pin is connected.</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>Liquid crystal alternating current signal I/O pin
M/S=HIGH: Output
M/S=LOW: Input
When the S1D15710 series is used for the master/slave configuration, each FR pin is connected.</td><td>1</td></tr>
<tr><td>SYNC</td><td>I/O</td><td>Liquid crystal synchronizing current signal I/O pin
M/S=HIGH: Output
M/S=LOW: Input
When the S1D15710 series is used for the master/slave configuration, each SYNC pin is connected.</td><td>2</td></tr>
<tr><td>$\overline{\text{DOF}}$</td><td>I/O</td><td>Liquid crystal display blanking control pin
M/S=HIGH: Output
M/S=LOW: Input
When the S1D15710 series is used for the master/slave configuration, each DOF pin is connected.</td><td>1</td></tr>
<tr><td>IRS</td><td>I</td><td>V_5 voltage adjusting resistor selection pin
IRS=HIGH: Built-in resistor used
IRS=LOW: Built-in resistor not used. The V_5 voltage is adjusted by the V_R pin and stand-alone split resistor.
Valid only at master operation. The pin is fixed to HIGH or LOW at slave operation.</td><td>1</td></tr>
<tr><td>$\overline{\text{HPM}}$</td><td>I</td><td>Power supply control pin of the power supply circuit for liquid crystal drive
$\overline{\text{HPM}}$=HIGH: Normal mode
HPM=LOW: High power supply mode
Valid only at master operation. The pin is fixed to HIGH or LOW at slave operation.</td><td>1</td></tr>
</table>

Liquid Crystal Drive Pin

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>SEG0
to
SEG223</td><td>O</td><td>Output pins for the LCD segment drive. Contents of the display RAM and FR signal are combined to select a desired level among V_{DD}, V_2, V_3 and V_5.
<table>
<tr><th rowspan="2">RAM data</th><th rowspan="2">FR</th><th colspan="2">Output voltage</th></tr>
<tr><th>Display normal operation</th><th>Display reversal</th></tr>
<tr><td>HIGH</td><td>HIGH</td><td>V_{DD}</td><td>V_2</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>V_5</td><td>V_3</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td>LOW</td><td>LOW</td><td>V_3</td><td>V_5</td></tr>
<tr><td>Power save</td><td>—</td><td colspan="2">V_{DD}</td></tr>
</table></td><td>224</td></tr>
<tr><td>COM0
to
COM63</td><td></td><td>Output pins for the LCD common drive. Scan data and FR signal are combined to select a desired level among V_{DD}, V_1, V_4 and V_5.
<table>
<tr><th>Scanning data</th><th>FR</th><th>Output voltage</th></tr>
<tr><td>HIGH</td><td>HIGH</td><td>V_5</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>V_{DD}</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>V_1</td></tr>
<tr><td>LOW</td><td>LOW</td><td>V_4</td></tr>
<tr><td>Power save</td><td>—</td><td>V_{DD}</td></tr>
</table></td><td>64</td></tr>
<tr><td>COMS</td><td>O</td><td>Indicator dedicated COM output pin
Set to OPEN when not used
When COMS is used for the master/slave configuration, the same signal is output to both the master and slave.</td><td>2</td></tr>
</table>

Test Pin

Pin name	I/O	Description	Number of pins
TEST1 ~ 4	I/O	Fix the pin to HIGH. To use a built-in temperature sensor circuit in the S1D15710⋆00⋆⋆/S1D15710⋆11⋆⋆, see 16, Temperature Sensor Circuit.	4
TEST10	I	Fix it to HIGH for the S1D15710⋆00⋆⋆/S1D15710⋆11⋆⋆; fix it to LOW for S1D15710⋆10⋆⋆.	1
TEST11~13	I/O	IC chip test pin. Fix the pin to HIGH.	3
TEST5 ~ 9, 14 ~ 16	I/O	IC chip test pin. Take into consideration so that the capacity of lines cannot be exhausted by setting the pin to OPEN.	13

6. FUNCTION DESCRIPTION

MPU Interface

Selection of interface type

The S1D15710 series transfers data through 8-bit bidirectional data buses (D7 to D0) or serial data input (SI). By setting the polarity of the P/S pin to either HIGH or LOW, the 8-bit parallel data entry or serial data entry can be selected as listed in Table 1.

Table 1

P/S	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
HIGH: Parallel data entry	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
LOW: Serial data entry	$\overline{CS1}$	CS2	A0	—	—	—	SI	SCL	(HZ)

Fix — to HIGH or LOW . HZ indicates the high impedance state.

Parallel interface

When the parallel interface is selected (P/S=HIGH), the S1D15705 series can directly be connected to the MPU bus of either the 80 or 68 series MPU by setting the C86 pin to HIGH or LOW as listed in Table 2.

Table 2

C86	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0
HIGH: 68 series MPU bus	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D7 to D0
LOW: 80 series MPU bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0

In addition, the data bus signal can be identified according to the combinations of the A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$) signals as listed in Table 3.

Table 3

Common	68 series	80 series		
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	Function
1	1	0	1	Display data read
1	0	1	0	Display data write
0	1	0	1	Status read
0	0	1	0	Control data write (command)

Serial interface

When the serial interface is selected (P/S=LOW), the serial data entry (SI) and serial clock input(SCL) can be accepted with the chip in the non-active state ($\overline{CS1}$=LOW or CS2=HIGH. The serial interface consists of an 8-bit shift register and a 3-bit counter. Serial data is fetched from the serial data entry pin in the order of D7, D6, ..., and D0 on the leading edge of the serial clock and converted into 8-bit parallel data on the leading edge of the 8th serial clock, then processed.
Whether to identify that the serial data entry is display data or command is judged by the A0 input, and A0=HIGH indicates display data and A0=LOW indicates the command. After the chip is set to the non-active state, the A0 input is read and identified at the timing on the 8 × n-th leading edge of the serial clock. Figure 1 shows the signal chart of the serial interface.

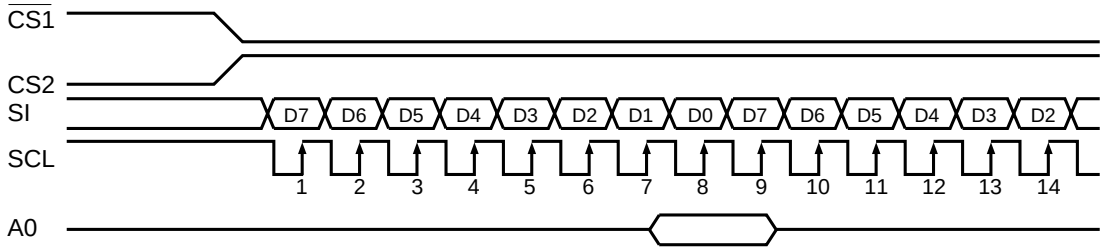


Figure 1

- When the chip is in the non-active state, both the shift register and counter are reset to the initial state.
- Cannot be read for the serial interface.
- For the SCL signal, pay careful attention to the terminating reflection of lines and external noise. The operation confirmation using actual equipment is recommended.

Chip select

The S1D15710 series has two chip select pins $\overline{CS1}$ and CS2 and enables the MPU interface or serial interface only when $\overline{CS1}$=LOW and CS2=HIGH.
When Chip Select is in the non-active state, D0 to D7 are in the high impedance state and the A0, $\overline{RD}$, and $\overline{WR}$ inputs become invalid. When the serial interface is selected, the shift register and counter are reset.

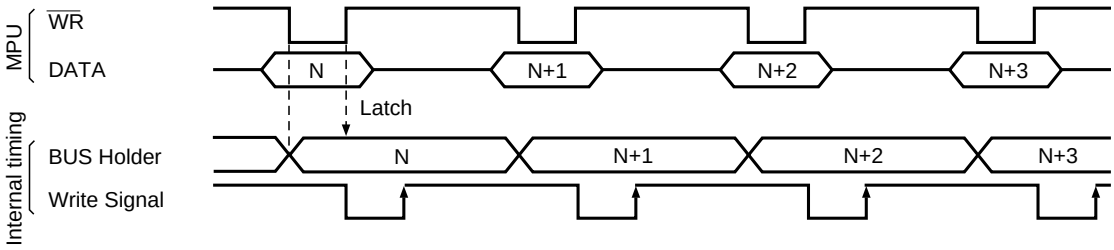
Display data RAM and internal register access

Since the S1D15710 series access viewed from the MUP side satisfies the cycle time and does not require the wait time, high-speed data transfer is enabled.
The S1D15710 series performs a kind of inter-LSI pipeline processing through the bus holder attached to the internal data bus when it performs the data transfer with the MPU.
For example, when data is written on the display data RAM, the data is first held in the bus holder and written on the display data RAM up to the next data write cycle. Further, when the MPU reads the contents of display data RAM, the read data at the first data read cycle (dummy) is held in the bus holder and read on the system bus from the bus holder up to the next data read cycle. The read sequence of the display data RAM is restricted. When the address is set, note that the specified address data is not output to the subsequent read instruction and output at the second data read. Therefore single dummy read is required after the address set and write cycle. Figure 2 shows this relationship.

Busy flag

When the busy flag is “1”, it indicates that the S1D15710 series is performing an internal operation, and only the status read instruction can be accepted. The busy flag is output to the D7 pin using the status read command. If the cycle time (t_{CYC}) is ensured, the MPU throughput can be improved greatly since this flag needs not be checked before each command.

• Write



• Read

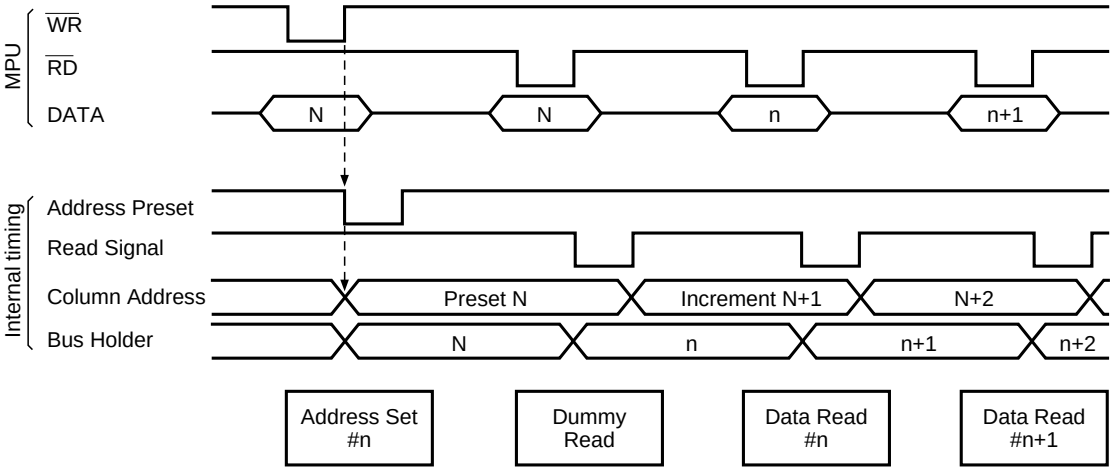


Figure 2

Display Data RAM

Display data RAM

This display data RAM stores display dot data and consists of 65 (8 pages × one 8 bit + 1) × 256 bits. Desired bits can be accessed by specifying page and column addresses.
Since the MPU display data D7 to D0 correspond to the common direction of the liquid crystal display, the restrictions at display data transfer is reduced and the display configuration with the high degree of freedom can easily be obtained when the S1D15710 series is used for the multiple chip configuration.
Besides, the read/write operation to the display data RAM is performed through the I/O buffer from the MPU side independently of the liquid crystal drive signal read. Therefore even when the display data RAM is asynchronously accessed during liquid crystal display, the access will not have any adverse effect on the display such as flickering.

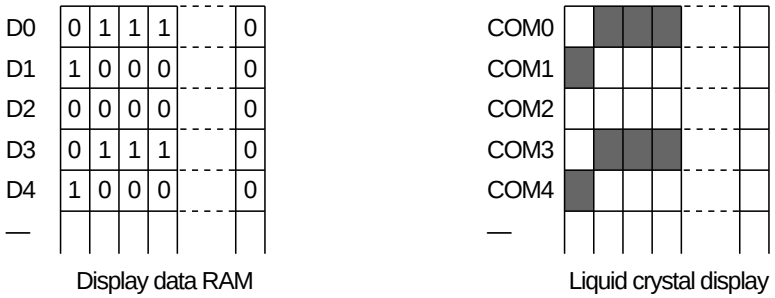


Figure 3

Page address circuit

As shown in Figure 4, the page address of the display data RAM is specified using the page address set command. To access the data using a new page, the page address is respecified.
The page address 8 (D3,D2,D1,D0=1,0,0,0) is an indicator dedicated RAM area and only the display data D0 is valid.

Column address circuit

As shown in Figure 4, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented by +1 at every input of display data read/write command. This allows the MPU to access the display data continuously.
Incrementation of the column address is stopped by FFH. When display data is accessed continuously, the column address continues to specify the FFH after access of the FFH. It should be noted that the column address FFH display data is accessed repeatedly. The column address and page address are independent of each other. Therefore, when shifting from the column of page 0 to the column of page 1, for example, it is necessary to specify each of the page address and column address again.

Furthermore, as shown in Table 4, the AD command (segment driver direction select command) can used to reverse the correspondence between the display data RAM column address and segment output. This allows constraints on IC layout to be minimized at the time of LCD module assembling.

Table 4

SEG output		SEG0 → SEG223
ADC	"0"	0 (H)→ Column Address→ DF (H)
(D0)	"1"	FF (H)←Column Address← 20 (H)

Line address circuit

When displaying contents of the display data RAM, the line address circuit is used for specifying the corresponding addresses. See Figure 4. Using the display start line address set command, the top line is normally selected (when the common output state is normal, COM0 is output. And, when reversed outputs COM63). For the display area of 65 lines is secured starting from the specified display start line address in the address incrementing direction.
Dynamically changing the line address using the display start line address set command enables screen scrolling and page change.

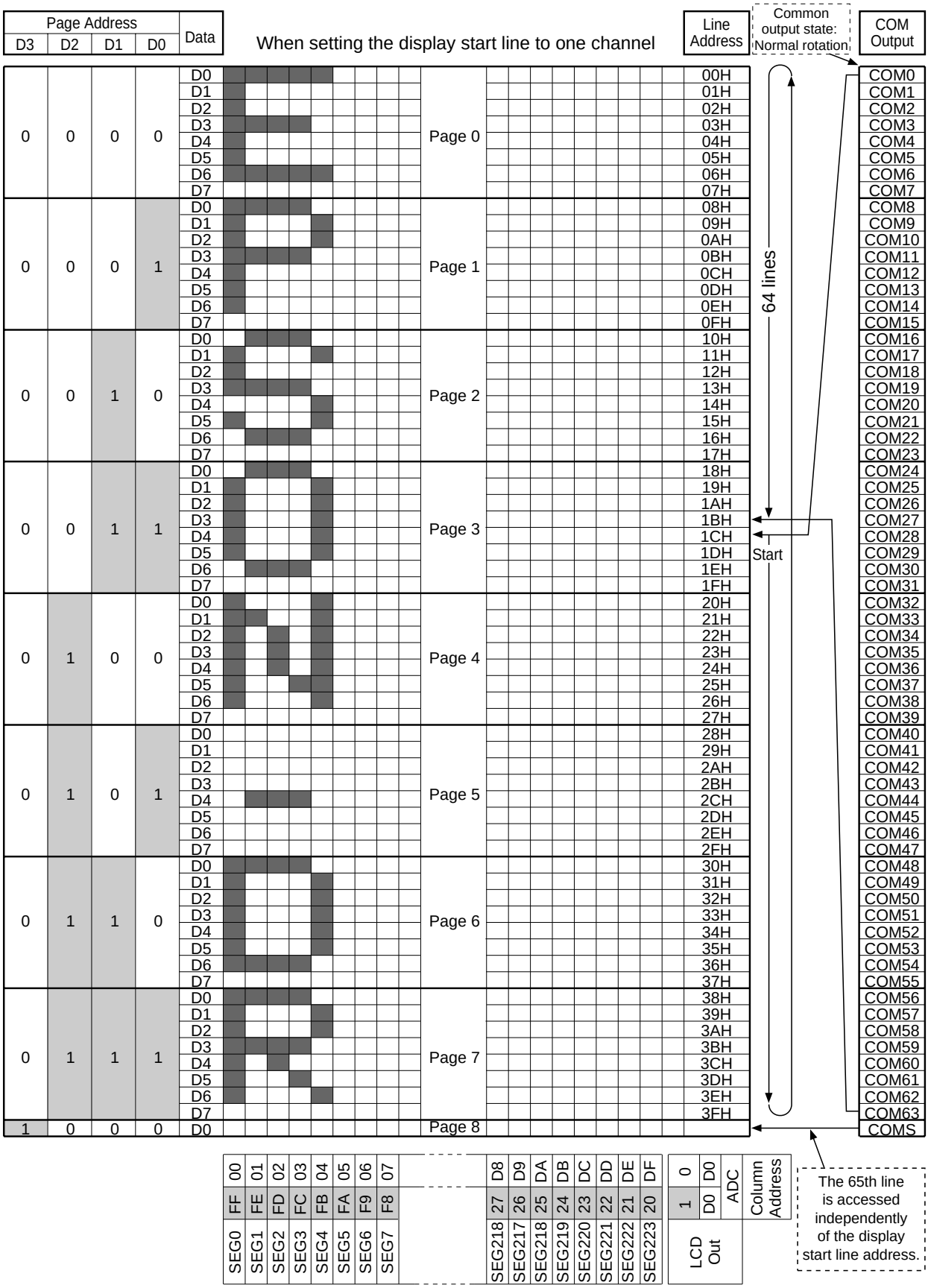

Page Address
D3 D2 D1 D0
Data
When setting the display start line to one channel
Line Address
Common output state: Normal rotation
COM Output
Page 0
Page 1
Page 2
Page 3
Page 4
Page 5
Page 6
Page 7
Page 8
64 lines
Start
COM0 COM1 COM2 COM3 COM4 COM5 COM6 COM7
COM8 COM9 COM10 COM11 COM12 COM13 COM14 COM15
COM16 COM17 COM18 COM19 COM20 COM21 COM22 COM23
COM24 COM25 COM26 COM27 COM28 COM29 COM30 COM31
COM32 COM33 COM34 COM35 COM36 COM37 COM38 COM39
COM40 COM41 COM42 COM43 COM44 COM45 COM46 COM47
COM48 COM49 COM50 COM51 COM52 COM53 COM54 COM55
COM56 COM57 COM58 COM59 COM60 COM61 COM62 COM63
COMS
00 01 02 03 04 05 06 07
FF FE FD FC FB FA F9 F8
SEG0 SEG1 SEG2 SEG3 SEG4 SEG5 SEG6 SEG7
D8 D9 DA DB DC DD DE DF
27 26 25 24 23 22 21 20
SEG218 SEG217 SEG218 SEG219 SEG220 SEG221 SEG222 SEG223
0 D0 ADC
1 D0 ADC
Column Address
LCD Out
The 65th line is accessed independently of the display start line address.

Figure 4

Display data latch circuit

The display data latch circuit is a latch that temporarily stores the display data output from the display data RAM to the liquid crystal drive circuit.
Since the Display Normal Rotation/Reversal, Display ON/OFF, and Display All Lighting ON/OFF commands control the data in this latch, the data within the display data RAM is not changed.

Oscillator Circuit

This oscillator circuit is a CR type oscillator and generates display clocks. The oscillator circuit is valid only when M/S=HIGH and CLS=HIGH and starts oscillation after the Built-in Oscillator Circuit ON command is entered. When CLS=LOW, the oscillation is stopped and the display clocks are entered from the CL pin.

Display Timing Generator Circuit

This display timing generator circuit generates timing signals from the display clocks to the line address circuit and the display latch circuit. It latches the display data to the display data latch circuit and outputs it to the segment drive output pin by synchronizing to the display clocks. The read operation of display data to the liquid crystal drive circuit is completely independent of the access to the display data RAM from the MPU. Therefore even when the display data RAM is asynchronously accessed during liquid crystal display, the access will not have any adverse effect on the display such as flickering.
The circuit also generates the internal common timing, liquid crystal alternating current signal (FR), and synchronous signal (SYNC) from the display clocks.
As shown in Figure 5, the FR normally generates the drive waveforms in the 2-frame alternating current drive system to the liquid crystal drive circuit. It can generate n-line reversal alternating current drive waveforms by setting data (n-1) to the n-line reversal drive register. If a display quality problem such as crosstalk occurs, it can be improved by using the n-line reversal alternating current drive waveforms. Determine the number of lines (n) to which alternating current is applied by actually displaying the liquid crystal.
SNYC is a signal that synchronizes the line counter and common timing generator circuit to the SYNC signal output side IC. Therefore the SYNC signal becomes a waveform at a duty ratio of 50% that synchronizes to the frame synchronization.
When the S1D15710 series is used for the multiple chip configuration, the slave side needs to supply the display timing signals (FR, SYNC, CL, and $\overline{DOF}$) from the master side.
Table 5 shows the state of FR, SYNC, CL, or $\overline{DOF}$.

Table 5

Operation mode		FR	SYNC	CL	$\overline{DOF}$
Master	Built-in oscillator circuit valid (CLS=HIGH)	Output	Output	Output	Output
(M/S=HIGH)	Built-in oscillator circuit invalid (CLS=LOW)	Output	Output	Input	Output
Slave	Built-in oscillator circuit valid (CLS=HIGH)	Input	Input	Input	Input
(M/S=LOW)	Built-in oscillator circuit invalid (CLS=LOW)	Input	Input	Input	Input

2-frame alternating current drive waveforms

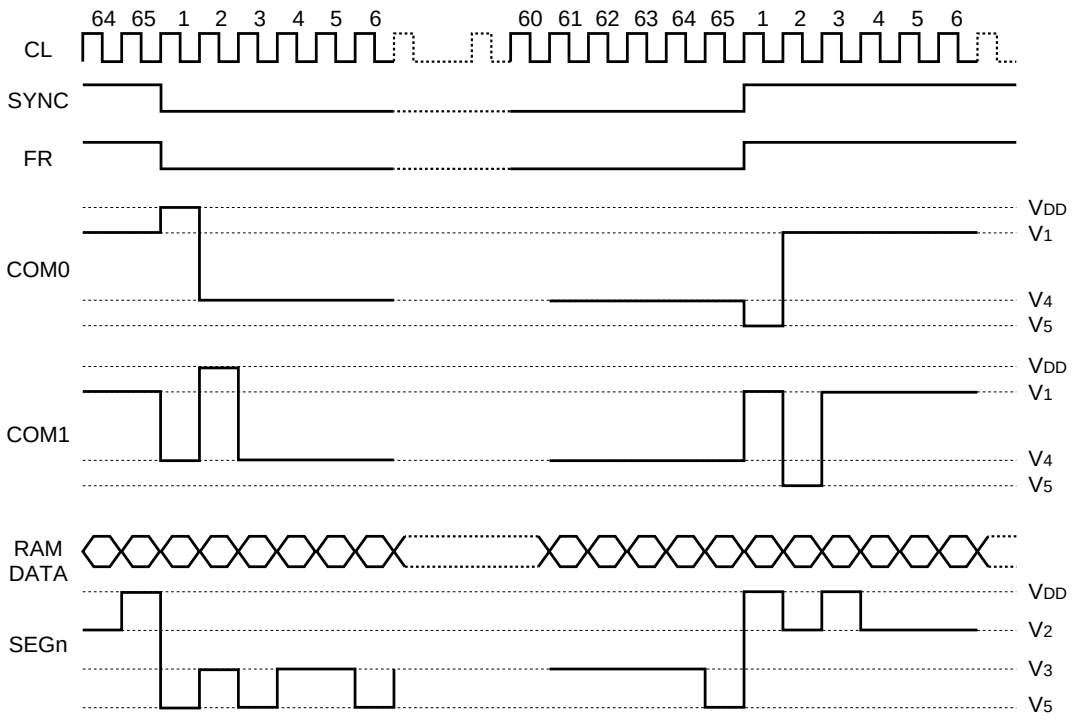


Figure 5

n-line reversal alternating current drive waveforms (Example of n=5: when the line reversal register is set to 4)

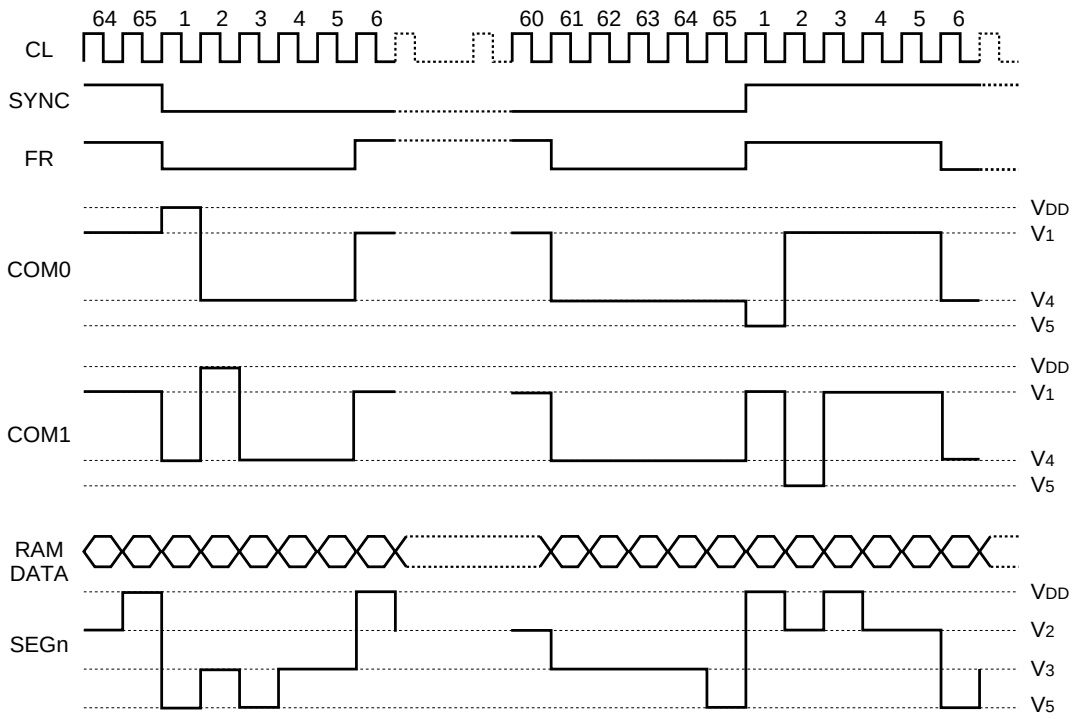


Figure 6

Common Output State Selection Circuit

The S1D15710 series can set the scanning direction of the COM output using the common output state selection command (see Figure 6). Therefore the IC assignment restrictions at LCD module assembly are reduced.

Table 6

State	COM scanning direction
Normal rotation	COM 0 → COM 63
Reversal	COM 63 → COM 0

Liquid Crystal Drive Circuit

This liquid crystal drive circuit is 289 sets of mutiplexers that generate quadruple levels for liquid crystal drive. It outputs the liquid crystal drive voltage that corresponds to the combinations of the display data, COM scanning signal, and FR signal.
Figure 6 shows examples of the SEG and COM output waveforms.

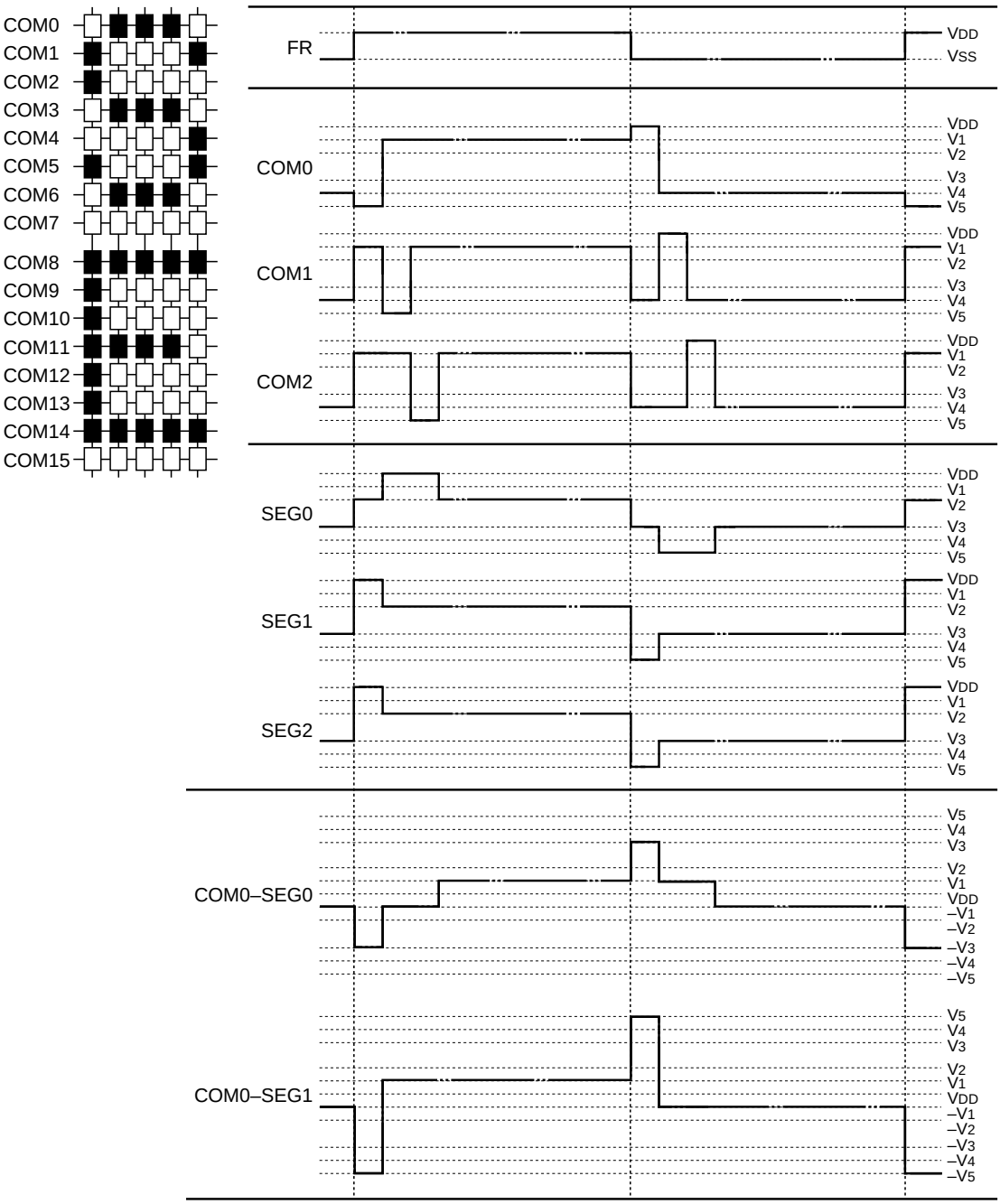

COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15
FR
VDD
VSS
COM0
COM1
COM2
SEG0
SEG1
SEG2
V1
V2
V3
V4
V5
COM0–SEG0
COM0–SEG1
–V1
–V2
–V3
–V4
–V5

Figure 7

Power Supply Circuit

This power supply circuit is a low power supply consumption one that generates the voltage required for the liquid crystal drive and consists of a boosting circuit, voltage adjusting circuit, and voltage follower circuit. It is valid only at master operation.
The power supply circuit ON/OFF controls the boosting circuit, voltage adjusting circuit, and voltage follower circuit using the power supply control set command, respectively.
Therefore, it can also use the partial functions of the external power supply and built-in power supply together. Table 7 lists the functions that control 3-bit data using the power control set command and Table 8 lists the reference combinations.

Table 7 Description of controlling bits using the power control set command

Item		State "1"	State "0"
D2	Boosting circuit control bit	ON	OFF
D1	Voltage adjusting circuit (V adjusting circuit) control bit	ON	OFF
D0	Voltage follower circuit (V/F circuit) control bit	ON	OFF

Table 8 Reference combinations

Status of use	D2	D1	D0	Boosting circuit	V adjusting circuit	V/F circuit	External voltage input	Boosting system pin
① Built-in power supply used	1	1	1	O	O	O	V_{SS2}	Used
② V adjusting circuit and V/F circuit only	0	1	1	X	O	O	V_{OUT}, V_{SS2}	OPEN
③ V/F circuit only	0	0	1	X	X	O	V_5, V_{SS2}	OPEN
④ External power supply only	0	0	0	X	X	X	V_1 to V_5	OPEN

- The boosting system pin indicates the CAP1+, CAP1–, CAP2+, CAP2–, or CAP3– pin.
- Although the combinations other than those listed in the above table are also possible, they cannot be recommended because they are not actual use methods.

Boosting circuit

The boosting circuit incorporated in the S1D15710 series enables the quadruple boosting, triple boosting, and double boosting of the V_{DD} – V_{SS2} potential.
For the quadruple boosting, the $V_{DD} \leftrightarrow V_{SS2}$ potential is quadruple-boosted to the negative side and output to the V_{OUT} pin by connecting the capacitor C1 between CAP1+↔and CAP1–, between CAP2+↔ and CAP2–, between CAP1+↔ and CAP3–, and between V_{SS2}↔ and V_{OUT}.
For the triple boosting, the $V_{DD} \leftrightarrow V_{SS2}$ potential is triple-boosted to the negative side and output to the V_{OUT} pin by connecting the capacitor C1 between CAP1+↔ and CAP1–, between CAP2+↔ and CAP2–, and between V_{SS2}↔ and V_{OUT} and strapping both CAP3– and V_{OUT} pins.
For the double boosting, the $V_{DD} \leftrightarrow V_{SS2}$ potential is doubly boosted to the negative side and output to the V_{OUT} pin by connecting the capacitor C1 between CAP1+↔ and CAP1–, and between V_{SS2}↔, setting CAP2+ to OPEN, and V_{OUT} and strapping CAP2–, CAP3–, and V_{OUT} pins.
Figure 8 shows the relationships of boosting potential.

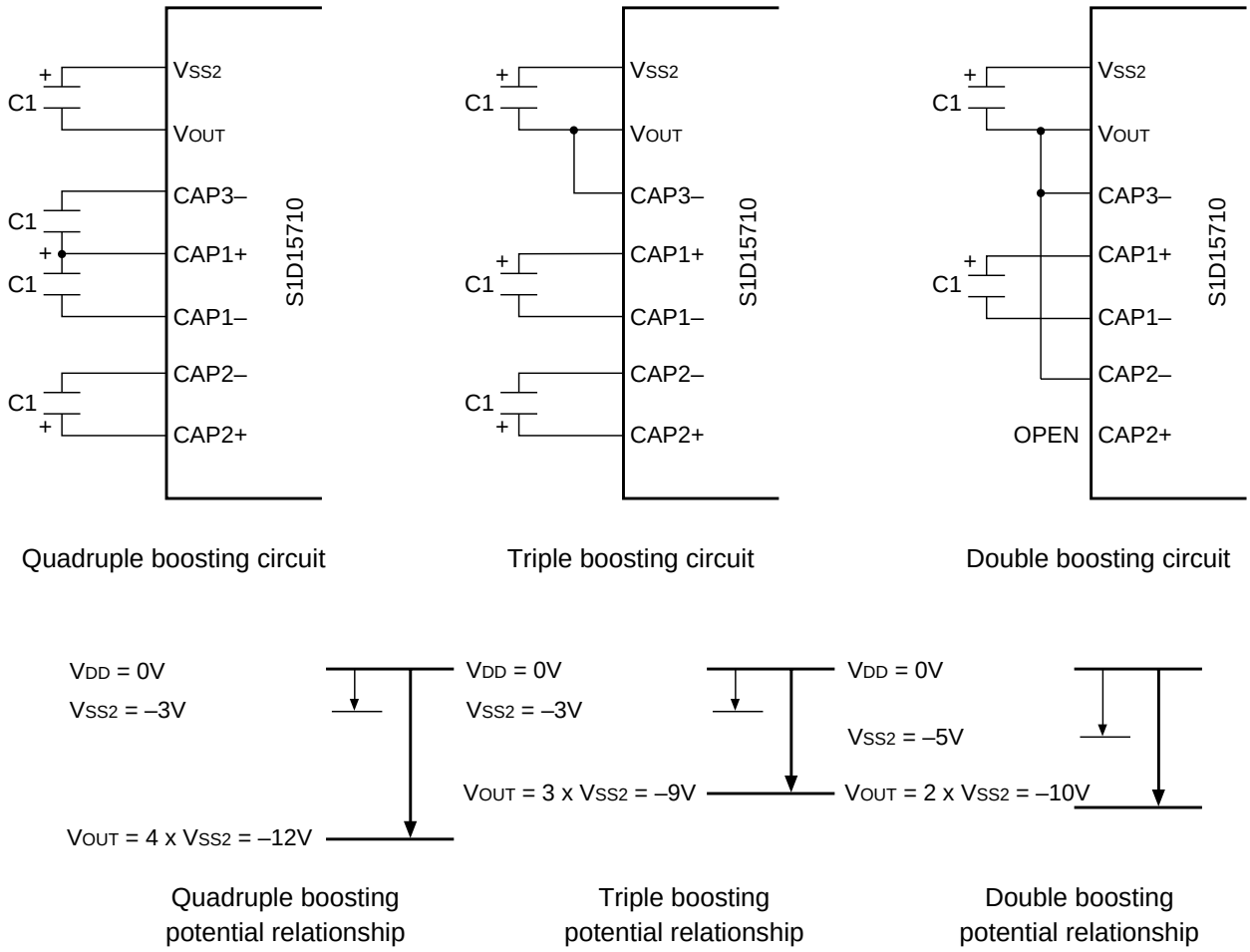


Figure 8

- Set the VSS2" voltage range so that the voltage of the VOUT pin cannot exceed the absolute maximum ratings.

Voltage adjusting circuit

The boosting voltage generated in VOUT outputs the liquid crystal drive voltage V5 through the voltage adjusting circuit.
Since the S1D15710 series incorporates a high-accuracy constant power supply, 64-step electronic control function, and V5 voltage adjusting resistor, a high-accuracy voltage adjusting circuit can eliminate and save parts.

(A) When using the V5 voltage adjusting built-in resistor
The liquid crystal power supply voltage V5 can be controlled only using the command without an external resistor and the light and shade of liquid crystal display be adjusted by using the V5 voltage adjusting built-in resistor and the electronic control function.
The V5 voltage can be obtained according to Expression A-1 within the range of |V5|<|VOUT|.

$$V_5 = \left(1+\frac{Rb}{Ra}\right)\cdot V_{EV} = \left(1+\frac{Rb}{Ra}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG} \quad \left[\Theta V_{EV} = \left(1-\alpha/162\right)\cdot V_{REG}\right] \qquad \text{(Expression A-1)}$$

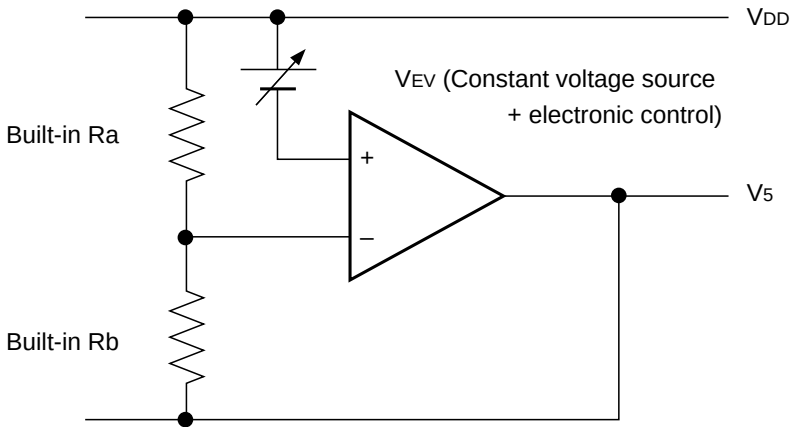


Figure 9

VREG is a constant voltage source within an IC, and the value at Ta=25°C is constant as listed in Table 9.

Table 9

Device	Temperature gradient	Unit	VREG	Unit
Internal power supply	–0.05	[%/°C]	–2.1	[V]

α indicates an electronic control command value. Setting data in a 6-bit electronic control register enters one state among 64 states. Table 10 lists the values of α based on the setup of the electronic control register.

Table 10

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
		⋮				⋮
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

Rb/Ra indicates the V5 voltage adjusting built-in resistance ratio and can be adjusted into eight steps using the V5 voltage adjusting built-in resistance ratio set command. The reference values of the (1+Rb/Ra) ratio are obtained as listed in Table 11 by setting 3-bit data in the V5 voltage adjusting built-in resistance ratio register.

Table 11 (Reference values)

Register			Device per temperature gradient [Unit: %/°C]
D2	D1	D0	–0.05
0	0	0	4.5
0	0	1	5.0
0	1	0	5.5
0	1	1	6.0
1	0	0	6.5
1	0	1	7.0
1	1	0	7.6
1	1	1	8.1

For the internal resistance ratio, a manufacturing dispersion of up to ±7% should be taken into account. When not within the tolerance, adjust the V5 voltage by externally mounting Ra and Rb.
Figure 10 show the V5 voltage reference values per temperature gradient device based on the values of the V5 voltage adjusting built-in resistance ratio register and electronic control register at Ta=25°C.

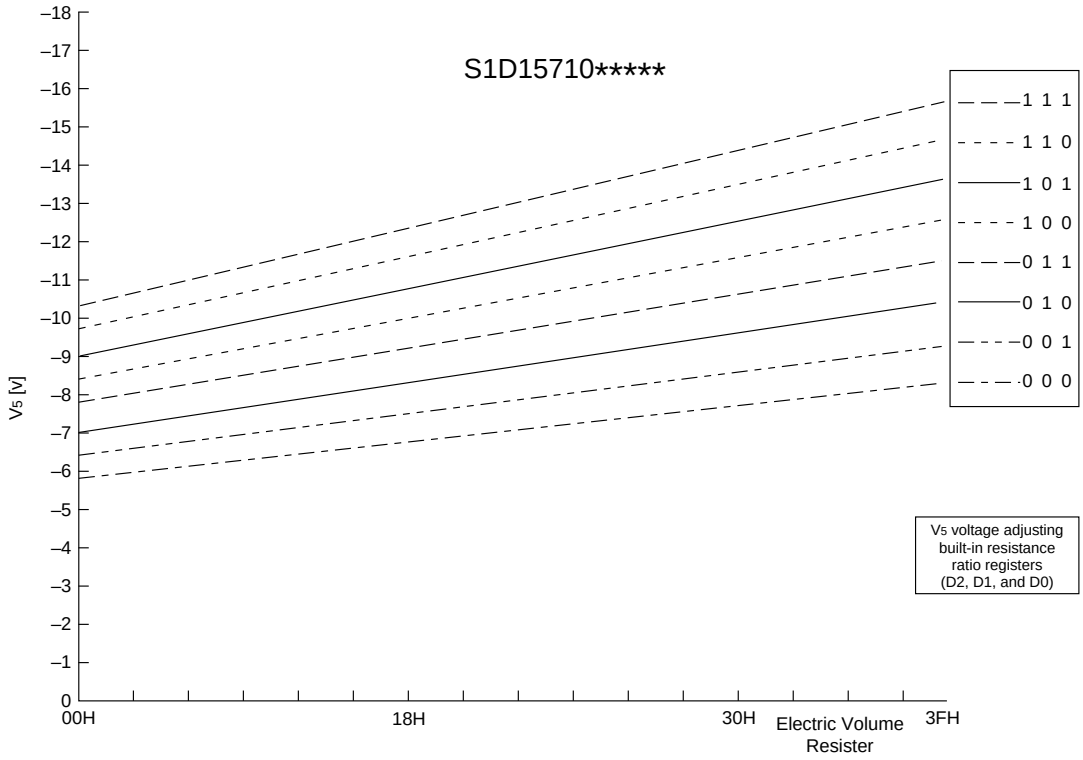


Figure 10 S1D15710***** Temperature gradient = –0.05%/°C

V_5 voltage based on the values of V_5 voltage adjusting built-in resistance ratio register and electronic control register

<Setting example: When setting V_5 = –9 V at Ta=25°C>
From Figure 8 and Expression A-1.

Table 12

Description	Register					
	D5	D4	D3	D2	D1	D0
V_5 voltage adjusting	–	–	–	0	1	0
electronic control	1	0	0	1	0	1

In this case, Table 13 lists the V_5 voltage variable range and pitch width using the electronic control function.

Table 13

V_5	Min.		Typ.		Max.	Unit
Variable range	–11.6	to	–9.3	to	–7.1	[V]
Pitch width			67			[mV]

(B) When using the external resistor (not using the V5 voltage adjusting built-in resistor) ①
The liquid crystal power supply voltage V5 can also be set by adding the resistors (Ra' and Rb') between VDD and VR and between VR and V5 without the V5 voltage adjusting built-in resistor (IRS pin=LOW). Also in this case, the liquid crystal power supply voltage V5 can be controlled using the command and the light and shade of liquid crystal display can be adjusted by using the electronic control function.

The V5 voltage can be obtained from Expression B-1 by setting the external resistors Ra' and Rb' within the range of |V5| < |VOUT|.

$$V_5 = \left(1+\frac{Rb'}{Ra'}\right)\cdot V_{EV} = \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG} \quad \left[\Theta V_{EV} = \left(1-\alpha/162\right)\cdot V_{REG}\right] \qquad \text{(Expression B-1)}$$

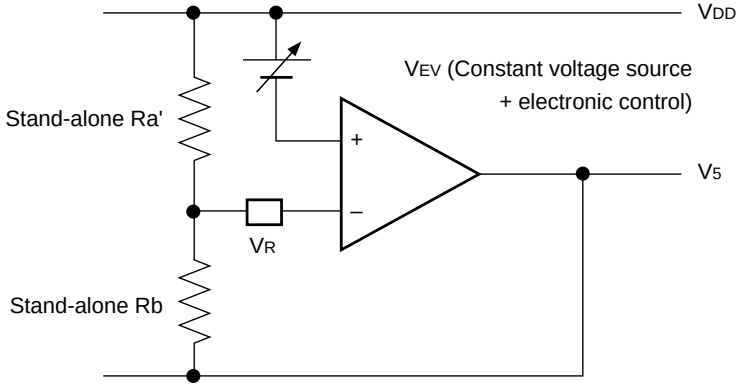


Figure 11

<Setting example: When setting V5=–9 V at Ta=25°C>

Set the value of the electronic control register as the intermediate value (D5, D4, D3, D2, D1, D0) = (1,0,0,0,0,0). From the foregoing we can establish the expression:

$$\alpha = 31$$
$$V_{REG} = -2.1V$$

From Expression B-1, it follows that

$$V_5 = \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG} \quad \text{(Expression B-2)}$$
$$-9V = \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{31}{162}\right)\cdot(-2.1)$$

Also, suppose the current applied to Ra' and Rb' is 5μA.

$$Ra'+Rb' = 1.8M\Omega \qquad \text{(Expression B-2)}$$

It follows that
Therefore from Expressions B-2 and B-3, we have

$$\frac{Rb'}{Ra'} = 4.3$$
$$Ra' = 340k\Omega$$
$$Rb' = 1460k\Omega$$

In this case, Table 14 lists the V5 voltage variable range and pitch width using the electronic control function.

Table 14

V5	Min.		Typ.		Max.	Unit
Variable range	–11.1	to	–9.0	to	–6.8	[V]
Pitch width			67			[mV]

(C) When using the external resistor (not using the V5 voltage adjusting built-in resistor) ②
In the use of the above-mentioned external resistor, the liquid crystal power supply voltage V5 can also be set by adding the resistors to finely adjust Ra' and Rb'. Also in this case, the liquid crystal power supply voltage V5 can be controlled using the command and the light and shade of liquid crystal display can be adjusted by using the electronic control function.

The V5 voltage can be obtained from the following expression C-1 by setting the external resistors R1, R2 (variable resistors), and R3 within the range of |V5| < |VOUT| and finely adjusting R2 (ΔR2).

$$V_5 = \left(1+\frac{R_3+R_2-\Delta R_2}{R_1+\Delta R_2}\right)\cdot V_{EV} = \left(1+\frac{R_3+R_2-\Delta R_2}{R_1+\Delta R_2}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG} \quad \left[\Theta V_{EV} = \left(1-\alpha/162\right)\cdot V_{REG}\right] \qquad \text{(Expression C-1)}$$

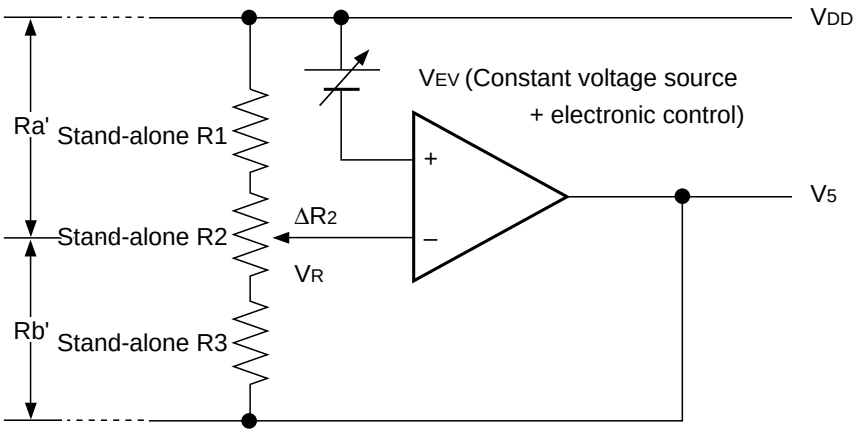


Figure 12

<Setting example: When setting V5=–7 to –11 V at Ta=25°C>

Set the value of the electronic control register as the intermediate value (D5, D4, D3, D2, D1, D0) = (1,0,0,0,0,0). From the foregoing we can establish the expression:

$$\alpha = 31$$
$$V_{REG} = -2.1V$$

When ΔR2=0Ω, to obtain V5=–9 V from Expression C-1, it follows that

$$-11V = \left(1+\frac{R_3+R_2}{R_1}\right)\cdot\left(1-\frac{31}{162}\right)\cdot(-2.1)$$

(Expression C-2)

When ΔR2=R2, to obtain V5=–7V, it follows that

$$-7V = \left(1+\frac{R_3}{R_1+R_2}\right)\cdot\left(1-\frac{31}{162}\right)\cdot(-2.1)$$

(Expression C-3)

Also, suppose the current applied between VDD and V5 is 5μA.

$$R_1 + R_2 + R_3 = 1.8M\Omega$$

(Expression C-4)

It follows that

Therefore from Expressions C-2, C-3, and C-4, we have

$$R_1 = 162k\Omega$$
$$R_2 = 278k\Omega$$
$$R_3 = 1363k\Omega$$

At this time, the V5 voltage variable range and notch width based on electronic volume function are given in the following Table when V5=–9 V by R2 is assumed:

Table 15

V5	Min.		Typ.		Max.	Unit
Variable range	–11.1	to	–9.0	to	–6.8	[V]
Pitch width			67			[mV]

- When using the V5 voltage adjusting built-in resistor or electronic control function, the state where at least the V5 voltage adjusting circuit and voltage follower circuit are operated together needs to be set using the power control set command. Also when the boosting circuit is OFF, the voltage needs to be applied from VOUT.
- The VR pin is valid only when the V5 voltage adjusting built-in resistor (IRS pin=LOW). Set the VR pin to OPEN when using the V5 voltage adjusting built-in resistor (IRS pin=HIGH).
- Since the VR pin has high input impedance, noise must be taken into consideration such as for short and shielded lines.

Liquid crystal voltage generator circuit

The V5 voltage is resistor-split within an IC and generates the V1, V2, V3, and V4 potentials required for the liquid crystal drive.
Further, the V1, V2, V3, and V4 potentials are impedance-converted by the voltage follower and supplied to the liquid crystal drive circuit.

Using the bias set command allows you to select a desired bias ratio from 1/9 or 1/7.

High power mode

The power supply circuit incorporated in the S1D15710 series has the ultra-low power consumption (normal mode: $\overline{\text{HPM}}$=HIGH). Therefore the display quality

may be deteriorated in large load liquid crystal or panels. In this case, the display quality can be improved by setting $\overline{HPM}$ pin=LOW (high power mode). Whether to use the power supply circuit in this mode should need the display confirmation by actual equipment.
Also, if improvement is insufficient even for the high power mode setting, use either the S1D15710D10B∗ or supply liquid crystal drive power externally. In either case, be sure to check the display thoroughly.

Command sequence when the built-in power supply is turned off

To turn off the built-in power supply, set it in the power save state and then turn off the power supply according to the command sequence shown in Figure 13 (procedure).

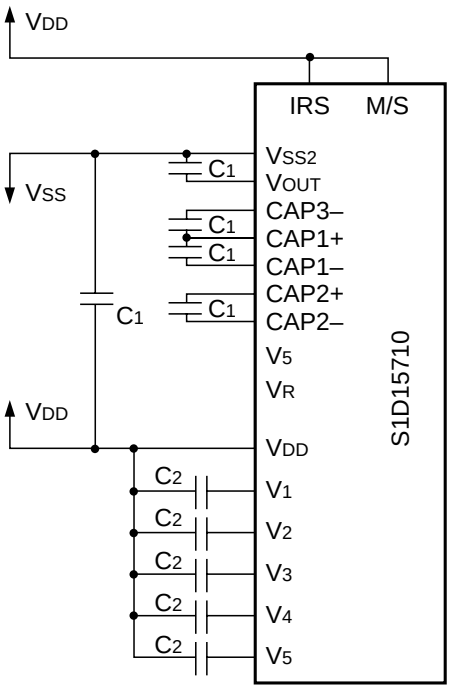
Procedure	Description (Command, state)	Command address D7	D6	D5	D4	D3	D2	D1	D0
Step1	Power save	1	0	1	0	1	0	0	0
Step2	Turning off the built -in power supply								1

Power save command (Both stand-by and sleep can be useal)

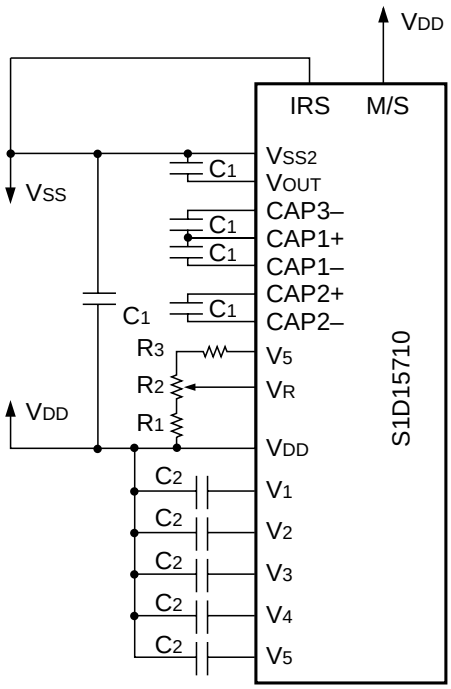
Figure 13

① All the built-in power supply used

(1) When using the V_5 voltage adjusting built-in resistor (Example of V_{SS2}=V_{SS}, quadruple boosting)

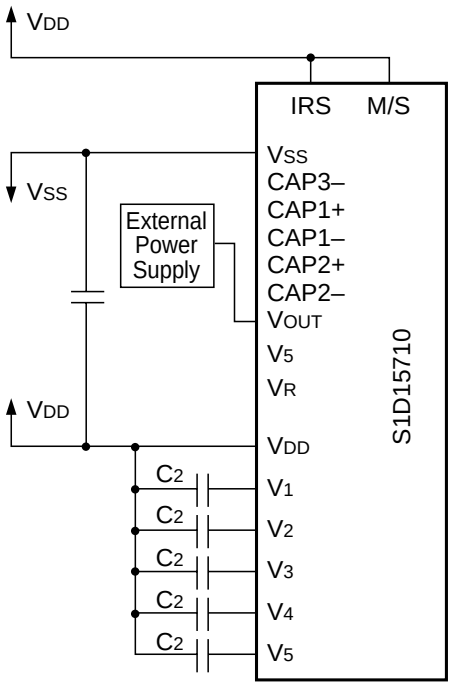


(2) When not using the V_5 voltage adjusting built-in resistor (Example of V_{SS2}=V_{SS}, quadruple boosting)

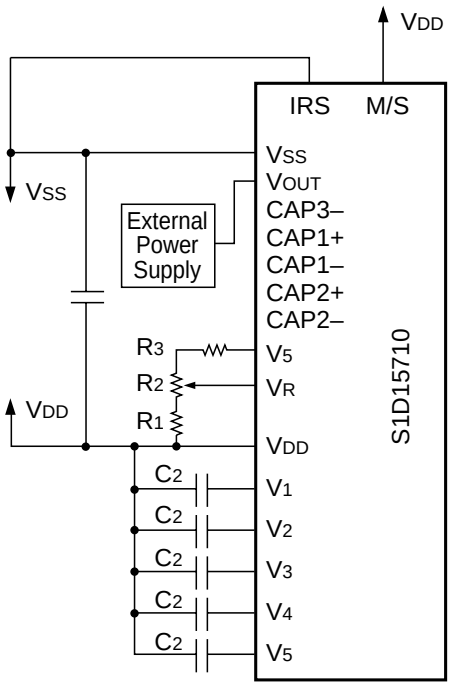


② Only the voltage adjusting circuit and V/F circuit used

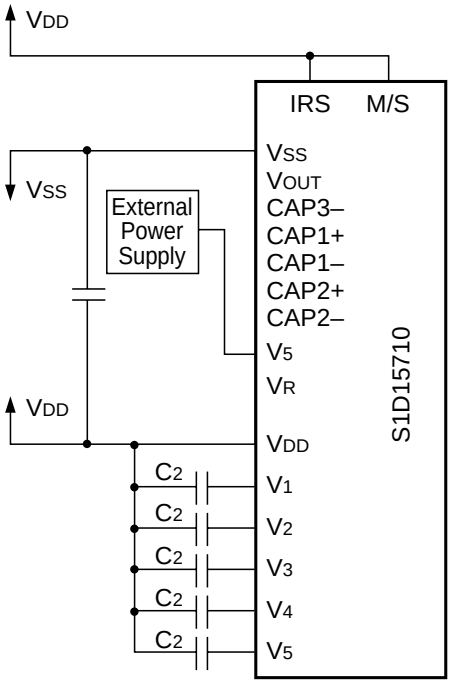
(1) When using the V_5 voltage adjusting built-in resistor



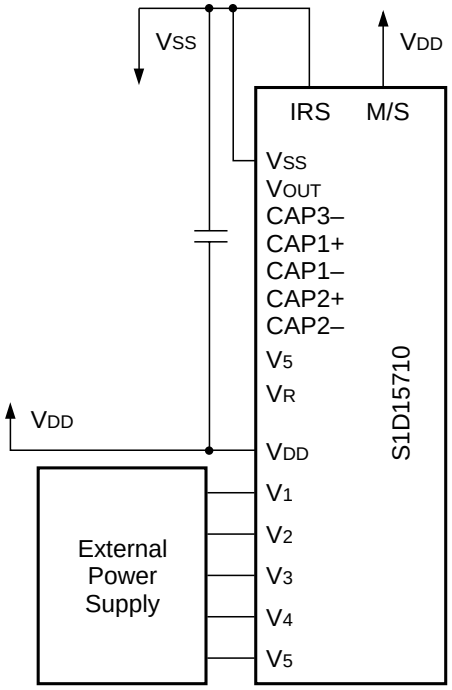
(2) When not using the V_5 voltage adjusting built-in resistor



③ Only the V/F circuit used



④ Only the external power supply used
Depending on all external power supplies



Common reference setting example
At V_5=–8 to –12 V variable

Item	Setting value	Unit
C_1	1.0 to 4.7	µF
C_2	0.01 to 1.0	µF

Figure 14

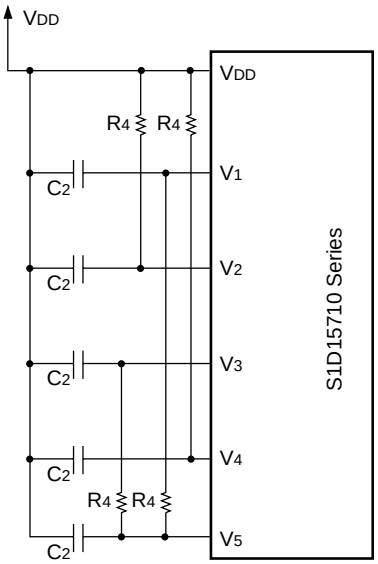
*1 Since the V_R terminal input impedance is high, use short leads and shielded lines. When the V_R terminal is not used, means should be taken to prevent capacitance of the line or others from being applied.

*2 C_1 and C_2 are determined according to the size of the LCD panel. Set a value so that the liquid crystal drive voltage can be stable.

[Setting example]
- Turn on the V_5 adjusting circuit and the V/F circuit and apply external voltage.
- Display LCD heavy load patterns like lateral stripes and determine C_2 so that the liquid crystal drive voltages (V_1 to V_5) can be stable.
- Then turn on all built-in power supplies and determine C_1.

*3 Capacity is connected in order to stabilize voltage between V_{DD} and V_{SS} power supplies.

*4 When the built-in V/F circuit is used to drive an LCD panel with heavy alternating or direct current load, we recommend that external resistance be connected in order to stabilize V/F outputs, or electric potentials, V_1, V_2, V_3 and V_4.



Adjust resistance value R_4 to the optimal level by checking driving waveform displayed on the LCD.

Reference setting: R_4 = 0.1 to 1.0 [MΩ]

Figure 15

*5 Precautions when installing the COG

When installing the COG, it is necessary to duly consider the fact that there exists a resistance of the ITO wiring occurring between the driver chip and the externally connected parts (such as capacitors and resistors). By the influence of this resistance, non-conformity may occur with the indications on the liquid crystal display.
Therefore, when installing the COG design the module paying sufficient considerations to the following three points.

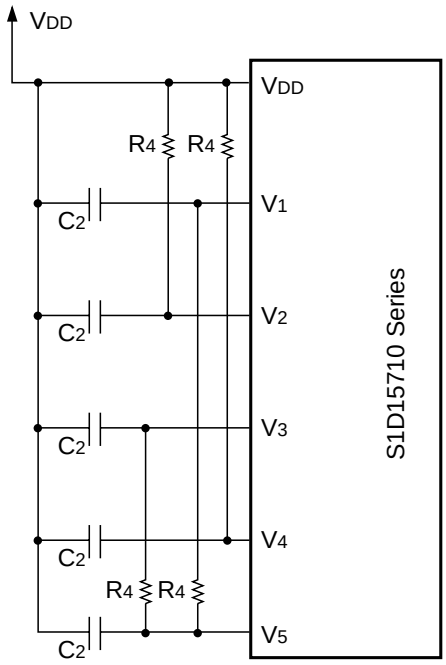
1. Suppress the resistance occurring between the driver chip pin to the externally connected parts as much as possible.
2. Suppress the resistance connecting to the power supply pin of the driver chip.
3. Make various COG module samples with different ITO sheet resistance to select the module with the sheet resistance with sufficient operation margin.

Also, as for this driver IC, pay sufficient attention to the following points when connecting to external parts for the characteristics of the circuit.

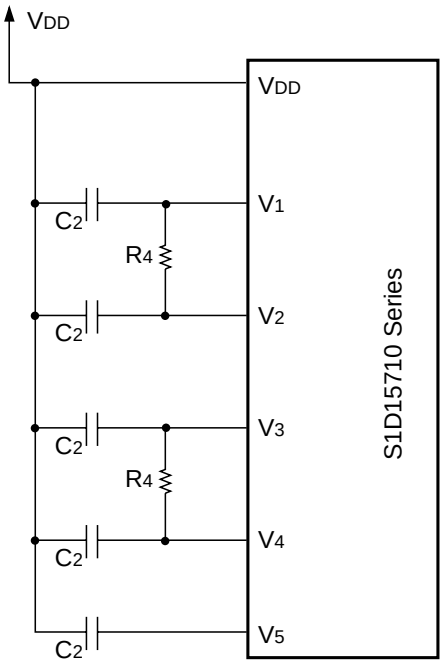
1. Connection to the boosting capacitors The boosting capacitors (the capacitors connecting to respective CAP pins and capacitor being inserted between V_{OUT} and V_{SS2}) of this IC are being switched over by use of the transistor with very low ON-resistance of about 10Ω. However, when installing the COG, the resistance of ITO wiring is being inserted in series with the switching transistor, thus dominating the boosting ability.
   Consequently, the boosting ability will be hindered as a result and pay sufficient attention to the wiring to respective boosting capacitors.
2. Connection of the smoothing capacitors for the liquid crystal drive
   The smoothing capacitors for the liquid crystal driving potentials (V_1. V_2, V_3 and V_4) are indispensable for liquid crystal drives not only for the purpose of mere stabilization of the voltage levels. If the ITO wiring resistance which occurs pursuant to installation of the COG is supplemented to these smoothing capacitors, the liquid crystal driving potentials become unstable to cause non-conformity with the indications of the liquid crystal display. Therefore, when using the COG module, we definitely recommend to connect reinforcing resistors externally.
   Reference value of the resistance is 100kΩ to 1MΩ. Meanwhile, because of the existence of these reinforcing resistors, current consumption will increase.

Indicated below is an exemplary connection diagram of external resistors.
Please make sufficient evaluation work for the display statuses with any connection tests.

Exemplary connection diagram 1.



Exemplary connection diagram 2.



Reference circuit examples

Reset Circuit

When the RES input is set to the LOW level, this LSI enters each of the initial setting states

1. Display OFF
2. Display Normal Rotation
3. ADC Select: Normal rotation (ADC command D0=0)
4. Power Control Register: (D2,D1,D0)=(0,0,0)
5. Register Data Clear within Serial Interface
6. LCD Power Supply Bias Ratio: 1/9 bias
7. n-Line Alternating Current Reversal Drive Reset
8. Power saving clear
9. Display All Lighting OFF: (Display All Lighting ON/OFF command D0=LOW)
10. Built-in Oscillator Circuit stopped
11. Static Indicator OFF
    Static Indicator Register: (D1,D2)=(0,0)
12. Read Modify Write OFF
13. Display start line set to the first line
14. Column address set to address 0
15. Page address set to page 0
16. Common Output State Normal rotation
17. V_5 Voltage Adjusting Built-in Resistance Ratio Register: (D2,D1,D0)=(0,0,0)
18. Electronic Control Register Set Mode Reset
    Electronic Control Register* (D5, D4, D3, D2, D1, D0) = (1,0,0,0,0,0)
19. n-Line Alternating Current Reversal Register: (D3, D2, D1, D0) = (0, 0, 0, 0)
20. Test Mode Reset

On the other hand, when using the reset command, only the items 11 to 20 of the above-mentioned initial setting are executed.

When the power is turned on, the initialization using the RES pin is required. After the initialization using the RES pin, each input pin needs to be controlled normally. Besides, when the MPU control signal has high impedance, overcurrent may be applied to an IC. After turning on the power, take action so that the input pin cannot have high impedance.
The S1D15710 Series discharge electric charges of V_5 and V_{OUT} at RES pin is set to the LOW level. If external power supplies for driving LCD are used, do not input external power while the RES pin is set to the LOW level to prevent short-circuiting between the external power supplies and V_{DD}.

7. COMMAND DESCRIPTION

The S1D15710 series identifies data bus signals according to the combinations of A0, $\overline{RD}$(E), and $\overline{WR}$(R/$\overline{W}$). Since the interpretation and execution of commands are performed only by the internal timing independently of external clocks, the S1D15710 performs high-speed processing that does not require busy check normally.
The 80 series MPU interface starts commands by inputting low pulses to the $\overline{RD}$ pin at read and to the $\overline{WR}$ pin at write operation. The 68 series MPU interface enters the read state when HIGH is input to the R/$\overline{W}$ pin. It enters the write state when LOW is input to the same pin. It starts commands by inputting high pulses to the E pin (for the timing, see the Timing Characteristics of Chapter 10). Therefore the 68 series MPU interface differs from the 80 series MPU interface in that $\overline{RD}$(E) is set to "1 (H)" at status read and display data read in the Command Description and Command Table. The command description is given below by taking the 80 series MPU interface as an example.
When selecting the serial interface, enter sequential data from D_7.

Command description

(1) Display ON/OFF

This command specifies display ON/OFF.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

For display OFF, the segment and common drivers output the V_{DD} level.

(2) Display Start Line Set

This command specifies the display start line address of the display data RAM shown in Figure 4. The display area is displayed for 65 lines from the specified line address to the line address increment direction. When this command is used to dynamically change the line address, the vertical smooth scroll and page change are enabled. For details, see the Line address circuit of "Function Description".

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	0	0	1	0	2
							↓				↓
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

(3) Page Address Set

This command specifies the page address that corresponds to the low address when accessing the display data RAM shown in Figure 4 from the MPU side. The display data RAM can access desired bits when the page address and column address are specified. Even when the page address is changed, the display state will not be changed. For details, see the Page address circuit of "Function Description".

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
								↓			↓
							0	1	1	1	7
							1	0	0	0	8

(4) Column Address Set

This command specifies the column address of the display data RAM shown in Figure 4. The column address is split into two sections (higher 4-bits and lower 4-bits) when it is set (set continuously in principle). Each time the display data RAM is accessed, the column address automatically increments (+), making it possible for the MPU to continuously read and write the display data. The column address increment is stopped at FFH, and the FFH is specified continuously. This must be noted when you want to access continuously. In this case, the page address is not changed continuously. For details, see "Column Address Circuit" in Function Description.

	A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
High-order bit →	0	1	0	0	0	0	1	A7	A6	A5	A4
Low-order bit →							0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
				↓				↓
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

(5) Status Read

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	When BUSY=1, indicates an internal operation being done or reset. The command cannot be accepted until BUSY=0 is reached. However, if the cycle time is satisfied, the command needs not be checked.
ADC	Indicates the correspondence relationship between the column address and segment driver. 0: Reversal (column address 199–n ↔ SEG n) 1: Normal rotation (column address n ↔ SEG n) (Reverses the polarity of ADC command.)
ON/OFF	ON/OFF: Specifies display ON/OFF 0: Display ON 1: Display OFF (Reverses the polarity of display ON/OFF command.)
RESET	Indicates the $\overline{RES}$ signal or that initial setting is being done using the reset command. 0: Operating state 1: Resetting

(6) Display Data Write

This command writes 8-bit data to the specified address of the display data RAM. Since the column address is automatically incremented by 1 after the data is written, the MPU can successively write the display data.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

(7) Display Data Read

This command reads the 8-bit data in the specified address of the display data RAM. Since the column address is automatically incremented by 1 after the data is written, the MPU can successively read the data consisting of multiple words.
Besides, immediately after the column address is set, dummy read is required one time. For details, see the description of the Display data RAM and internal register access of "Function Description".
When using the serial interface, the display cannot be read.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

(8) ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence relationship between the column address of the display RAM data shown in Figure 4 and the segment driver output. Therefore the order of the segment driver output pin can be reversed using the command. After the display data is written and read, the column address is incremented by 1 according to the column address of Figure 4. For details, see the Column address circuit of "Function Description".

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Clockwise (normal rotation)
										1	Counterclockwise (reversal)

(9) Display Normal Rotation/Reversal

This command can reversal display lighting and non-lighting without overwriting the contents of display data RAM. In this case, the contents of display data RAM are held.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	LCD on potential (normal rotation) RAM data HIGH
										1	LCD on potential (reversal) RAM data LOW

(10) Display All Lighting ON/OFF

This command can forcedly make all display set in the lighting state irrespective of the contents of display data RAM. In this case, the contents of display data RAM are held.
This command has priority over the display normal rotation/reversal command.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display state
										1	Display all lighting

(11) LCD Bias Set

This command selects the bias ratio of the voltage required for liquid crystal drive. The command is valid when the V/F circuit of the power supply circuit is operated.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected state
0	1	0	1	0	1	0	0	0	1	0	1/9 bias
										1	1/7 bias

(12) Read Modify Write

This command is used together with the end command. Once this command is entered, the column address can be incremented by 1 only using the display data write command instead of being changed using the display read command. This state is held until the end command is entered. When the end command is entered, the column address returns to the address when the read modify write command is entered. This function can reduce the load of the MPU when repeatedly changing data for a specific display area such as a blinking cursor.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

* The commands other than Display Data Read/Write can be used even in Read Modify Write mode. However, the column address set command cannot be used.

• Sequence for cursor display

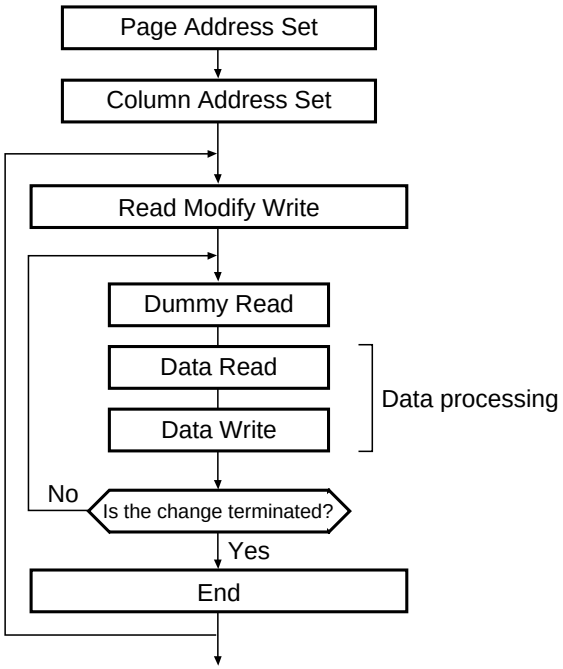


Figure 16

(13) End

This command resets the Read Modify Write mode and returns the column address to the mode initial address.

A0	$\overline{E}$ $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

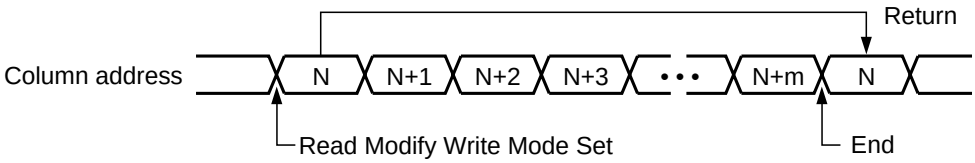


Figure 17

(14) Reset

This command initializes Display Start Line, Column Address, Page Address, Common Output State, V_5 Voltage Adjusting Built-in Resistance Ratio, Electronic Control, and Static Indicator and resets the Read Modify Write mode and Test mode. This will not have any effect on the display data RAM. For details, see the Reset of " Function Description".
Reset operation is performed after the reset command is entered.

A0	$\overline{E}$ $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The initialization when the power is applied is performed using the reset signal to the $\overline{RES}$ pin. The reset command cannot be substituted for the signal.

(15) Common Output State Selection

This command can select the scanning direction of the COM output pin. For details, see the Common Output State Selection Circuit of "Function Description".

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Selected state	
0	1	0	1	1	0	0	0	*	*	*	Normal rotation	COM0 → COM63
							1				Reversal	COM63 → COM0

*: Invalid bit

(16) Power Control Set

This command sets the function of the power supply circuit. For details, see the Power Supply Circuit of "Function Description".

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Selected state
0	1	0	0	0	1	0	1	0			Boosting circuit: OFF
								1			Boosting circuit: ON
									0		V adjusting circuit: OFF
									1		V adjusting circuit: ON
										0	V/F circuit: OFF
										1	V/F circuit: ON

(V/F circuit: Voltage follower circuit, V adjusting circuit: voltage adjusting circuit)

(17) V_5 Voltage Adjusting Built-in Resistance Ratio Set

This command sets the V_5 voltage adjusting built-in resistance ratio. For details, see the Power Supply Circuit of "Function Description".

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Rb to Ra ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									↓		↓
								1	1	0	
								1	1	1	Large

(18) Electronic Control (2-Byte Command)

This command controls the liquid crystal drive voltage V_5 output from the voltage adjusting circuit of the built-in liquid crystal power supply and can adjust the light and shade of liquid crystal display.
Since this command is a 2-byte command that is used together with the electronic control mode set command and electronic control register set command, always use both the commands consecutively.

• Electronic Control Mode Set
Entering this command validates the electronic control register set command. Once the electronic control mode is set, the commands other than the electronic control register set command cannot be used. This state is reset after data is set in the register using the electronic control register set command.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

• Electronic Control Register Set
This command is used to set 6-bit data in the electronic volume register to allow the liquid crystal drive voltage V_5 to enter one-state voltage value among 64-state voltage values.
After this command is entered and the electronic control register is set, the electronic control mode is reset.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	| V5 |
0	1	0	*	*	0	0	0	0	0	0	Small
0	1	0	*	*	0	0	0	0	0	1	
0	1	0	*	*	0	0	0	0	1	0	
							↓				↓
0	1	0	*	*	1	1	1	1	1	0	
0	1	0	*	*	1	1	1	1	1	1	Large

*: Invalid bit

When not using the electronic control function, set (1,0,0,0,0,0).

• Sequence of the electronic control register set

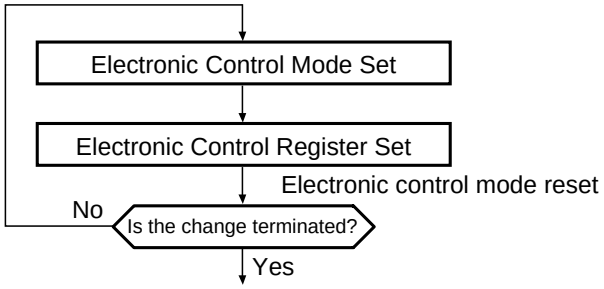


Figure 18

(19) Static Indicator (2-Byte Command)

This command controls the indicator display of the static drive system. The static indicator display is controlled only using this command, and this command is independent of other display control commands.
The static indicator is used to connect the SYNC pin to one of its liquid crystal drive electrodes and the FRS pin to the other. For the electrodes used for the static indicator, the pattern separated from the electrodes for dynamic drive are recommended. When this pattern is too adjacent, the deterioration of liquid crystal and electrodes may be caused.
Since the static indicator ON command is a 2-byte command that is used together with the static indicator register set command, always use both the commands consecutively. (The static indicator OFF command is a 1-byte command.)

• Static Indicator ON/OFF
Entering the static indicator ON command validates the static indicator register set command. Once the static indicator ON command is entered, the commands other than the static indicator register set command cannot be used. This state is reset after the data is set in the register using the static indicator register set command.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Static indicator
0	1	0	1	0	1	0	1	1	0	0	OFF
										1	ON

• Static Indicator Register Set
This command sets data in the 2-bit static indicator register and sets the blinking state of the static indicator.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Indicator display state
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON (blinks at an interval of approximately 0.5 second.)
									1	0	ON (blinks at an interval of approximately one second.)
									1	1	ON (goes on at all times.)

*: Invalid bit

• Sequence of Static Indicator Register Set

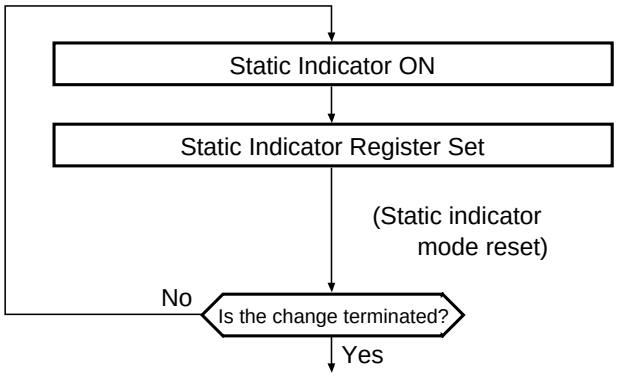


Figure 19

(20) Power Save

This command makes the static indicator enter the power save state and can greatly reduce the power consumption. The power save state consists of the sleep state and stand-by state.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Power save state
0	1	0	1	0	1	0	1	0	0	0	Stand-by state
										1	Sleep state

The operating state before the display data and power save activation is held in the sleep and stand-by states, and the display data RAM can also be accessed from the MPU.

• Sleep State
This command stops all the operations of LCD display systems, and can reduce the power consumption approximate to the static current when they are not accessed from the MPU. The internal state in the sleep state is as follows:
(1) The oscillator circuit and the LCD power supply circuit are stopped.
(2) All liquid crystal drive circuit is stopped and the segment and common drivers output the V_{DD} level.

• Stand-by State

This command stops the operation of the duty LCD display system and operates only the static drive system for indicators. Consequently the minimum current consumption required for the static drive is obtained. The internal state in the stand-by state is as follows:

(1) The LCD power supply circuit is stopped. The oscillator circuit is operated.

(2) The duty drive system liquid crystal drive circuit is stopped and the segment and common drivers output the V_{DD} level. The static drive system is operated.

* When using external power supplies, it is recommended that the function of the external power supply circuit should be stopped at power save activation. For example, when providing each level of the liquid crystal drive voltage using a stand-alone split resistor circuit, it is recommended that the circuit which cuts off the current applied to the split resistor circuit should be added at power save activation. The S1D15710 series has the liquid crystal display blanking control pin $\overline{DOF}$ and is set to $\underline{LOW}$ at power save activation. The function of the external power supply circuit can be stopped using the $\overline{DOF}$ output.

(21) Power Save Reset

This command resets the power save state and returns the state before power save activation.

A0	$\underline{E}$ $\underline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	1

(22) n-Line Reversal Drive Register Set

This command sets the number of reversal lines of the liquid crystal drive in the register. 2 to 16 lines can be set. For details, see the Display Timing Generator Circuit of “Function Description”.

A0	$\underline{E}$ $\underline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Line of reversal lines
0	1	0	0	0	1	1	0	0	0	0	—
							0	0	0	1	2
							0	0	1	0	3
									↓		↓
							1	1	1	0	15
							1	1	1	1	16

(23) n-Line Reversal Drive Reset

This command resets the n-line reversal alternating current drive and returns to the normal 2-frame reversal alternating current drive system. The value of the n-line reversal alternating current drive register is not changed.

A0	$\underline{E}$ $\underline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	1	0	0

(24) Built-in Oscillator Circuit ON

This command starts the operation of the built-in CR oscillator circuit. This command is valid only for the master operation (M/S=HIGH) and built-in oscillator circuit valid (CLS=HIGH).

A0	$\underline{E}$ $\underline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	1	1

(25) NOP

Non-OPeration

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

(26) Test

IC chip test command. Do not use this command. If the test command is used incorrectly, it can be reset by setting the $\overline{RES}$ input to LOW or by using the reset command or NOP.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

*: Invalid bit

(Note) Although the S1D15710 series holds the command operating state, it may change the internal state if excessive foreign noise is entered. Such action that suppresses the generation of noise and prevents the effect of noise needs to be taken on installation and systems. Besides, to prevent sudden noise, it is recommended that the operating state should periodically be refreshed.

Table 16 S1D15710 Series Commands

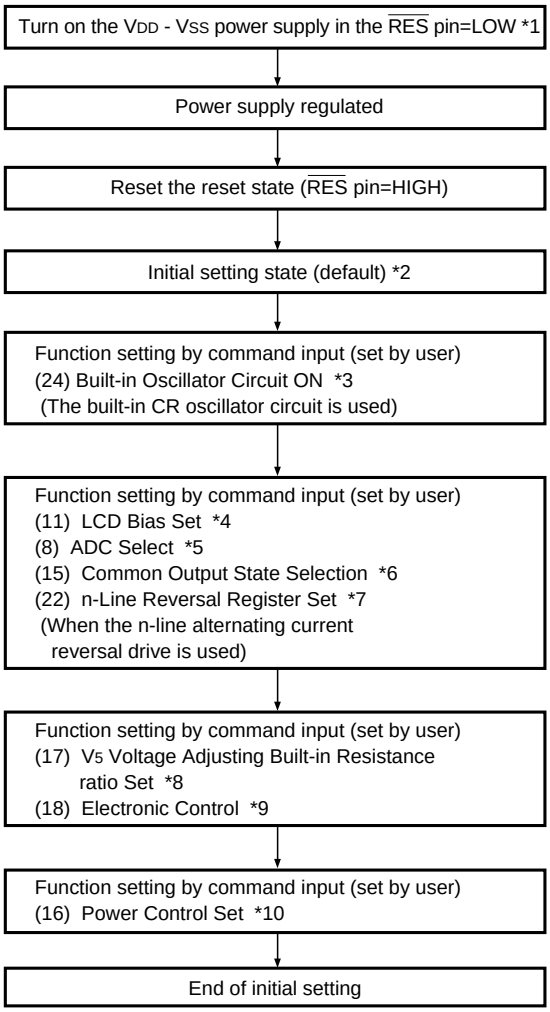
Command	Command code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display Start Line Set	0	1	0	0	1	Display start address						Sets the display start line address of the display RAM.
(3) Page Address Set	0	1	0	1	0	1	1	Page Address				Sets the page address of the display RAM.
(4) Column Address Set High-Order Bit	0	1	0	0	0	0	1	High order Column address				Sets the high-order four bits of the column address of the display RAM.
Column Address Set Low-Order Bit	0	1	0	0	0	0	0	Low order Column address				Sets the low-order four bits of the column address of the display RAM.
(5) Status Read	0	0	1	Status				0	0	0	0	Reads the status information.
(6) Display Data Read	1	1	0	Write data								Writes data on the display RAM.
(7) Display Data Write	1	0	1	Read data								Reads data from the display RAM.
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Supports the SEG output of the display RAM address. 0: normal rotation, 1: Reversal
(9) Display Normal Rotation/Reversal	0	1	0	1	0	1	0	0	1	1	0 1	LCD display normal rotation/ reversal 0: normal rotation, 1: Reversal
(10) Display All Lighting ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all lighting 0: normal display, 1: All ON
(11) LCD Bias Set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio. 0: 1/9, 1: 1/7
(12) Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increments the column address. At write operation: By 1, at read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Resets Read Modify Write.
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal resetting
(15) Common Output State Selection	0	1	0	1	1	0	0	0 1	*	*	*	Selects the scanning direction of the COM output. 0: Normal rotation, 1: Reversal
(16) Power Control Set	0	1	0	0	0	1	0	1	Operating state			Selects the state of the built-in power supply
(17) V_5 Voltage Adjusting Internal Resistance Ratio Set	0	1	0	0	0	1	0	0	Resistance ratio setting			Selects the state of the built-in resistance ratio (Rb/Ra).
(18) Electronic Control Mode Set	0	1	0	1	0	0	0	0	0	0	1	
Electronic Control Register Set	0	1	0	*	*	Electronic control value						Sets the V_5 output voltage in the electronic register.
(19) Static Indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1	0: OFF, 1: ON
Static Indicator Register Set	0	1	0	*	*	*	*	*	*	State		Sets the blinking state.
(20) Power Save	0	1	0	1	0	1	0	1	0	0	0 1	Moves to the power save state. 0: Stand-by, 1: Sleep
(21) Power Save Reset	0	1	0	1	1	1	0	0	0	0	1	Resets power save.
(22) n-Line Reversal Drive Register Set	0	1	0	0	0	1	1	Number of reversal Line				Sets the number of line reversal drive lines.
(23) n-Line Reversal Drive Reset	0	1	0	1	1	1	0	0	1	0	0	Resets the line reversal drive.
(24) Built-in Oscillator Circuit ON	0	1	0	1	0	1	0	1	0	1	1	Starts the operation of the built-in CR oscillator circuit.
(25) NOP	0	1	0	1	1	1	0	0	0	1	1	Non-Operation command
(26) Test	0	1	0	1	1	1	1	*	*	*	*	Do not use the IC chip test command.

*: Invalid bit

8. COMMAND SETTING

Instruction Setup: Reference

(1) Initial Setting



Notes: Reference items

*1: If external power supplies for driving LCD are used, do not supply voltage on VOUT or V5 pin during the period when RES = LOW. Instead, input voltage after releasing the reset state.
6. Function Description "Reset Circuit"

*2: The contents of DDRAM are not defined even in the initial setting state after resetting.
6. Function Description Section "Reset Circuit"

*3: 7. Command Description Item (24) "Built-in oscillator circuit ON"

*4: 7. Command Description Item (11) "LCD bias set"

*5: 7. Command description Item (8) "ADC select"

*6: 7. Command Description Item (15) "Common output state selection"

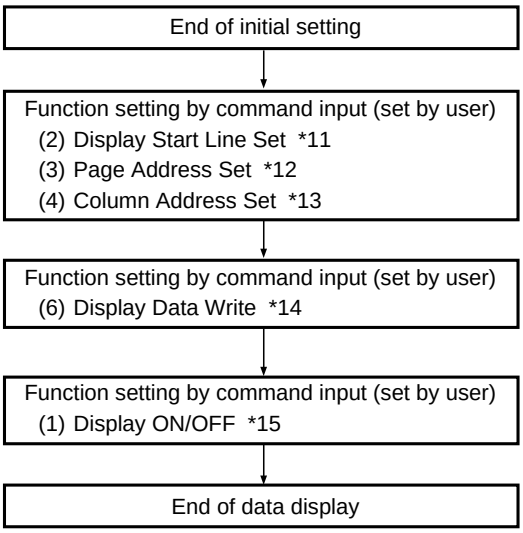
*7: 6. Function Description Section "Display Timing Generator Circuit", 7. Command Description Item (22) "n-Line Reversal Register Set"

*8: 6. Function Description Section "Power Supply Circuit" and 7. Command Description Item (17) "V5 Voltage Adjusting Built-in Resistance ratio Set"

*9: 6. Function Description Section "Power Supply Circuit" and 7. Command Description Item (18) "Electronic Control"

*10: 6. Function Description Section "Power Supply Circuit" and 7. Command Description Item (16) "Power Control Set"

(2) Data Display



Notes: Reference items

*11: 7. Command Description Item (2) “Display Start Line Set”

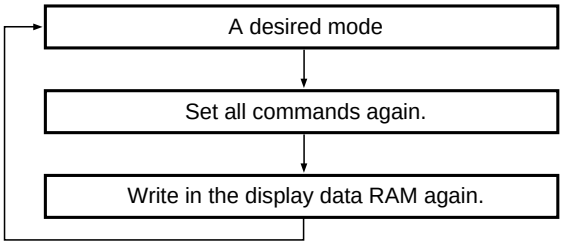
*12: 7. Command Description Item (3) “Page Address Set”

*13: 7. Command Description Item (4) “Column Address Set”

*14: The contents of DDRAM is not defined after completing initial setting. Enter data in each DDRAM to be used for display.
7. Command Description Item (6) “Display Data Write”

*15: Avoid activating the display function with entering space characters as the data if possible.
7. Command Description Item (1) “Display ON/OFF”

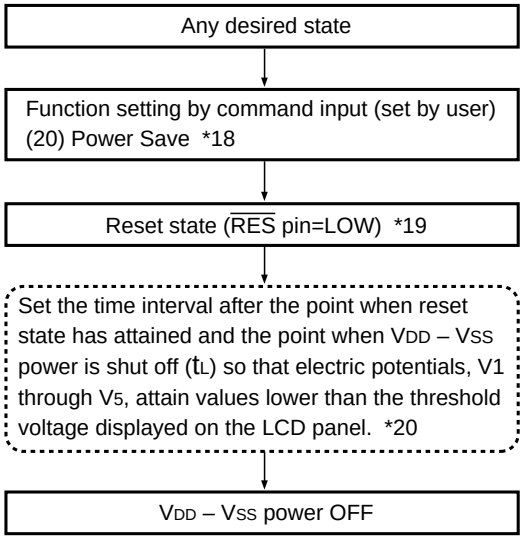
(3) Refresh *16



Notes: Reference items

*16: It is recommended that the operating modes and display contents be refreshed periodically to prevent the effect of unexpected noise.

(4) Power *17



Notes: Reference items

*17: This IC is a V_{DD} – V_{SS} power system circuit controlling the LCD driving circuit for the V_{DD} – V_5 power system. Shutting of power with voltage remaining in the V_{DD} – V_5 power system may cause uncontrolling voltage to be output from the SEG and COM pins. Follow the Power OFF sequence.

*18: 7. Command Description Item (20) "Power Saving"

*19: When external power supplies for driving LCD are used, turn all external power supplies off before entering reset state.
6. Function Description Item "Reset Circuit"

*20: The threshold voltage of the LCD panel is about 1 [V].
When the internal power supply circuit is used, discharge time t_H from the start of resetting to the voltage between V_{DD} and V_5 being reduced to 1 volt depends on capacitor C2 to be connected between V_1 – V_5 and V_{DD}. Figure 5 shows the reference values.

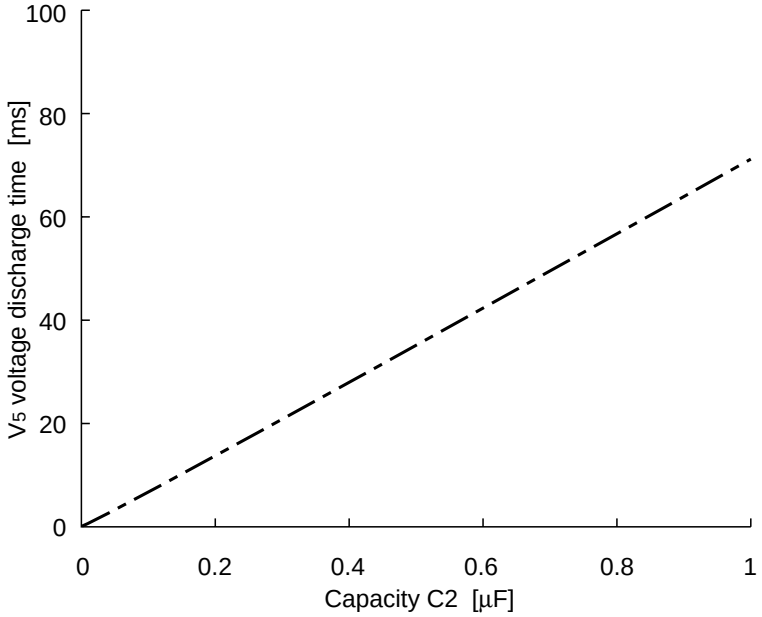


Figure 20

Set up t_L so that the relationship, $t_L > t_H$, is maintained. A state of $t_L < t_H$ may cause faulty display.

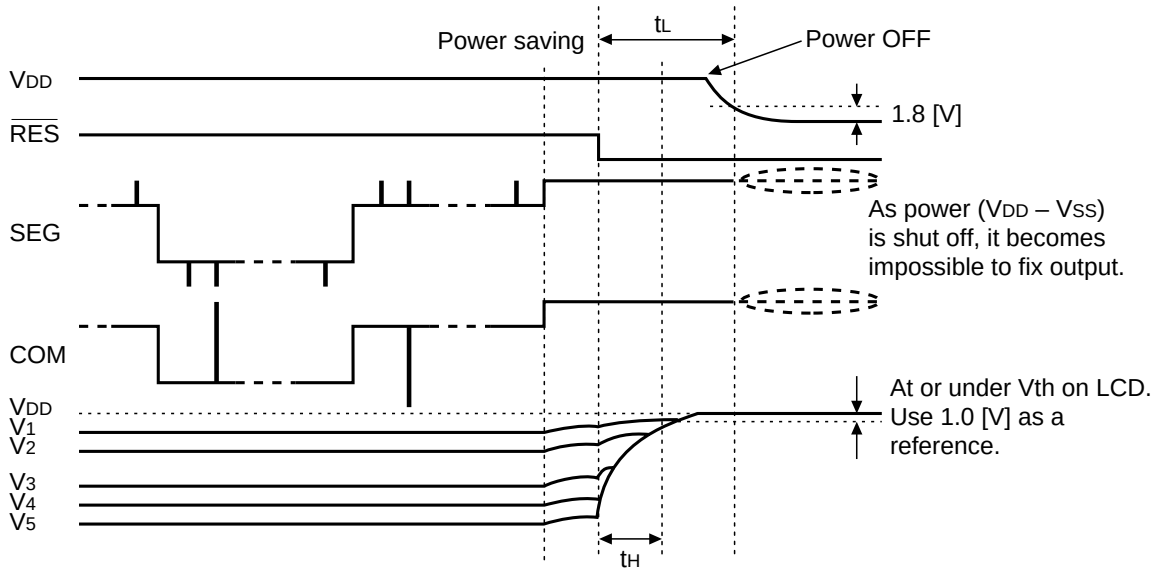
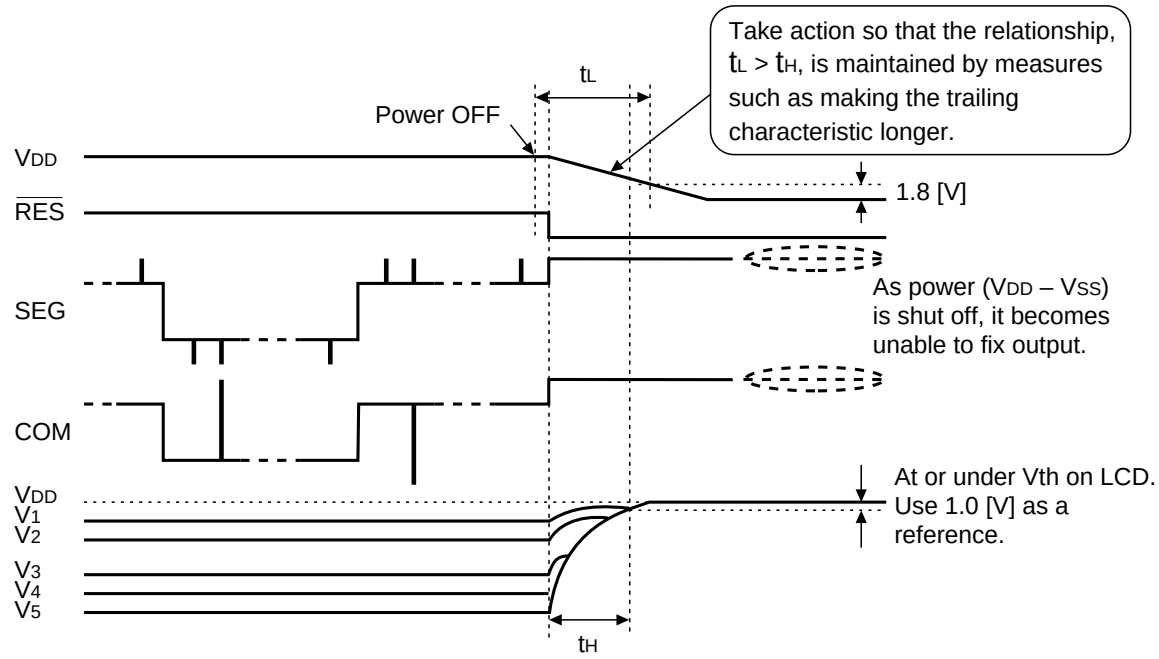


Figure 21



If command control is disabled when power is OFF, take action so that the relationship, $t_L > t_H$, is maintained by measures such as making the trailing characteristic of power ($V_{DD} – V_{SS}$) longer.

Figure 22

9. ABSOLUTE MAXIMUM RATINGS

Table 17

V_{SS}=0 V unless specified otherwise

Item		Symbol	Specification value			Unit
Power supply voltage		V_{DD}	–0.3	to	+7.0	V
Power supply voltage (2) (Based on V_{DD})		V_{SS2}	–7.0	to	+0.3	
	At triple boosting		–6.0	to	+0.3	
	At quadruple boosting		–4.5	to	+0.3	
Power supply voltage (3) (Based on V_{DD})		V_5, V_{OUT}	–22.0	to	+0.3	
Power supply voltage (4) (Based on V_{DD})		V_1, V_2, V_3, V_4	V_5	to	+0.3	
Input voltage		V_{IN}	–0.3	to	V_{DD}+0.3	
Output voltage		V_O	–0.3	to	V_{DD}+0.3	
Operating temperature		T_{OPR}	–40	to	+85	°C
Storage temperature	TCP	T_{STR}	–55	to	+100	
	Bare chip		–55	to	+125	

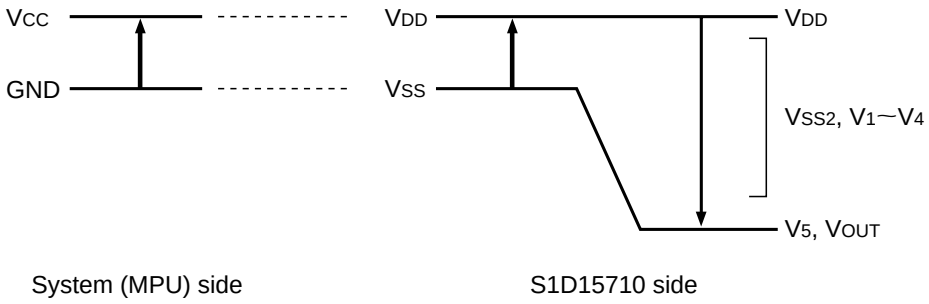


Figure 23

(Notes) 1. The values of the V_{SS2}, V_1 to V_5, and V_{OUT} voltages are based on V_{DD}=0 V.
2. The V_1, V_2, V_3, and V_4 voltages must always satisfy the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$.
3. Insure that voltage levels V_{SS2} and V_{OUT} are always such that the relationship of $V_{DD} \geq V_{SS} \geq V_{SS2} \geq V_{OUT}$ is maintained.
4. When LSI is used exceeding the absolute maximum ratings, the LSI may be damaged permanently. Besides, it is desirable that the LSI should be used in the electrical characteristics condition for normal operation. If this condition is exceeded, the LSI may malfunction and have an adverse effect on the reliability of the LSI.

10. DC CHARACTERISTICS

Table 18

V_{SS}=0 V, V_{DD}=3.0 V ± 10%, and Ta=–40 to 85°C

Item		Symbol	Condition		Specification value Min.	Typ.	Max.	Unit	Applicable pin
Operating voltage (1)	Recommended operation	V_{DD}			2.7	—	3.3	V	V_{DD} *1
	Operable	V_{DD}			1.8	—	5.5		V_{DD} *1
Operating voltage (2)	Recommended operation	V_{SS2}	(Based on V_{DD})		–3.3	—	–2.7		V_{SS2}
	Operable	V_{SS2}	(Based on V_{DD})		–6.0	—	–1.8		V_{SS2}
Operating voltage (3)	Operable	V_5	(Based on V_{DD})		–18.0	—	–4.5		V_5 *2
	Operable	V_1, V_2	(Based on V_{DD})		0.4×V_5	—	V_{DD}		V_1, V_2
	Operable	V_3, V_4	(Based on V_{DD})		V_5	—	0.6×V_5		V_3, V_4
High level input voltage		V_{IHC}			0.8×V_{DD}	—	V_{DD}		*3
Low level input voltage		V_{ILC}			V_{SS}	—	0.2×V_{DD}		*3
High level output voltage		V_{OHC}	I_{OH}=–0.5mA		0.8×V_{DD}	—	V_{DD}		*4
Low level output voltage		V_{OLC}	I_{OL}=0.5mA		V_{SS}	—	0.2×V_{DD}		*4
Input leak current		I_{LI}	V_{IN}=V_{DD} or V_{SS}		–1.0	—	1.0	µA	*5
Output leak current		I_{LO}			–3.0	—	3.0		*6
Liquid crystal driver On resistance		R_{ON}	Ta=25°C	V_5=–14.0V	—	2.0	3.5	kΩ	SEGn
			(Based on V_{DD})	V_5=–8.0V	—	3.2	5.4		COMn *7
Static current consumption		I_{SSQ}			—	0.01	5	µA	V_{SS}, V_{SS2}
Output leak current		I_{5Q}	V_5=–18.0V (Based on V_{DD})		—	0.01	15		V_5
Input pin capacity		C_{IN}	Ta=25°C, f=1MHz		—	5.0	8.0	pF	
Oscillating frequency	Built-in oscillation	f_{OSC}	Ta=25°C		18	22	26	kHz	*8
	External input	f_{CL}			4.5	5.5	6.5		CL *8

Table 19

Item		Symbol	Condition		Specification value Min.	Typ.	Max.	Unit	Applicable pin
Built-in power supply circuit	Input voltage	V_{SS2}	At triple boosting (Based on V_{DD})		–6.0	—	–1.8	V	V_{SS2}
		V_{SS2}	At quadruple boosting (Based on V_{DD})		–5.0	—	–1.8		V_{SS2}
	Boosting output voltage	V_{OUT}	(Based on V_{DD})		–20.0	—	—		V_{OUT}
	Voltage adjusting circuit operating voltage	V_{OUT}	(Based on V_{DD})		–20.0	—	–6.0		V_{OUT}
	V/F circuit operating voltage	V_5	(Based on V_{DD})		–18.0	—	–4.5		V_5 *9
	Reference voltage	V_{REG0}	Ta=25°C,	–0.05%/°C	–2.04	–2.10	–2.16		*10

[*: see Page 49.]

Dynamic current consumption value (1) During display operation and built-in power supply OFF
Current values dissipated by the whole IC when the external power supply is used

Table 20 Display All White — Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
S1D15710D00B* /D11B*	I_{DD} (1)	V_{DD}=5.0V, V_5–V_{DD}=–11.0V	—	25	42	µA	*11
		V_{DD}=3.0V, V_5–V_{DD}=–11.0V	—	25	42		

Table 21 Display Checker Pattern — Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
S1D15710D00B* /D11B*	I_{DD} (1)	V_{DD}=5.0V, V_5–V_{DD}=–11.0V	—	38	64	µA	*11
		V_{DD}=3.0V, V_5–V_{DD}=–11.0V	—	38	64		

Dynamic current consumption value (2) During display operation and built-in power supply ON
Current values dissipated by the whole IC containing the built-in power supply circuit

Table 22 Display All White — Ta=25°C

Item	Symbol	Condition		Specification value			Unit	Remarks
				Min.	Typ.	Max.		
S1D15710 D00B*/D11B*	I_{DD} (2)	V_{DD}=5.0V, Triple boosting	Normal mode	—	92	154	µA	*12
		V_5–V_{DD}=–11.0V	High power mode	—	242	405		
		V_{DD}=3.0V, Quadruple boosting	Normal mode	—	129	216		
		V_5–V_{DD}=–11.0V	High power mode	—	310	518		
S1D15710D10B*		V_{DD}=5.0V, Triple boosting	Normal mode	—	135	225		
		V_5–V_{DD}=–11.0V	High power mode	—	288	480		
		V_{DD}=3.0V, Quadruple boosting	Normal mode	—	176	294		
		V_5–V_{DD}=–11.0V	High power mode	—	363	605		

Table 23 Display Checker Pattern — Ta=25°C

Item	Symbol	Condition		Specification value			Unit	Remarks
				Min.	Typ.	Max.		
S1D15710 D00B*/D11B*	I_{DD} (2)	V_{DD}=5.0V, Triple boosting	Normal mode	—	132	221	µA	*12
		V_5–V_{DD}=–11.0V	High power mode	—	280	468		
		V_{DD}=3.0V, Quadruple boosting	Normal mode	—	167	279		
		V_5–V_{DD}=–11.0V	High power mode	—	350	585		
S1D15710D10B*		V_{DD}=5.0V, Triple boosting	Normal mode	—	178	297		
		V_5–V_{DD}=–11.0V	High power mode	—	330	550		
		V_{DD}=3.0V, Quadruple boosting	Normal mode	—	220	367		
		V_5–V_{DD}=–11.0V	High power mode	—	406	677		

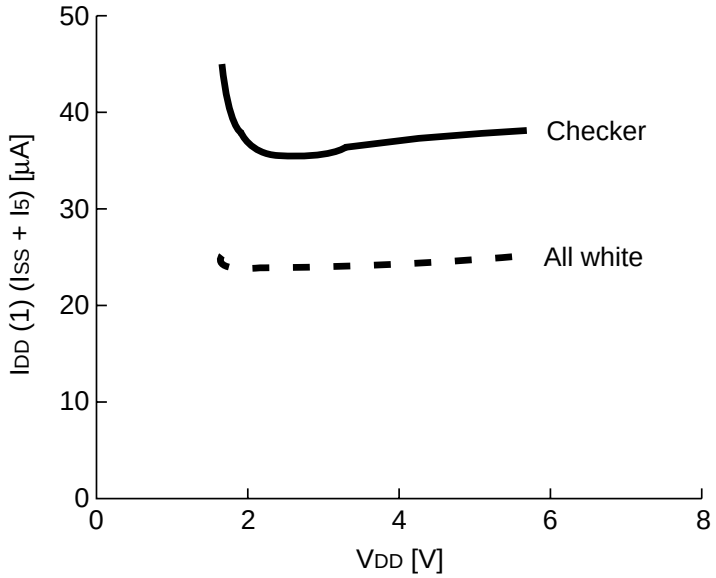
Current consumption at power save V_{SS}=0 V and V_{DD}=3.0 V ±10%

Table 24 — Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
Sleep state	I_{DDS1}		—	0.01	5	µA	
Stand-by state	I_{DDS2}		—	4	8		

[*: see Page 49.]

[Reference data 1]
• Dynamic current consumption (1) External power supply used and LCD being displayed

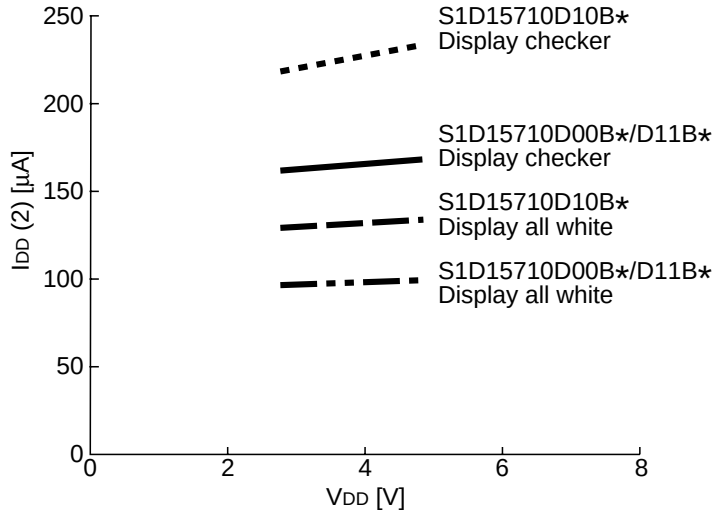


Condition: Built-in power supply OFF
External power supply used
$V_5 - V_{DD} = -11.0$ V
Display pattern: All white/ checker
Ta = 25°C

Remarks: *11

Figure 24

[Reference data 2]
• Dynamic current consumption (2) Built-in power supply used and LCD being displayed



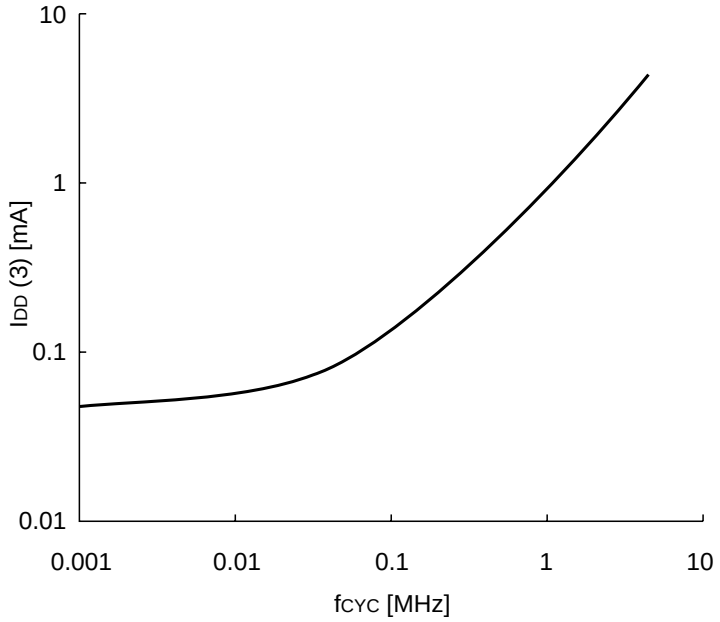
Condition: Built-in power supply ON
Quadruple boosting
$V_5 - V_{DD} = -11.0$ V
Normal mode
Display pattern: All white/ checker
Ta = 25°C

Remarks: *12

[*: see page 49.]

Figure 25

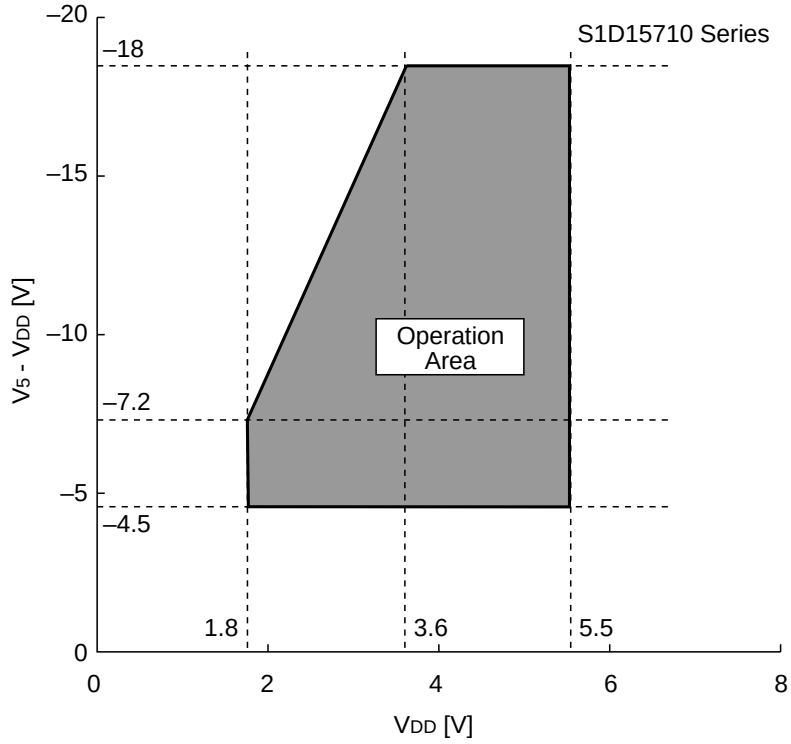
[Reference data 3]
• Dynamic current consumption (3) During access



Indicates the current consumption when the checker pattern is always written at fCYC.
Only IDD (1) when not accessed
Condition: Built-in power supply OFF and external power supply used
VDD – VSS = 3.0 V,
V5 – VDD = –11.0 V
Ta = 25°C

Figure 26

[Reference data 4]



VSS and V5 system operating voltage ranges

Remarks: *2

Figure 27

[*: see page 49.]

Relationships between the oscillating frequency fOSC, display clock frequency fCL, and liquid crystal frame frequency fFR

Table 25

Item	fCL	fFR
When built-in oscillator circuit used	$\frac{f_{OSC}}{4}$	$\frac{f_{OSC}}{4*65}$
When built-in oscillator circuit not used	External input (fCL)	$\frac{f_{CL}}{65}$

(fFR indicates the alternating current cycle of the liquid crystal and does not indicate that of the FR signal.)

[Reference items marked by *]

*1 The wide operating voltage range is not warranted. However, when there is a sudden voltage change during MPU access, it cannot be warranted.

*2 For the VDD and V5 operating voltage ranges, see Figure 27. These ranges are applied when using the external power supply.

*3 A0, D0 to D5, D6 (SCL), D7 (SI), $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, CL, FR, M/S, C86, P/S, $\overline{DOF}$, $\overline{RES}$, $\overline{IRS}$ and $\overline{HPM}$ pins

*4 D0 to D7, FR, FRS, $\overline{DOF}$ and CL pins

*5 A0, $\overline{RD}$ (E), $\overline{WR}$ (R/W), $\overline{CS1}$, CS2, CLS, M/S, C86, P/S, $\overline{RES}$, IRS and $\overline{HPM}$ pins

*6 Applied when D0 to D5, D6 (SCL), D7 (SI), CL, FR, and $\overline{DOF}$ pins are in the high impedance state

*7 Resistance value when the 0.1 V voltage is applied between the output pin SEGn or COMn and power supply pins (V1, V2, V3, and V4). Specified within the range of operating voltage (3)
RON = 0.1 V/ΔI (ΔI indicates the current applied when 0.1 V is applied between the power ON.)

*8 For the relationship between the oscillating frequency and frame frequency. The specification value of the external input item is a recommended value.

*9 The V5 voltage adjusting circuit is adjusted within the voltage follower operating voltage range.

*10 This is the internal voltage reference supply for the V5 voltage regulator circuit. The thermal slope VREG of the S1D15710 Series is about –0.05%/°C.

*11 and *12 Indicate the current dissipated by a single IC at built-in oscillator circuit used, 1/9 bias, and display ON.
Does not include the current due to the LCD panel capacity and wireing capacity.
Applicable only when there is no access from the MPU.

*12 When the V5 voltage adjusting built-in resistor is used

Timing Characteristics

System bus read/write characteristics 1 (80 series MPU)

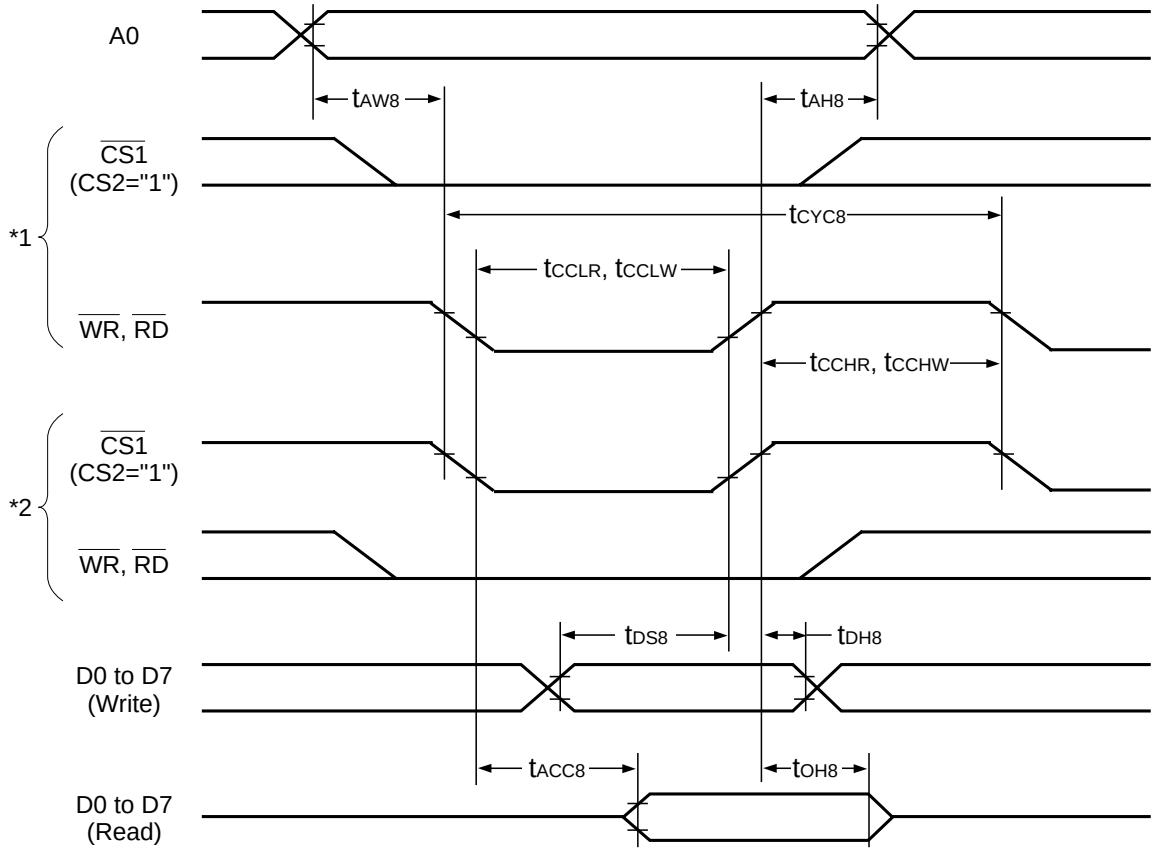


Figure 28

*1 is set when $\overline{CS}$ is LOW and access is made with $\overline{WR}$ and $\overline{RD}$.
*2 is used when $\overline{WR}$ and $\overline{RD}$ are LOW and accessed with $\overline{CS}$.

Table 26

[V_{DD}=4.5V to 5.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time	A0	t_{CYC8}		333	—	
Control LOW pulse width (Write)	$\overline{WR}$	t_{CCLW}		30	—	
Control LOW pulse width (Read)	$\overline{RD}$	t_{CCLR}		70	—	
Control HIGH pulse width (Write)	$\overline{WR}$	t_{CCHW}		30	—	
Control HIGH pulse width (Read)	$\overline{RD}$	t_{CCHR}		30	—	
Data setup time	D0 to D7	t_{DS8}		30	—	
Data hold time		t_{DH8}		10	—	
$\overline{RD}$ access time		t_{ACC8}	CL=100pF	—	70	
Output disable time		t_{OH8}		5	50	

Table 27

[V_{DD}=2.7V to 4.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time	A0	t_{CYC8}		500	—	
Control LOW pulse width (Write)	$\overline{WR}$	t_{CCLW}		60	—	
Control LOW pulse width (Read)	$\overline{RD}$	t_{CCLR}		120	—	
Control HIGH pulse width (Write)	$\overline{WR}$	t_{CCHW}		60	—	
Control HIGH pulse width (Read)	$\overline{RD}$	t_{CCHR}		60	—	
Data setup time	D0 to D7	t_{DS8}		40	—	
Data hold time		t_{DH8}		15	—	
$\overline{RD}$ access time		t_{ACC8}	CL=100pF	—	140	
Output disable time		t_{OH8}		10	100	

Table 28

[V_{DD}=1.8V to 2.7V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time	A0	t_{CYC8}		1000	—	
Control LOW pulse width (Write)	$\overline{WR}$	t_{CCLW}		120	—	
Control LOW pulse width (Read)	$\overline{RD}$	t_{CCLR}		240	—	
Control HIGH pulse width (Write)	$\overline{WR}$	t_{CCHW}		120	—	
Control HIGH pulse width (Read)	$\overline{RD}$	t_{CCHR}		120	—	
Data setup time	D0 to D7	t_{DS8}		80	—	
Data hold time		t_{DH8}		30	—	
$\overline{RD}$ access time		t_{ACC8}	CL=100pF	—	280	
Output disable time		t_{OH8}		10	200	

*1. This is the case of accessing by $\overline{WR}$ and $\overline{RD}$ when $\overline{CS1}$ = LOW.
*2. This is the case of accessing by $\overline{CS1}$ when $\overline{WR}$ and $\overline{RD}$ = LOW.
*3 The rise and fall times (t_r and t_f) of the input signal are specified for less than 15 ns. When using the system cycle time at high speed, they are specified for $(t_r+t_f) \leq (t_{CYC8}–t_{CCLW}–t_{CCHW})$ or $(t_r+t_f) \leq (t_{CYC8}–t_{CCLR}–t_{CCHR})$.
*4 All timings are specified based on the 20 and 80% of V_{DD}.
*5 t_{CCLW} and t_{CCLR} are specified for the overlap period when $\overline{CS1}$ is at LOW (CS2= HIGH) level and $\overline{WR}$, $\overline{RD}$ are at the LOW level.

System bus read/write characteristics 2 (68 series MPU)

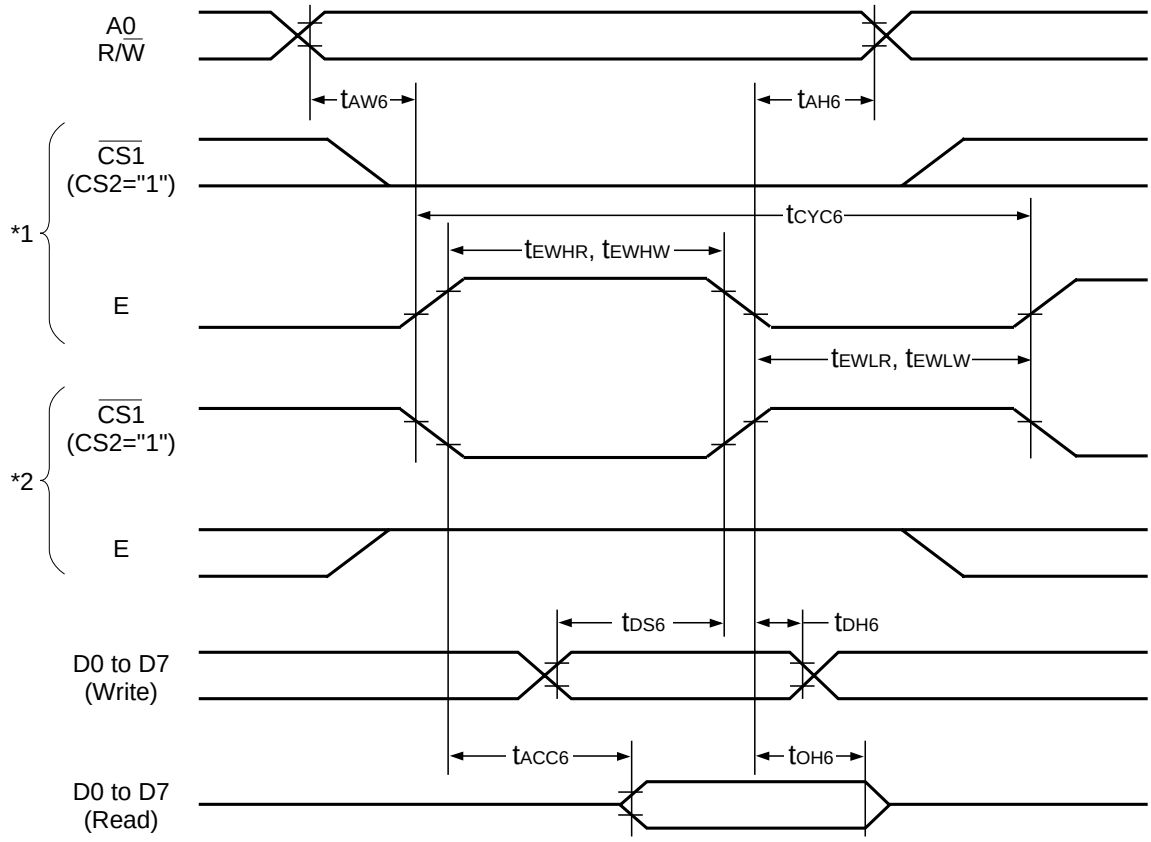


Figure 29

*1 is set when $\overline{CS}$ is LOW and access is made with E.
*2 is used when E is HIGH and access is made with $\overline{CS}$.

Table 29

[V_{DD}=4.5V to 5.5V, Ta=–40 to 85°C]

Item		Signal	Symbol	Condition	Specification value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		0	—	ns
Address setup time			t_{AW6}		0	—	
System cycle time			t_{CYC6}		333	—	
Data setup time		D0 to D7	t_{DS6}		30	—	
Data hold time			t_{DH6}		10	—	
Access time			t_{ACC6}	CL=100pF	—	70	
Output disable time			t_{OH6}		10	50	
Enable HIGH pulse width	Read	E	t_{EWHR}		70	—	
	Write		t_{EWHW}		30	—	
Enable LOW pulse width	Read	E	t_{EWLR}		30	—	
	Write		t_{EWLW}		30	—	

Table 30

[V_{DD}=2.7V to 4.5V, Ta=–40 to 85°C]

Item		Signal	Symbol	Condition	Specification value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		0	—	ns
Address setup time			t_{AW6}		0	—	
System cycle time			t_{CYC6}		500	—	
Data setup time		D0 to D7	t_{DS6}		40	—	
Data hold time			t_{DH6}		15	—	
Access time			t_{ACC6}	CL=100pF	—	140	
Output disable time			t_{OH6}		10	100	
Enable HIGH pulse width	Read	E	t_{EWHR}		120	—	
	Write		t_{EWHW}		60	—	
Enable LOW pulse width	Read	E	t_{EWLR}		60	—	
	Write		t_{EWLW}		60	—	

Table 31

[V_{DD}=1.8V to 2.7V, Ta=–40 to 85°C]

Item		Signal	Symbol	Condition	Specification value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		0	—	ns
Address setup time			t_{AW6}		0	—	
System cycle time			t_{CYC6}		1000	—	
Data setup time		D0 to D7	t_{DS6}		80	—	
Data hold time			t_{DH6}		30	—	
Access time			t_{ACC6}	CL=100pF	—	280	
Output disable time			t_{OH6}		10	200	
Enable HIGH pulse width	Read	E	t_{EWHR}		240	—	
	Write		t_{EWHW}		120	—	
Enable LOW pulse width	Read	E	t_{EWLR}		120	—	
	Write		t_{EWLW}		120	—	

*1 This is the case of accessing by E when $\overline{CS1}$ = LOW.
*2 This is the case of accessing by $\overline{CS1}$ when E = HIGH.
*3 The rise and fall times (t_r and t_f) of the input signal are specified for less than 15 ns. When using the system cycle time at high speed, they are specified for $(t_r+t_f) \leq (t_{CYC6}-t_{EWLW}-t_{EWHW})$ or $(t_r+t_f) \leq (t_{CYC6}-t_{EWLR}-t_{EWHR})$.
*4 All timings are specified based on the 20 and 80% of V_{DD}.
*5 t_{EWLW} and t_{EWLR} are specified for the overlap period when $\overline{CS1}$ is at LOW (CS2 = HIGH) level and E is at the HIGH level.

Serial interface

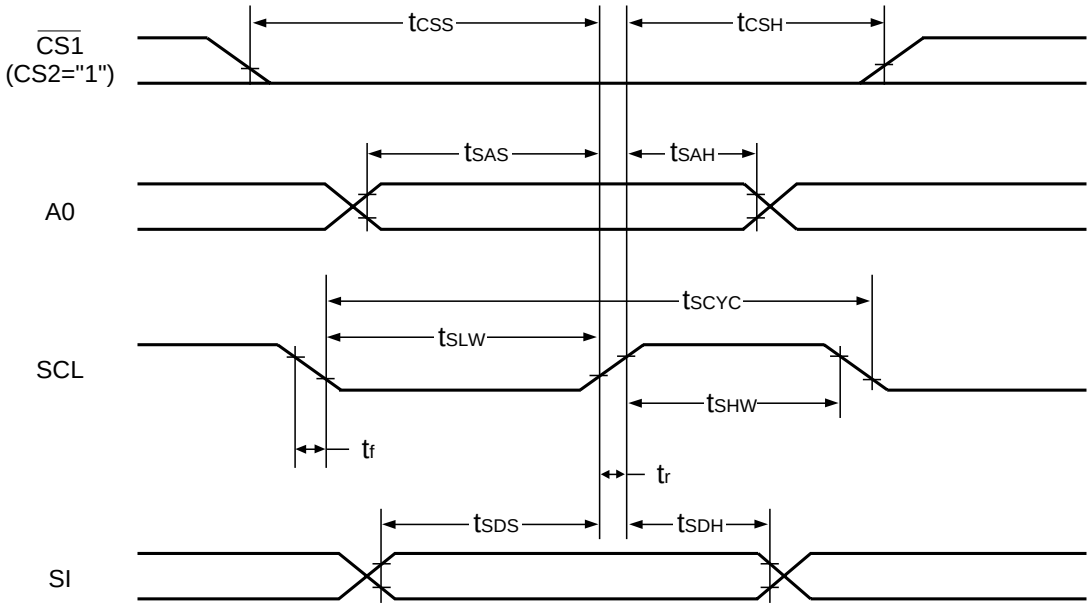


Figure 30

Table 32

[V_{DD}=4.5V to 5.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	t_{SCYC}		200	—	ns
SCL HIGH pulse width		t_{SHW}		75	—	
SCL LOW pulse width		t_{SLW}		75	—	
Address setup time	A0	t_{SAS}		50	—	
Address hold time		t_{SAH}		100	—	
Data setup time	SI	t_{SDS}		50	—	
Data hold time		t_{SDH}		50	—	
CS-SCL time	CS	t_{CSS}		100	—	
		t_{CSH}		100	—	

Table 33

[V_{DD}=2.7V to 4.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	t_{SCYC}		250	—	ns
SCL HIGH pulse width		t_{SHW}		100	—	
SCL LOW pulse width		t_{SLW}		100	—	
Address setup time	A0	t_{SAS}		150	—	
Address hold time		t_{SAH}		150	—	
Data setup time	SI	t_{SDS}		100	—	
Data hold time		t_{SDH}		100	—	
CS-SCL time	CS	t_{CSS}		150	—	
		t_{CSH}		150	—	

Table 34

[V_{DD}=1.8V to 2.7V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	t_{SCYC}		400	—	ns
SCL HIGH pulse width		t_{SHW}		150	—	
SCL LOW pulse width		t_{SLW}		150	—	
Address setup time	A0	t_{SAS}		250	—	
Address hold time		t_{SAH}		250	—	
Data setup time	SI	t_{SDS}		150	—	
Data hold time		t_{SDH}		150	—	
CS-SCL time	CS	t_{CSS}		250	—	
		t_{CSH}		250	—	

*1 The rise and fall times (tr and tf) of the input signal are specified for less than 15 ns.
*2 All timings are specified based on the 20 and 80% of V_{DD}.

Display control output timing

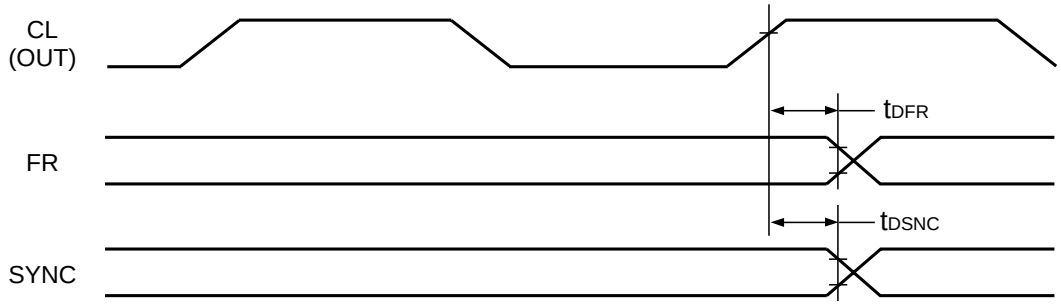


Figure 31

Table 35

[V_{DD}=4.5V to 5.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL=50pF	—	10	40	ns
SYNC delay time	SYNC	t_{DSNC}	CL=50pF	—	10	40	ns

Table 36

[V_{DD}=2.7V to 4.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL=50pF	—	20	80	ns
SYNC delay time	SYNC	t_{DSNC}	CL=50pF	—	20	80	ns

Table 37

[V_{DD}=1.8V to 2.7V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL=50pF	—	50	200	ns
SYNC delay time	SYNC	t_{DSNC}	CL=50pF	—	50	200	ns

*1 Valid only when the master mode is selected.
*2 All timings are specified based on the 20 and 80% of V_{DD}.
*3 Pay attention not to cause delays of the timing signals CL, FR and SYNC to the salve side by wiring resistance, etc., while master/slave operations are in progress. If these delays occur, indication failures such as flickering may occur.

Reset input timing

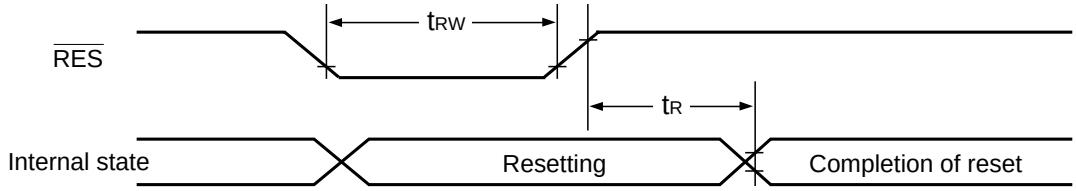


Figure 32

Table 38

[VDD=4.5V to 5.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		tR		—	—	0.5	µs
Reset LOW pulse width	$\overline{RES}$	tRW		0.5	—	—	

Table 39

[VDD=2.7V to 4.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		tR		—	—	1	µs
Reset LOW pulse width	$\overline{RES}$	tRW		1	—	—	

Table 40

[VDD=1.8V to 2.7V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		tR		—	—	1.5	µs
Reset LOW pulse width	$\overline{RES}$	tRW		1.5	—	—	

*1 All timings are specified based on the 20 and 80% of VDD.

11. MICROPROCESSOR (MPU) INTERFACE: REFERENCE

The S1D15710 series can directly be connected to the 80 system MPU and 68 series MUP. It can also be operated with a fewer signal lines by using the serial interface.
The S1D15710 series is used for the multiple chip configuration to expand the display area. In this case, it can select the ICs that are accessed individually using the Chip Select signal.
After the initialization using the $\overline{RES}$ pin, the respective input pins of the S1D15710 series need to be controlled normally.

80 series MPU

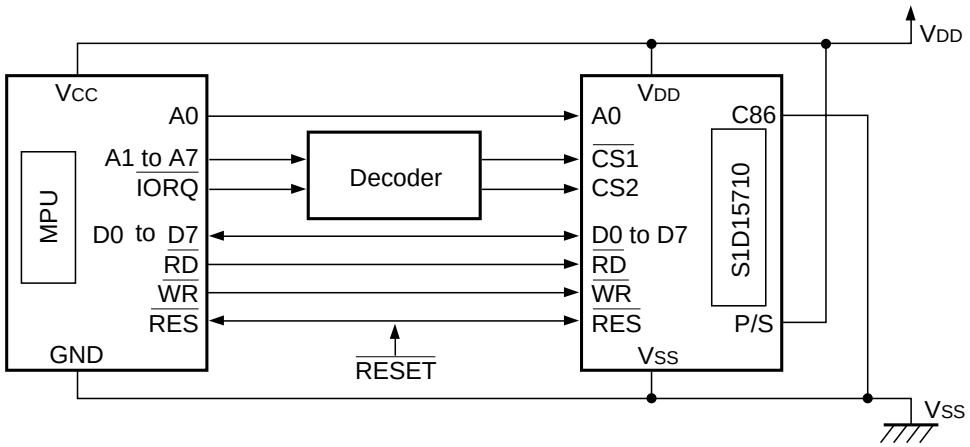


Figure 33-1

68 series MPU

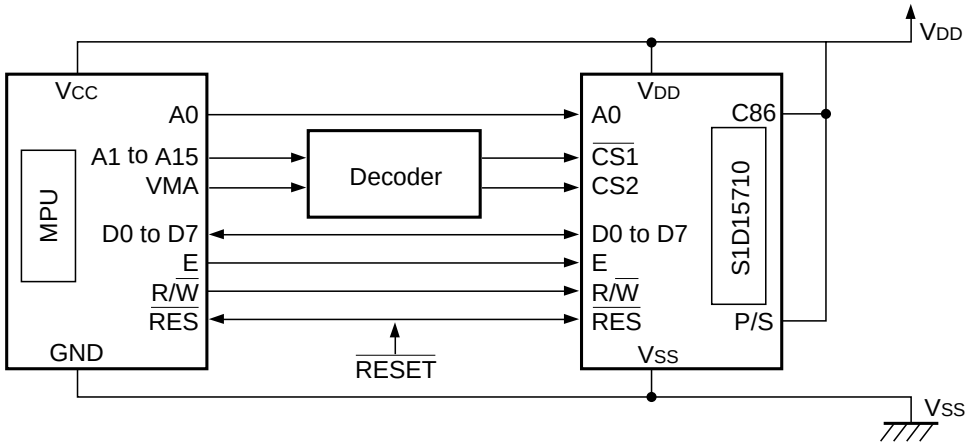


Figure 33-2

Serial interface

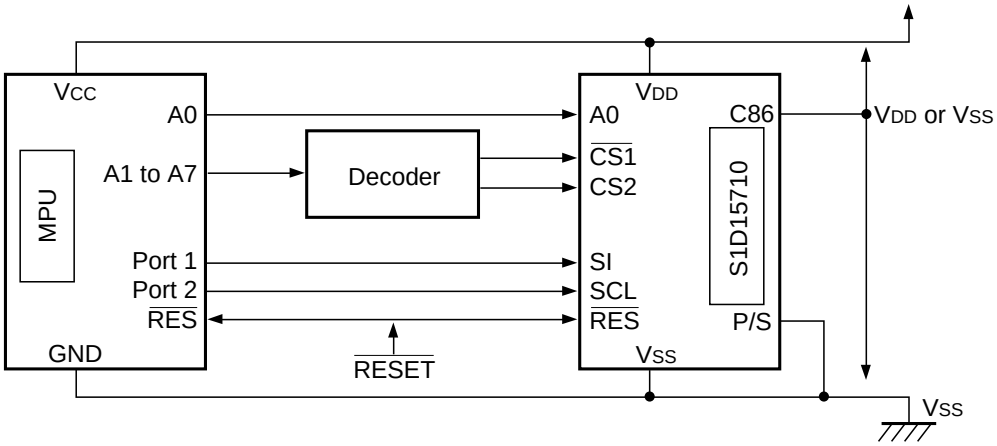


Figure 33-3

12. CONNECTION BETWEEN LCD DRIVERS: REFERENCE

The S1D15710 series is used for the multiple chip configuration to easily expand the liquid crystal display area. Use the same device (S1D15710*****/S1D15710*****) for the master/slave.

S1D15710 (master) ↔ S1D15710 (slave)

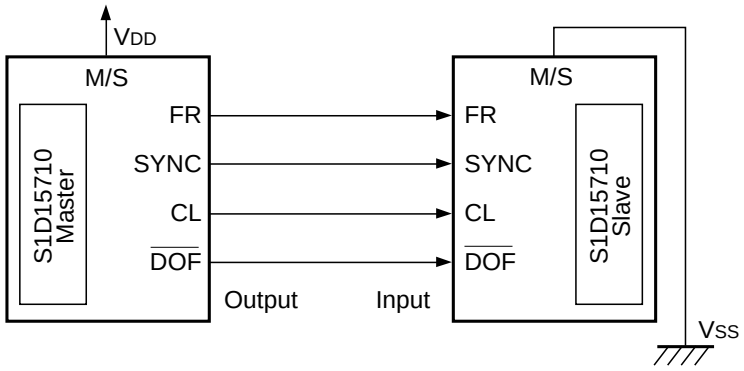


Figure 34

13. LCD PANEL WIRING: REFERENCE

The S1D15710 series is used for the multiple chip configuration to easily expand the liquid crystal display area. Use the same device (S1D15710*****/S1D15710*****) for the multiple chip configuration.

1-chip configuration

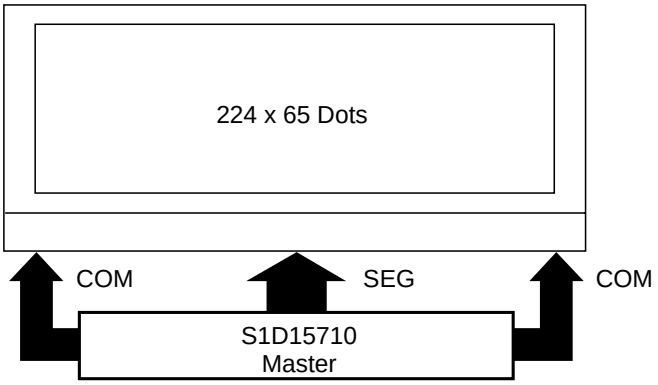


Figure 35-1

2-chip configuration

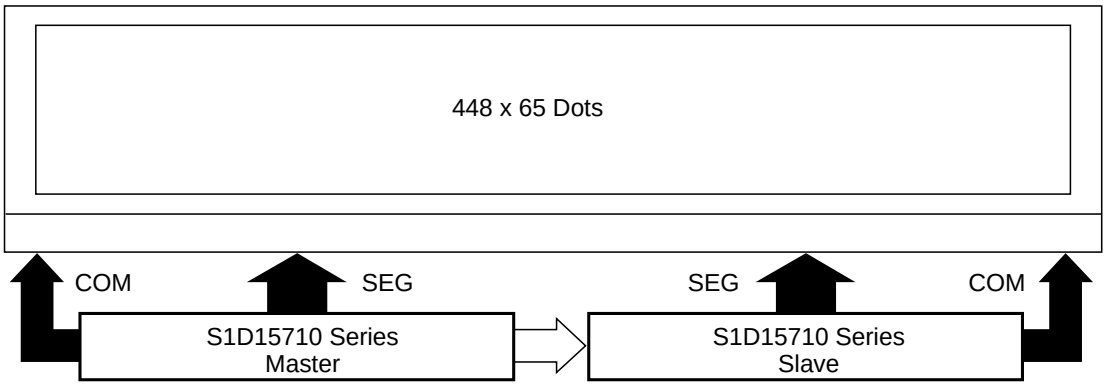
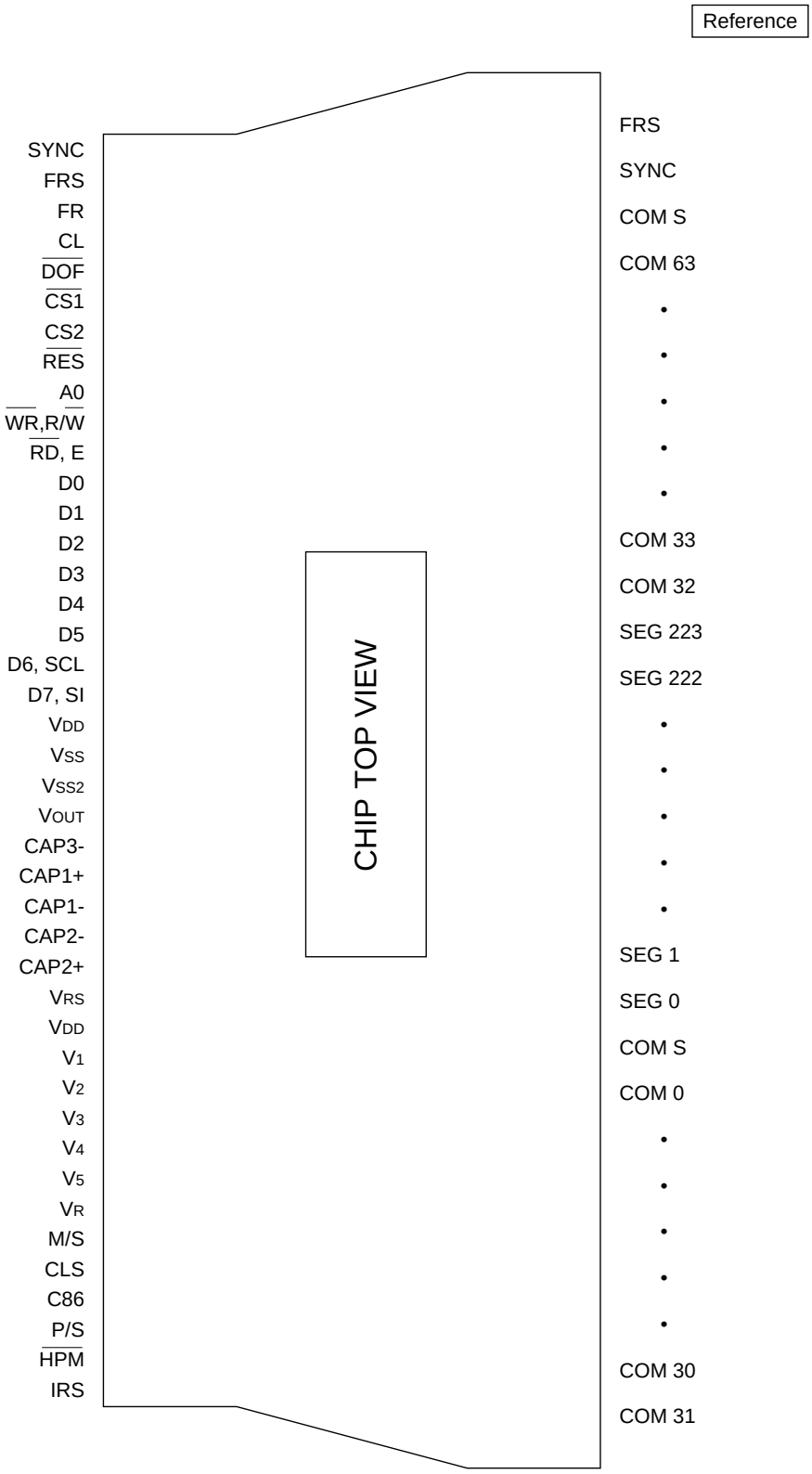


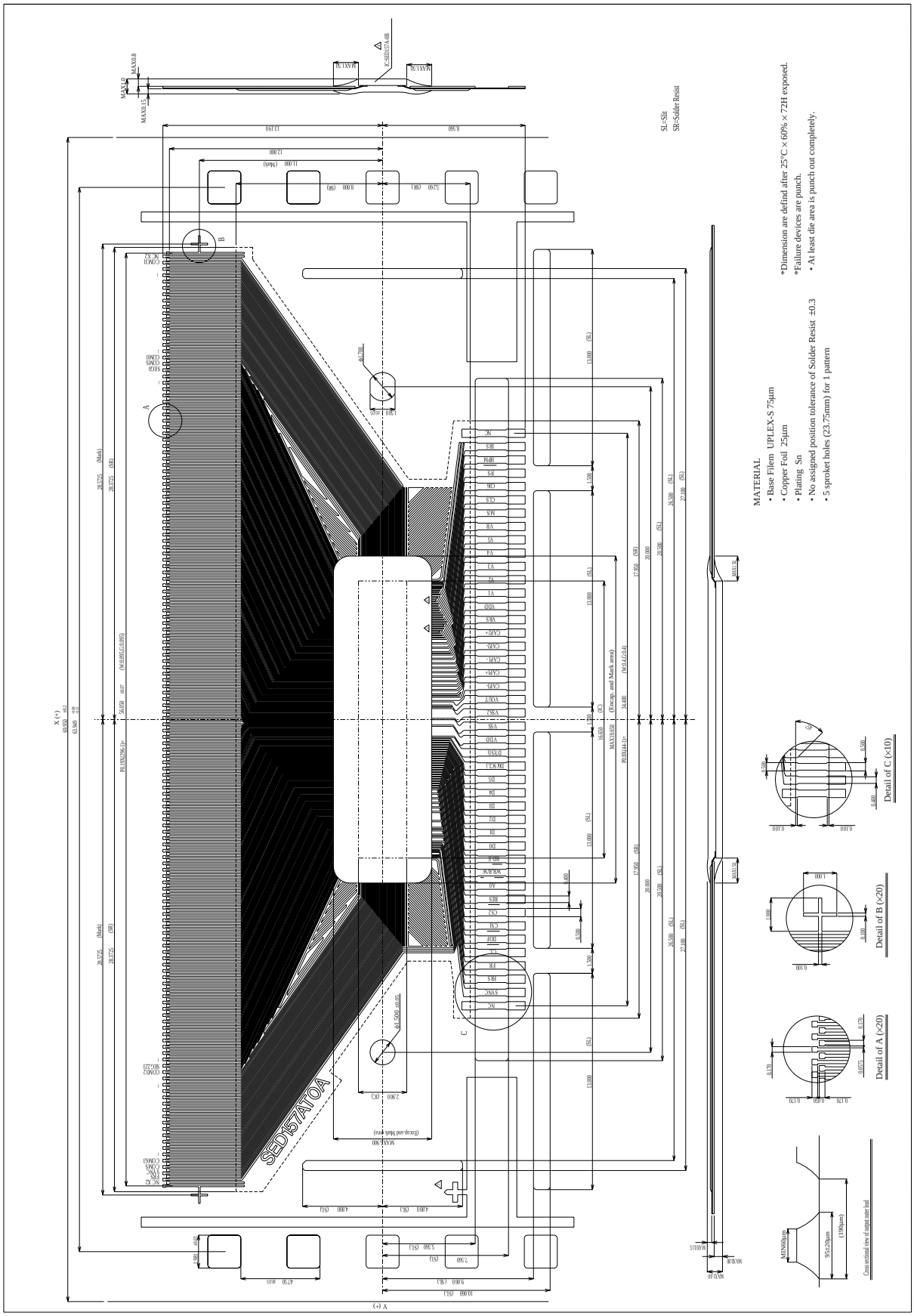
Figure 35-2

14. TCP PIN LAYOUT



Note) This TCP pin layout does not specify the TCP dimensions.

15. TCP DIMENSIONS



16. TEMPERATURE SENSOR CIRCUIT

Both the S1D15710∗10∗∗ and S1D15710∗11∗∗ have built-in temperature sensor circuits with analog voltage output terminals having a temperature gradient of 11.4mV/°C (Typ.). By controlling the liquid crystal drive voltage at V_5 by inputting an electric volume register value corresponding to the temperature sensor output value from the MPU enables liquid crystal to display appropriate light and shade over a wide range of temperatures.
Build a system to compensate for variations in the output voltage by feeding back the output voltage value sampled at a constant temperature to the MPU and store it as the standard voltage in order to achieve higher control of the liquid crystal drive voltage.

1. Terminal description

*Terminals related to the temperature sensor circuit are allocated to TEST 1 and 2, and are named V_{SEN1} for TEST1 and SVS1 for TEST2. Use the temperature sensor as indicated in the table below. When not in use, fix each terminal at HIGH.

Pin name	I/O	Description	Number of pins
SVS1	Power	Power terminal of the temperature sensor. Apply compulsory operation voltage to V_{DD}.	1
V_{SEN1}	O	Analog voltage output terminal of temperature sensor. Monitor the output voltage to V_{DD}.	1

2. Electrical characteristics

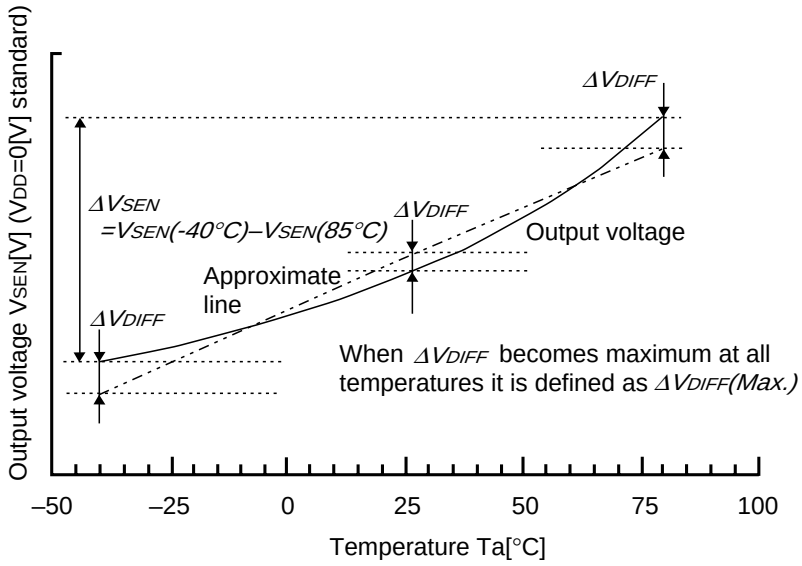
Item	Symbol	Condition	Specification value			Unit	Applicable PIN
			Min.	Typ.	Max.		
Operating voltage	SVS	(V_{DD} standard)	–5.5	–5.0	–4.5	V	SVS1
Output voltage	V_{SEN}	(V_{DD} standard) Ta=–40°C (V_{DD} standard) Ta=25°C (V_{DD} standard) Ta=85°C	–4.35 –3.48 –2.92	–3.62 –2.88 –2.20	–2.89 –2.28 –1.47	V	V_{SEN1}
Output voltage temperature gradient	V_{GRA}	*1	9.4	11.4	13.4	mV/°C	V_{SEN1}
Output voltage linearity	ΔVL	*2	–1.5	–	1.5	%	V_{SEN1}
Output voltage setup time	t_{SEN}	*3	100	–	–	mS	V_{SEN1}
Operating current	I_{SEN}	Ta=25°C	–	40	150	μA	SVS1

*Notes:

*1: Slope of approximate line of Typ. output voltage.

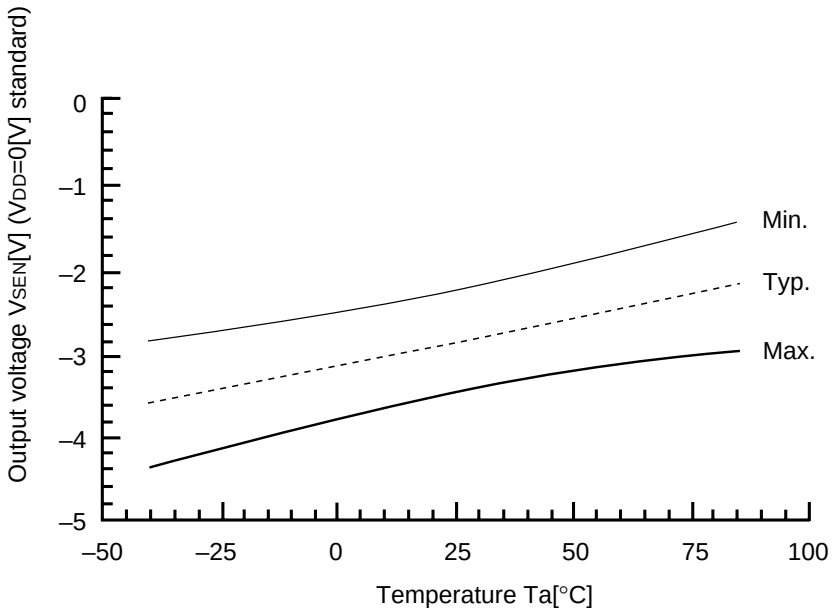
*2: Maximum deviation of output voltage curve and approximate line.
When the output voltage difference between –40°C and 85°C is ΔV_{SEN}, the difference between the approximate line and the output voltage value is ΔDIFF and the maximum value is ΔDIFF(Max.), output voltage linearity ΔV_L will be expressed using the following formula:

$$\Delta V_L = \frac{\Delta DIFF(Max.)}{\Delta V_{SEN}} \times 100$$



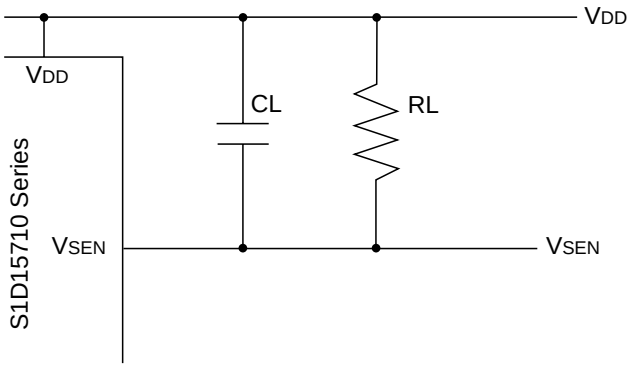
*3: Waiting time until monitoring is enabled with stable output voltage after applying power voltage SVS to terminal SVS1. The output voltage needs to be sampled after a longer than standard waiting time.

■ Output voltage characteristics



3. Output terminal load

Load capacity CL of VSEN output terminal VSEN1 should be under 100pF and load resistance RL higher than 1MΩ. Be careful not to build a current path between VSS in order to obtain an accurate output voltage value.



12. S1D15A06 Series

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1. DESCRIPTION

The S1D15A06 series is a single-chip liquid crystal display (=LCD) driver for dot-matrix LCDs that can be connected directly to a microprocessor (=MPU) bus. It accepts 8-bit parallel or serial display data from a MPU, stores it in an on-chip display data RAM (=DDRAM), and generates a LCD drive signal independent of the MPU clock.
The use of the on-chip DDRAM of 65×102 bits and a one-to-one correspondence between LCD panel pixel dots and on-chip DDRAM bits offer high flexibility in graphic display.
The S1D15A06 series does not need external operation clock for DDRAM read/write operations, and has a on-chip LCD power supply circuit featuring very low current consumption with few external components, and moreover has a on-chip CR oscillator circuit.
And the S1D15A06 does not need smoothing capacitor on the LCD power supply.
Consequently, the S1D15A06 series can be realize a high-performance handy display system with a minimum current consumption and the fewest components.

2. FEATURES

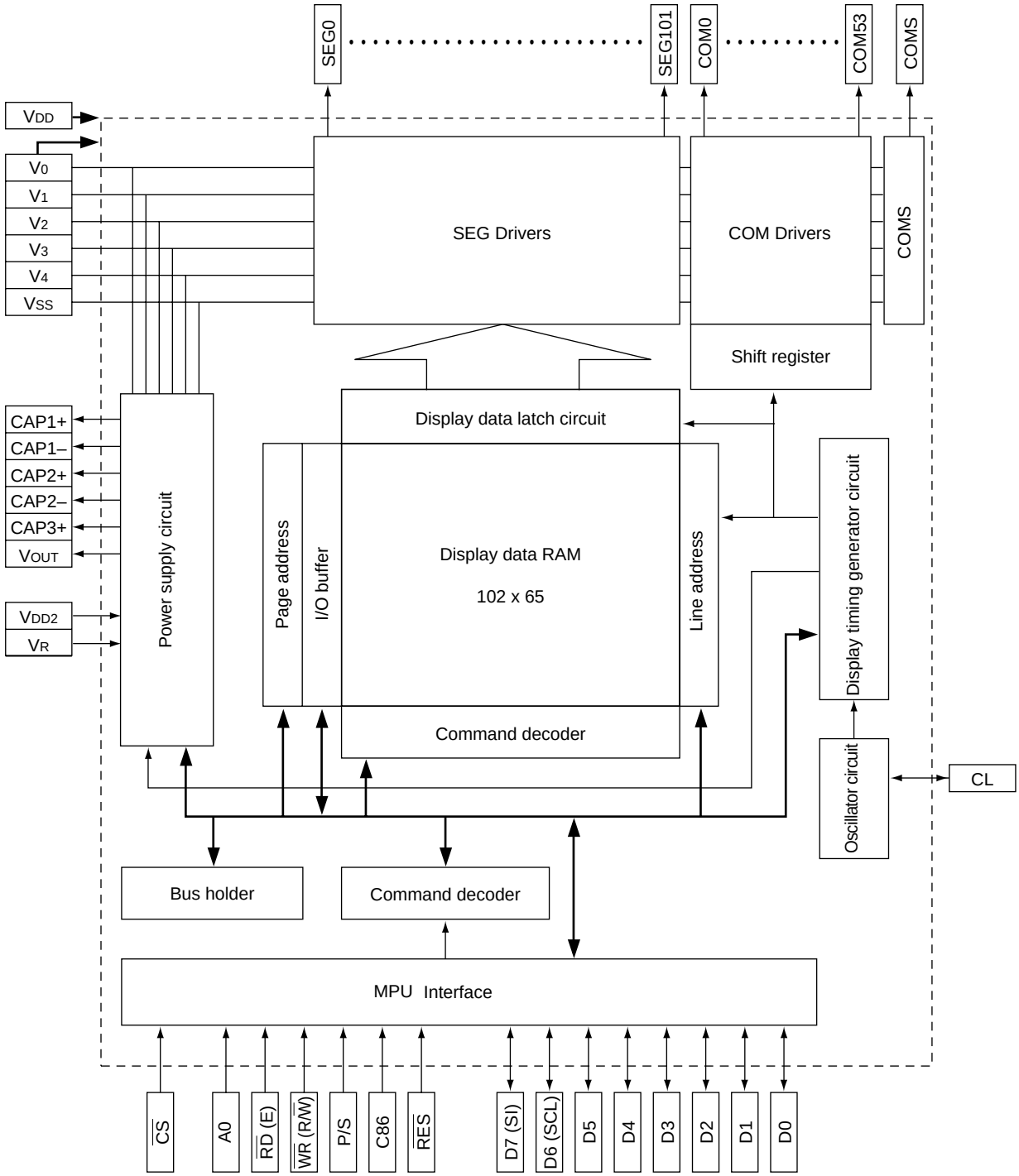
- Direct display of RAM data through the display data RAM.
- RAM bit data : "1" Non-illuminated
  "0" Illuminated
  (during normal display)
- RAM capacity 65×102 = 6630 bits
- Display driver circuits
  S1D15A06***** : 55 common output and 102 segment outputs
- High-speed 8-bit MPU interface(The chip can be connected directly to the 8080 series MPUs and the 6800 series MPUs)
- High-speed Serial interface are supported.
- Abundant command functions
  Display data Read/Write, display ON/OFF, Normal/Reverse display mode, page address set, display start line set, column address set, display all points ON/OFF, LCD bias set, electronic volume, read/modify/write, segment driver direction select, power saver, common driver direction select, V_0 voltage regulation internal resistor ratio set.
- Low-power liquid crystal display power supply circuit equipped internally.
  Booster circuit(with Boost ratios of Double/Triple/Quad, where the step-up voltage reference power supply can be input externally)
  - High-accuracy voltage adjustment circuit (Thermal gradient –0.1%/°C)
  - V_0 voltage divider resistors equipped internally, V_1 to V_4 voltage divider resistors equipped internally, electronic volume function equipped internally, voltage follower.
- Component that can be omitted (you may omit the smoothing capacitor on the voltage follower).
- CR oscillator circuit equipped internally(external clock can also be input)
- Extremely low power consumption
  Operating power when the built-in power supply is used(an example)
  S1D15A06D00B* (79μA)
  Condition : V_{DD}–V_{SS} = 1.8V, V_{DD2}–V_{SS} = 3.3V, V_0–V_{SS} = 9.0V, triple boosting, all white is displayed, Ta = 25°C
- Power supply
  Operable on the low 1.8 voltage
  Logic power supply : V_{DD}–V_{SS} = 1.8V to 3.6V
  Boost reference voltage : V_{DD2}–V_{SS} = 1.8V to 5.0V
  Liquid crystal drive power supply : V_0–V_{SS} = 4.5V to 9.0V
- Wide range of operating temperatures : -40 to +85°C
- CMOS process
- Shipping forms include bare chip and TCP.
- There chip not designed for resistance to light or resistance to radiation.

Series Specifications

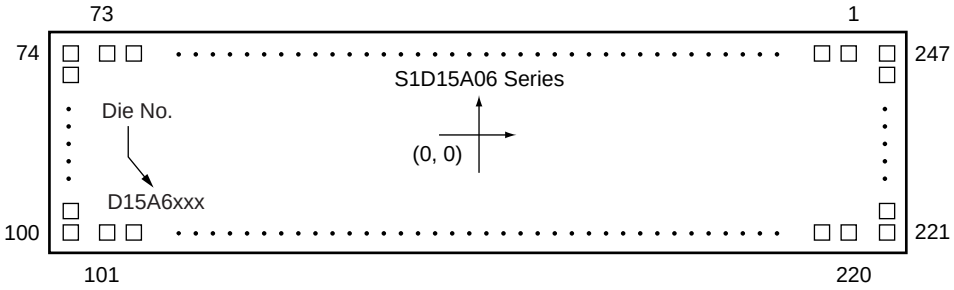
Product Name	Duty	Bias	SEG Dr	COM Dr	V_{REG} Temperature Gradient	Power supply specification	Shipping Forms
S1D15A06D00B*	1/55	1/6,1/8	102	55	–0.1%/°C	Built-in power supply is only used	Bare Chip
S1D15A06D01B	1/55	1/6,1/8	102	55	–0.1%/°C	V_0 or V_{OUT} External supply voltage follower is used	Bare Chip
S1D15A06D02B	1/55	1/6,1/8	102	55	–0.1%/°C	External power supply is only used	Bare Chip
*S1D15A06T00**	1/55	1/6,1/8	102	55	–0.1%/°C		TCP

* : Being planned

3. BLOCK DIAGRAM



4. PIN LAYOUT



		Size X	Size Y	Unit
Chip Size		9.93	2.15	mm
Chip Thickness		0.625		mm
Bump Pitch		70 (Min.)		µm
Bump Size	PAD No.1 to 73	85	85	µm
	PAD No.74	85	74	µm
	PAD No.75 to 99	85	45	µm
	PAD No.100	85	74	µm
	PAD No.101 to 220	52	85	µm
	PAD No.221	85	74	µm
	PAD No.222 to 246	85	45	µm
	PAD No.247	85	74	µm
Bump Height		17 (Typ.)		µm

S1D15A06***** Pad Center Coordinates

Units: μm

PAD No.	Pin Name	X	Y
1	(NC)	4570	921
2	TEST0	4449	
3	TEST1	4300	
4	V_{SS}	4151	
5	TEST2	4030	
6	TEST3	3910	
7	$\overline{RES}$	3789	
8	$\overline{CS}$	3668	
9	V_{SS}	3547	
10	$\overline{WR}$(R/$\overline{W}$)	3427	
11	$\overline{RD}$(E)	3306	
12	V_{DD}	3185	
13	CL	3065	
14	A0	2944	
15	D7(SI)	2823	
16	D6(SCL)	2703	
17	D5	2582	
18	D4	2461	
19	D3	2340	
20	D2	2220	
21	D1	2099	
22	D0	1978	
23	V_{DD}	1858	
24	V_{DD}	1737	
25	V_{DD}	1616	
26	V_{DD2}	1496	
27	V_{DD2}	1375	
28	V_{DD2}	1254	
29	V_{DD}	1133	
30	P/S	1013	
31	C86	892	
32	V_{SS}	771	
33	TEST4	651	
34	TEST5	474	
35	TEST6	297	
36	V_{SS}	120	
37	V_{SS}	0	
38	V_{SS}	–121	
39	TEST7	–298	
40	TEST8	–475	
41	TEST9	–652	
42	TEST10	–828	
43	V_{OUT}	–949	
44	V_{OUT}	–1070	
45	V_{OUT}	–1190	
46	V_{SS}	–1311	
47	V_R	–1432	
48	V_0	–1553	
49	V_1	–1673	
50	V_2	–1794	

PAD No.	Pin Name	X	Y
51	V_3	–1915	921
52	V_4	–2035	
53	CAP2+	–2156	
54	CAP2+	–2277	
55	(NC)	–2397	
56	(NC)	–2518	
57	(NC)	–2639	
58	(NC)	–2760	
59	(NC)	–2880	
60	CAP2–	–3001	
61	CAP2–	–3122	
62	(NC)	–3242	
63	(NC)	–3363	
64	(NC)	–3484	
65	(NC)	–3604	
66	CAP1+	–3725	
67	CAP1+	–3864	
68	CAP1–	–3967	
69	CAP1–	–4087	
70	CAP3+	–4208	
71	CAP3+	–4329	
72	V_{OUT}	–4449	
73	(NC)	–4570	
74	(NC)	–4808	926
75	COMS		842
76	COM26		771
77	COM25		701
78	COM24		631
79	COM23		561
80	COM22		491
81	COM21		421
82	COM20		351
83	COM19		281
84	COM18		210
85	COM17		140
86	COM16		70
87	COM15		0
88	COM14		–70
89	COM13		–140
90	COM12		–210
91	COM11		–281
92	COM10		–351
93	COM9		–421
94	COM8		–491
95	COM7		–561
96	COM6		–631
97	COM5		–701
98	COM4		–771
99	COM3		–842
100	(NC)		–926

PAD No.	Pin Name	X	Y
101	(NC)	–4623	–921
102	(NC)	–4545	
103	COM2	–4467	
104	COM1	–4389	
105	COM0	–4312	
106	(NC)	–4234	
107	(NC)	–4156	
108	(NC)	–4079	
109	(NC)	–4001	
110	SEG0	–3923	
111	SEG1	–3846	
112	SEG2	–3768	
113	SEG3	–3690	
114	SEG4	–3613	
115	SEG5	–3535	
116	SEG6	–3457	
117	SEG7	–3380	
118	SEG8	–3302	
119	SEG9	–3224	
120	SEG10	–3146	
121	SEG11	–3069	
122	SEG12	–2991	
123	SEG13	–2913	
124	SEG14	–2836	
125	SEG15	–2758	
126	SEG16	–2680	
127	SEG17	–2603	
128	SEG18	–2525	
129	SEG19	–2447	
130	SEG20	–2370	
131	SEG21	–2292	
132	SEG22	–2214	
133	SEG23	–2136	
134	SEG24	–2059	
135	SEG25	–1981	
136	SEG26	–1903	
137	SEG27	–1826	
138	SEG28	–1748	
139	SEG29	–1670	
140	SEG30	–1593	
141	SEG31	–1515	
142	SEG32	–1437	
143	SEG33	–1360	
144	SEG34	–1282	
145	SEG35	–1204	
146	SEG36	–1127	
147	SEG37	–1049	
148	SEG38	–971	
149	SEG39	–893	
150	SEG40	–816	

Units: µm

PAD No.	Pin Name	X	Y
151	SEG41	–738	–921
152	SEG42	–660	
153	SEG43	–583	
154	SEG44	–505	
155	SEG45	–427	
156	SEG46	–350	
157	SEG47	–272	
158	SEG48	–194	
159	SEG49	–117	
160	SEG50	–39	
161	SEG51	39	
162	SEG52	117	
163	SEG53	194	
164	SEG54	272	
165	SEG55	350	
166	SEG56	427	
167	SEG57	505	
168	SEG58	583	
169	SEG59	660	
170	SEG60	738	
171	SEG61	816	
172	SEG62	893	
173	SEG63	971	
174	SEG64	1049	
175	SEG65	1127	
176	SEG66	1204	
177	SEG67	1282	
178	SEG68	1360	
179	SEG69	1437	
180	SEG70	1515	
181	SEG71	1593	
182	SEG72	1670	
183	SEG73	1748	
184	SEG74	1826	
185	SEG75	1903	
186	SEG76	1981	
187	SEG77	2059	
188	SEG78	2136	
189	SEG79	2214	
190	SEG80	2292	
191	SEG81	2370	
192	SEG82	2447	
193	SEG83	2525	
194	SEG84	2603	
195	SEG85	2680	
196	SEG86	2758	
197	SEG87	2836	
198	SEG88	2913	
199	SEG89	2991	
200	SEG90	3069	

PAD No.	Pin Name	X	Y
201	SEG91	3146	–921
202	SEG92	3224	
203	SEG93	3302	
204	SEG94	3380	
205	SEG95	3457	
206	SEG96	3535	
207	SEG97	3613	
208	SEG98	3690	
209	SEG99	3768	
210	SEG100	3846	
211	SEG101	3923	
212	(NC)	4001	
213	(NC)	4079	
214	(NC)	4156	
215	(NC)	4234	
216	COM27	4312	
217	COM28	4389	
218	COM29	4467	
219	(NC)	4545	
220	(NC)	4623	
221	(NC)	4808	–926
222	COM30		–842
223	COM31		–771
224	COM32		–701
225	COM33		–631
226	COM34		–561
227	COM35		–491
228	COM36		–421
229	COM37		–351
230	COM38		–281
231	COM39		–210
232	COM40		–140
233	COM41		–70
234	COM42		0
235	COM43		70
236	COM44		140
237	COM45		210
238	COM46		281
239	COM47		351
240	COM48		421
241	COM49		491
242	COM50		561
243	COM51		631
244	COM52		701
245	COM53		771
246	COMS		842
247	(NC)		926

5. PIN DESCRIPTION

Power supply pins

Name	I/O	Description	Number of pins
V_{DD}	Supply	Power supply. Connect to MPU power pin V_{CC}.	5
V_{DD2}	Supply	Externally-input reference power supply for booster circuit.	3
V_{SS}	Supply	This is a 0V terminal connected to the system GND.	7
V_0, V_1, V_2 V_3, V_4	Supply	Multi-level power supply for LCD drive. The voltages are determined by LCD cell.The voltages should maintain the following relationship : $V_0 \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_{SS}$. When on-chip power supply circuit turns on, V_0 voltage are generated, and the following voltages are generated to V_1 to V_4. Either voltage can be selected by LCD bias set command. S1D15A06***** : V_1 = 5/6 • V_0, 7/8 • V_0; V_2 = 4/6 • V_0, 6/8 • V_0; V_3 = 2/6 • V_0, 2/8 • V_0; V_4 = 1/6 • V_0, 1/8 • V_0	5

LCD power supply circuit pins

Name	I/O	Description	Number of pins
CAP1+	O	Boosting capacitor positive connection pin. Capacitor is connected across CAP1- pins.	2
CAP1–	O	Boosting capacitor negative connection pin. Capacitor is connected across CAP1+ pins.	2
CAP2+	O	Boosting capacitor positive connection pin. Capacitor is connected across CAP2– pins.	2
CAP2–	O	Boosting capacitor negative connection pin. Capacitor is connected across CAP2+ pins.	2
CAP3+	O	Boosting capacitor positive connection pin. Capacitor is connected across CAP1– pins.	2
V_{OUT}	O	Booster output. Capacitor is connected across V_{SS} or V_{DD2}.	4
V_R	I	Voltage adjustment pin. Provides V_0 voltage using external resistors. When internal resistors are used, this pin cannot be used. Operable only when the built-in resistor for V_0 adjustment is not used. [V_0 resistance ratio is (D2, D1, D0) = (1.1.1)] This pin is disabled when the built-in resistor for V_0 adjustment is used. This pin must be open in this case.	1

System bus connection pins

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>D7 to D0
(SL)
(SCL)</td><td>I/O</td><td>8-bit bi-directional data bus to be connected to the standard 8-bit or 16-bit MPU data bus.
When the serial interface is selected (P/S=LOW) ;
D7 : Serial data input (SI)
D6 : Serial clock input (SCL)
At this time, D0 through D5 will go under the Hz mode.
When the chip selects are in non-active state, D0 through D7 will go under the Hz mode.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Control/data flag input.
A0=HIGH : The data on D7 to D0 is display data.
A0=LOW : The data on D7 to D0 is control data.</td><td>1</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>Chip select input. Data input is enable when $\overline{CS}$ is low.</td><td>1</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>When $\overline{RES}$ is caused to go low, initialization is executed.
A reset operation is performed at the signal level.</td><td>1</td></tr>
<tr><td>$\overline{RD}$
(E)</td><td>I</td><td>• When connected to an 8080-series MPU ;
This is active-LOW. This pin is connected to the $\overline{RD}$ signal of the 8080-series MPU. While this signal is low, S1D15A06 series data bus in an output status.
• When connected to an 6800-series MPU ;
This is active-HIGH. This is used as an enable clock input pin of the 6800-series MPU.</td><td>1</td></tr>
<tr><td>$\overline{WR}$
(R/$\overline{W}$)</td><td>I</td><td>• When connected to an 8080-series MPU ;
This is active-LOW. This pin is connected to the $\overline{WR}$ signal of the 8080-series MPU. The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal.
• When connected to an 6800-series MPU ;
This is the read/write control signal input .
R/$\overline{W}$=HIGH : Read.
R/$\overline{W}$=LOW : Write.</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>MPU interface selection pin.
C86=HIGH : 6800-series MPU interface
C86=LOW : 8080-series MPU interface</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>Serial data input/parallel data input selection pin.
P/S=HIGH : Parallel data input
P/S=LOW : Serial data input
The following applies depending on the P/S status :
<table>
<tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr>
<tr><td>HIGH</td><td>A0</td><td>D7 to D0</td><td>$\overline{RD}$, $\overline{WR}$</td><td>–</td></tr>
<tr><td>LOW</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr>
</table>
In serial mode, no data can be read from DDRAM.
When P/S=LOW,D5 to D0 are HZ. D5 to D0 may be HIGH, LOW or Open, and moreover A0, $\overline{RD}$, $\overline{WR}$, C86 may be HIGH or LOW.</td><td>1</td></tr>
</table>

LCD driver pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>CL</td><td>I</td><td>This pin is used for enabling or disabling the built-in oscillation circuit for the display clock.
CL = HIGH: Built-in oscillation circuit is enabled.
CL = LOW: Built-in oscillation circuit (external input) is disabled.
Select CL = LOW to turn the external clock off.
When using the built-in oscillation circuit, select CL = HIGH (V_{DD}).</td><td>1</td></tr>
<tr><td>SEG0
to SEG101</td><td>O</td><td>These pins output the signal for the segment drive of LCD.
One of V_0, V_2, V_3 and V_{SS} levels is selected depending on a given combination of display RAM data and internal FR signal.
<table>
<tr><th rowspan="2">RAM data</th><th rowspan="2">Internal FR signal</th><th colspan="2">Output voltage</th></tr>
<tr><th>Normal display</th><th>Reversing display</th></tr>
<tr><td>HIGH</td><td>HIGH</td><td>V_0</td><td>V_2</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>V_{SS}</td><td>V_3</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>V_2</td><td>V_0</td></tr>
<tr><td>LOW</td><td>LOW</td><td>V_3</td><td>V_{SS}</td></tr>
<tr><td>Power save</td><td>–</td><td colspan="2">V_{SS}</td></tr>
</table></td><td>102</td></tr>
<tr><td>COM0
to COM53</td><td>O</td><td>These pins output the signal for the common drive of LCD.
Following number of pins are assigned to S1D15A06*****.
<table>
<tr><th>Model</th><th>COM</th><th>Number of COM pins</th></tr>
<tr><td>S1D15A06*****</td><td>COM0~COM53</td><td>54</td></tr>
</table>
One of V_0, V_1, V_4 and V_{SS} levels is selected depending on a given combination of scan data and FR signal.
<table>
<tr><th>Scan data</th><th>FR</th><th>Output voltage</th></tr>
<tr><td>HIGH</td><td>HIGH</td><td>V_{SS}</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>V_0</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>V_1</td></tr>
<tr><td>LOW</td><td>LOW</td><td>V_4</td></tr>
<tr><td>Power save</td><td>–</td><td>V_{SS}</td></tr>
</table></td><td>54</td></tr>
<tr><td>COMS</td><td>O</td><td>They are COM pins exclusively used for the indicator.
Both pins output the same signal.
They must be made open when not used.</td><td>2</td></tr>
</table>

Test pins

Name	I/O	Description	Number of pins
TEST0 to 10	I/O	These are terminals for IC chip testing. They are set to OPEN.	11

Total : 220 pins for the S1D15A06*****.

Note and caution

• If control signal from MPU is Hz,an over-current may flow through the IC. A protection is required to prevent the Hz signal at the input pins.

6. FUNCTIONAL DESCRIPTION

Microprocessor Interface

Interface type selection

The S1D15A06 series can transfer data via 8-bit bi-directional data buses (D7 to D0) or via serial data input (SI). Through selecting the P/S pin polarity to the HIGH or LOW, it is possible to select either 8-bit parallel data input or serial data input as shown in Table 1.

Table 1

P/S	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
HIGH:Parallel Input	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
LOW:Serial Input	$\overline{CS}$	A0	–	–	–	SI	SCL	–

– : Must always be HIGH or LOW

Parallel interface

When the parallel interface has been selected (P/S =HIGH), then it is possible to connect directly to either an 8080-series MPU or a 6800-series MPU (as shown in Table 2) by selecting C86 pin to either HIGH or LOW.

Table 2

C86	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0
HIGH:6800-series MPU bus	$\overline{CS}$	A0	E	R/$\overline{W}$	D7 to D0
LOW:8080-series MPU bus	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0

Moreover, the S1D15A06 series identifies the data bus signal according to A0, $\overline{RD}$(E), $\overline{WR}$(R/$\overline{W}$)signals, as shown in Table 3.

Table 3

Common	6800-series	8080-series		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	1	1	0	Writes control data (command)

Serial interface

When the serial interface has been selected (P/S=LOW) then when the chip is in active state($\overline{CS}$=LOW) the serial data input (SI) and the serial clock input (SCL) can be received.

The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the eighth serial clock for the processing.

The A0 input is used to determine whether the serial data input is display data or command data; when A0=HIGH, the data is display data, and when A0=LOW then the data is command data.

The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active.

Figure 1 is a serial interface signal chart.

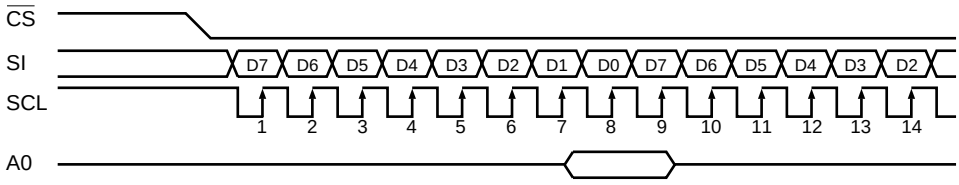


Figure 1

* When the chip is inactive, the shift register and the counter is reset to the initial state.
* Data read is not available as long as the serial interface is selected.
* Reasonable care must be exercised so that SCL signal may not be exposed undesirable effects resulting from, for instance, terminal reflection of wiring or external noises. Before using the signal, it is recommended to test the signal in actual system.

Chip select input

The MPU interface (either papallel or serial) is enabled only when $\overline{CS}$=LOW.
When the chip select is inactive, D7 to D0 enter a high impedance state, and A0, $\overline{RD}$ and $\overline{WR}$ inputs are disabled. When the serial interface is selected, the shift register and the counter are reset.

Access to DDRAM and internal registers

In accessing the DDRAM and the internal registers of the S1D15A06 series,the MPU is required to satisfy the only cycle time (t_{CYC}),and is not needed to consider the wait time. Accordingly, it is possible to transfer data at higher speed.
In order to realize the higher speed accessing, the S1D15A06 series can perform a type of pipeline processing between LSIs using bus holder of internal data bus when data is sent from/to the MPU. For example, when the MPU writes data to the DDRAM, once the data is stored in the bus holder, then it is written to the DDRAM before the next data write cycle. And when the MPU reads the contents of the DDRAM, the first data read cycle (dummy read cycle) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle. Thus,there is a certain restriction in the DDRAM read sequence. When an address is set, the specified address data is NOT output at the immediately following read instruction. The address data is output during second data read. A single dummy read must be inserted after address setup and after write cycle (refer to Figure 2).

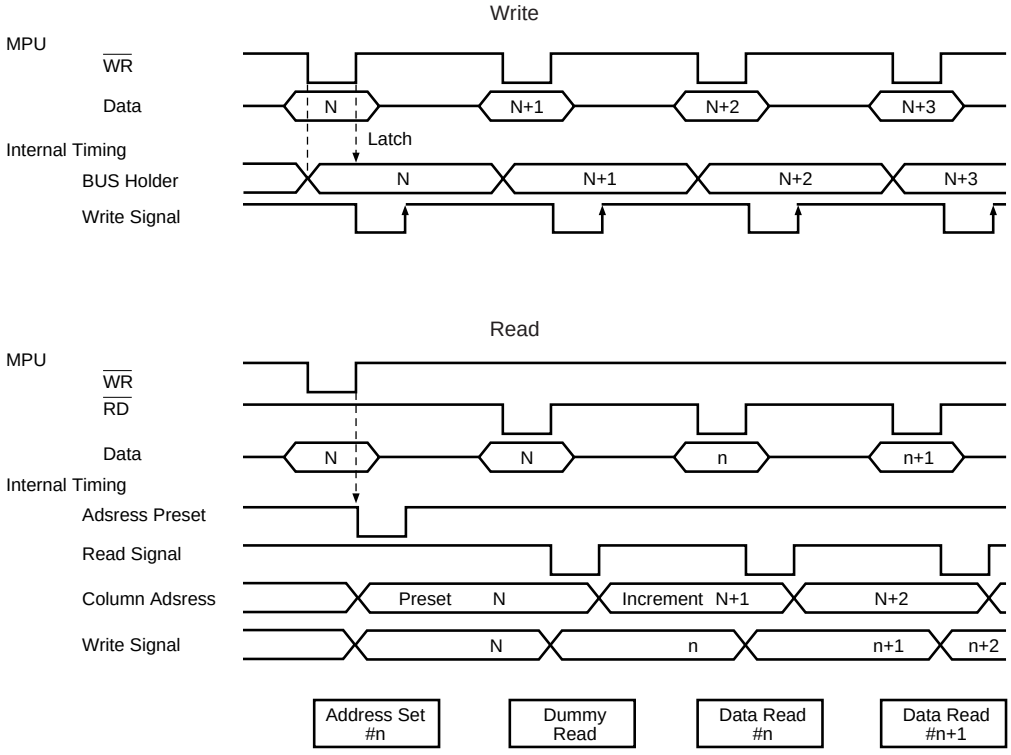


Figure 2

DDRAM

DDRAM and page/column address circuit

The DDRAM stores pixel data for LCD. It is a 65-row (8 page by 8 bit + 1) by 102-column addressable array. As is shown in Figure 3, the D7 to D0 display data from the MPU corresponds to the LCD common direction. Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).

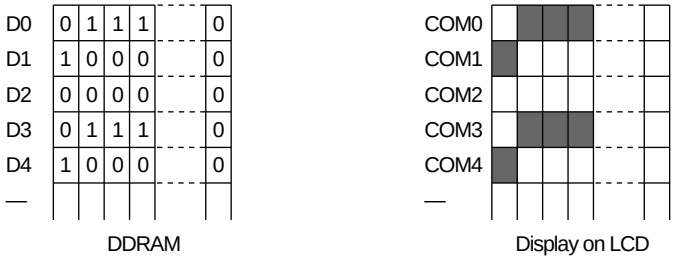


Figure 3

Page address circuit

Each pixel can be selected when page address and column address are specified(refer to Figure 5).
The MPU issues Page address set command to change the page and access to another page. Page address 8 (D3,D2,D1,D0 = 1,0,0,0) is DDRAM area dedicate to the indicator, and display data D0 is only valid.
The DDRAM column address is specified by Column address set command.The specified column address is automatically incremented by +1 when a Display data read/write command is entered. After the last column address (65H) ,column address returns to 00H and page address incremented by +1 (refer to Figure 4). After the very last address (column = 65H,page = 7H),both column address and page address return to 00H (column address = 00H, page address = 0H).

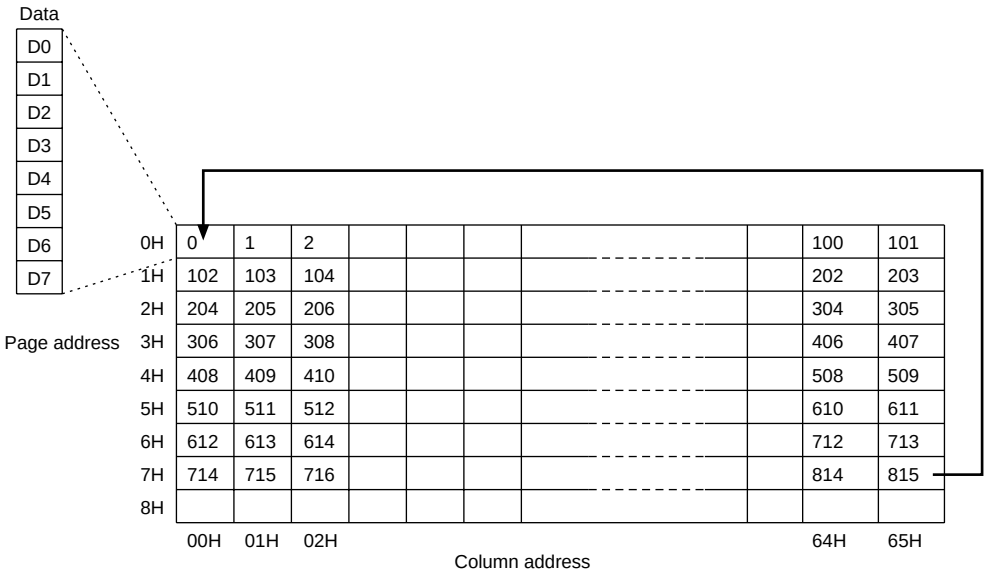


Figure 4

Column address circuit

Designate the column side address of the indication data RAM as shown in Fig. 5, using the column address setting command. Since the designated column address increments (+1) each time an indication data•read/write command is input, the MPU can make access to the indication data in succession.
Also, as shown in Fig. 4, after an access has been made to the final column address (65H), the column address will return to (00H) and the page address will be automatically incremented (by +1). Thanks to this feature, it is possible to write continuous data being divided between adjoining pages. Furthermore, after accesses have been made to the final addresses of both of the page and column (column = 65H and page = 7H), both of the column address and the page address returns to (00H).
(The page will not increment to "8H". Therefore, be careful when executing "read•modify•write" processes.)
Also, as shown in Table 4, the correlation between the column address of the indication data RAM and the segment output can be reversed by use of the ADC command (segment driver direction select command). Thanks to this feature, IC layout limitations when constituting an LCD module can be lessened.

Table 4

Column Address	00H	01H	02H		63H	64H	65H
Normal Direction	SEG0	SEG1	SEG2		SEG99	SEG100	SEG101
Reverse Direction	SEG101	SEG100	SEG99		SEG2	SEG1	SEG0

Line address circuit

The line address circuit specifies the line address (as shown Figure 5) relating to the COM output when the contents of the DDRAM are displayed. The display start line address, what is normally the top line of the display, can be specified by Display start line address set command. And Common driver direction select command can be used to reverse the relationship between the DDRAM line address and common output. For example, as is shown in Table 5, the display start line address corresponds to the COM0 output when the common driver direction is normal, or the COM53 output when common driver direction is reversed.And the display area is followed by the higher number line addresses in ascending order from the display start line address, corresponding to the duty cycle. This allows flexible IC layout during LCD module assembly.
If the display start line address is changed dynamically using the Display start line address set command,then screen scrolling and page swapping can be performed.

Table 5 (at display start line address=1CH)

Line Address	1CH	1DH		3FH	00H		11H	12H
Normal Direction	COM0	COM1		COM35	COM36		COM52	COM53
Reverse Direction	COM53	COM52		COM18	COM17		COM1	COM0

Display data latch circuit

The display data latch circuit is a latch temporarily stored the display data that is output to the LCD driver circuit from the DDRAM.
Display ON/OFF command, Display normal/reverse command, and Displayd all points ON/OFF command control only the data within the latch,and do not change the data within the DDRAM.

Display data RAM

The display data RAM stores pixel data for the LCD. It is a 102-column × 65-row addressable array as shown in Figure 5.

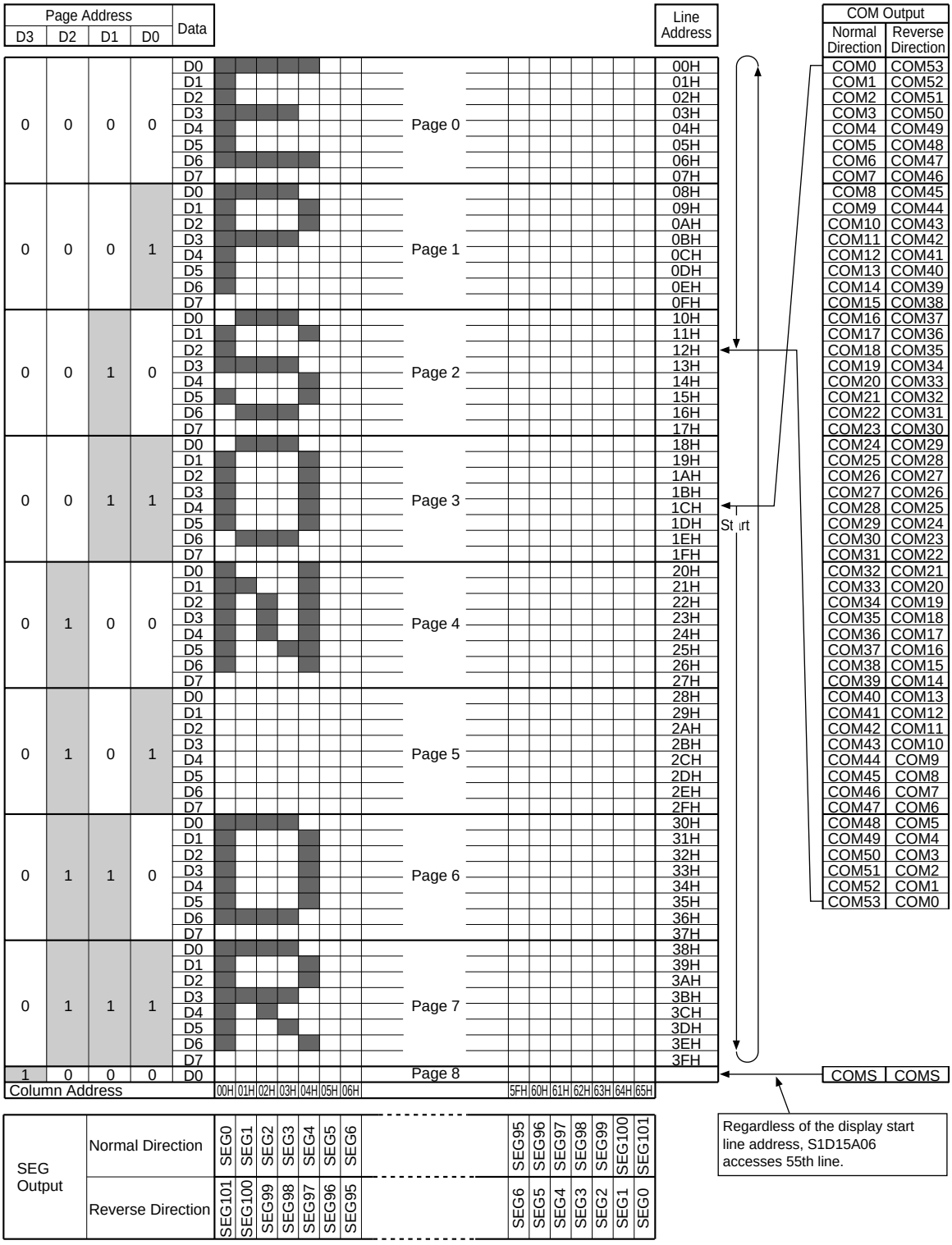


Figure 5

Oscillation circuit

The S1D15A06 series generates display clocks using its built-in CR oscillation circuit. The built-in oscillation circuit is enabled when CL = HIGH is selected and the power save mode is turned off.

You can stop operation of the CR oscillation circuit by selecting CL = LOW. Display clock can be externally entered via CL pin (when external clock is turned off, CL pin must be placed in LOW).

Table 6

CL	Operation
HIGH	Built-in CR oscillation circuit is enabled.
LOW	Built-in CR oscillation circuit is turned off [display clock is turned off].
Clock input	External clock input mode

Table 7 shows relationship between frequency of external clock (f_{CL}), frequency of built-in clock circuit (f_{OSC}) and f_{FR}.

Since CL pin is used for resetting the built-in CR clock circuit, it must satisfy the f_{CL} requirements given in the "DC Characteristics".

Table 7

Item		f_{FR} computation formula
S1D15A06*****	When built-in oscillation circuit is used	$f_{FR}=f_{OSC}$ / (55×8) [Hz]
	When external clock input is used	$f_{FR}=f_{CL}$ / (55×16) [Hz]

Display timing generator circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit, and generates COM scan signal and the LCD AC signal (dual-frame AC driver waveform).

LCD driver circuits

These are multiplexers outputting the LCD panel driving 4-level signal which level is determined by a combination of display data, COM scan signal, and LCD AC signal (FR). Figure 6 shows an example of SEG and COM output waveforms.

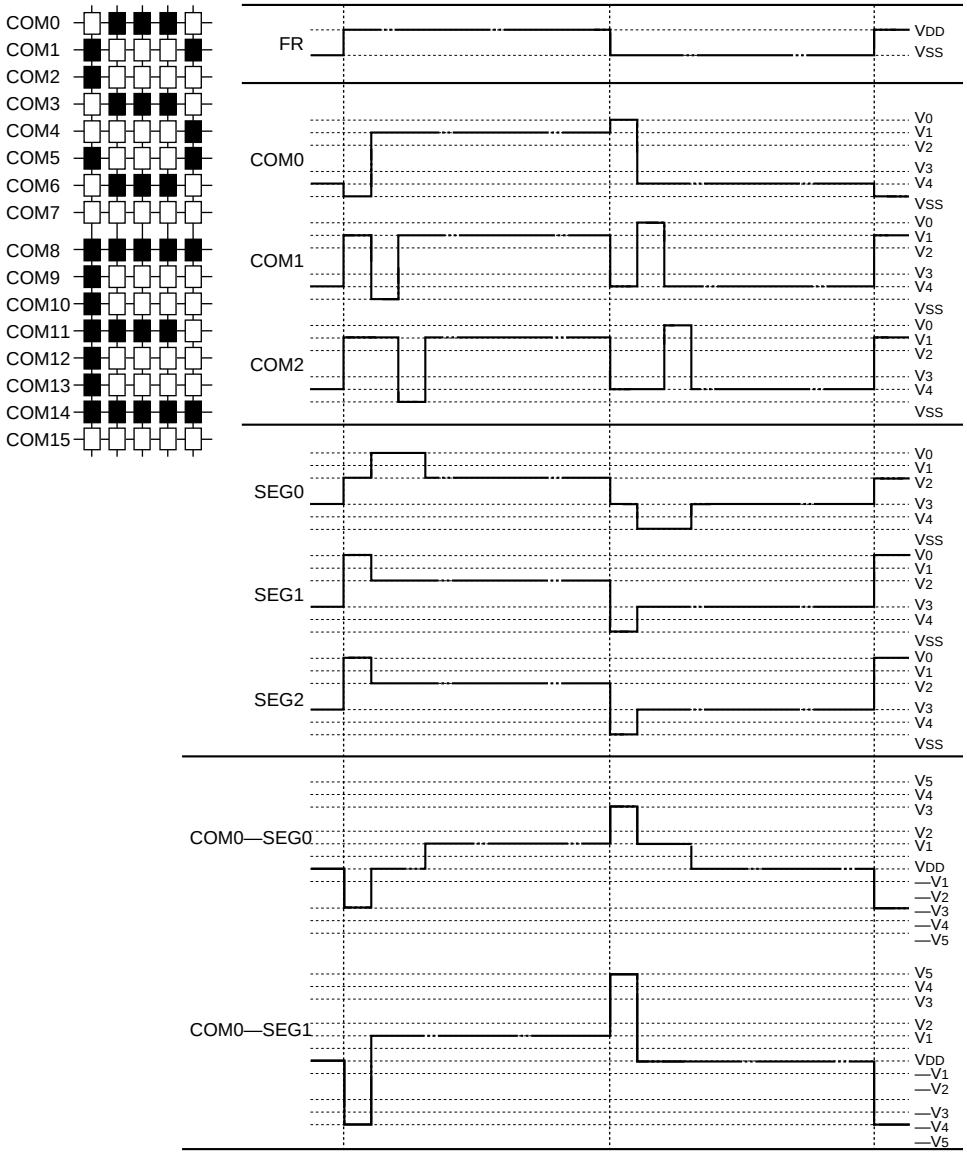

COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15
FR
VDD
VSS
COM0
COM1
COM2
V0
V1
V2
V3
V4
VSS
SEG0
SEG1
SEG2
V5
COM0—SEG0
COM0—SEG1
—V1
—V2
—V3
—V4
—V5

Figure 6

Power supply circuit

The power supply circuit generates the voltage to drive the LCD panel at low power consumption.
The power supply circuit consists of a booster circuit, voltage regulator circuit, and voltage follower circuit, and is controlled by Power control set command. Using this command, the booster circuit, the voltage regulator circuit, and the voltage follower circuit can be independently turned ON or OFF. Consequently, the external power supply and part of internal power supply circuit functions can be used simultaneously. Table 8 shows reference combinations.
Table 8 lists the functions controllable from 3 bits data of the power control set command. And, Table 9 shows sample combinations of the bits.
Select the models depending on the state of use.

Table 8

Item	State	
	"1"	"0"
D2 Booster circuit control bit	ON	OFF
D1 Voltage adjusting circuit (V adjusting circuit) control bit	ON	OFF
D0 Voltage follower circuit (V/F circuit) control bit	ON	OFF

Table 9

Usage	Model	D2	D1	D0	Booster circuit.	V adjusting circuit.	V/F circuit.	External voltage entered.	Pins on booster circuit
Built-in power supply alone is used	*1	1	1	1	ON	ON	ON	V_{DD2}	Used
V adjusting and	*2	0	1	1	OFF	ON	ON	V_{OUT} *4	OPEN
V/F circuits alone are used V/F circuit alone is used	*2	0	0	1	OFF	OFF	ON	V_0 *4	OPEN
External power supply alone is used	*3	0	0	0	OFF	OFF	OFF	V_0 to V_4 *4	OPEN

* Pins on the booster circuits denote CAP1+, CAP1–, CAP2+, CAP2– and CAP3+ pins.
* Although other combinations than the above are available, they are not pragmatic and thus not recommendable.
*1: S1D15A06D00B∗ *2: S1D15A06D01B∗ *3: S1D15A06D02B∗
*4: V_{DD2} is recommended to short-circuit to V_{DD}

Booster circuit

Using the booster circuit, it is possible to produce Quad/Triple/Double boosting of the V_{DD2}–V_{SS} voltage level.
Quad boosting : If capacitor are inserted between CAP1+ and CAP1-, between CAP2+ and CAP2-, between CAP3+ and CAP1-, between V_{OUT} and V_{DD2}, the potential between V_{DD2} and V_{SS} is boosted to quadruple toward the positive side and it is output at V_{OUT} pin.
Triple boosting : If capacitor are inserted between CAP1+ and CAP1-, between CAP2+ and CAP2-, between V_{OUT} and V_{DD2}, and jumper between CAP3+ and V_{OUT}, the triple boosted voltage appears at V_{OUT} pin.
Double boosting : If capacitor are inserted between CAP1+ and CAP1-, between V_{OUT} and V_{DD2}, open CAP2-, and jumper between CAP2+, CAP3+ and V_{OUT}, the double boosted voltage appears at V_{OUT} pin.
The boosted voltage relationships are shown in Figure 7.

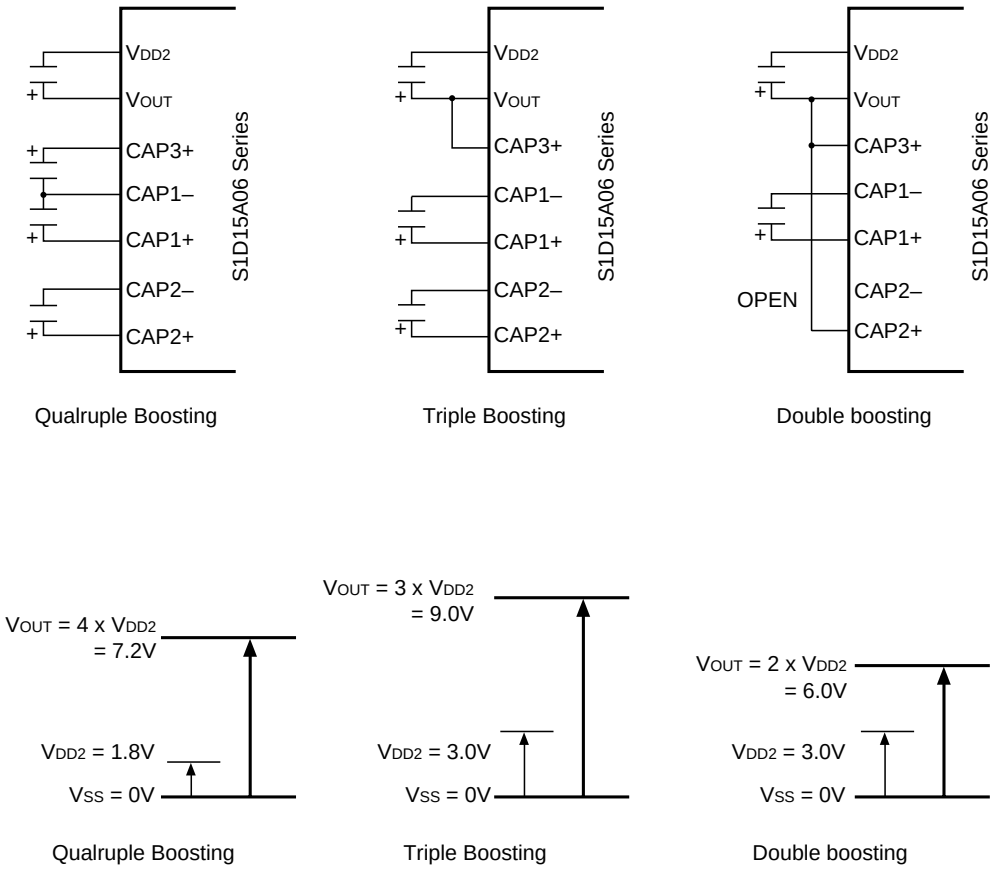


Figure 7

*V_{DD2} voltage must be set so that V_{OUT} voltage does not exceed the absolute maximun rated value.
*The Capacitance depend on the load of the LCD panel to be driven. Set a value that LCD driver voltage may be stable (reference value = 1.0 to 4.7μF).

Voltage regulator circuit

The boosting voltage occurring at the V_{OUT} pin is sent to the voltage regulator, and the V_0 voltage (LCD driver voltage) is output.
Because the S1D15A06 series has the high-accuracy constant voltage source, the 32-level electronic volume function and the internal resistor for the V_0 voltage regulator (= V_0-resistor), it is possible to construct a high-accuracy voltage regulator circuit without external component. And V_0 voltage can be adjusted by commands only to adjust the LCD contrast.

The V_0 voltage can be calculated using the following equation within the range of $V_0 < V_{OUT}$.

$$V_0 = (1+Rb/Ra) \cdot V_{EV}$$
$$= (1+Rb/Ra) \cdot (1-\alpha/200) V_{REG} \quad \text{(Expression A-1)}$$
$$V_{EV} = (1-\alpha/200) \cdot V_{REG}$$

V_{REG} is the on-chip constant voltage as shown in Table 10 at Ta=25°C.

Table 10

Model	V_{REG}	Thermal Gradient
S1D15A06D**	1.2V	–0.1%/°C

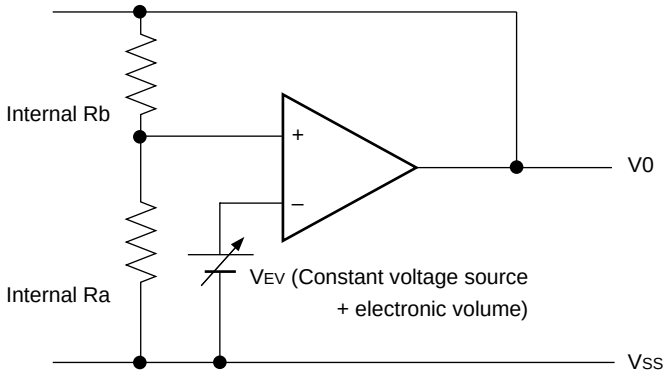


Figure 8

α is a value of the electronic volume, and can be set to one of 32-states by Electronic volume command setting the 5-bit data in the electronic volume register.Table 11 shows the value of α.

Table 11

D4	D3	D2	D1	D0	α
0	0	0	0	0	31
0	0	0	0	1	30
0	0	0	1	0	29
		⋮			⋮
1	1	1	0	0	3
1	1	1	0	1	2
1	1	1	1	0	1
1	1	1	1	1	0

Rb/Ra is the V_0-resistor ratio, and can be set to one of 7-states by V_0-resistor ratio set command setting the 3-bit data in the V_0-resistor ratio register. Table 12 shows the value of (1+Rb/Ra) ratio (reference value).

Table 12

D3	D2	D1	1+Rb/Ra SED15A6 (Typ.)
0	0	0	5.45
0	0	1	5.71
0	1	0	6.00
0	1	1	6.32
1	0	0	6.67
1	0	1	7.06
1	1	0	7.50
1	1	1	External resistor can be used.

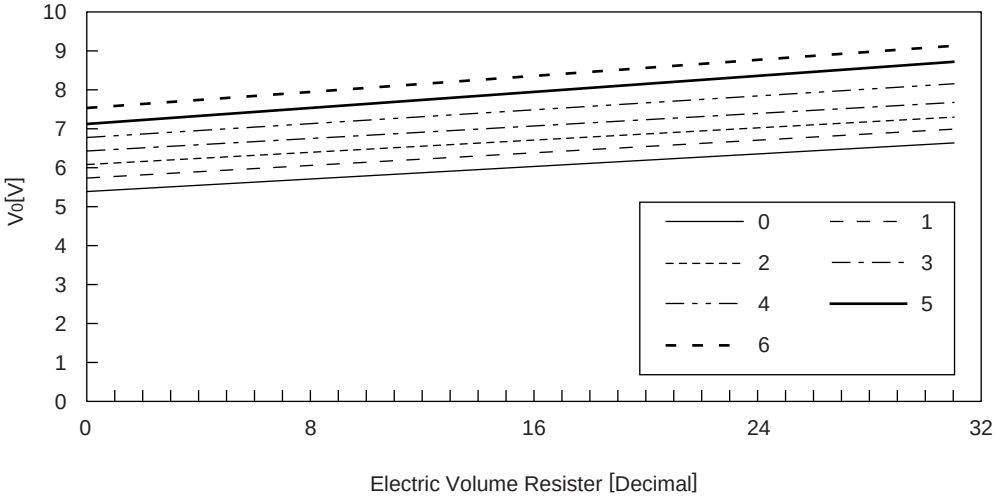


Figure 9 The V_0 voltage as a function of the V_0 voltage regulator internal resister internal resistor and the electronic volume register [Ta=25°C]

<Setup example : When setting Ta = 25C and V_0 = 7V on an S1D15A06***** model with temperature gradient of –0.1% /˚C>

From Figure 9 and expression A-1, the following setting will be employed.

Table 13

Content	Resistors							
	D7	D6	D5	D4	D3	D2	D1	D0
Resistance ratio of V_0 adjusting built-in resistors	0	0	1	0	0	0	1	1
Electronic volume	1	0	0	1	0	0	0	0

Table 14 shows V_0 voltage variable range and its variable step available from the electronic volume function when the above setting is employed.

Table 14

V_0	Min.		Typ.		Max.	Unit
Variable range	6.41[80H]	to	7.0[90H]	to	7.58[9FH]	[V]
Variable step			37.92			[mV]

[ ]: Commands selected from the electronic volume.

When external resistor is used (when the built-in resistor for V_0 adjustment is not used)

It is also possible to select a supply voltage V_0 for LCD without using the built-in V_0 voltage adjusting resistors (resistance ratio select command [27H] for the built-in V_0 voltage adjusting resistors) by adding a resistor across V_{SS} and V_R as well as V_R and V_0. In this case too, using the electronic volume allows you to control LCD V_0 through the command and, thus, adjust contrast of LCD display.

Voltage V_0 is given by the following expression when external resistance values Ra' and Rb' are specified in the range of $V_0 < V_{OUT}$:

$$V_0 = (1+Rb/Ra)\cdot V_{EV}$$
$$= (1+Rb/Ra)\cdot(1-\alpha/200)V_{REG} \quad \text{(Expression B-1)}$$
$$V_{EV} = (1-\alpha/200)\cdot V_{REG}$$

V_{REG} represents the constant voltage source on the IC. Its value at Ta = 25°C is constant as shown in Table 10.

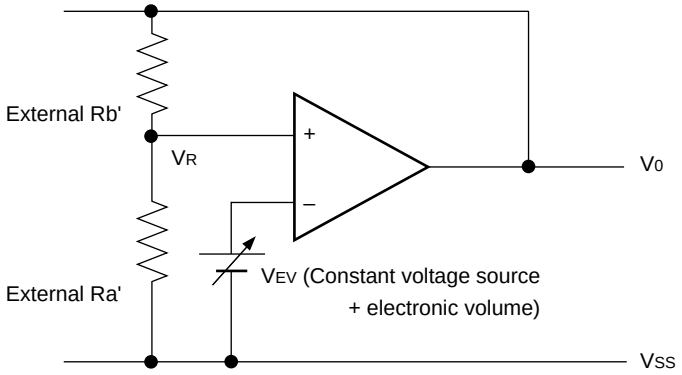


Figure 10

<A setting example: When setting Ta = 25C and V_0 = 7V on an S1D15A06***** model with temperature gradient =–0.1% C>
When the intermediate resistor values (D4, D3, D2, D1, D0) = (1, 0, 0, 0) are selected from the electronic volume, the following is given by expression B-1 since α = 15 and V_{REG} = 1.2V (Expression B-2).

$$V_0 = (1+Rb'/Ra') \cdot (1- \alpha /200) \cdot V_{REG}$$
$$7V = (1+Rb'/Ra') \cdot (1- 15 /200) \cdot 1.2 \quad \text{(Expression B-2)}$$

If you select 5 μA for the current conducted to Ra' and Rb', the following expression is derived:

$$Ra' + Rb' = 1.4M\Omega \quad \text{(Expression B-3)}$$

Thus, the following is derived from expressions B-2 and B-3:

$$Rb' / Ra' = 5.31$$
$$\therefore Ra' = 220k\Omega, \quad Rb' = 1180k\Omega$$

Table 14 shows the command selected from the electronic volume. Table 16 lists V_0 voltage variable range and variable steps available from the electronic volume function.

Table 15

Content	Resistors							
	D7	D6	D5	D4	D3	D2	D1	D0
Resistance ratio of built-in V_0 voltage adjusting resistors	0	0	1	0	0	1	1	1
Electronic volume	1	0	0	1	0	0	0	0

Table 16

V_0	Min.		Typ.		Max.	Unit
Variable range	6.45[80H]	to	7.0[90H]	to	7.64[9FH]	[V]
Variable step			38.4			[mV]

[ ]: Commands selected from the electronic volume.

When using external resistors (When using variable resistors in stead of the built-in V_0 voltage adjusting resistors)

Adding external variable resistors to the above mentioned external resistors allows you to select an LCD drive voltage V_0 through fine tuning of Ra' and Rb'. In this case too, using the electronic volume function permits you to control an LCD voltage through the command and, thus, adjust contrast of the LCD display.
You can determine the V_0 voltage from the following expression when fine adjustment of Ra' and Rb' is done by specifying resistance values of external resistors R1 and R2 (variable resistors) and R3 within the range of $|V_0| < |V_{OUT}|$:

$$V_0 = \{1+(R3+R2-\Delta R2) / (R1+\Delta R2)\} \cdot V_{EV}$$
$$= \{1+(R3+R2-\Delta R2) / (R1+\Delta R2)\} \cdot (1- \alpha/200) \cdot V_{REG} \quad \text{(Expression C-1)}$$
$$[V_{EV} = (1-\alpha/200) \cdot V_{REG}]$$

Where, V_{REG} is the constant voltage source in the IC and its value remains at a constant level as shown in Table 10.

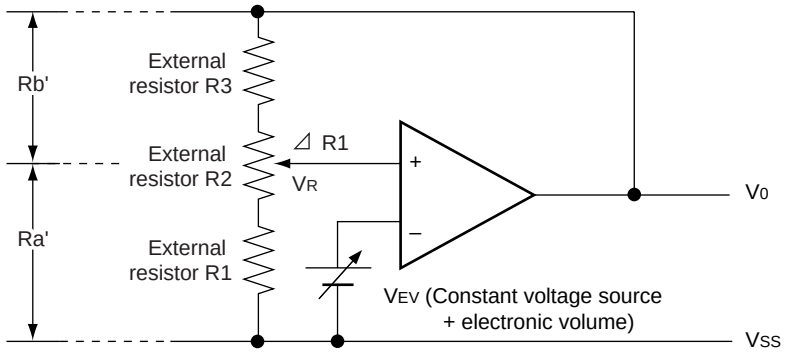


Figure 11

<A setting example: When setting Ta = 25C and V_0 = 5 to 9V on an S1D15A06***** model with Temperature gradient = –0.1% C>
α = 15 and V_{REG} = 1.2V when intermediate resistor values (D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0) are selected from the electronic volume. Thus, using expression C-1, you can select V_0 = 9V when $\Delta R2 = 0\Omega$ in the following manner:

9V ={1+(R3+R2) / R1} • (1–15/200) • 1.2
R3 + R2=7.11 • R1 (Expression C-2)

If you select 5 uA for the current to be conducted across V_0 and V_{SS} when V_0 = 7V, sum of resistance of R1, R2 and R3 can be derived as shown below:

R1 + R2 + R3 = 1.4MΩ (Expression C-3).

From expressions C-2 and C-3, R1 = 1.4MΩ/8.11=173kΩ.
And, you can select V = 5V when ΔR2 = R2 through the following computation:

5V = ={1+R3/(R1+R2) } • (1–15/200) • 1.2
R3/(R1 + R2) = 3.5 (Expression C-4).

R2 = 137@ and R3 = 1.09 MΩ are derived from expressions C-2, C-3 and C-4.
Table 15 lists the commands used, and Table 17 shows V_0 voltage variable voltage range and variable steps available from the electronic volume.

Table 17

V_0	Min.		Typ.		Max.	Unit
Variable range	6.39[80H]	to	7.0[90H]	to	7.57[9FH]	[V]
Variable step			38.1			[mV]

[ ]: Commands selected from the electronic volume.

* When using the built-in V_0 voltage adjusting resistors or the electronic volume function, both of the voltage adjustment circuit and the voltage follower circuit must be activated, as a minimum requirement, by the power control set command. When the booster is circuit is turned off, necessary voltage must be supplied from V_{OUT}.
* V_R pin is enabled only when the built-in V_0 voltage adjusting resistors are not used. V_R pin must be made open when these resistors are used.
* Since V_R pin has a higher input impedance, appropriate noise protection measures must provided including cutting the wiring distance shorter or using shielded wire.

Voltage Follower Circuit

The V_0 voltage is divided to generate the V_1, V_2, V_3 and V_4 voltages by on-chip resistor circuit. And the V_1, V_2, V_3 and V_4 voltages are impedance-converted by voltage follower, and provide to LCD driver circuit.
LCD bias ratio can be selected by LCD bias set command which is 1/6 bias or 1/8 bias for S1D15A06 series.

On-chip Power Supply Turn Off Sequence

Before turning the built-in power supply off, to discharge the remaining electric charge of LCD panel and power supply PIN etc., it is recommended to turn on the power save mode employing the following command sequence. You can also turn the built-in power supply off by initializing it using RES pin or the reset command. Here, of S1D15A06D00B∗with built-in power supply being only used, LOW level signal entering RES pin discharges V_{OUT}, thereby introducing shorting across V_{OUT}–V_{DD2} and V_0–V_{SS}. Of S1D15A06D01B∗/S1D15A06D02B∗ with external power supply being used, discharge the electric charge by short-circuiting the external power supply to V_{SS} when the power supply is off or power is being saved. (V_{OUT} and V_0 electric charge discharging functions are not in the IC)

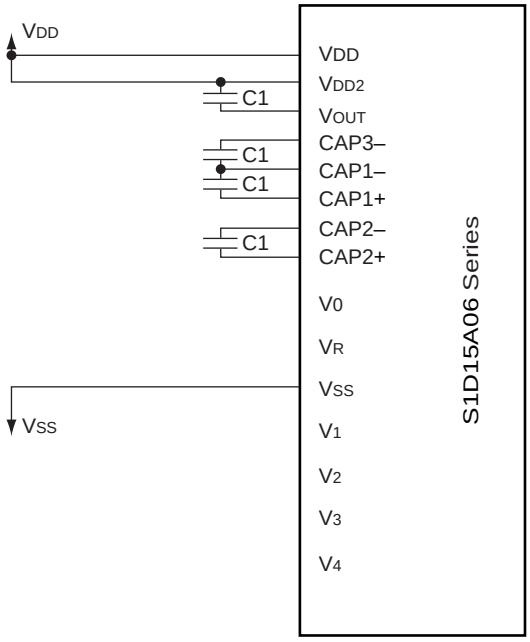
Table 18

Sequence	Contents (command and state)	Command address								
		D7	D6	D5	D4	D3	D2	D1	D0	
Step1	Display OFF	1	0	1	0	1	1	1	0	Power save command (composite command)
	↓									
Step2	Display all points on	1	0	1	0	0	1	0	1	
	↓									
End	Built-in power OFF	0	0	1	0	1	0	0	0	

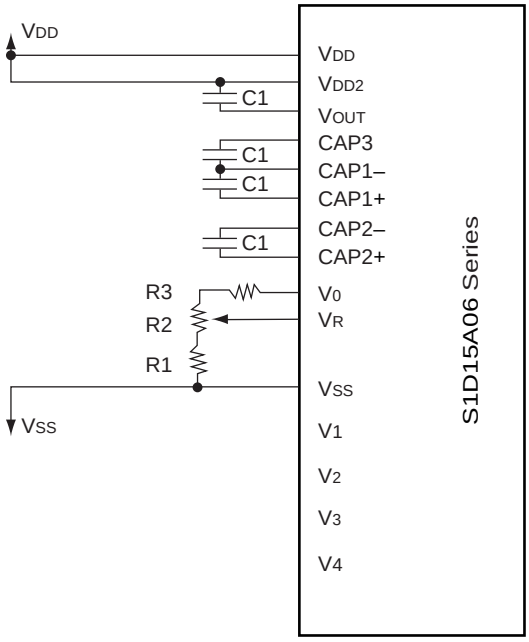
Sample Circuits

1. When the booster, voltage adjustment and V/F circuits are all used [S1D15A06D00B∗]

(1) When built-in V_0 voltage adjusting resistors are used (When $V_{DD2} = V_{DD}$ is boosted 4 times)

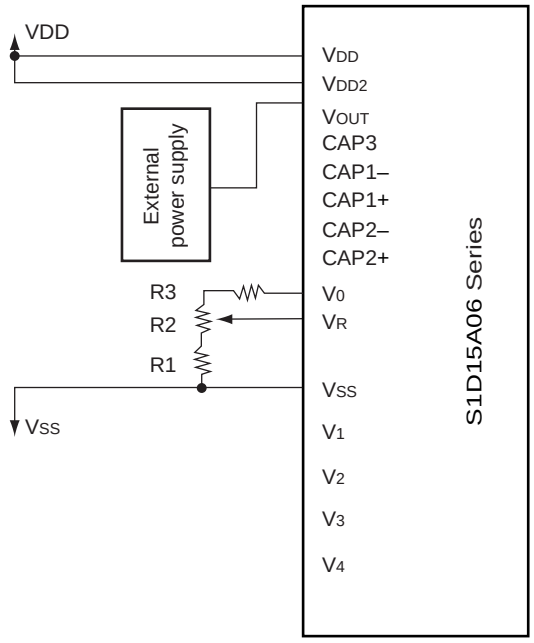


(2) When built-in V_0 voltage adjusting resistors are not used (When $V_{DD2} = V_{DD}$ boosted 4 times)

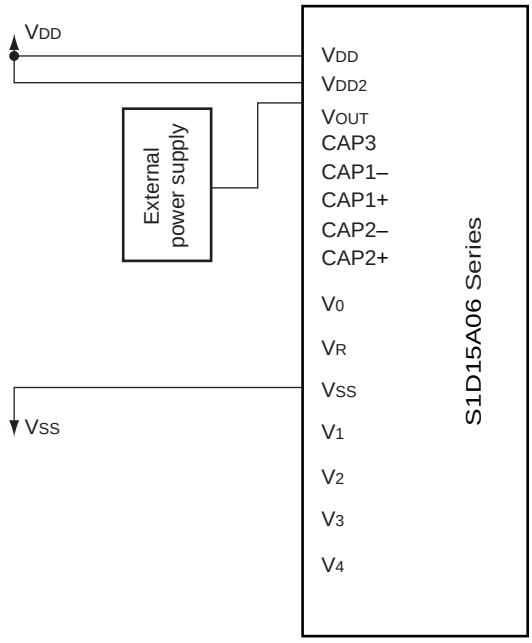


2. When the voltage adjustment and V/F circuits alone are used

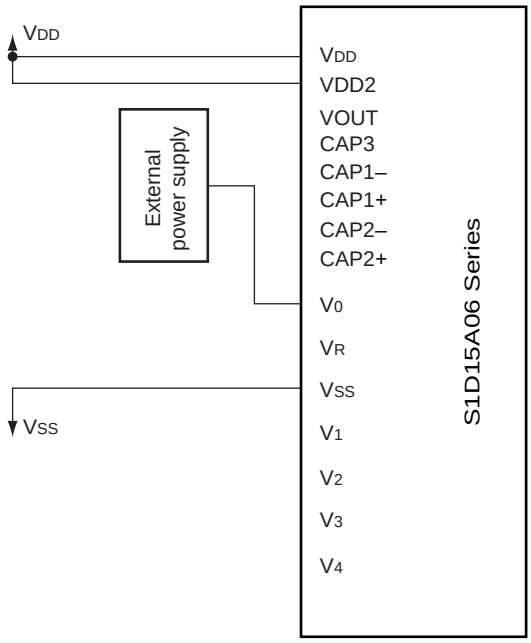
(1) When built-in V_0 voltage adjusting resistors are not used [S1D15A06D01B∗]



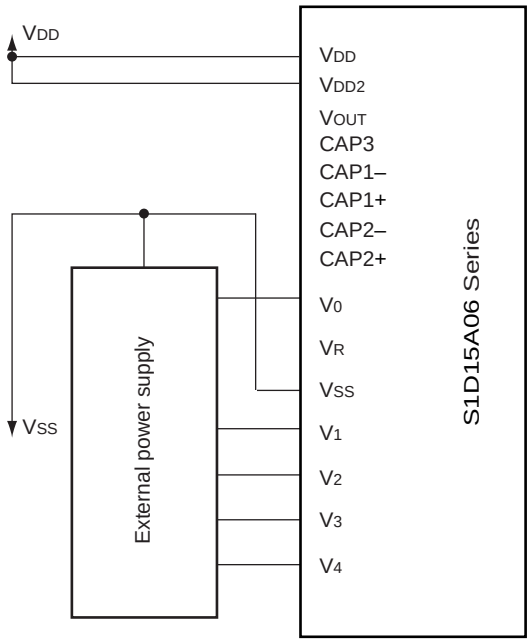
(2) When built-in V_0 voltage adjusting resistors are used Voltage Follower Circuit [S1D15A06D01B∗]



3. When V/F circuit alone is used [S1D15A06D01B∗]



4. When built-in power supply is not used[S1D15A06D02B∗]



∗ Since V_R pin has a higher impedance, wiring distance must be minimized or shielded wire must be used.

Sample setting
When V_0 is varied between 8 and 9V.

Item	Setting	Unit
C1	1.0 to 4.7	μF

Figure 12

Reset Circuit

When pin goes low, $\overline{RES}$ or when Reset command is used, this LSI is initialized.

Initialized states

- Serial interface internal shift register and counter clear
- Power saver mode is entered.
  - Oscillation circuit is stopped.
  - The LCD power supply circuit is stopped.
  - Display OFF
  - Display all points ON (Display all points ON ON/ OFF command D0 = "1")
  - Segment/common driver outputs go to the V_{SS} level.
- Display normal
- Page address=0H
- Column address=0H
- Display start line address=set at the first line
- Segment driver direction=normal
- Common driver direction=normal
- Read modify write OFF
- Power control register (D2, D1, D0) = (0, 0, 0)
- V_0-resistor ratio register (D2, D1, D0) = (0, 0, 0)
- Electronic volume register (D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0)
- LCD power supply bias ratio = 1/6 bias (S1D15A06)
- Test mode is released.

*** Voltage short-circuit across V_{OUT} and V_{DD2} as well as Vo and V_{SS} [allowed only when $\overline{RES}$ pin = LOW level].**

When reset is detected, this LSI is set to above initialized states. However it has no effect on contents of DDRAM. As seen in "Microprocessor Interface (Reference Example)", connect $\overline{RES}$ pin to the reset pin of the MPU and initialize the MPU at the same time. The initialization by $\overline{RES}$ pin is always required during power-on.
If the control signal from MPU is HZ, an overcurrent may flow through the LSI. A protection is required to prevent the HZ signal at the input pin during power-on.
In case the S1D15A06 series does not use the on-chip LCD power supply circuit, after $\overline{RES}$ pin is turnd LOW to HIGH, the external LCD power supply must be turned on.

7. COMMANDS

The S1D15A06 series identifies the data bus by a combination of A0, $\overline{RD}$ (E), $\overline{WD}$(R/$\overline{W}$) signals.
In the 8080-series MPU interface, the command is activated when a low pulse is input to $\overline{RD}$ pin for reading and when a low pulse is input to $\overline{WD}$ pin for writing. In the 6800-series MPU interface, the S1D15A06 series enters a read mode when a high level is input to R/$\overline{W}$ pin and a write mode when a low level is input to R/$\overline{W}$ pin, and the command is activated when a high pulse is input to E pin. Therefore, in the command explanation and command table, the 6800-series MPU interface is different from the 8080-series MPU interface in that $\overline{RD}$(E) becomes "1 (H)" in Display data read command.
And when the serial interface is selected, the data is input in sequence starting with D7.
Taking the 8080-series MPU interface as an example, commands will be explained below.

Explanation of commands

(1) Display ON/OFF

This command turns the display ON and OFF.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	0 1	Display OFF Display ON

When the Display OFF command is executed when in the Display all points ON mode , Power saver mode is entered. See the section on the Power saver for details.

(2) Display normal/reverse

This command can reverse the lit and unlit display without overwriting the contents of the DDRAM.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0 1	Normal:DDRAM Data HIGH =LCD ON voltage Reverse:DDRAM Data LOW =LCD ON voltage

(3) Display all points ON/OFF

This command makes it possible to force all display points ON regardless of the content of the DDRAM. Even when this is done, the DDRAM contents are maintained. This command takes priority over the Display normal/reverse command.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0 1	Normal display mode Display all points ON

When the Display all points ON command is executed when in the Display OFF mode, Power saver mode is entered. See the section on the Power saver for details.

(4) Page address set

This command specifies the page address of the DDRAM (refer to Figure 5).
Specifying the page address and column address enables to access a desired bit of the DDRAM. After the last column address (65H), page address incremented by +1 (refer to Figure 4). After the very last address (column = 65H, page = 7H), page address return to 0H.
Page address 8H is the DDRAM area dedicate to the indicator, and only D0 is valid for data change.
See the function explanation in “DDRAM and page/column address circuit”, for detail.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0H
							0	0	0	1	1H
							0	0	1	0	2H
								:			:
							0	1	1	1	7H
							1	0	0	0	8H

(5) Column address set

This command specifies the column address of the DDRAM (refer to Figure 5).
The column address is split into tow sections (the upper 3-bits and lower 4-bits) when it is set (fundamentally, set continuously).
Each time the DDRAM is accessed, the column address automatically increments by +1, making it possible for the MPU to continuously access to the display data. After the last column address (65H) ,column address returns to 00H (refer to Figure 4).
See the function explanation in “DDRAM and page/column address circuit”, for detail.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	0	0	1	*	A6	A5	A4	Upper bit address
						0	A3	A2	A1	A0	Lower bit address

*Disabled bit

A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	00H
0	0	0	0	0	0	1	01H
0	0	0	0	0	1	0	02H
			:				:
1	1	0	0	1	0	0	64H
1	1	0	0	1	0	1	65H

(6) Display start line address set

This command is used to specify the display start line address of the DDRAM (refer to Figure 5).
If the display start line address is changed dynamically using this command, then screen scrolling, page swapping can be performed.
See the function explanation in “Line address circuit”, for detail.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	00H
					0	0	0	0	0	1	01H
					0	0	0	0	1	0	02H
							:				:
					1	1	1	1	1	0	3EH
					1	1	1	1	1	1	3FH

(7) ADC Select (Segment driver direction select)

This command can reverse the correspondence between the DDRAM column address and the segment driver output.
See the function explanation in “DDRAM and page/column address circuit”, for detail.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

(8) Common driver direction select

This command can reverse the correspondence between the DDRAM line address and the common driver output. See the function explanation in “Line address circuit”, for detail.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	1	0	0	0	*	*	*	Normal
							1				Reverse

*Disabled bit

(9) Display data read

This command reads 8-bit data from the specified DDRAM address. Since the column address is automatically incremented by +1 after each read ,the MPU can continuously read multiple-word data. One dummy read is required immediately after the address has been set. See the function explanation in “Access to DDRAM and internal registers” and “DDRAM and page/column address circuit”, for detail.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

(10) Display data write

This command writes 8-bit data to the specified DDRAM address. Since the column address is automatically incremented by +1 after each write ,the MPU can continuously write multiple-word data. See the function explanation in “DDRAM and page/column address circuit”, for detail.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write Data							

(11) Read modify write

This command is used paired with End command. Once this command is issued, the column address is not incremented by Display data read command, but is incremented by Display data write command. This mode is maintained until End command is issued. When End command is issued, the column address returns to the address it was at when Read modify write command was issued. This function makes it possible to reduce the MPU load when there are the data to change repeatedly in a specified display region, such as blinking cursor.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

*When End command is issued, only column address returns to the address it was at when Read modify write command was issued, but page address does not return. Consequently, Read modify Write mode cannot be used over pages. When you want to maintain the current page address after a read modify write operation done on a column address between the start and the final column address (65H), you must specify the page address again after the operation is over.

*Even if Read modify write mode, other commands besides Display data read/write can also be used. However, Column address set command cannot be used.

The sequence for cursor display

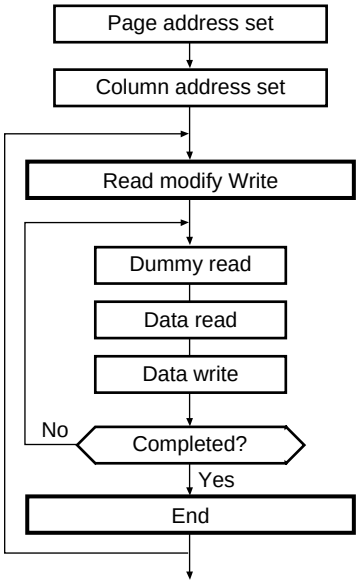


Figure 13

(12) End

This command releases the Read modify write mode, and returns the column address to the address it was when Read modify write command was issued .

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

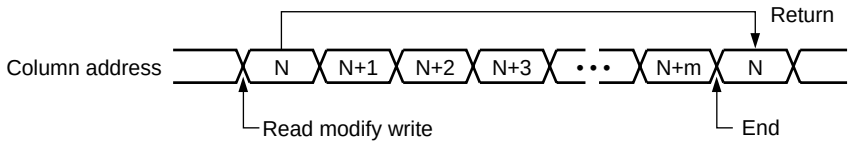


Figure 14

(13) Power control set

This command sets the on-chip power supply function ON/OFF. See the function explanation in “Power supply circuit”, for detail.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Mode
0	1	0	0	0	1	0	1	0			Booster : OFF
								1			Booster : ON
									0		Voltage regulator : OFF
									1		Voltage regulator : ON
										0	Voltage follower : OFF
										1	Voltage follower : ON

(14) V0-resistor ratio set

This command sets the internal resistor ratio “Rb/Ra” for the V0 voltage regulator to adjust the contrast of LCD panel display. See the function explanation in “Power supply circuit”, for detail.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra : V0 voltage
0	1	0	0	0	1	0	0	0	0	0	small low
								0	0	1	
								0	1	0	
								0	1	1	↓ ↓
								1	0	0	
								1	0	1	
								1	1	0	large high
								1	1	1	External resistor mode

(15) Electronic volume

This command sets a value of electronic volume "α" for the V_0 voltage regulator to adjust the contrast of LCD panel display. See the function explanation in "Power supply circuit", for detail.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	α : V0 voltage
0	1	0	1	0	0	0	0	0	0	0	31 low
						0	0	0	0	1	30
						0	0	0	1	0	29
								↓			↓ ↓
						1	1	1	1	0	1
						1	1	1	1	1	0 high

(16) LCD bias set

This command selects the voltage bias ratio required for the LCD. This command is enabled when the voltage follower circuit operates.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Bias S1D15A06
0	1	0	1	0	1	0	0	0	1	0	1/8 bias
										1	1/6 bias

(17) Power saver

When the display all points ON command is executed when in the display OFF mode, power saver mode is entered, and the power consumption can be greatly reduced.
This mode stops every operation of the LCD display system, and can reduce current consumption nearly to a static current value if no access is made from the MPU. The internal states in the power saver mode is as follows:

- The oscillation circuit is stopped.
- The LCD power supply circuit is stopped.
- The LCD driver circuit is stopped and segment/common driver outputs output the V_{SS} level.
- The display data and operation mode before execution of the Power saver command are held, and the MPU can access to the DDRAM and internal registers.

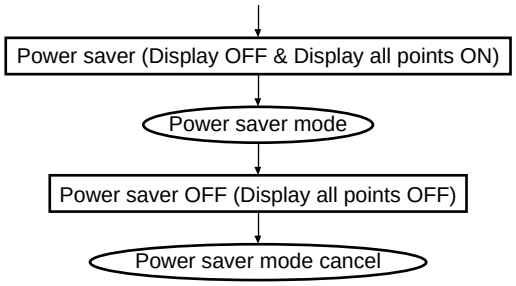


Figure 15

(18) Reset

When this command is issued, this LSI is initialized. This command, however, is not used for introducing short circuit across V_{OUT} and V_{DD2} or V_0 and V_{SS} (only when $\overline{RES}$ pin = LOW). Also note that initialization of the display data RAM does not take place in parallel with initialization of the LSI. See the function explanation in "Reset circuit", for detail.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

When initializing the LSI while power is turned on, reset signal to the $\overline{RES}$ pin is used. This signal cannot be replaced by the reset command.

(19) NOP

Non-operation command

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

(20) Test

This is a command for LSI chip testing. Please do not use. If the test command is issued by accident, it can be cleared by applying an LOW signal to the pin, or by issuing the Reset command or the Display ON/OFF command.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	*	1	*	*	*	*

* Disabled bit

(Note):
The S1D15A06 series chip maintain their operating modes ,but excessive external noise,etc.,may happen to change them. Thus in the packaging and system design it is necessary to suppress the noise or take measures to prevent the noise. Moreover, it is recommended that the operating modes are refreshed periodically to prevent the effects of unanticipated noise.

Command Table

Table 19

Command	Code											Function
	A0	XR	XW	D7	D6	D5	D4	D3	D2	D1	D0	
(1)Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display 0:OFF, 1:ON
(2)Display normal/reverce	0	1	0	1	0	1	0	0	1	1	0 1	LCD display 0:normal, 1:reverce
(3)Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	LCD display 0:normal display, 1:all points ON
(4)Page address set	0	1	0	1	0	1	1	address				Sets the DDRAM page address
(5)Column address set Upper 3-bit address	0	1	0	0	0	0	1	*	address			Sets the DDRAM column address
Column address set Lower 4-bit address	0	1	0	0	0	0	0	address				
(6)Display start line address set	0	1	0	0	1	address						Sets the DDRAM display start line address.
(7)Segment driver directuin select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the correspondence between the DDRAM column address and the SEG driver output. 0:normal, 1:reverse
(8)Common driver direction select	0	1	0	1	1	0	0	0 1	*	*	*	Sets the correspondence between the DDRAM line address and the COM driver output. 0:normal, 1:reverse
(9)Display data read	1	0	1	Read data								Reads from the DDRAM.
(10)Display data write	1	1	0	Wtite data								Writes to the DDRAM.
(11)Read modify write	0	1	0	1	1	1	0	0	0	0	0	Column address increment at write:+1, at read:0.
(12)End	0	1	0	1	1	1	0	1	1	1	0	Releases Read modify write mode.
(13)Power control set	0	1	0	0	0	1	0	1	Operating mode			Sets the on-chip power supply circuit operating mode.
(14)V_0-resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Sets the V_0-resistor ratio value.
(15)Electronic volume	0	1	0	1	0	0	Electronic volume value					Sets the electronic volume value.
(16)LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio. S1D15A06 0:1/8bias, 1:1/6bias
(17)Power saver	-	-	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Display all points ON
(18)Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(19)NOP	0	1	0	1	1	1	0	0	0	1	1	Non-operation
(20)Test	0	1	0	1	1	*	1	*	*	*	*	IC test command. Do not use.

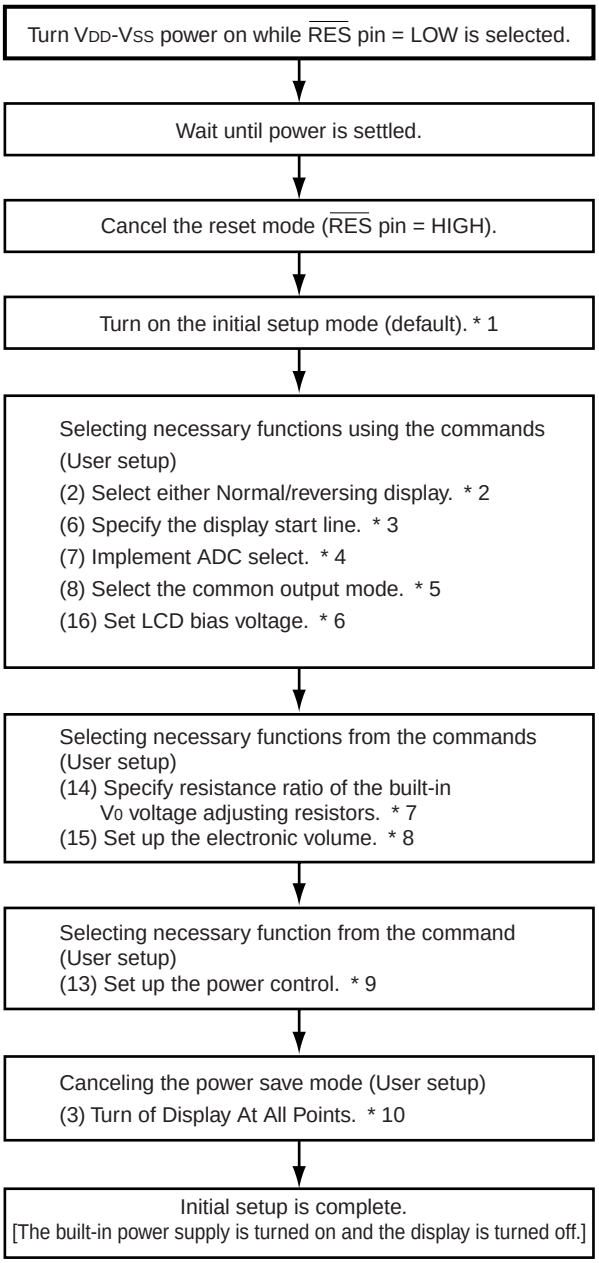
(Note)*:disabled bit

8. COMMAND SETTING

Instruction Setup Example (For your reference)

Note: If charge remains on the smoothing capacitor connected across the LCD drive voltage output pin and V_{DD2} pin, troubles (such as momentary blackening) can occur on the display screen during its powering on process. In order to avoid such troubles, it is recommended to implement the following flow.

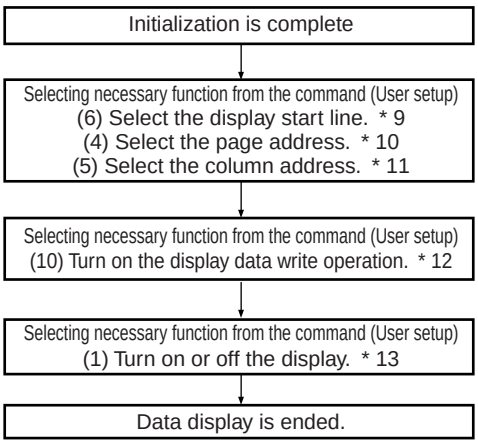
1. When switching to the built-in power supply takes place immediately after powering on:



Note: Reference Items

* 1: Refer to the 6. Functions Description “Reset Circuit”.
  In the initial setup mode (default), too, contents of the display data RAM is still uncertain.
* 2: Refer to the 7. Commands Description “(2) Normal/reversing Display”.
* 3: Refer to the 7. Commands Description “(6) Display Line Setup”.
* 4: Refer to the 7. Commands Description “(7) ADC Select”.
* 5: Refer to the 7. Commands Description “(8) Common Output Mode Select”.
* 6: Refer to the 7. Commands Description “(16) LCD Bias Set”.
* 7: Refer to the 6. Functions Description Power Supply Circuit and 7. Commands Description “(14) Specifying resistance ratio of built-in V0 voltage adjusting resistors”.
* 8: Refer to the 6. Functions Description Power Supply Circuit and 7.Commands Description “(15) Electronic Volume”.
* 9: Refer to the 6. Functions Description Power Supply Circuit and 7. Commands Description “(13) Setting Up Power Control”.
* 10: Refer to the 7. Commands Description “(17) Power Save”.

2. Data display

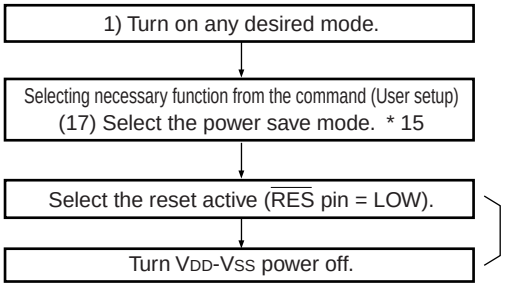


Note: Reference Items

* 9: Refer to the 7. Commands Description “(6) Setup of Display Start Line”.
* 10: Refer to the 7. Commands Description “(4) Page Address Set”.
* 11: Refer to the 7. Commands Description “(5) Column Address Set”.
* 12: Refer to the 7. Commands Description “(10) Display Data Write”.
* 13: Refer to the 7. Commands Description “(1) Display Data ON/OFF”.

The all-white display of data should be avoided as much as practicable right after the display mode is turned on (right after the display has been turned on).

3. Powering off * 14



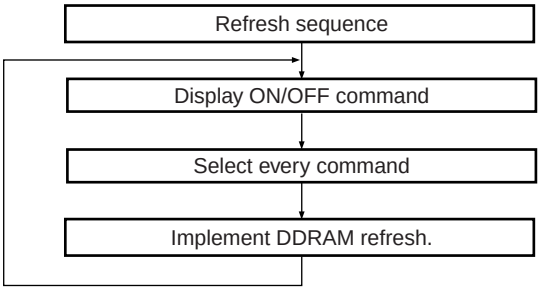
The time (tL) provided between turning on of the reset active and turning off of V_{DD}-V_{SS} power (V_{DD}-V_{SS} = 1.8V) must be longer than the time required for V_0-V_4 potential to go lower (tH) than the threshold voltage set on the LCD (usually 1V).
For “t_H”, see the “Reference data” in the following section. If “t_H” is excessively long, it must be cut short by installing a resistor across V_0 and V_{SS}.

Note:

* 14: This IC is provided on the power supply V_{DD}-V_{SS} logic circuit to offer control over the V_0-V_{SS} drivers on the LCD power supply. Thus, if the power supply V_0-V_{SS} is turned off while voltage is still remaining on the LCD power supply V_0-V_{SS}, the drivers (both COM and SEG) can generate uncontrolled output. Make sure to observe the following powering off procedure:
  • Turn off the built-in power supply first, then, after making sure that potential on V_0 to V_4 is lower than the LCD panel threshold voltage, turn the IC power (V_{DD}-V_{SS}) off. Also refer to the 6. Functions Description "Power Supply Circuit".
* 15: Refer to the 7. Command Description “(17) Power Save”.
After entering the power save command, you must implement reset procedure from the $\overline{RES}$ pin before turning off V_{DD}-V_{SS} power.

4. Refresh

It is recommended that the operating modes and display contents be refreshed periodically to prevent the effect of unexpected noise.



5. Precautions on powering off

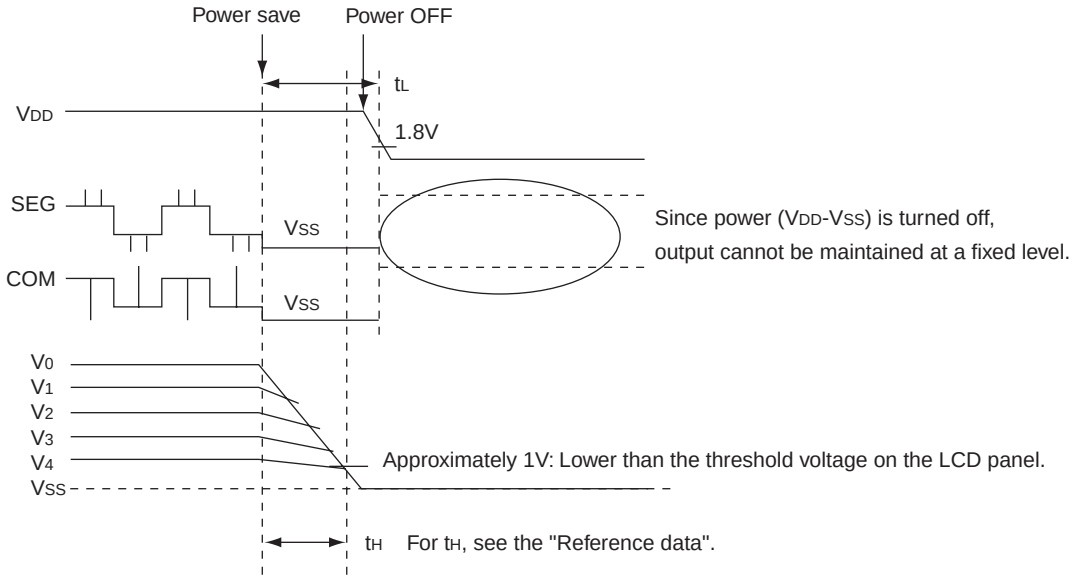
<Powering off (V_{DD}-V_{SS}) off>

Turn the power (V_0-V_{SS}) save mode off -> Then, turn the power (V_{DD}-V_{SS}) off.

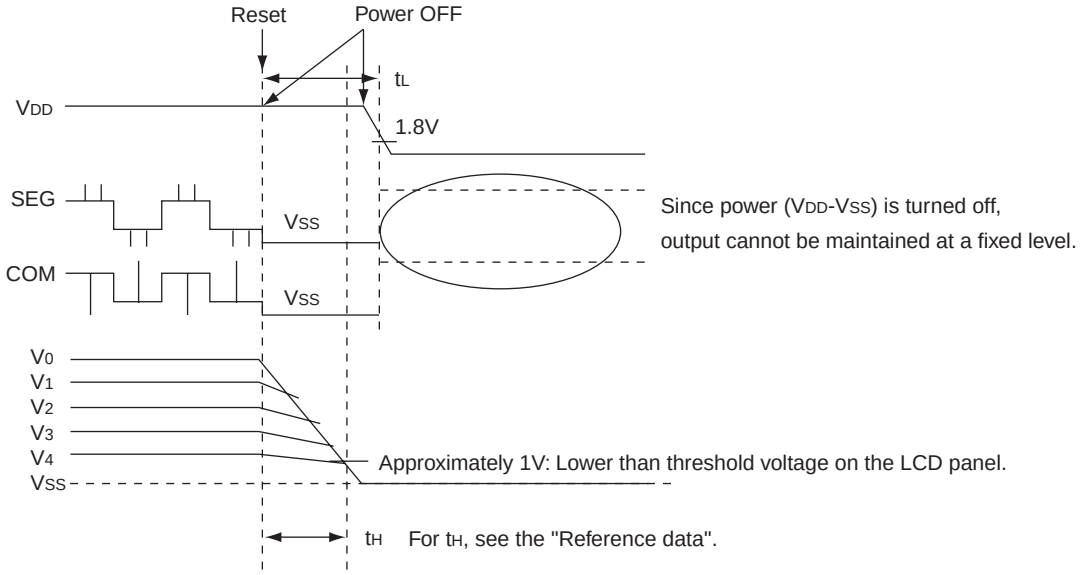
* The requirement "$t_L > t_H$" must be strictly observed.
* If "$t_L < t_H$", display failures can result.

t_L must be specified on software from MPU.

t_H depends on discharging capability of the drivers. See the "Reference data" in the following section. It also depends on a given LCD panel, thus actual timing must be determined after experimenting on your LCD panel.



<When powering off (V_{DD}-V_{SS}) is not available with the command>
Turn off the reset mode (LCD power (V_0-V_{SS}) system).
-> Then, turn power (V_{DD}-V_{SS}) off.
* The requirement "$t_L > t_H$" must be observed.
* When specifying t_L, measures such as extending fall time of power supply (V_{DD}-V_{SS}) should be considered. t_H depends on the drivers' discharging capability. See the "Reference data" in the following section. It also depends on model of a given LCD panel, thus actual timing must be determined after experimentation on your LCD panel.



6. Reference data
The following data is for your reference alone. t_H is significantly affected by capacity of V_0 pin, thus you must verify appropriateness of a selected t_H on the panel being equipped with the pin.

[Conditions: V_{DD} = 1.8V, voltage is tripled and capacity of the boosting capacitor = 1.0 µF]

When V_0 is under no-load, t_H per voltage is 22 µs. It becomes 220 µs when V_0 = 9V.
Capacity dependency is 1 pF. Δt_H per voltage is 50 ns.

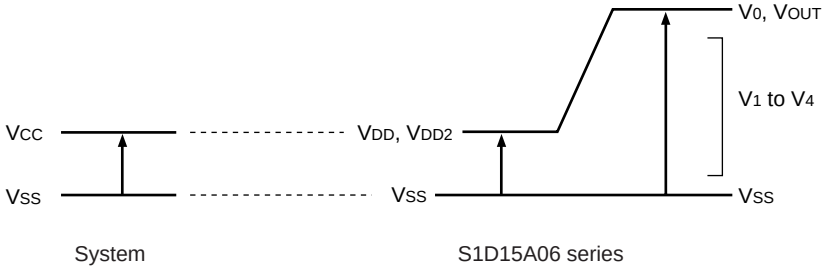
An example: When V_{DD} = 1.8V, V_0 = 8V and V_0 pin capacity [board capacity] (CL) = 100 pF.
$t_H = 22\mu s \times 8V + 50ns \times 100pF \times 8V = 216\mu s$

9. ABSOLUTE MAXIMUM RATING

Unless otherwise noted, V_{SS} = 0V.

Table 20

Parameter		Symbol	Conditions	Unit
Power supply voltage (1)		V_{DD}	–0.3 to 0.6	V
Power supply voltage (2)		V_{DD2}	–0.3 to 0.6	V
	Double boosting		–0.3 to 5.0	
	Triple boosting		–0.3 to 3.3	
	Quadruple boosting		–0.3 to 2.5	
Power supply voltage (3)		V_0, V_{OUT}	–0.3 to 10.0	V
Power supply voltage (4)		V_1, V_2, V_3, V_4	–0.3 to V_0	V
Input voltage		V_{IN}	–0.3 to V_{DD}+0.3	V
Output voltage		V_O	–0.3 to V_{DD}+0.3	V
Operating temperature		T_{OPR}	–40 to 85	°C
Storage temperature	TCP	T_{STR}	–55 to 100	°C
	Bare chip		–55 to 125	



Notes and Conditions

1. V_{SS} = 0V is assumed for every voltage indicated above.
2. Voltage V_0, V_1, V_2, V_3, V_4 must always keep up the condition of $V_0 \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_{SS}$ and $V_{OUT} \geqq V_0 \geqq V_{SS}$.
3. If the LSI exceeds its absolute maximum rating, it may be damage permanently. It is desirable to use it under electrical characteristics conditions during general operation. Otherwise, a malfunction of the LSI may be caused and LSI reliability may be affected.

10. DC CHARACTERISTICS

Table 21 V_{SS}=0V, V_{DD}=3V±10%, Ta=–40~85°C unless otherwise noted.

Item		Symbol	Condition	Standard value			Unit	Pin used
				Min.	Typ.	Max.		
Supply voltage(1)	Recommended operation	V_{DD}	(V_{SS} is used as the reference)	2.7	–	3.3	V	V_{DD} *1
	Operational available	V_{DD}	(V_{SS} is used as the reference)	1.8	–	3.6	V	
Supply voltage(2)	Recommended operation	V_{DD2}	(V_{SS} is used as the reference)	1.8	–	5.0	V	V_{DD2} *1
Supply voltage(3)	Operational available	V_0	(V_{SS} is used as the reference)	4.5	–	9.0		V_0 *2
	Operational available	V_1, V_2	(V_{SS} is used as the reference)	0.6×V_0	–	V_0	V	V_1, V_2
	Operational available	V_3, V_4	(V_{SS} is used as the reference)	V_{SS}	–	0.4×V_0		V_3, V_4
High-level input voltage		V_{IH}		0.7×V_{DD}	–	V_{DD}	V	*3
Low-level input voltage		V_{IL}		V_{SS}	–	0.3×V_{DD}	V	
High-level output voltage		V_{OH}	I_{OH}=–0.5mA	0.7×V_{DD}	–	V_{DD}	V	*4
Low-level output voltage		V_{OL}	I_{OL}=0.5mA	V_{SS}	–	0.3×V_{DD}	V	
Input leak current		I_{LI}	V_{IN}=V_{DD} or V_{SS}	–1.0	–	1.0	µA	*5
Output leakage current		I_{LO}		–3.0	–	3.0	µA	*6
LCD driver ON resistance		R_{ON}	V_0=7.0V Ta=25°C	–	2.0	5.0	kΩ	SEGn, COMn *7
Static current consumption		I_{DDQ}	Ta=25°C	–	0.01	5.0	µA	V_{DD},V_{DD2}
Output leak current		I_{0Q}	V_0=7.0V Ta=25°C	–	0.01	15.0	µA	V_0
Input terminal capacitance		C_{IN}	Ta=25°C, f =1MHz		10.0	15.0	pF	
Oscillation frequency	Built-in oscillation	f_{OSC}	Ta=25°C	31.68	35.20	38.72	kHz	*8
	External input	f_{CL}		35.2	70.4	140.8		CL *8

Table 22

Item		Symbol	Condition	Standard value			Unit	Pin used
				Min.	Typ.	Max.		
Built-in power supply circuit	Input voltage	V_{DD2}	When voltage is doubled (Vss is used as the reference)	1.8	–	5.0	V	V_{DD2} *1
			When voltage is tripled (Vss is used as the reference)	1.8	–	3.3		
			When voltage is quadrupled (Vss is used as the reference)	1.8	–	2.5		
	Boosted output voltage	V_{OUT}	(Vss is used as the reference)	–	–	10.0		V_{OUT}
	Operating current of voltage adjustment circuit	V_{OUT}	(Vss is used as the reference)	5.0	–	10.0		V_{OUT}
	V/F circuit operating voltage	V_0	(Vss is used as the reference)	4.5	–	9.0		V_0 *9
	Reference voltage	V_{REG}	–0.1%/°C Ta=25°C (Vss is used as the reference)	1.16	1.2	1.24		*10

Note 1: V_{SS} = 0V is assumed for every voltage indicated.

Note 2: Voltages V_0, V_1, V_2, V_3 and V_4 must conform to the requirements that $V_0 \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_{SS}$ as well as $V_{OUT} \geqq V_0 \geqq V_{SS}$.

Note 3: Operating the LSI is operated beyond the maximum absolute rating can damage it permanently. In the normal operation, it is desirable to use the LSI in compliance with its electric characteristics. If the LSI is used under any conditions conflicting with its electric characteristics, not only its malfunctioning but also serious loss of reliability can result.

◊ Dynamic operating current (1) - When display is turned on with the built-in power supply being disconnected [Ta = 25°C and output under no-load].
Following shows current consumed by entire IC when external power supply is used.

Table 23-1 Display: All-white

Item	Symbol	Requirement	Min.	Typ.	Max.	Unit	Remarks
S1D15A06*****	I_{SS}(1)	V_{DD}=V_{DD2}=1.8V, V_0=7.2V	–	23	48	µA	*11
	I_{SS}(1)	V_{DD}=V_{DD2}=1.8V, V_0=9.0V	–	25	50		

Table 23-2 Display: Checker pattern

Item	Symbol	Requirement	Min.	Typ.	Max.	Unit	Remarks
S1D15A06*****	I_{SS}(1)	V_{DD}=V_{DD2}=1.8V, V_0=7.2V	–	26	54	µA	*11
	I_{SS}(1)	V_{DD}=V_{DD2}=1.8V, V_0=9.0V	–	29	57		

◊ Dynamic operating current (2) - When display is turned on with the built-in power supply being connected [Ta = 25°C and output under no-load].

Table 24-1 Display: All-white

Item	Symbol	Requirement	Min.	Typ.	Max.	Unit	Remarks
S1D15A06*****	I_{SS}(2)	V_{DD}=1.8V,V_{DD2}=3.3V, V_0=7.2V, and voltage is tripled.	–	68	101	µA	*12
	I_{SS}(2)	V_{DD}=1.8V,V_{DD2}=3.3V, V_0=7.2V, and voltage is tripled.	–	79	112		

Table 24-2 Display: Checker pattern

Item	Symbol	Requirement	Min.	Typ.	Max.	Unit	Remarks
S1D15A06*****	I_{SS}(2)	V_{DD}=1.8V,V_{DD2}=3.3V, V_0=7.2V, and voltage is tripled.	–	75	103	µA	*12
	I_{SS}(2)	V_{DD}=1.8V,V_{DD2}=3.3V, V_0=7.2V, and voltage is tripled.	–	87	112		

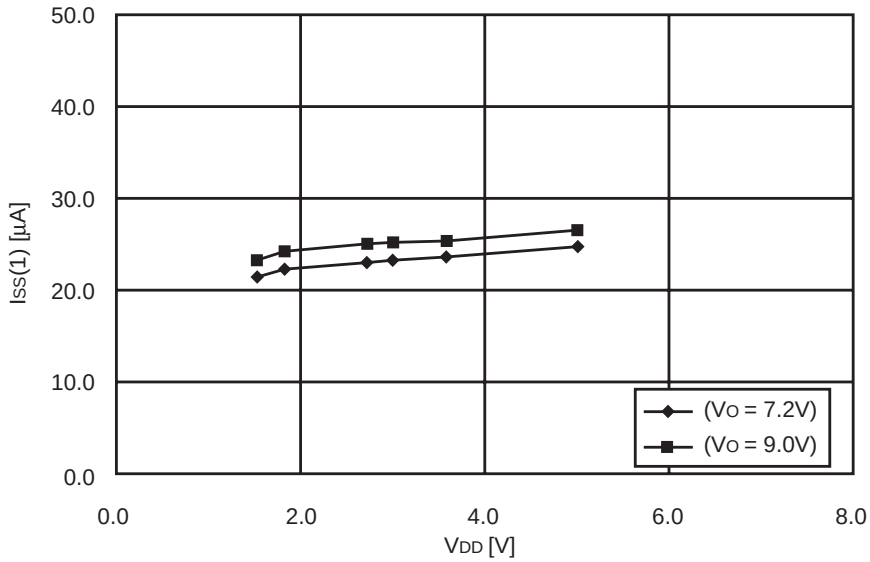
◊ Current consumption in the power save mode [Ta = 25°C and output under no-load]

Table 25

Item	Symbol	Requirement	Min.	Typ.	Max.	Unit	Remarks
S1D15A06*****	I_{SS}(3)	V_{DD}=V_{DD2}=1.8~3.6V	–	0.01	5	µA	

[Reference data 1]

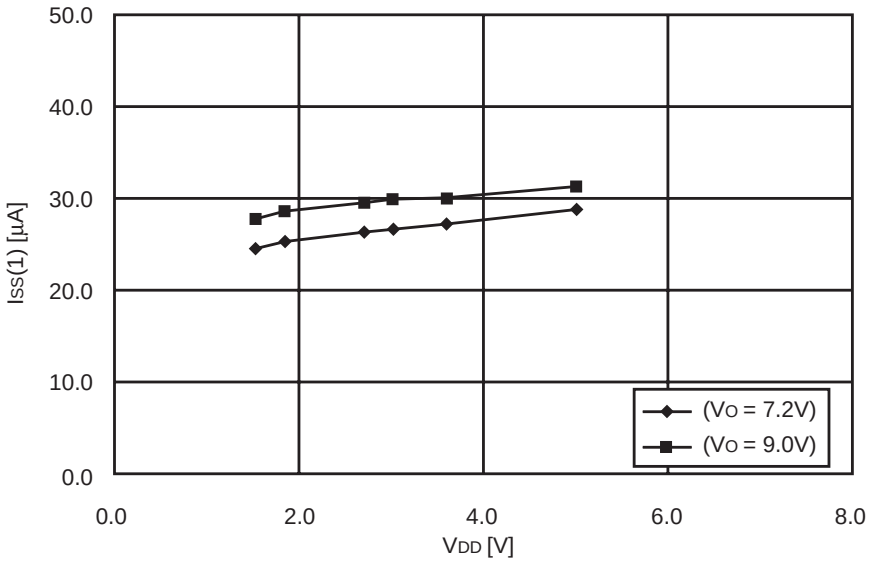
◊ Dynamic operating current (1) - When LCD display is turned on with external power supply being connected (All-white display)



Conditions:
Built-in power supply OFF
External power supply ON
V_{DD2}-V_{SS} = 1.8V
V_{DD}-V_{SS} = 1.8V
V_0-V_{SS} = 7.2V
V_0-V_{SS} = 9.0V
Ta = 25°C
Display pattern: All-white.
Remarks: See * 11.

Figure 16

◊ Dynamic operating current (1) - When LCD display is turned on with external power supply being connected (Checker pattern display)

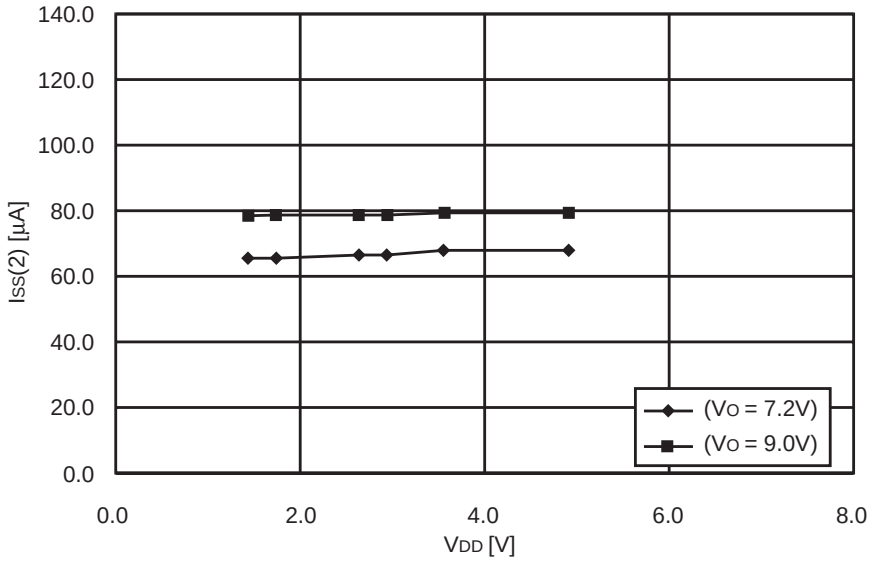


Conditions:
Built-in power supply OFF
External power supply ON
V_{DD2}-V_{SS} = 1.8V
V_{DD}-V_{SS} = 1.8V
V_0-V_{SS} = 7.2V
V_0-V_{SS} = 9.0V
Ta = 25°C
Display pattern: Checker.
Remarks: See * 11.

Figure 17

[Reference data 2]

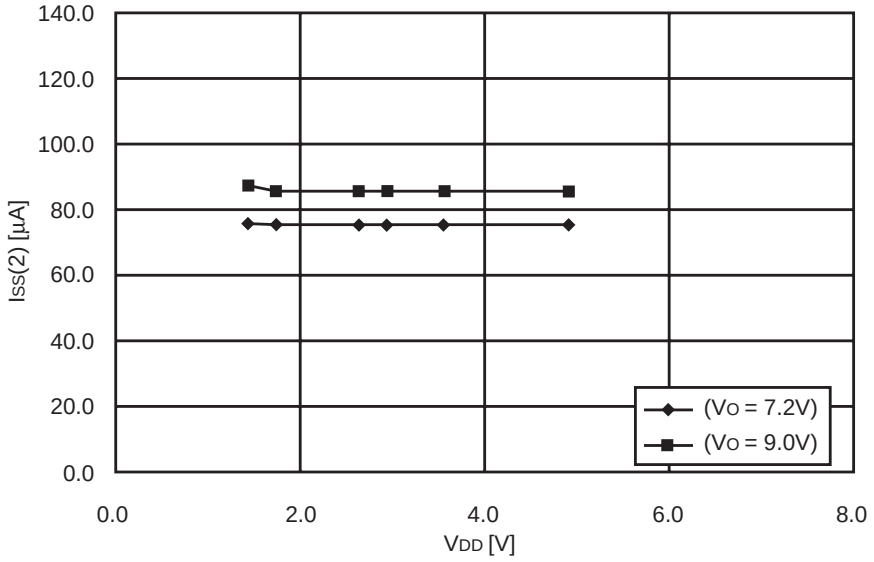
◊ Dynamic operating current (2) - When LCD display is turned on with built-in power supply being connected (All-white display)



Conditions:
Built-in power supply ON
Voltage tripled
V_{DD2}-V_{SS} = 3.3V
V_{DD}-V_{SS} = 1.8V
V_0-V_{SS} = 7.2V
V_0-V_{SS} = 9.0V
Ta = 25°C
Display pattern: All-white.
Remarks: See * 12.

Figure 18

◊ Dynamic operating current (2) - When LCD display is turned on with built-in power supply being connected (Checker pattern display)

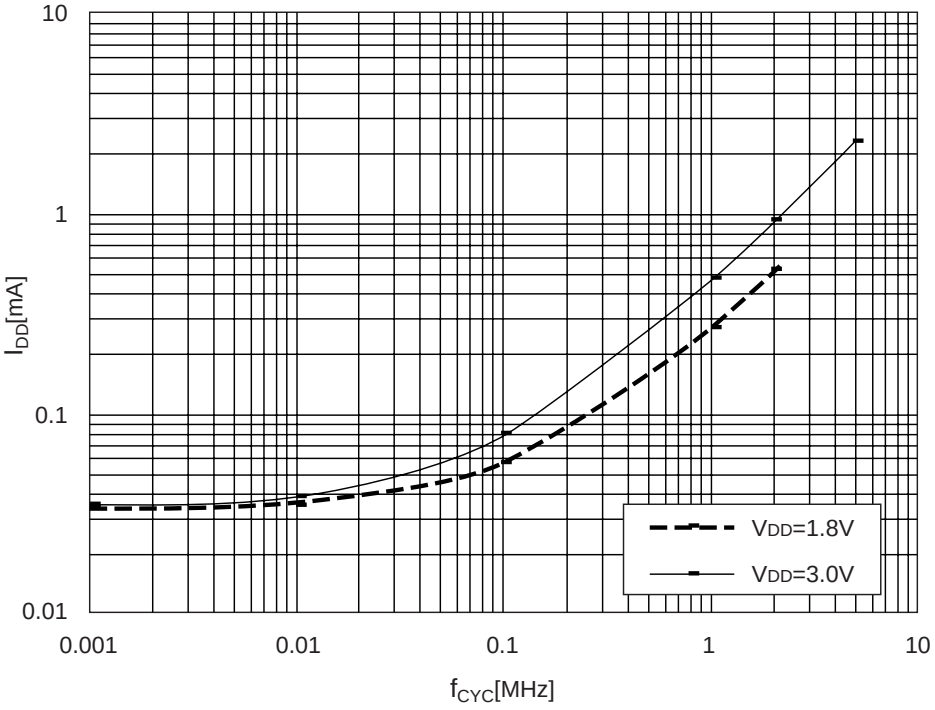


Conditions:
Built-in power supply ON
Voltage tripled
V_{DD2}-V_{SS} = 3.3V
V_{DD}-V_{SS} = 1.8V
V_0-V_{SS} = 7.2V
V_0-V_{SS} = 9.0V
Ta = 25°C
Display pattern: Checker.
Remarks: See * 12.

Figure 19

[Reference data 3]

◊ Dynamic operating current (3) - During an access is being made



This chart shows current consumption when the checker pattern write is constantly implemented in f_{CYC}.
Iss (1) alone is consumed when an access is not taking place.

Conditions:
Built-in power supply OFF
External power supply ON
V_{DD2}—V_{SS}=3.0V
V_0—V_{SS}=9.0V
Ta=25¡C

Figure 20

[Reference data 4]
◊ Operating voltage range of V_{DD} and V_0 systems.

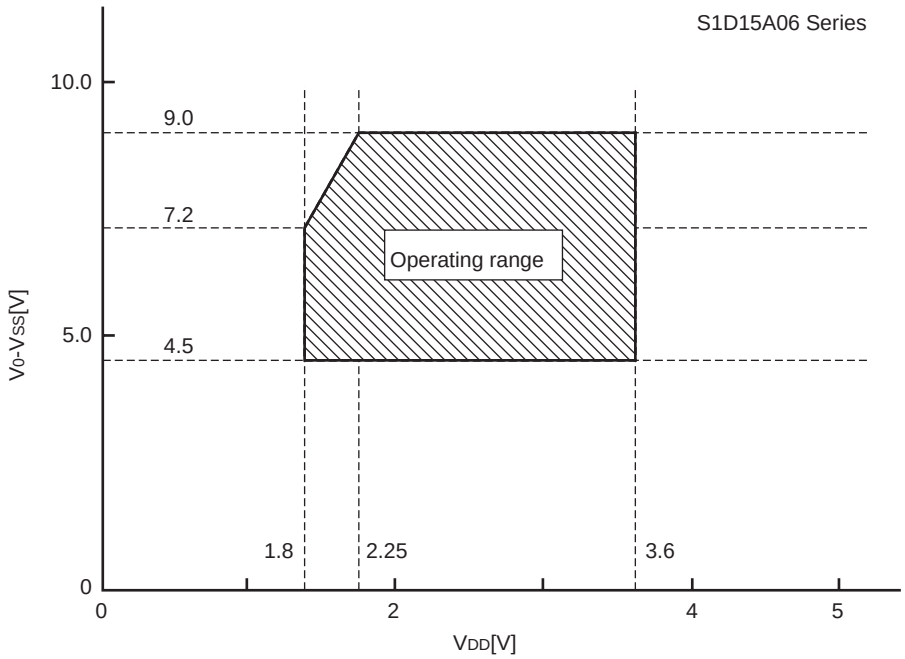


Figure 21

[Reference items]

* 1 : Although wide operating voltage range is warranted, an exemption to it is when an access made by MPU is accompanied with radical voltage fluctuations.
* 2 : See Figure 21 for the operating voltage range of V_{DD} and V_0 systems. It is applicable when an external power supply is used.
* 3 : A0, D0 to D5, D6 (SCL), D7 (SI), $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), CS, CL, C86, P/S and $\overline{RES}$ pins. $V_{IH} = 0.8 \times V_{DD}$ to V_{DD}, $V_{IL} = V_{SS}$ to $0.2 \times V_{DD}$ when $V_{DD} = 1.8V$ to 2.7V.
* 4 : D0 to D7 pins. $I_{OH} = -0.25mA$, $I_{OL} = 0.25mA$ when $V_{DD} = 1.8V$ to 2.7V.
* 5 : A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS}$, C86, CL and $\overline{RES}$ pins.
* 6 : It is applicable when D0 to D5, D6 (SCL) and D7 (SI) pins are placed in high impedance.
* 7 : It represents the resistance value to be employed when 0.1V is applied across the output pin SEGn or COMn and respective power terminals (V_1, V_2, V_3 and V4). It must be selected within the operating voltage range (3). $R_{ON} = 0.1V/\Delta I$ (ΔI represents the current conducted when 0.1V is applied when the power supply is turned on).
* 8 : For the relationship between the oscillating frequency and frame frequency, refer to Table 6. External inputs listed in the standard value space are recommended values.
* 9 : Adjustment of the V_0 voltage adjustment circuit must be done within the operating voltage range of the voltage follower circuit.
* 10 : The built-in reference voltage source of the V_0 voltage adjustment circuit. Two types of V_{REG} temperature gradients are supported by the S1D15A06; (1) Approximately –0.1%/°C and (2) External input.
* 11/12 : The built-in oscillation circuit is used. It indicates current consumed by the independent IC when the display is turned on. Current consumption of the S1D15A06 indicated here is one when the 1/6 bias mode is turned on. It does not includes current consumed due to the LCD panel capacity or wiring capacity (driver output is under no-load). These values are applicable when an access is not made by MPU.
* 12 : These values are applicable when the V_0 voltage adjusting built-in resistors are used on an S1D15A06 model with V_{REG} optional temperature gradient of –0.1%/°C.

11. AC CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080-series MPU)

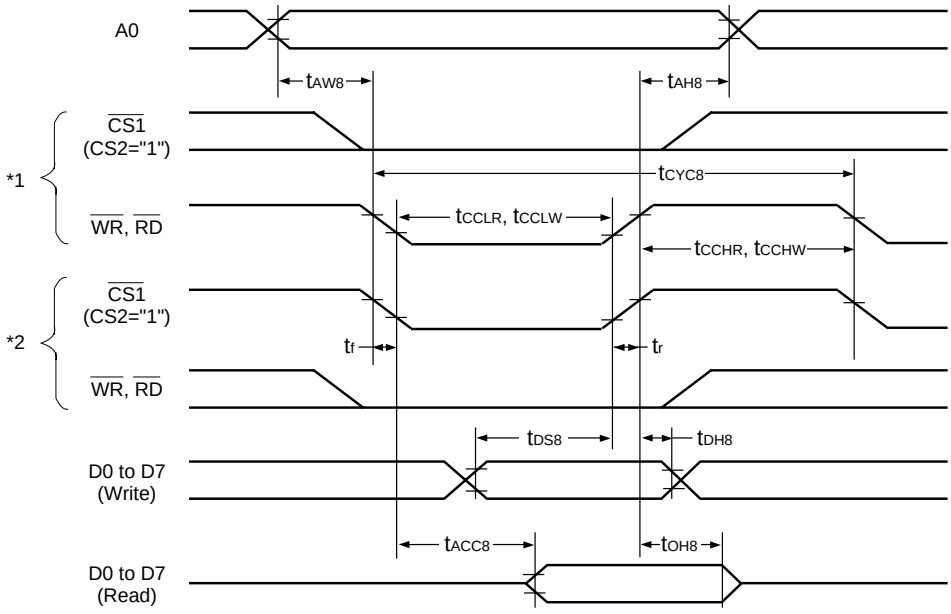


Figure 22

Table 26 [V_{DD}=2.7V to 3.6V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Min.	Max.	Units
Address hold time	A0	t_{AH8}		0	–	ns
Address setup time		t_{AW8}		0	–	
System cycle time		t_{CYC8}		500	–	
Control LOW pulse width(Write)	$\overline{WR}$	t_{CCLW}		100	–	
Control LOW pulse width(Read)	$\overline{RD}$	t_{CCLR}		200	–	
Control HIGH pulse width(Write)	$\overline{WR}$	t_{CCHW}		100	–	
Control HIGH pulse width(Read)	$\overline{RD}$	t_{CCHR}		100	–	
Data setup time	D7 to D0	t_{DS8}		70	–	
Data hold time		t_{DH8}		0	–	
Access time		t_{ACC8}	CL=100pF	–	180	
Output disable time		t_{OH8}		10	100	

Table 27 [V_{DD}=1.8V to 2.7V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Min.	Max.	Units
Address hold time	A0	t_{AH8}		0	–	ns
Address setup time		t_{AW8}		0	–	
System cycle time		t_{CYC8}		1000	–	
Control LOW pulse width(Write)	$\overline{WR}$	t_{CCLW}		150	–	
Control LOW pulse width(Read)	$\overline{RD}$	t_{CCLR}		300	–	
Control HIGH pulse width(Write)	$\overline{WR}$	t_{CCHW}		150	–	
Control HIGH pulse width(Read)	$\overline{RD}$	t_{CCHR}		150	–	
Data setup time	D7 to D0	t_{DS8}		120	–	
Data hold time		t_{DH8}		0	–	
Access time		t_{ACC8}	CL=100pF	–	260	
Output disable time		t_{OH8}		10	200	

*1. This is in the case of making the access by $\overline{WR}$ and $\overline{RD}$, setting the $\overline{CS1}$=LOW.
*2. This is in the case of making the access by $\overline{CS1}$, setting the $\overline{WR}$, $\overline{RD}$=LOW.
*3. The rise and fall times (tr and tf) of the input signal are specified for less than 15 ns. When using the system cycle time at high speed, they are specified for (tr+tf) $\leqq$ (t_{CYC8}-t_{CCLW}) or (tr+tf) $\leqq$ (t_{CYC8}-t_{CCLR}-t_{CCHR}).
*4. All timings are specified based on the 20 and 80% of V_{DD}.
*5. t_{CCLW} and t_{CCLR} are specified for the overlap period when $\overline{CS1}$ is at LOW (CS2=HIGH) level and $\overline{WR}$,$\overline{RD}$ are at the LOW level.

System Bus Read/Write Characteristics 2 (For the 6800-series MPU)

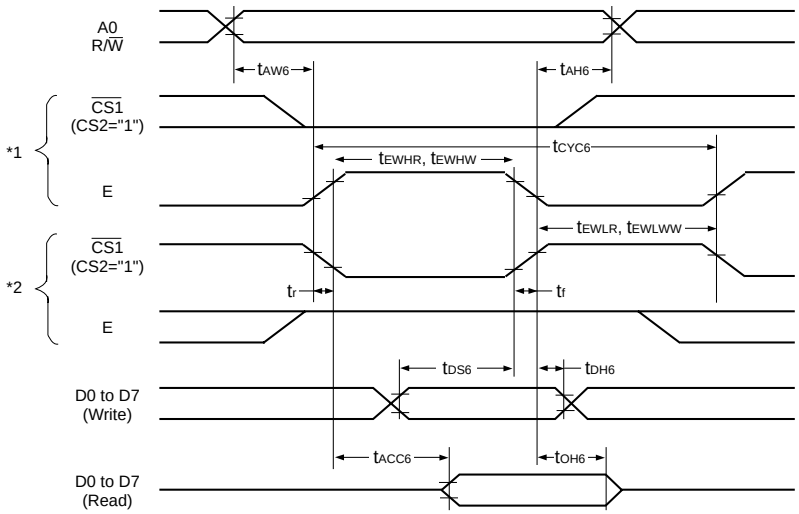


Table 28 Figure 23 [V_{DD}=2.7V to 3.6V, Ta=–40 to 85°C]

Item		Signal	Symbol	Condition	Min.	Max.	Units
Address hold time		A0,	t_{AH6}		0	–	ns
Address setup time		$\overline{WR}$	t_{AW6}		0	–	
System cycle time			t_{CYC6}		500	–	
Enable	width	E	t_{EWHW}		100	–	
HIGH pulse width	Read		t_{EWHR}		200	–	
Enable	width		t_{EWLW}		100	–	
LOW pulse width	Read		t_{EWLR}		100	–	
Data setup time		D7 to D0	t_{DS6}		70	–	
Data hold time			t_{DH6}		0	–	
Access time			t_{ACC6}	CL=100pF	–	180	
Output disable time			t_{OH6}		10	100	

Table 29 [V_{DD}=1.8V to 2.7V, Ta=–40 to 85°C]

Item		Signal	Symbol	Condition	Min.	Max.	Units
Address hold time		A0,	t_{AH6}		0	–	ns
Address setup time		$\overline{WR}$	t_{AW6}		0	–	
System cycle time			t_{CYC6}		1000	–	
Enable	width	E	t_{EWHW}		150	–	
HIGH pulse width	Read		t_{EWHR}		300	–	
Enable	width		t_{EWLW}		150	–	
LOW pulse width	Read		t_{EWLR}		150	–	
Data setup time		D7 to D0	t_{DS6}		120	–	
Data hold time			t_{DH6}		0	–	
Access time			t_{ACC6}	CL=100pF	–	260	
Output disable time			t_{OH6}		10	200	

*1. This is in the case of making the access by E, setting the $\overline{CS1}$=LOW.
*2. This is in the case of making the access by $\overline{CS1}$, setting the E=HIGH.
*3. The rise and fall times (tr and tf) of the input signal are specified for less than 15 ns. When using the system cycle time at high speed, they are specified for (tr+tf) $\leqq$ (t_{CYC6}-t_{EWLW}-t_{EWHW}) or (tr+tf) $\leqq$ (t_{CYC6}-t_{EWLR}-t_{EWHR}).
*4. All timings are specified based on the 20 and 80% of V_{DD}.
*5. t_{EWLW} and t_{EWLR} are specified for the overlap period when $\overline{CS1}$ is at LOW (CS2=HIGH) level and E is at the HIGH level.

Serial interface

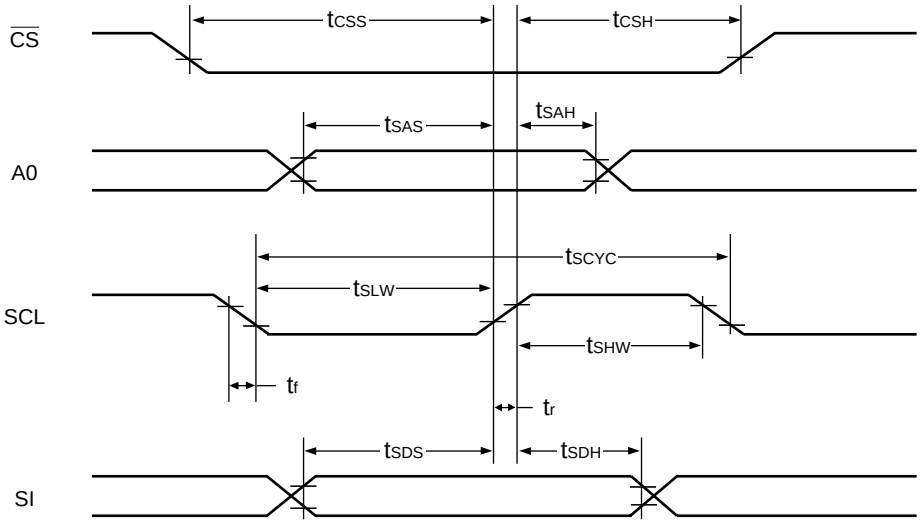


Figure 24

Table 30 [V_{DD}=2.7V to 3.6V, Ta=–40 to 85°C]

Parameter	Signal	Symbol	Condition	Min.	Max.	Units
Serial clock cycle	SCL	t_{SCYC}		125	–	ns
Serial clock HIGH pulse width		t_{SHW}		50	–	
Serial clock LOW pulse width		t_{SLW}		50	–	
Address setup time	A0	t_{SAS}		75	–	
Address hold time		t_{SAH}		75	–	
Data setup time	SI	t_{SDS}		50	–	
Data hold time		t_{SDH}		50	–	
$\overline{CS}$ serial clock time	$\overline{CS}$	t_{CSS}		75	–	
		t_{CSH}		75	–	

Table 31 [V_{DD}=1.8V to 2.7V, Ta=–40 to 85°C]

Parameter	Signal	Symbol	Condition	Min.	Max.	Units
Serial clock cycle	SCL	t_{SCYC}		200	–	ns
Serial clock HIGH pulse width		t_{SHW}		75	–	
Serial clock LOW pulse width		t_{SLW}		75	–	
Address setup time	A0	t_{SAS}		75	–	
Address hold time		t_{SAH}		75	–	
Data setup time	SI	t_{SDS}		50	–	
Data hold time		t_{SDH}		50	–	
$\overline{CS}$ serial clock time	$\overline{CS}$	t_{CSS}		100	–	
		t_{CSH}		100	–	

Note : 1. The input Signal rise and fall times must be with in 15ns.
2. Every timing is specified on the basis of 20% and 80% of V_{DD}.

Reset timing

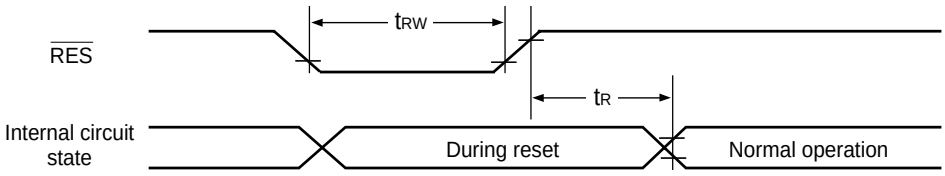


Figure 25

Table 32 [V_{DD}=2.7V to 3.6V, Ta=–40 to 85°C]

Parameter	Signal	Symbol	Condition	Min.	Max.	Units
Reset time		t_R		–	1000	ns
Reset LOW pulse width	$\overline{RES}$	t_{RW}		1000	–	

Table 33 [V_{DD}=1.8V to 2.7V, Ta=–40 to 85°C]

Parameter	Signal	Symbol	Condition	Min.	Max.	Units
Reset time		t_R		–	1500	ns
Reset LOW pulse width	$\overline{RES}$	t_{RW}		1500	–	

Note : 1. The input Signal rise and fall times must be with in 15ns.
2. Every timing is specified on the basis of 20% and 80% of V_{DD}.

12. MPU INTERFACE (EXAMPLES)

The S1D15A06 series can be directly connected to the 80 series MPU or 68 series MPU. Adding a serial interface allows you to drive the S1D15A06 with less number of signal lines.

After initialization is completed from the $\overline{RES}$ pin, make sure that respective input pins on the S1D15A06 series are normally controlled.

(1) 80 series MPU

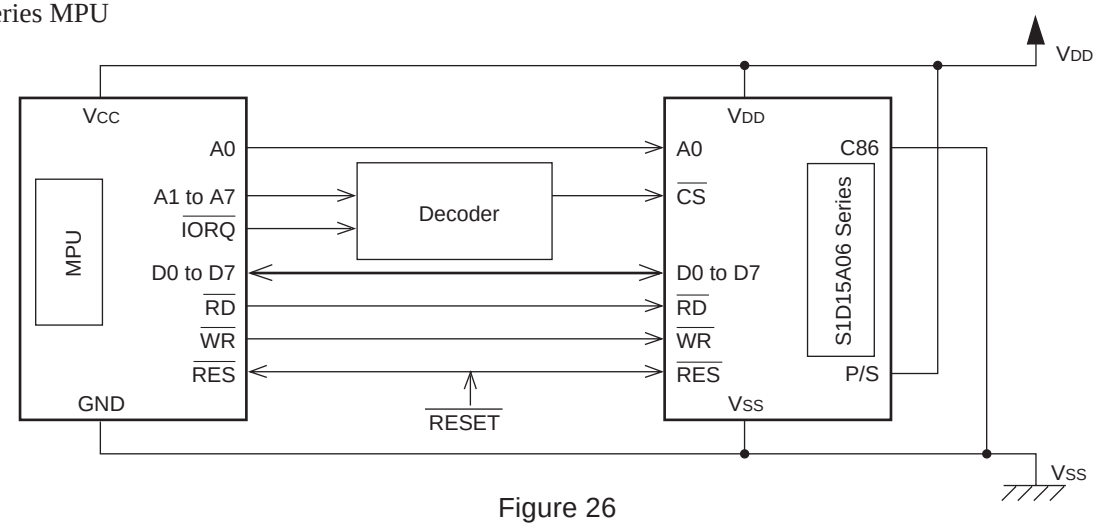


Figure 26

(2) 68 series MPU

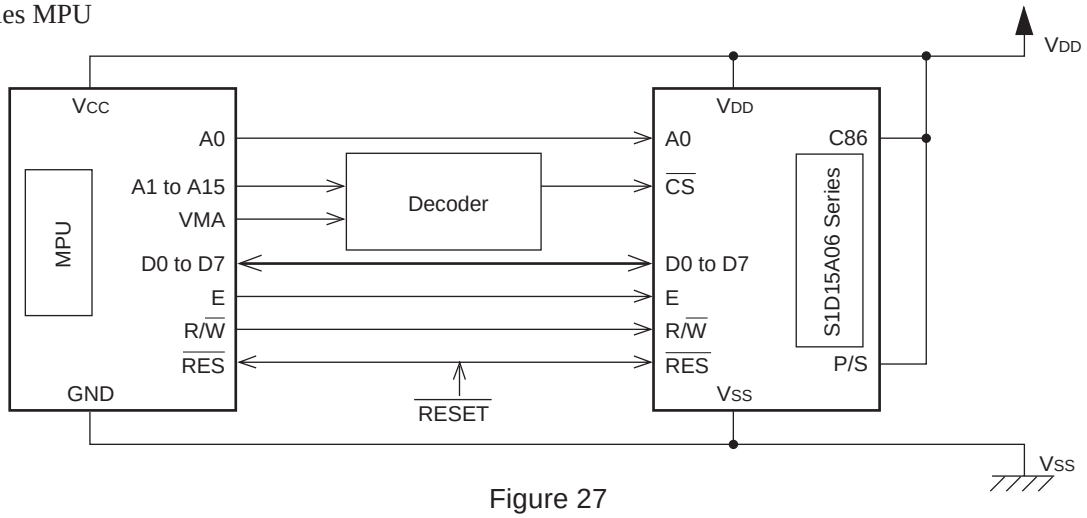


Figure 27

(3) Serial interface

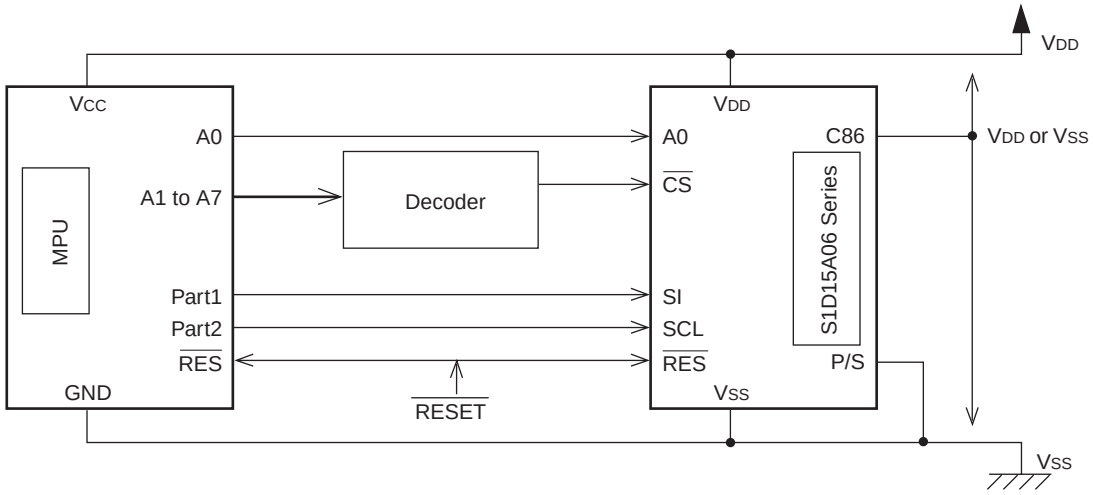


Figure 28

13. S1D15B01 Series

Contents

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1. DESCRIPTION

The S1D15B01 series is a single-chip liquid crystal display (=LCD) driver for dot-matrix LCDs that can be connected directly to a microprocessor (=MPU) bus. It accepts 8-bit parallel or serial display data from a MPU, stores it in an on-chip display data RAM (=DDRAM), and generates a LCD drive signal independent of the MPU clock.
The use of the on-chip DDRAM of 65×132 bits and a one-to-one correspondence between LCD panel pixel dots and on-chip DDRAM bits offer high flexibility in graphic display.
The S1D15B01 series does not need external operation clock for DDRAM read/write operations, and has a on-chip LCD power supply circuit featuring very low current consumption with few external components, and moreover has a on-chip CR oscillator circuit.
Consequently, the S1D15B01 can be realize a high-performance handy display system with a minimum current consumption and the fewest components.

2. FEATURES

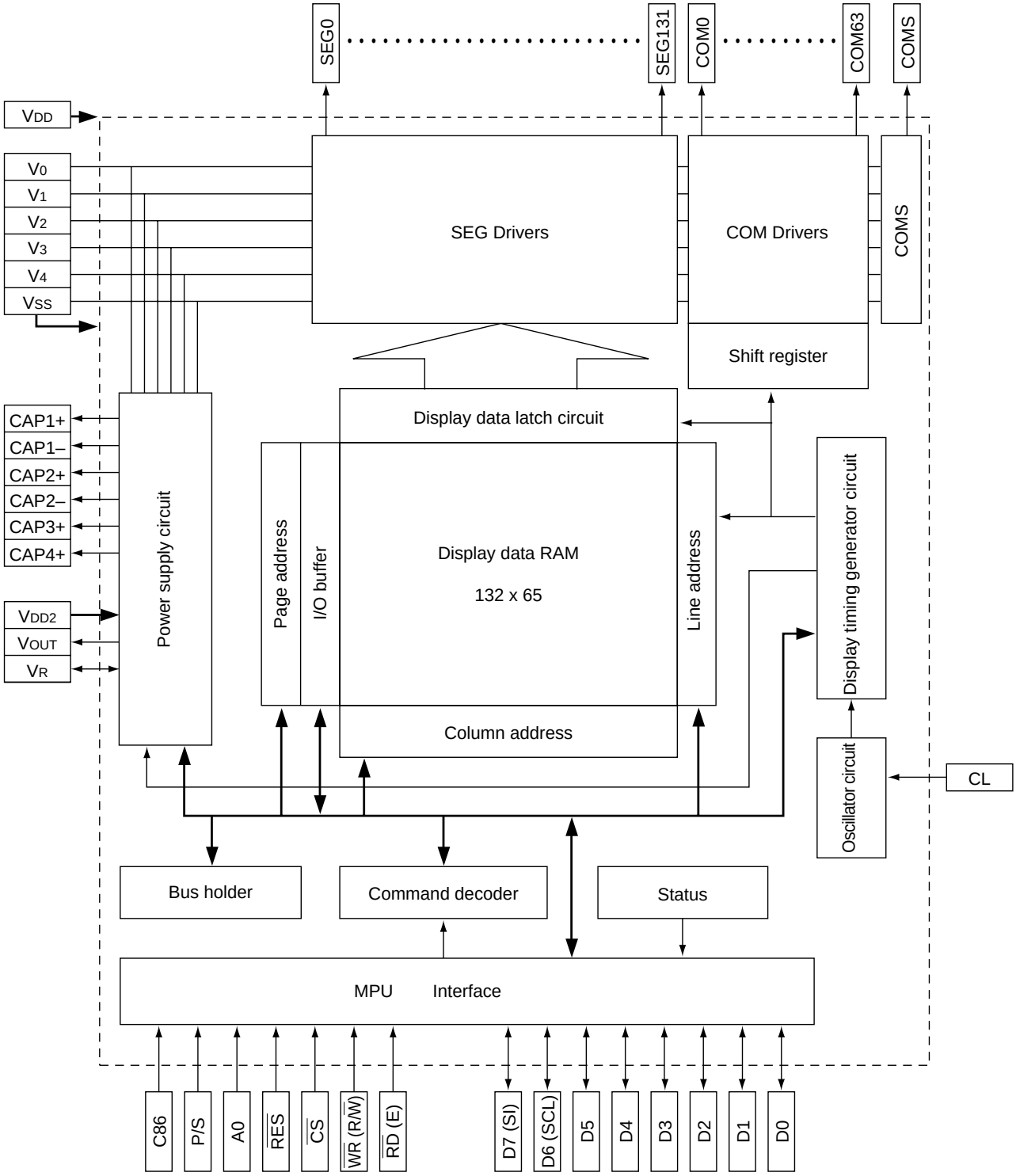
- Direct display by DDRAM :
  Bit data of DDRAM "0" .... a dot of display is OFF
  "1" .... a dot of display is ON
  (at Display normal)
- DDRAM capacity : 65×132=8580bits
- High-speed 8-bit Serial interface/8-bit MPU interface (The chip can be connected directly to both the 8080-series MPUs and the 6800-series MPUs) .
- Many command functions :
  Display ON/OFF, Display normal/reverse, Display all points ON/OFF,
  Page address set, Column address set, Display start line address set,
  Segment/Common driver direction select,
  Display data Read/Write ,Read modify write,
  Power control set, Electronic contrast control, LCD bias set,
  Power saver, Reset
- On-chip low power supply circuit for LCD driving voltage generation
  Booster circuit (with boost ratios of Double/Triple/Quadruple/Quintuple)
  Voltage regulator circuit (with high-accuracy electronic voltage adjustment function)
  Voltage follower (with V_1 to V_4 voltage dividing resistors)
- On-chip CR oscillation circuit (external clock can also be input.)
- Very low power consumption
- Power supply :
  Logic power supply : V_{DD}-V_{SS}=1.7 to 5.5V
  Booster reference supply : V_{DD2}-V_{SS}=1.7 to 5.5V
  LCD driving power supply : V_0-V_{SS}=4.5 to 16.0V
- Wide range of operating temperatures -40 to 85°C
- CMOS process
- Package : Au bump chip and TCP
- These ICs are not designed for strong radio/optical activity proof.

Series Specifications

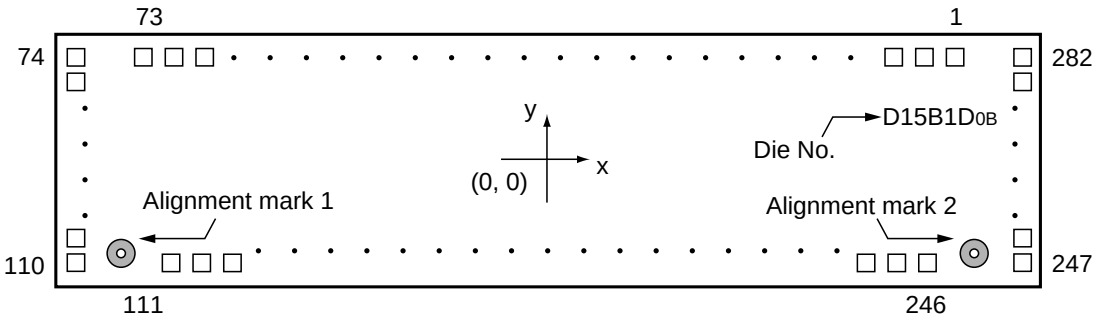
Product Name	Duty	Bias	SEG Dr	COM Dr	V_{REG} Temperature Gradient	Voltage Condition	Shipping Forms
S1D15B01D00B*	1/65	1/9,1/7	132	65	–0.05%/˚C	Internal voltage	Bare Chip
S1D15B01D01B	1/65	1/9,1/7	132	65	–0.05%/˚C	V_0 or V_{OUT}	Bare Chip external voltage
S1D15B01D02B	1/65	1/9,1/7	132	65	–0.05%/˚C	V_0 ~ V_4 extarnal	Bare Chip voltage
*S1D15B01T00**	1/65	1/9,1/7	132	65	–0.05%/˚C		TCP

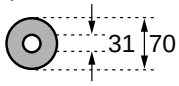
* : Start the development on demands
** : Under development

3. BLOCK DIAGRAM



4. PIN LAYOUT



Chip size	10.82mm×2.81mm		
Bump pitch	70μm (Min.)		
Bump size	PAD No.1 to 73	91μm×	91μm
	PAD No.74 to 110	91μm×	45.5μm
	PAD No.111 to 246	45.5μm×	91μm
	PAD No.247 to 282	91μm×	45.5μm
Bump height	17μm (Typ.)		
Chip thickness	625μm		
Ground bias	VSS		
Alignment mark 1	Center coordinates (μm)	(–4965, –1231)	
	Size (μm)		
Alignment mark 2	Center coordinates (μm)	(4947, –1224)	
	Size (μm)		

Pad Center Coordinates

Unit: µm

PAD No.	Pin Name	X	Y
1	(NC)	4852	1248
2	(NC)	4722	
3	TEST0	4592	
4	TEST1	4462	
5	TEST2	4332	
6	V_{SS}	4202	
7	TEST3	4072	
8	TEST4	3942	
9	TEST5	3812	
10	$\overline{RES}$	3682	
11	$\overline{CS}$	3552	
12	V_{SS}	3422	
13	$\overline{WR}$	3292	
14	$\overline{RD}$	3162	
15	V_{DD}	3032	
16	CL	2902	
17	A0	2772	
18	D7,SI	2642	
19	D6,SCL	2512	
20	D5	2382	
21	D4	2252	
22	D3	2122	
23	D2	1992	
24	D1	1862	
25	D0	1732	
26	V_{DD}	1602	
27	V_{DD}	1472	
28	V_{DD}	1342	
29	V_{DD2}	1212	
30	V_{DD2}	1082	
31	V_{DD2}	952	
32	TEST6	822	
33	V_{DD}	692	
34	P/S	562	
35	C86	432	
36	V_{SS}	302	
37	TEST7	172	
38	TEST8	3	
39	TEST9	–166	
40	V_{SS}	–335	
41	V_{SS}	–465	
42	V_{SS}	–595	
43	(NC)	–725	
44	V_{OUT}	–855	
45	V_{OUT}	–985	
46	V_{OUT}	–1115	
47	(NC)	–1245	
48	TEST10	–1414	
49	TEST11	–1583	
50	TEST12	–1713	
51	TEST13	–1882	1248
52	V_{SS}	–2051	
53	V_R	–2181	
54	V_0	–2311	
55	V_1	–2441	
56	V_2	–2571	
57	V_3	–2701	
58	V_4	–2831	
59	CAP2+	–2961	
60	CAP2+	–3091	
61	CAP2–	–3221	
62	CAP2–	–3351	
63	CAP4+	–3481	
64	CAP4–	–3611	
65	V_{OUT}	–3741	
66	CAP1+	–3871	
67	CAP1+	–4001	
68	CAP1–	–4131	
69	CAP1–	–4261	
70	CAP3+	–4391	
71	CAP3+	–4521	
72	(NC)	–4651	
73	(NC)	–4781	
74	(NC)	–5255	1264
75	(NC)		1194
76	COM31		1124
77	COM30		1054
78	COM29		984
79	COM28		913
80	COM27		843
81	COM26		774
82	COM25		703
83	COM24		633
84	COM23		562
85	COM22		492
86	COM21		422
87	COM20		352
88	COM19		282
89	COM18		211
90	COM17		141
91	COM16		71
92	COM15		1
93	COM14		–69
94	COM13		–140
95	COM12		–210
96	COM11		–280
97	COM10		–350
98	COM9		–420
99	COM8		–491
100	COM7		–561
101	COM6	–5255	–631
102	COM5		–701
103	COM4		–771
104	COM3		–842
105	COM2		–912
106	COM1		–982
107	COM0		–1052
108	COMS		–1122
109	(NC)		–1193
110	(NC)		–1263
111	(NC)	–4738	–1248
112	(NC)	–4668	
113	SEG0	–4598	
114	SEG1	–4528	
115	SEG2	–4458	
116	SEG3	–4388	
117	SEG4	–4317	
118	SEG5	–4247	
119	SEG6	–4177	
120	SEG7	–4107	
121	SEG8	–4037	
122	SEG9	–3966	
123	SEG10	–3896	
124	SEG11	–3826	
125	SEG12	–3756	
126	SEG13	–3686	
127	SEG14	–3615	
128	SEG15	–3545	
129	SEG16	–3475	
130	SEG17	–3405	
131	SEG18	–3335	
132	SEG19	–3264	
133	SEG20	–3194	
134	SEG21	–3124	
135	SEG22	–3054	
136	SEG23	–2984	
137	SEG24	–2913	
138	SEG25	–2843	
139	SEG26	–2773	
140	SEG27	–2703	
141	SEG28	–2633	
142	SEG29	–2562	
143	SEG30	–2492	
144	SEG31	–2422	
145	SEG32	–2352	
146	SEG33	–2282	
147	SEG34	–2211	
148	SEG35	–2141	
149	SEG36	–2071	
150	SEG37	–2001	

Unit: µm

PAD No.	Pin Name	X	Y
151	SEG38	–1931	–1248
152	SEG39	–1860	
153	SEG40	–1790	
154	SEG41	–1720	
155	SEG42	–1650	
156	SEG43	–1580	
157	SEG44	–1509	
158	SEG45	–1439	
159	SEG46	–1369	
160	SEG47	–1299	
161	SEG48	–1229	
162	SEG49	–1158	
163	SEG50	–1088	
164	SEG51	–1018	
165	SEG52	–948	
166	SEG53	–878	
167	SEG54	–807	
168	SEG55	–737	
169	SEG56	–667	
170	SEG57	–597	
171	SEG58	–527	
172	SEG59	–456	
173	SEG60	–386	
174	SEG61	–316	
175	SEG62	–246	
176	SEG63	–176	
177	SEG64	–105	
178	SEG65	–35	
179	SEG66	35	
180	SEG67	105	
181	SEG68	175	
182	SEG69	246	
183	SEG70	316	
184	SEG71	386	
185	SEG72	456	
186	SEG73	526	
187	SEG74	597	
188	SEG75	667	
189	SEG76	737	
190	SEG77	807	
191	SEG78	877	
192	SEG79	948	
193	SEG80	1018	
194	SEG81	1088	
195	SEG82	1158	
196	SEG83	1228	
197	SEG84	1299	
198	SEG85	1369	
199	SEG86	1439	
200	SEG87	1509	

PAD No.	Pin Name	X	Y
201	SEG88	1579	–1248
202	SEG89	1650	
203	SEG90	1720	
204	SEG91	1790	
205	SEG92	1860	
206	SEG93	1930	
207	SEG94	2001	
208	SEG95	2071	
209	SEG96	2141	
210	SEG97	2211	
211	SEG98	2281	
212	SEG99	2352	
213	SEG100	2422	
214	SEG101	2492	
215	SEG102	2562	
216	SEG103	2632	
217	SEG104	2703	
218	SEG105	2773	
219	SEG106	2843	
220	SEG107	2913	
221	SEG108	2983	
222	SEG109	3054	
223	SEG110	3124	
224	SEG111	3194	
225	SEG112	3264	
226	SEG113	3334	
227	SEG114	3405	
228	SEG115	3475	
229	SEG116	3545	
230	SEG117	3615	
231	SEG118	3685	
232	SEG119	3756	
233	SEG120	3826	
234	SEG121	3896	
235	SEG122	3966	
236	SEG123	4036	
237	SEG124	4107	
238	SEG125	4177	
239	SEG126	4247	
240	SEG127	4317	
241	SEG128	4387	
242	SEG129	4458	
243	SEG130	4528	
244	SEG131	4598	
245	(NC)	4668	
246	(NC)	4738	
247	(NC)	5248	–1225
248	COM32		–1155
249	COM33		–1085
250	COM34		–1015

PAD No.	Pin Name	X	Y
251	COM35	5248	–944
252	COM36		–874
253	COM37		–804
254	COM38		–734
255	COM39		–664
256	COM40		–593
257	COM41		–523
258	COM42		–453
259	COM43		–383
260	COM44		–313
261	COM45		–242
262	COM46		–172
263	COM47		–102
264	COM48		–32
265	COM49		38
266	COM50		109
267	COM51		179
268	COM52		249
369	COM53		319
270	COM54		389
271	COM55		460
272	COM56		530
273	COM57		600
274	COM58		670
275	COM59		740
276	COM60		811
277	COM61		881
278	COM62		951
279	COM63		1021
280	COMS		1091
281	(NC)		1162
282	(NC)		1232

5. PIN DESCRIPTION

Power supply pins

Name	I/O	Description	Number of pins
V_{DD}	Supply	Power supply. Connect to MPU power pin V_{CC}.	5
V_{DD2}	Supply	Externally-input reference power supply for booster circuit.	3
V_{SS}	Supply	This is a 0V terminal connected to the system GND.	7
V_0, V_1, V_2 V_3, V_4	Supply	Multi-level power supply for LCD drive. The voltages are determined by LCD cell.The voltages should maintain the following relationship : $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$. When on-chip power supply circuit turns on, V_0 voltage are generated, and the following voltages are generated to V_1 to V_4. Either voltage can be selected by LCD bias set command.	5

	SED15B1
V_1	6/7 • V_0, 8/9 • V_0
V_2	5/7 • V_0, 7/9 • V_0
V_3	2/7 • V_0, 2/9 • V_0
V_4	1/7 • V_0, 1/9 • V_0

LCD power supply circuit pins

Name	I/O	Description	Number of pins
CAP1+	O	Boosting capacitor positive connection pin.	2
CAP1–	O	Boosting capacitor negative connection pin.	2
CAP2+	O	Boosting capacitor positive connection pin.	2
CAP2–	O	Boosting capacitor negative connection pin.	2
CAP3+	O	Boosting capacitor positive connection pin.	2
CAP4+	O	Boosting capacitor positive connection pin.	2
V_{OUT}	O	Booster output.	4
V_R	I	Voltage adjustment pin. Provides V_0 voltage using external resistors. When internal resistors are used, this pin cannot be used.	1

System bus connection pins

Name	I/O	Description	Number of pins
D7 to D0 (SI) (SCL)	I/O	8-bit bi-directional data bus to be connected to the standard 8-bit or 16-bit MPU data bus. When the serial interface is selected (P/S=LOW) ; D7 : Serial data input (SI) D6 : Serial clock input (SCL)	8
A0	I	Control/data flag input. A0=HIGH : The data on D7 to D0 is display data. A0=LOW : The data on D7 to D0 is control data.	1
$\overline{CS}$	I	Chip select input. Data input is enable when $\overline{CS}$ is low.	1
$\overline{RES}$	I	When $\overline{RES}$ is caused to go low, initialization is executed. A reset operation is performed at the $\overline{RES}$ signal level.	1

Pin name	I/O	Description	Number of pins
$\overline{RD}$ (E)	I	• When connected to an 8080-series MPU ; This is active-LOW. This pin is connected to the $\overline{RD}$ signal of the 8080-series MPU. While this signal is low, SED15B1 series data bus is an output status. • When connected to an 6800-series MPU ; This is active-HIGH. This is used as an enable clock input pin of the 6800-series MPU.	1
$\overline{WR}$ (R/$\overline{W}$)	I	• When connected to an 8080-series MPU ; This is active-LOW. This pin is connected to the $\overline{WR}$ signal of the 8080-series MPU. The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal. •When connected to an 6800-series MPU ; This is the read/write control signal input . R/$\overline{W}$=HIGH : Read. R/$\overline{W}$=LOW : Write.	1
C86	I	MPU interface selection pin. C86=HIGH : 6800-series MPU interface C86=LOW : 8080-series MPU interface	1
P/S	I	Serial data input/parallel data input selection pin. P/S=HIGH : Parallel data input P/S=LOW : Serial data input The following applies depending on the P/S status :	1

P/S	Data/Command	Data	Read/Write	Serial Clock
HIGH	A0	D7 to D0	$\overline{RD}$, $\overline{WR}$	
LOW	A0	SI (D7)	Write only	SCL (D6)

In serial mode, no data can be read from DDRAM.
When P/S=LOW,D5 to D0 are HZ. D5 to D0 may be HIGH, LOW or Open, and moreover A0, $\overline{RD}$, $\overline{WR}$, C86 may be HIGH, LOW or Open.

LCD driver pins

Name	I/O	Description	Number of pins
CL	I	External clock input. When external clock is halted, CL must be LOW. If internal clock (on-chip CR oscillation circuit) is selected, CL connected to V_{DD}.	1
SEG0 to SEG131	O	LCD segment driver output.	132
COM0 to COM63	O	LCD common driver output.	64
COMS	O	LCD common driver output for the indicator. When it is not used, it is made open.	2

Test pins

Name	I/O	Description	Number of pins
TEST0 to TEST13	I/O	These are terminals for IC chip testing. TEST1 to TEST4 are recommended to connect to V_{DD} or V_{SS}.The others set to open.	14

Note and caution

- If control signal from MPU is HZ, an over-current may flow through the IC. A protection is required to prevent the HZ signal at the input pins.

6. FUNCTIONAL DESCRIPTION

Microprocessor Interface

Interface type selection

The S1D15B01 series can transfer data via 8-bit bi-directional data buses (D7 to D0) or via serial data input (SI). Through selecting the P/S pin polarity to the HIGH or LOW, it is possible to select either 8-bit parallel data input or 8-bit serial data input as shown in Table 1.

Table 1

P/S	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
HIGH:Parallel Input	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
LOW:Serial Input	$\overline{CS}$	A0	–	–	–	SI	SCL	–

– : HIGH, LOW or Open

Parallel interface

When the parallel interface has been selected (P/S= HIGH), then it is possible to connect directly to either an 8080-series MPU or a 6800-series MPU (as shown in Table 2) by selecting C86 pin to either HIGH or LOW.

Table 2

C86	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0
HIGH:6800-series MPU bus	$\overline{CS}$	A0	E	R/$\overline{W}$	D7 to D0
LOW:8080-series MPU bus	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0

Moreover, the S1D15B01 series identifies the data bus signal according to A0, $\overline{RD}$(E), $\overline{WR}$(R/$\overline{W}$) signals, as shown in Table 3.

Table 3

Common	6800-series	8080-series		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	0	1	0	Writes control data (command)

Serial interface

When the serial interface has been selected (P/S= LOW),only writing display data and control data is possible by four input signals. The serial data input (SI) and serial clock input (SCL) are enabled when $\overline{CS}$ is low. When chip is not selected, the shift register and counter which compose serial interface are reset.
The serial data is read from the serial data input pin in the rising edge of the serial clocks D7,D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the eighth serial clock for the processing.
The A0 input is used to determine whether the serial data input is display data or command data; when A0=HIGH, the data is display data, and when A0=LOW then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active.
Figure 1 is a serial interface signal chart.

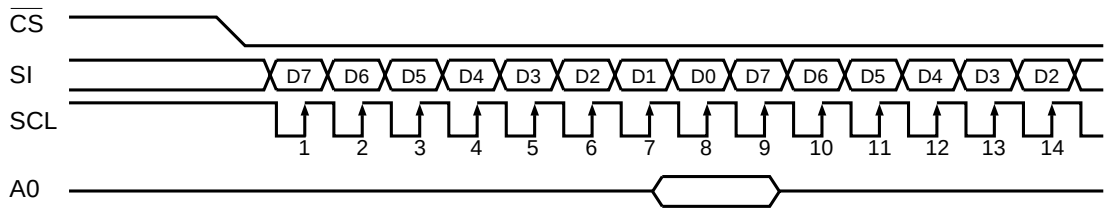


Figure 1

* When the chip is not active, the shift registers and the counter are reset to their states.
* Reading is not possible while in serial interface mode.
* Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

Chip select input

The MPU interface (either parallel or serial) is enabled only when $\overline{CS}$=LOW.
When the chip select is inactive, D7 to D0 enter a high impedance state, and A0, $\overline{RD}$ and $\overline{WR}$ inputs are disabled. When the serial interface is selected, the shift register and the counter are reset.

Access to DDRAM and internal registers

In accessing the DDRAM and the internal registers of the S1D15B01 series, the MPU is required to satisfy the only cycle time (t_{CYC}), and is not needed to consider the wait time. Accordingly, it is possible to transfer data at higher speed.

In order to realize the higher speed accessing, the S1D15B01 series can perform a type of pipeline processing between LSIs using bus holder of internal data bus when data is sent from/to the MPU. For example, when the MPU writes data to the DDRAM, once the data is stored in the bus holder, then it is written to the DDRAM before the next data write cycle. And when the MPU reads the contents of the DDRAM, the first data read cycle (dummy read cycle) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle. Thus, there is a certain restriction in the DDRAM read sequence. When an address is set, the specified address data is NOT output at the immediately following read instruction. The address data is output during second data read. A single dummy read must be inserted after address setup and after write cycle (refer to Figure 2).

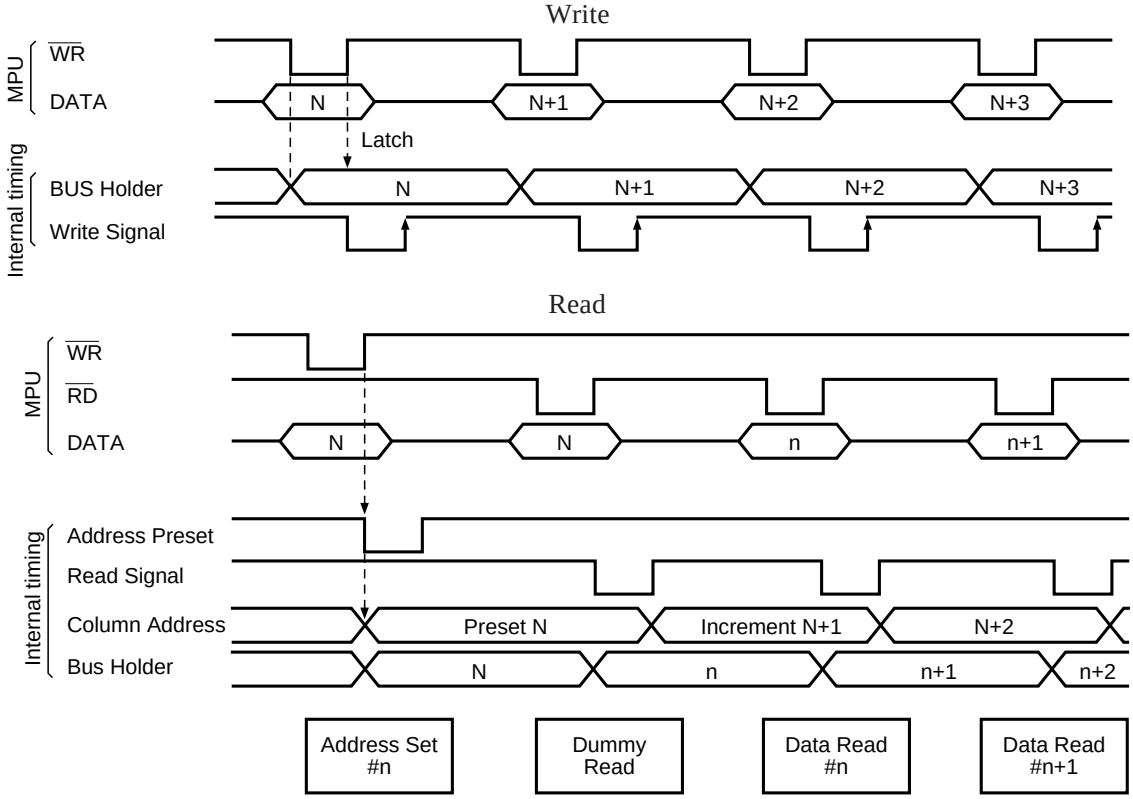


Figure 2

DDRAM and page/column address circuit

The DDRAM stores pixel data for LCD. It is a 65-row (8 page by 8 bit + 1) by 132-column addressable array.

As is shown in Figure 3, the D7 to D0 display data from the MPU corresponds to the LCD common direction.

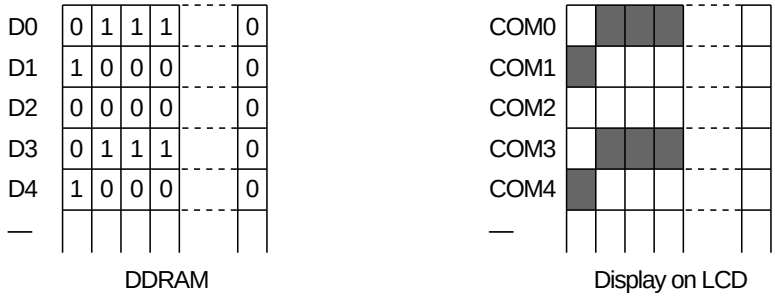


Figure 3

Each pixel can be selected when page address and column address are specified(refer to Figure 5).
The MPU issues Page address set command to change the page and access to another page. Page address 8 (D3,D2,D1,D0 = 1,0,0,0) is DDRAM area dedicate to the indicator, and display data D0 is only valid.
The DDRAM column address is specified by Column address set command. The specified column address is automatically incremented by +1 when a Display data read/write command is entered. After the last column address (83H), column address returns to 00H and page address incremented by +1 (refer to Figure 4). After the very last address (column = 83H,page = 8H),both column address and page address return to 00H (column address = 00H, page address = 0H).

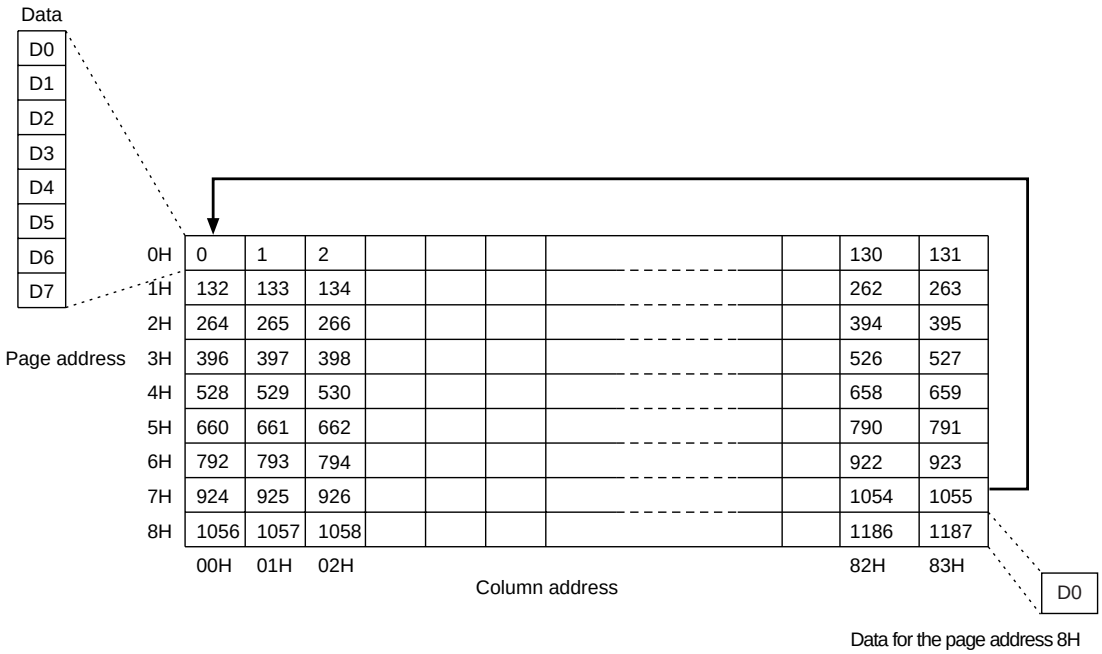


Figure 4

The MPU reads from and writes to the DDRAM through the I/O buffer independent of the LCD controller operation. Therefore, data can be written to the DDRAM at the same time as data is being displayed, without causing the LCD to flicker.

Furthermore, as is shown in Table 4, Segment driver direction select command can be used to reverse the relationship between the DDRAM column address and segment output. This allows flexible IC layout during LCD module assembly.

Table 4

Column Address	00H	01H	02H		81H	82H	83H
Normal Direction	SEG0	SEG1	SEG2		SEG129	SEG130	SEG131
Reverse Direction	SEG131	SEG130	SEG129		SEG2	SEG1	SEG0

Line address circuit

The line address circuit specifies the line address (as shown Figure 5) relating to the COM output when the contents of the DDRAM are displayed. The display start line address, what is normally the top line of the display, can be specified by Display start line address set command. And Common driver direction select command can be used to reverse the relationship between the DDRAM line address and common output. For example, as is shown in Table 5, the display start line address corresponds to the COM0 output when the common driver direction is normal, or the COM63 output when common driver direction is reversed.And the display area is followed by the higher number line addresses in ascending order from the display start line address, corresponding to the duty cycle. This allows flexible IC layout during LCD module assembly.
If the display start line address is changed dynamically using the Display start line address set command,then screen scrolling and page swapping can be performed.

Table 5 (at display start line address=1CH)

Line Address	1CH	1DH		3FH	00H		1AH	1BH
Normal Direction	COM0	COM1		COM35	COM36		COM62	COM63
Reverse Direction	COM63	COM62		COM28	COM27		COM1	COM0

Display data latch circuit

The display data latch circuit is a latch temporarily stored the display data that is output to the LCD driver circuit from the DDRAM.
Display ON/OFF command, Display normal/reverse command, and Displayed all points ON/OFF command control only the data within the latch, and do not change the data within the DDRAM.

Display Data RAM

The display data RAM stores pixel data for the LCD.
It is a 132-columm×65-row addressale array as shown in Figure 5.

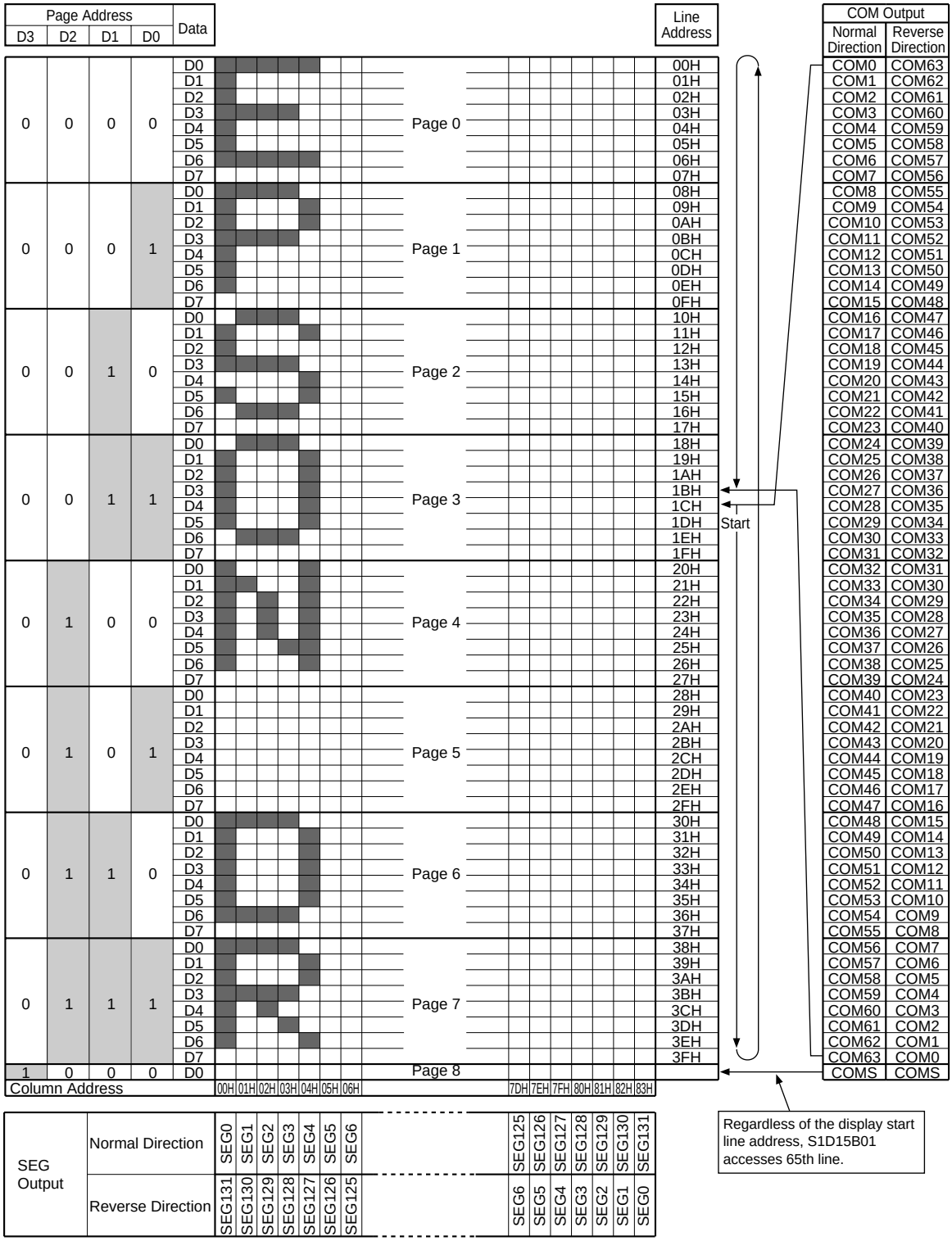


Figure 5

Oscillation circuit

The S1D15B01 series has a complete on-chip CR oscillation circuit, and its output is used as the display timing signal source.
The on-chip oscillation circuit is available when CL = HIGH.
And the S1D15B01 series is also capable external clock input from CL pin. (When external clock is halted, CL must be LOW.)

Display timing generator circuit

The display timing generator circuit generates the timing signals from the display clocks to the line address circuit and the display data latch circuit. The display data is latched to the display data latch circuit and is output to the segment drive output pin by synchronizing to the display clocks. The read operation of display data to the liquid crystal drive circuit is completely independent of the access to the display data RAM from MPU. Therefore even when the display data RAM is asynchronously accessed during liquid crystal display, the access will not have any adverse effect on the display such as flickering.
The circuit also generates COM scan signal and the LCD AC signal (FR) from the display clocks. As shown in Figure 6, the FR normally generates the 2- frame AC drive waveforms .

2-frame AC drive waveforms

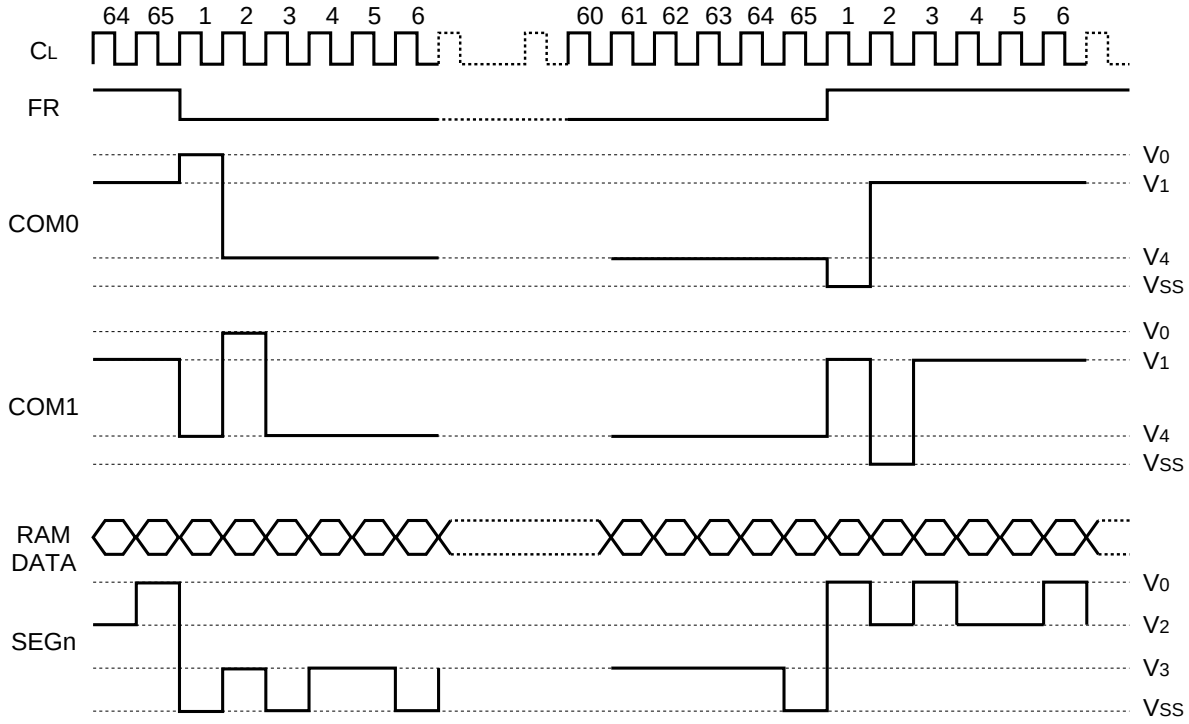


Figure 6

LCD driver circuits

These are multiplexers outputting the LCD panel driving 4-level signal which level is determined by a combination of display data, COM scan signal, and LCD AC signal (FR). Figure 7 shows an example of SEG and COM output waveforms.

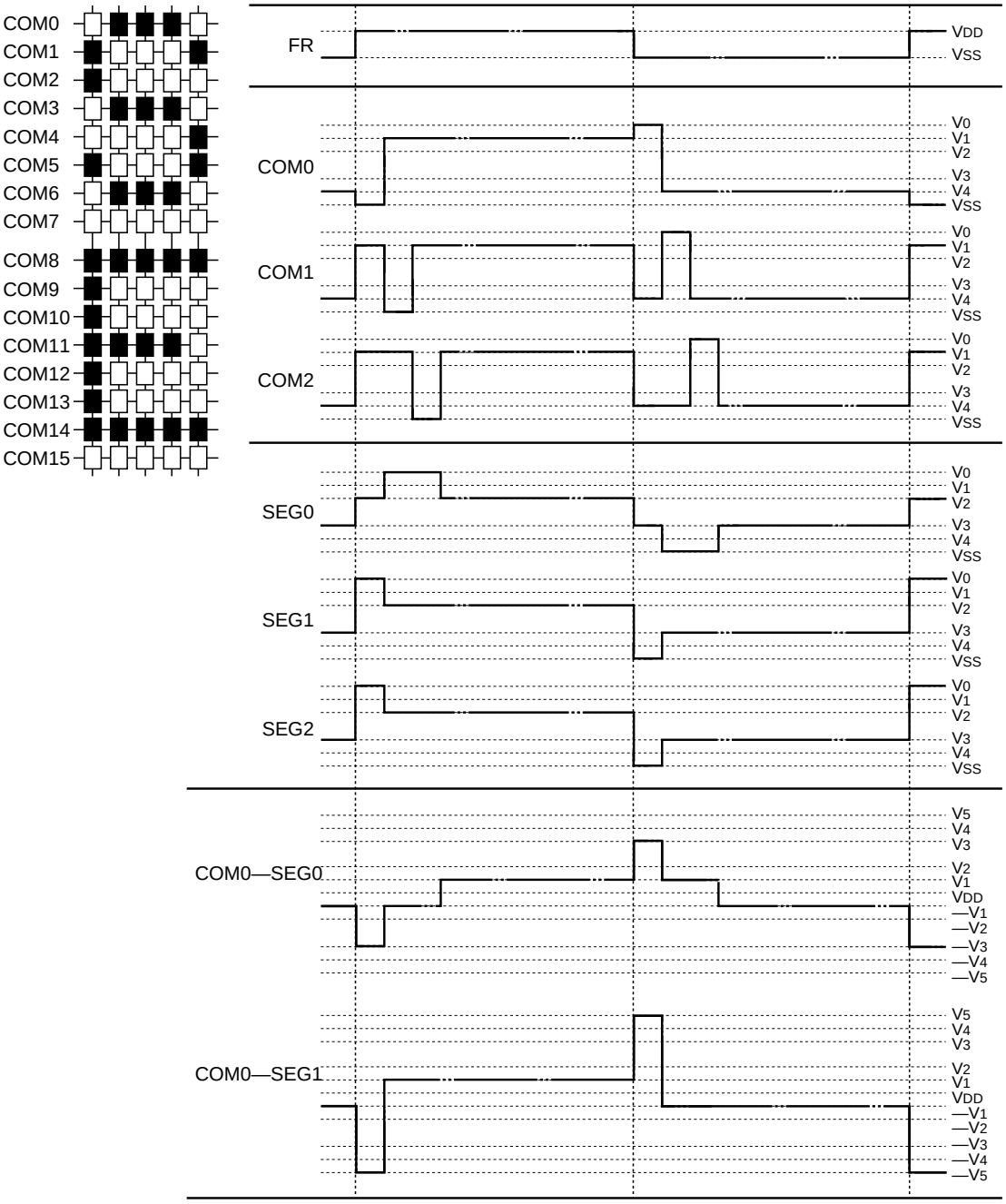


Figure 7

Power supply circuit

The power supply circuit generates the voltage to drive the LCD panel at low power consumption.
The power supply circuit consists of a booster circuit, voltage regulator circuit, and voltage follower circuit, and is controlled by Power control set command. Using this command, the booster circuit, the voltage regulator circuit, and the voltage follower circuit can be independently turned ON or OFF. In the case of using S1D15B01D00B* which use a booster circuit, voltage regulator circuit, and voltage follower circuit, every circuit is required to be turnend ON or OFF at the same time by Power control set command. In the case of using S1D15B01D00B*/S1D15B01D02B* which need the external power supply and use part of on-chip power supply circuit, each must be set the appropriate state as shown in the Table 6.

Table 6

Power supply condition	Product name*2	Booster circuit	Voltage regulator circuit	Voltage follower circuit	External voltage input	Boosting system pin*3
On-chip power supply used	S1D15B01D00B*	ON	ON	ON	V_{DD2}	Used
Voltage regulator circuit and Voltage follower circuit only	S1D15B01D01B*	OFF	ON	ON	V_{OUT}	Open
Voltage follower circuit only	S1D15B01D01B*	OFF	OFF	ON	V_0=V_{OUT}*4	Open
External power supply only	S1D15B01D02B*	OFF	OFF	OFF	V_0=V_{OUT}*4 V_1 to V_4	Open

*1 Combinations other than those shown in above table are possible but impractical.
*2 Chose the appropriate product according to the power supply condition.
*3 The boosting system pin indicates the CAP+, CAP1–, CAP2+, CAP2–, CAP3+, and CAP4+ pin.
*4 Both V_0 pin and V_{OUT} pin should be connected to external power supply.

Booster circuit

Using the booster circuit, it is possible to produce Quintuple/Quadruple/Triple/Double boosting of the V_{DD2}-V_{SS} voltage level.

Quintuple boosting :
Connect capacitor between CAP1+ and CAP1–, between CAP2+ and CAP2–, between CAP3+ and CAP1–, between CAP4+ and CAP2–, between V_{OUT} and V_{DD2}, the potential between V_{DD2} and V_{SS} is boosted to quintuple toward the positive side and it is output at V_{OUT} pin.

Quadruple boosting :
Connect capacitor between CAP1+ and CAP1–, between CAP2+ and CAP2–, between CAP3+ and CAP1–, between V_{OUT} and V_{DD2}, and jumper between CAP4+ and V_{OUT}, the potential between V_{DD2} and V_{SS} is boosted to quadruple toward the positive side and it is output at V_{OUT} pin.

Triple boosting :
Connect capacitor between CAP1+ and CAP1–, between CAP2+ and CAP2–, between V_{OUT} and V_{DD2}, and jumper between CAP3+, CAP4+ and V_{OUT}, the triple boosted voltage appears at V_{OUT} pin.

Double boosting :
Connect capacitor between CAP1+ and CAP1–, between V_{OUT} and V_{DD2}, open CAP2–, and jumper between CAP2+, CAP3+, CAP4+ and V_{OUT}, the double boosted voltage appears at V_{OUT} pin.

The boosted voltage relationships are shown in Figure 8.

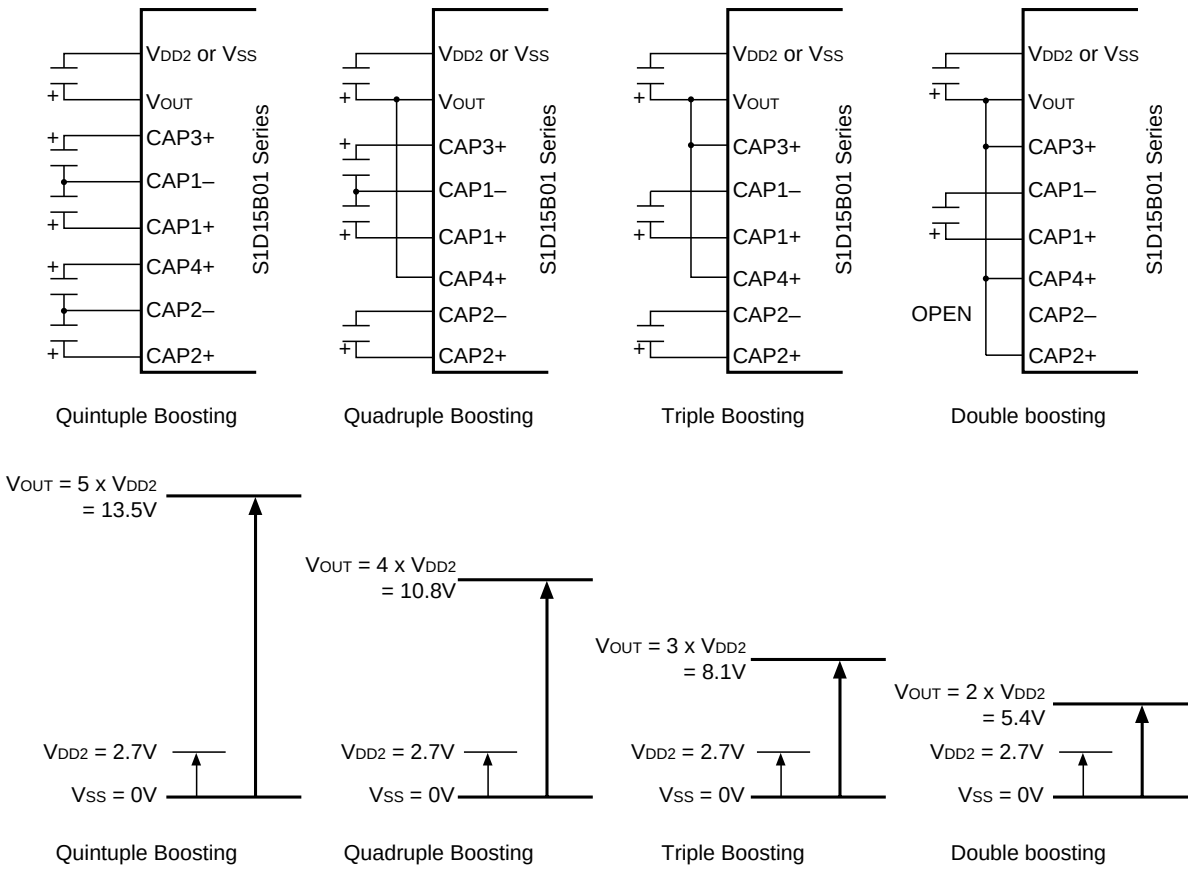


Figure 8

* V_{DD2} voltage must be set so that V_{OUT} voltage does not exceed the absolute maximum rated value.
* The Capacitance depend on the load of the LCD panel to be driven. Set a value that LCD driver voltage may be stable (reference value = 1.0 to 4.7 μF).

Voltage regulator circuit

The boosting voltage occurring at the V_{OUT} pin is sent to the voltage regulator, and the V_0 voltage (LCD driver voltage) is output.
Because the S1D15B01 series has the high-accuracy constant voltage source, the 32-level electronic volume function and the internal resistor for the V_0 voltage regulator (= V_0-resistor), it is possible to construct a high-accuracy voltage regulator circuit without external component. And V_0 voltage can be adjusted by commands only to adjust the LCD contrast.
(A) When the V_0-resistor is used.
Through the use of the V_0-resistor and the electronic volume function, V_0 voltage can be controlled by commands only (without adding any external resistors). The V_0 voltage can be calculated using the following equations within the range of $V_0 < V_{OUT}$.

$$V_0 = (1+Rb/Ra) \cdot V_{EV}$$

$$V_{EV} = (1-\alpha/200) \cdot V_{REG} \quad \text{(Equation A-1)}$$

V_{REG} is the on-chip constant voltage as shown in Table 7 at Ta=25°C.

Table 7

Model	V_{REG}	Thermal Gradient
S1D15B01*****	1.3V	–0.05%/°C

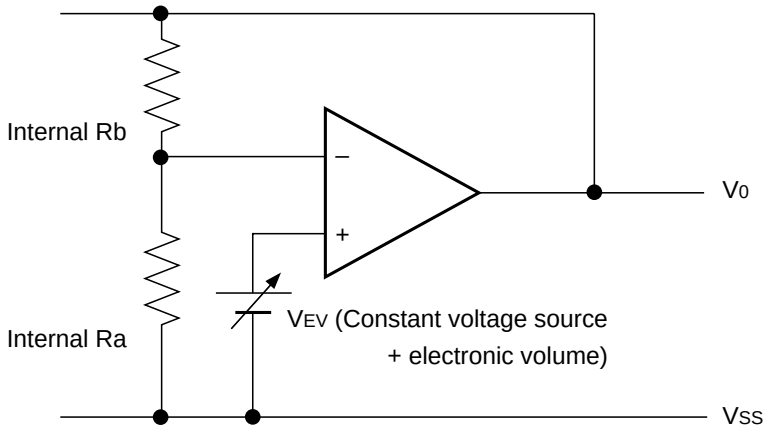


Figure 9

α is a value of the electronic volume, and can be set to one of 32-states by Electronic volume command setting the 5-bit data in the electronic volume register. Table 8 shows the value of α.

Rb/Ra is the V0-resistor ratio, and can be set to one of 7-states by V0-resistor ratio set command setting the 3-bit data in the V0-resistor ratio register. Table 9 shows the value of (1+Rb/Ra) ratio (reference value).

Table 8

D4	D3	D2	D1	D0	α
0	0	0	0	0	31
0	0	0	0	1	30
0	0	0	1	0	29
		⋮			⋮
1	1	1	0	1	2
1	1	1	1	0	1
1	1	1	1	1	0

Table 9

			1+Rb/Ra
D3	D2	D1	S1D15B01
0	0	0	5.60
0	0	1	5.86
0	1	0	6.15
0	1	1	6.46
1	0	0	6.81
1	0	1	7.20
1	1	0	7.64
1	1	1	External resistor can be used.

Figure 10 shows V0 voltage measured by V0-resistor ratio and electronic voltage at Ta=25°C.

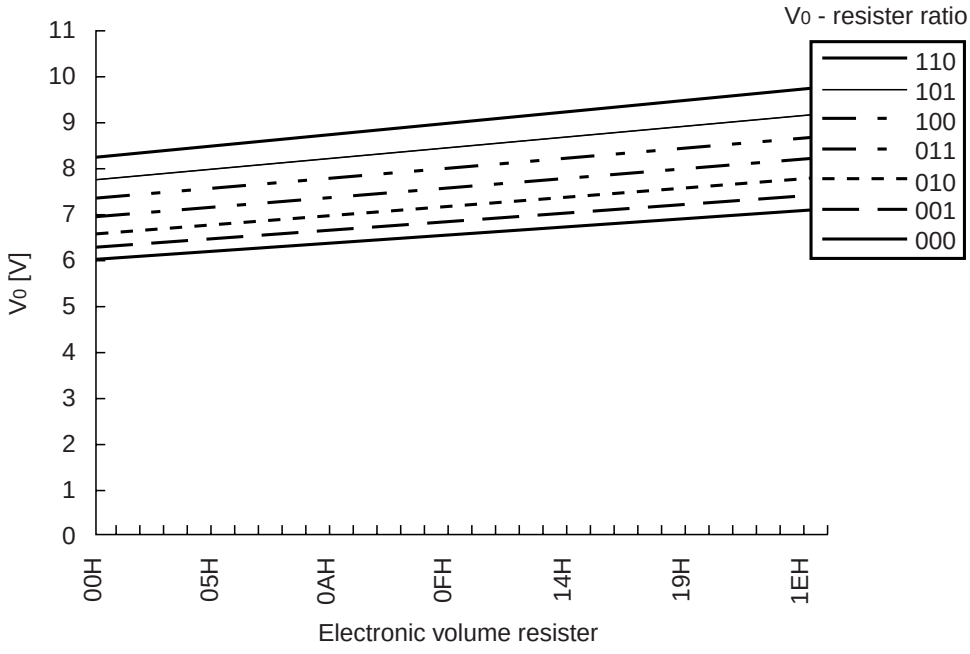


Figure 10

<Setup example>
When selection Ta=25°C and V_0=7V for S1D15B01 series on which temperature gradient=–0.05%/°C. Using Figure 10 and equation A-1, the following setup is enabled.

Table 10

Commands	Register							
	D7	D6	D5	D4	D3	D2	D1	D0
V_0-resister ratio set	0	0	1	0	0	0	0	1
Electronic volume	1	0	0	1	0	0	0	1

In this case, the variable range and the notch width of the V_0 voltage is shown as Table 11, as dependent on the electronic volume.

Table 11

V_0	Min.	Typ.	Max.	Units
Variable range	6.44[α=31]	7.05[α=15]	7.62[α=0]	[V]
Notch width		37		[mV]

(B) When external resistors are used. (1)

(The V_0-resistor is not used.)

The V_0 voltage can also be set without using the V_0-resistor by adding resistors Ra' and Rb' between V_{SS} and V_R, and between V_R and V_0, respectively. In this case, the electronic volume command makes it possible to adjust the contrast of the LCD by controlling V_0 voltage. In the range where $V_0 < V_{OUT}$, the V_0 voltage can be calculated using equation B-1 based on the external resistors Ra' and Rb'.

$$V_0=(1+Rb'/Ra')\cdot V_{EV}$$

$$V_{EV}=(1-\alpha/200)\cdot V_{REG} \qquad \text{(Equation B-1)}$$

V_{REG} is the on-chip constant voltage as shown in Table 8 at Ta=25°C.

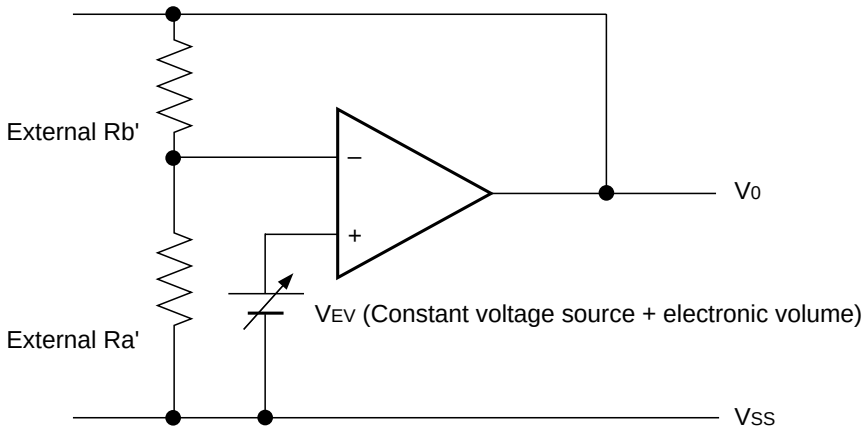


Figure 11

<Setup example>
When selection Ta=25°C and V_0=11V for S1D15B01 series on which temperature gradient=–0.05%/°C.
The central value of the electronic volume register is (D5, D4, D3, D2, D1, D0)=(1, 0, 0, 0, 0,), that is α=15.
So, according to equation B-1 and V_{REG}=1.3V, the Rb'/Ra' is shown as follows.

$$V_0 = (1+Rb'/Ra') \cdot (1-\alpha/200) \cdot V_{REG}$$

$$11V = (1+Rb'/Ra') \cdot (1-15/200) \cdot 1.3V \qquad \text{(Equation B-2)}$$

Moreover, when the value of the current running through Ra' and Rb' is set to 5 μA,

$$Ra'+Rb' = 2.2M\Omega \qquad \text{(Equation B-3)}$$

Consequently, by equation B-2 and B-3,

$$Rb'+Ra' = 8.15$$

$$Ra' = 240k\Omega$$

$$Ra' = 1960k\Omega$$

In this case, the variable range and the notch width of the V_0 voltage is, as shown Table 12, as dependent on the electronic volume.

Table 12

V_0	Min.	Typ.	Max.	Units
Variable range	10.01[α=31]	11.0[α=15]	11.9[α=0]	[V]
Notch width		59		[mV]

(C) When external resistors are used. (2)
(The V_0-resistor is not used.)
When the external resistors described above are used, adding a variable resistor as well make it possible to perform fine adjustments on Ra' and Rb', to set the V_0 voltage. In this case, the electronic volume function makes it possible to control the V_0 voltage by commands to adjust the LCD contrast. In the range where $V_0 < V_{OUT}$ the V_0 voltage can be calculated by equation C-1 below based on the R1 and R2 (variable resistors) and R3 settings, where R2 can be subjected to fine adjustments (Δ R2).

$$V_0 = \{1+(R3+R2-\Delta R2)/(R1+\Delta R2)\} \cdot V_{EV}$$

$$= \{1+(R3+R2-\Delta R2)/(R1+\Delta R2)\} \cdot (1-\alpha/200) \cdot V_{REG}$$

$$[\because V_{EV} = (1-\alpha/200) \cdot V_{REG}] \qquad \text{(Equation C-1)}$$

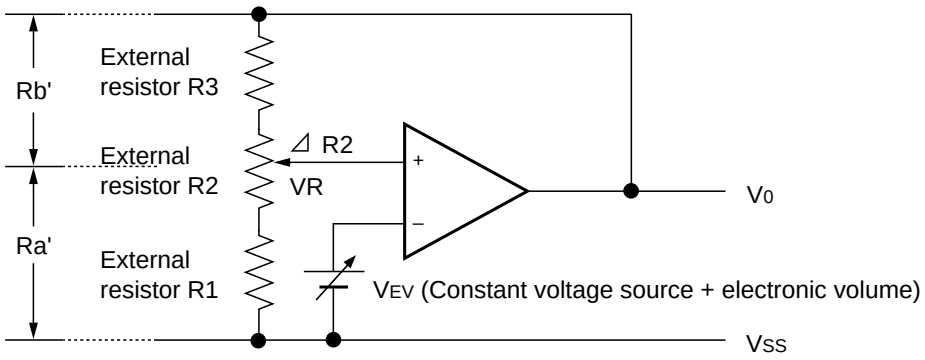


Figure 12

<Setup example>
When selection Ta=25°C and V_0=5V to V_0=9V (using R2) for S1D15B01 series on which temperature gradient=–0.05%/°C.
The central value of the electronic volume register is (D5, D4, D3, D2, D1, D0)=(1, 0, 0, 0, 0,), that is α=15.
So, according to equation C-1 and V_{REG}=1.3V, the R1, R2, R3, are shown as follows. (when Δ R2=0Ω at V_0=9V and Δ R2=R2 at V_0=5V)

$$9V = \{1+(R3+R2)/R1\} \cdot (1-15/200) \cdot 1.3V \quad \text{(Equation C-2)}$$

$$5V = \{1+R3/(R1+R2)\} \cdot (1-15/200) \cdot 1.3V \quad \text{(Equation C-3)}$$

Moreover, when the value of the current running through V_0 and V_{SS} is set to 5 μ A at V_0=7V (central value),

$$R1+R2+R3=1.4M\Omega \quad \text{(Equation C-3)}$$

With this, according to equation C-2, C-3 and C-4,

R1=187kΩ
R2=150kΩ
R3=1063kΩ

In this case, if V_0 is set to 7V as central value, Δ R2 becomes 53kΩ
And, the variable range and the notch width of the V_0 voltage is, as shown Table 13, as dependent on the electronic volume. (Δ R2=53kΩ)

Table 13

V_0	Min.	Typ.	Max.	Units
Variable range	6.41[α=31]	7.0[α=15]	7.58[α=0]	[V]
Notch width		37		[mV]

* When the V_0-resistor or the electronic volume function is used, it is necessary to at least set the voltage regulator circuit and the voltage follower circuit to an operating mode using the power control set commands. Moreover, it is necessary to provide a voltage from V_{OUT} when the Booster circuit is OFF.
* The V_R terminal is enabled only when the V_0-resistor is not used. When the V_0-resistor is used, then the V_R terminal is left open.
* Because the input impedance of the V_R terminal is high, it is necessary to take into consideration short leads, shield cables, etc. to handle noise.

Voltage Follower Circuit

The V_0 voltage is divided to generate the V_1, V_2, V_3 and V_4 voltages by on-chip resistor circuit. And the V_1, V_2, V_3 and V_4 voltages are impedance-converted by voltage follower,and provide to LCD driver circuit.
LCD bias ratio can be selected by LCD bias set command which is 1/7 bias or 1/9 bias for S1D15B01 series.

Power supply turn off sequence

Only S1D15B01D00B* which is used as on-chip power supply LCD driver, has the faculty of V_{OUT} shorts to V_{DD2} when the $\overline{RES}$ pin is LOW, and V_0 shorts to V_{SS} when the $\overline{RES}$ pin is LOW or reset command is issued. When the on-chip power supply is turned off, it is recommended to be the $\overline{RES}$ pin is LOW., for the purpose of the electric discharge on the LCD panel.
S1D15B01D00B*/S1D15B01D02B* which is used as external power supply LCD driver, don't have such a discharge faculty, so that V_{OUT} and V_0 need to short to V_{SS}, when the external power supply turn off or power saver.
See the section on the Command Description for details.

Reference Circuit Examples

Figure 13 ~ 18 shoes reference circuit examples.

(1) When used all of the booster circuit, voltage regulator circuit and V/F circuit [S1D15B01D00B∗]

① Use the voltage regulator with V0-resistor
(Example where VDD=VDD2, with 5 × boosting)

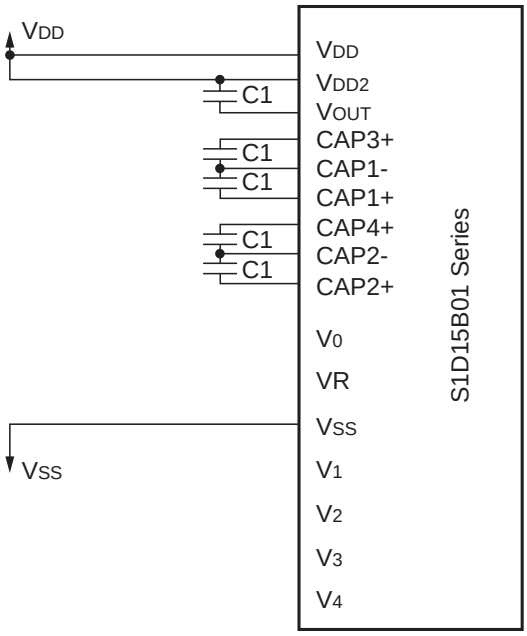


Figure 13

② Use the voltage regulator with external resistor
(Example where VDD=VDD2, with 5 × boosting)

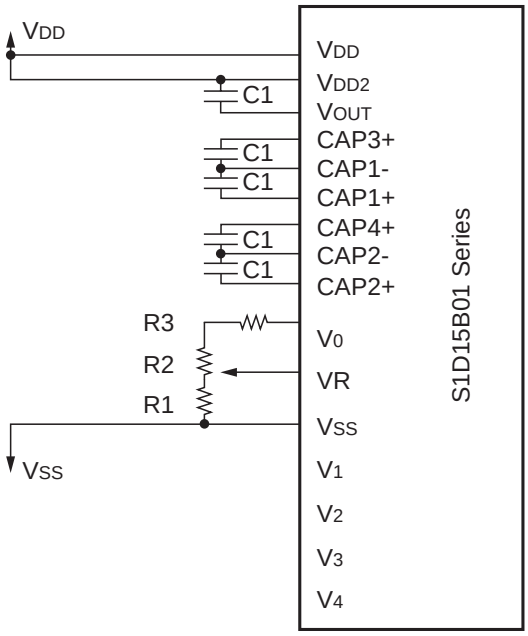


Figure 14

(2) When used only the voltage regulator circuit and V/F circuit [S1D15B01D01B∗]

① Use the voltage regulator with V0-resistor

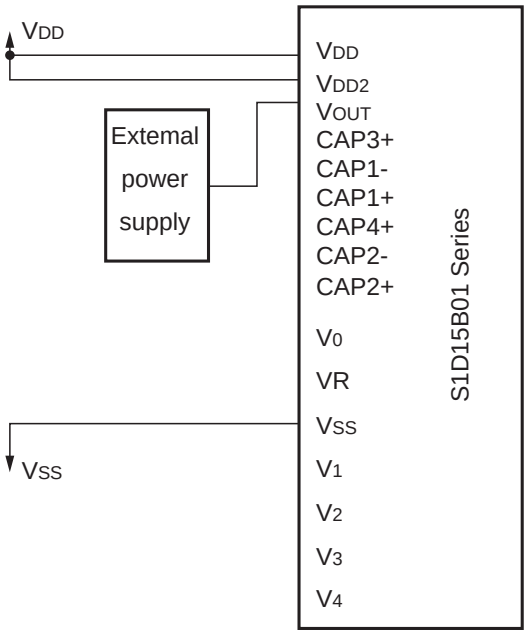


Figure 15

② Use the voltage regulator with external resistor

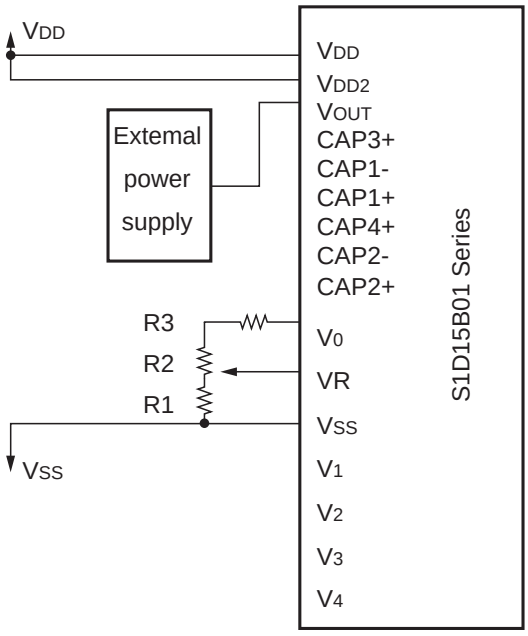


Figure 16

(3) When used only the V/F circuit
[S1D15B01D01B∗]

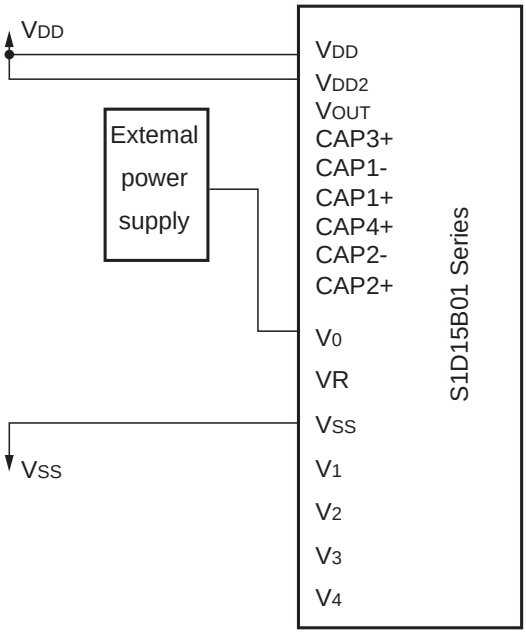


Figure 17

(4) When the on-chip power supply is not used
[S1D15B01D02B∗]

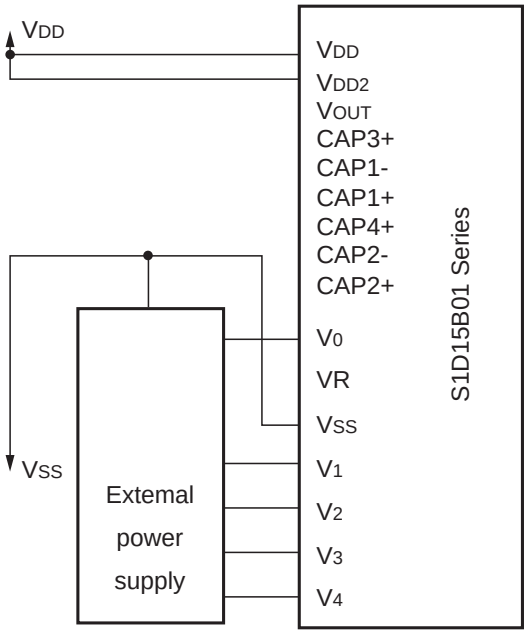


Figure 18

Example of shared reference settings
When V_0 can vary between 8 and 12V

Item	Set value	Units
C_1	1.0 ~ 4.7	µF

Figure 14

* Because the V_R terminal input impedance is high, use short leads and shield lines.

Reset Circuit

When $\overline{RES}$ pin goes low,or when Reset command is used,this LSI is initialized.
Initialized states :

- Serial interface internal shift register and counter clear
- Power saver mode is entered.
  - Oscillation circuit is stopped.
  - The LCD power supply circuit is stopped.
  - Display OFF
  - Display all points ON
  - Segment/common driver outputs go to the V_{SS} level.
- Display normal
- Page address=0H
- Column address=00H
- Display start line address=00H
- Segment driver direction = normal
- Common driver direction = normal
- Read modify write OFF
- Power control register (D2, D1, D0) = (0, 0, 0)
- V_0-resistor ratio register (D2, D1, D0) = (0, 0, 0)
- Electronic volume register (D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0)
- LCD power supply bias ratio = 1/7 bias
- Test mode is released.
- V_0 is shorted to V_{SS} *1
- V_{OUT} is shorted to V_{DD2} *1*2

When reset is detected, this LSI is set to above initialized states. However it has no effect on contents of DDRAM. As seen in "Microprocessor Interface (Reference Example)", connect $\overline{RES}$ pin to the reset pin of the MPU and initialize the MPU at the same time. The initialization by $\overline{RES}$ pin is always required during power-on.
If the control signal from MPU is HZ, an overcurrent may flow through the LSI. A protection is required to prevent the HZ signal at the input pin during power-on. In case the S1D15B01 series does not use the on-chip LCD power supply circuit, $\overline{RES}$ pin must be HIGH when the external LCD power supply is turned on.

*1 This faculty is available only S1D15B01D00B∗.
*2 This faculty is not available by reset command, it is abailable only when hard reset : $\overline{RES}$=LOW is active.

7. COMMAND DESCRIPTION

The S1D15B01 series identifies the data bus by a combination of A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$) signals.
In the 8080-series MPU interface, the command is activated when a low pulse is input to $\overline{RD}$ pin for reading and when a low pulse is input to $\overline{WR}$ pin for writing. In the 6800-series MPU interface, the S1D15B01 series enters a read mode when a high level is input to R/$\overline{W}$ pin and a write mode when a low level is input to R/$\overline{W}$ pin, and the command is activated when a high pulse is input to E pin. Therefore, in the command explanation and command table, the 6800-series MPU interface is different from the 8080-series MPU interface in that $\overline{RD}$ (E) becomes "1 (H)" in Display data read command. And when the serial interface is selected, the data is input in sequence starting with D7.
Taking the 8080-series MPU interface as an example, commands will be explained below.

Explanation of commands

(1) Display ON/OFF

This command turns the display ON and OFF.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	0 1	Display OFF Display ON

When the Display OFF command is executed when in the Display all points ON mode , Power saver mode is entered. See the section on the Power saver for details.

(2) Display normal/reverse

This command can reverse the lit and unlit display without overwriting the contents of the DDRAM.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0 1	Normal:DDRAM Data HIGH =LCD ON voltage Reverse:DDRAM Data LOW =LCD ON voltage

(3) Display all points ON/OFF

This command makes it possible to force all display points ON regardless of the content of the DDRAM. Even when this is done, the DDRAM contents are maintained. This command takes priority over the Display normal/reverse command.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0 1	Normal display mode Display all points ON

When the Display all points ON command is executed when in the Display OFF mode, Power saver mode is entered. See the section on the Power saver for details.

(4) Page address set

This command specifies the page address of the DDRAM (refer to Figure 5).
Specifying the page address and column address enables to access a desired bit of the DDRAM. After the last column address (83H), page address incremented by +1 (refer to Figure 4). After the very last address (column = 83H, page = 8H), page address return to 0H.
Page address 8H is the DDRAM area dedicate to the indicator, and only D0 is valid for data change.
See the function explanation in "DDRAM and page/column address circuit", for detail.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0H
							0	0	0	1	1H
							0	0	1	0	2H
								:			:
							0	1	1	1	7H
							1	0	0	0	8H

(5) Column address set

This command specifies the column address of the DDRAM (refer to Figure 5).
The column address is split into two sections (the upper 4-bits and lower 4-bits) when it is set (fundamentally, set continuously).
Each time the DDRAM is accessed, the column address automatically increments by +1, making it possible for the MPU to continuously access to the display data. After the last column address (83H) ,column address returns to 00H (refer to Figure 4).
See the function explanation in "DDRAM and page/column address circuit", for detail.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	0	0	1	A7	A6	A5	A4	Upper bit address
						0	A3	A2	A1	A0	Lower bit address

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	00H
0	0	0	0	0	0	0	1	01H
0	0	0	0	0	0	1	0	02H
				:				:
1	0	0	0	0	0	1	0	82H
1	0	0	0	0	0	1	1	83H

(6) Display start line address set

This command is used to specify the display start line address of the DDRAM (refer to Figure 5).
If the display start line address is changed dynamically using this command, then screen scrolling, page swapping can be performed.
See the function explanation in "Line address circuit", for detail.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	00H
					0	0	0	0	0	1	01H
					0	0	0	0	1	0	02H
							:				:
					1	1	1	1	1	0	3EH
					1	1	1	1	1	1	3FH

(7) ADC Select (Segment driver direction select)

This command can reverse the correspondence between the DDRAM column address and the segment driver output. See the function explanation in “DDRAM and page/column address circuit”, for detail.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

(8) Common driver direction select

This command can reverse the correspondence between the DDRAM line address and the common driver output. See the function explanation in “Line address circuit”, for detail.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	1	0	0	0	*	*	*	Normal
							1				Reverse

*Disabled bit

(9) Display data read

This command reads 8-bit data from the specified DDRAM address. Since the column address is automatically incremented by +1 after each read ,the MPU can continuously read multiple-word data. One dummy read is required immediately after the address has been set. See the function explanation in “Access to DDRAM and internal registers” and “DDRAM and page/column address circuit”, for detail.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

(10) Display data write

This command writes 8-bit data to the specified DDRAM address. Since the column address is automatically incremented by +1 after each write ,the MPU can continuously write multiple-word data. See the function explanation in “DDRAM and page/column address circuit”, for detail.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write Data							

(11) Read modify write

This command is used paired with End command. Once this command is issued, the column address is not incremented by Display data read command, but is incremented by Display data write command. This mode is maintained until End command is issued. When End command is issued, the column address returns to the address it was at when Read modify write command was issued. This function makes it possible to reduce the MPU load when there are the data to change repeatedly in a specified display region, such as blinking cursor.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

*When End command is issued, only column address returns to the address it was at when Read modify write command was issued, but page address does not return. Consequently, Read modify Write mode cannot be used over pages.
*Even if Read modify write mode, other commands besides Display data read/write can also be used. However, Column address set command cannot be used.

The sequence for cursor display

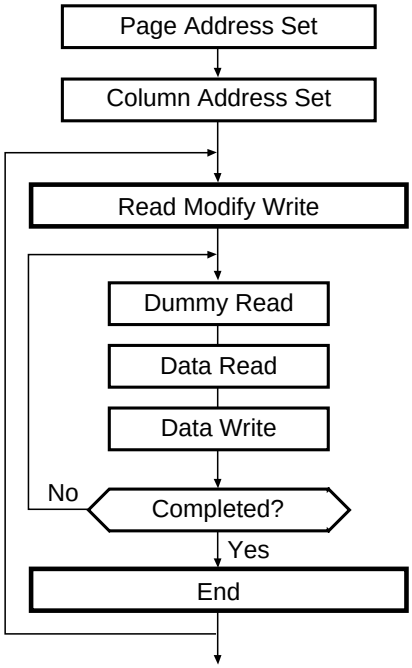


Figure 19

(12) End

This command releases the Read modify write mode, and returns the column address to the address it was when Read modify write command was issued .

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

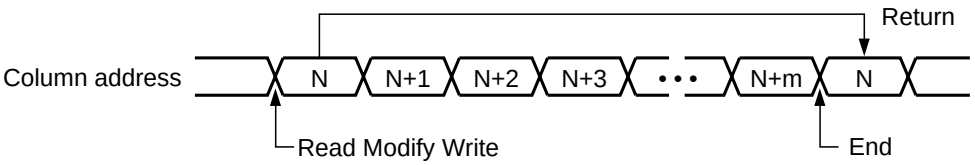


Figure 20

(13) Power control set

This command sets the on-chip power supply function ON/OFF. See the function explanation in “Power supply circuit”, for detail.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Mode
0	1	0	0	0	1	0	1	0			Booster : OFF
								1			Booster : ON
									0		Voltage regulator : OFF
									1		Voltage regulator : ON
										0	Voltage follower : OFF
										1	Voltage follower : ON

(14) V_0-resistor ratio set

This command sets the internal resistor ratio “Rb/Ra” for the V_0 voltage regulator to adjust the contrast of LCD panel display. See the function explanation in “Power supply circuit”, for detail.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra : V_0 voltage
0	1	0	0	0	1	0	0	0	0	0	SMALL LOW
								0	0	1	
								0	1	0	
								0	1	1	↓ ↓
								1	0	0	
								1	0	1	
								1	1	0	LARGE HIGH
								1	1	1	External resistor mode

(15) Electronic volume

This command sets a value of electronic volume "α" for the V_0 voltage regulator to adjust the contrast of LCD panel display. See the function explanation in "Power supply circuit", for detail.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	α : V0 voltage
0	1	0	1	0	0	0	0	0	0	0	31 : LOW
						0	0	0	0	1	
						0	0	0	1	0	
								↓			↓ : ↓
						1	1	1	1	0	
						1	1	1	1	1	0 : HIGH

(16) LCD bias set

This command selects the voltage bias ratio required for the LCD. This command is enabled when the voltage follower circuit operates.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Bias S1D15B01
0	1	0	1	0	1	0	0	0	1	0	1/9 bias
										1	1/7 bias

(17) Power saver

When the display all points ON command is executed when in the display OFF mode, power saver mode is entered, and the power consumption can be greatly reduced.

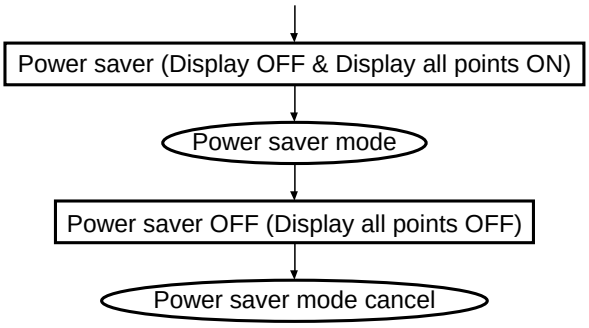


Figure 21

This mode stops every operation of the LCD display system, and can reduce current consumption nearly to a static current value if no access is made from the MPU. The internal states in the power saver mode is as follows:

- The oscillation circuit is stopped.
- The LCD power supply circuit is stopped.
- The LCD driver circuit is stopped and segment/common driver outputs output the V_{SS} level.
- The display data and operation mode before execution of the Power saver command are held, and the MPU can access to the DDRAM and internal registers.

(18) Reset

This LSI is in initialized by this command. And when S1D15B01D00B* is used, V0 is shorted to VSS. (Only when $\overline{RES}$= LOW, VOUT is shorted to VSS. So VOUT is not shorted to VSS by this commands.) See the function explanation in "Reset circuit", for detail.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

(19) NOP

Non-operation command

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

(20) Test

This is a command for LSI chip testing. Please do not use. If the test command is issued by accident, it can be cleared by applying an LOW signal to the $\overline{RES}$ pin, or by issuing the Reset command or the Display ON/OFF command.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	*	1	*	*	*	*

* Disabled bit

(Note):
The S1D15B01 series chip maintain their operating modes ,but excessive external noise, etc., may happen to change them. Thus in the packaging and system design it is necessary to suppress the noise or take measures to prevent the noise. Moreover, it is recommended that the operating modes are refreshed periodically to prevent the effects of unanticipated noise.

Command Table

Table 14

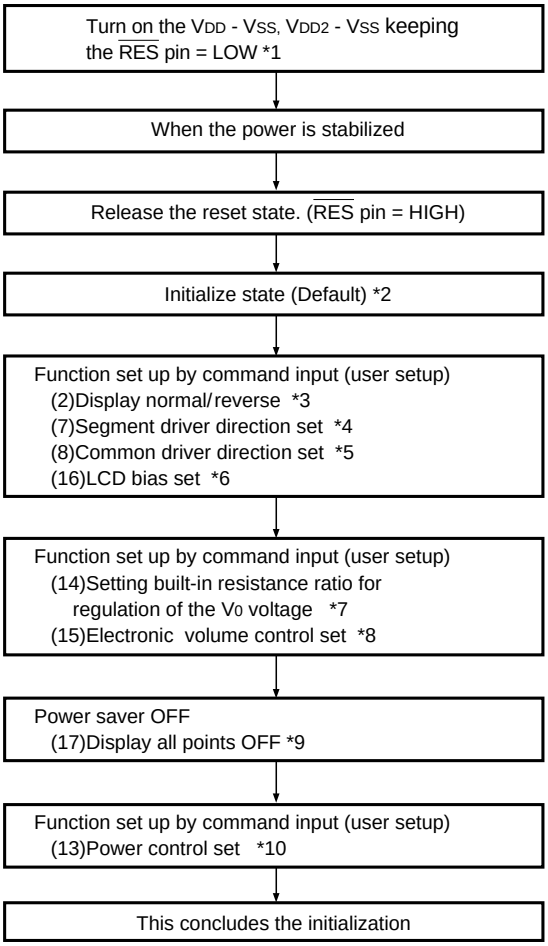
Command	Code											Function
	A0	XR	XW	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display 0:OFF, 1:ON
(2) Display normal/reverce	0	1	0	1	0	1	0	0	1	1	0 1	LCD display 0:normal, 1:reverce
(3) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	LCD display 0:normal display, 1:all points ON
(4) Page address set	0	1	0	1	0	1	1	address				Sets the DDRAM page address
(5) Column address set Upper 4-bit address	0	1	0	0	0	0	1	address				Sets the DDRAM column address
Column address set Lower 4-bit address	0	1	0	0	0	0	0	address				
(6) Display start line address set	0	1	0	0	1	address						Sets the DDRAM display start line address.
(7) Segment driver directuin select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the correspondence between the DDRAM column address and the SEG driver output. 0:normal, 1:reverse
(8) Common driver direction select	0	1	0	1	1	0	0	0 1	*	*	*	Sets the correspondence between the DDRAM line address and the COM driver output. 0:normal, 1:reverse
(9) Display data read	1	0	1	Read data								Reads from the DDRAM.
(10) Display data write	1	1	0	Write data								Writes to the DDRAM.
(11) Read modify write	0	1	0	1	1	1	0	0	0	0	0	Column address increment at write:+1, at read:0.
(12) End	0	1	0	1	1	1	0	1	1	1	0	Releases Read modify write mode.
(13) Power control set	0	1	0	0	0	1	0	1	Operating mode			Sets the on-chip power supply circuit operating mode.
(14) V_0-resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Sets the V_0-resistor ratio value.
(15) Electronic volume	0	1	0	1	0	0	Electronic volume value					Sets the electronic volume value.
(16) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio. S1D15B01 0:1/9bias, 1:1/7bias
(17) Power saver	-	-	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Display all points ON
(18) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(19) NOP	0	1	0	1	1	1	0	0	0	1	1	Non-operation
(20) Test	0	1	0	1	1	*	1	*	*	*	*	IC test command. Do not use.

(Note)*:disabled bit

8. COMMAND SETTING

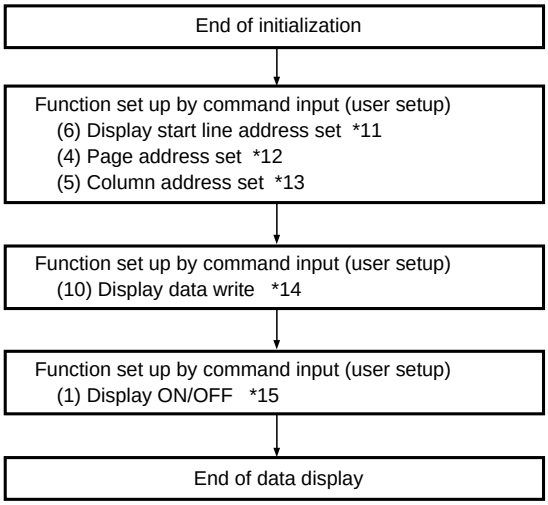
Instruction Setup of S1D15B01D00B* : Reference

(1) Initialization



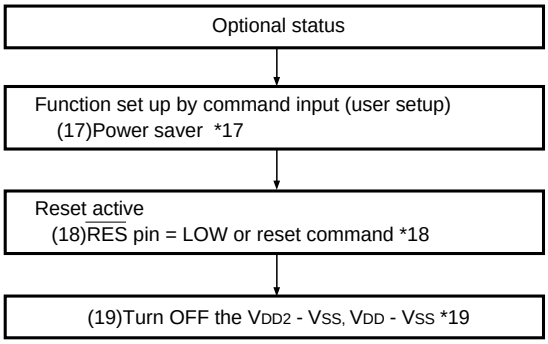
Notes: Refer to respective sections or paragraphs listed below
*1: Description of Timing characteristics; Notes for Power on Sequence
*2: Description of functional; Reset Circuit
*3: 7.Command Description; Display normal/reverse
*4: 7.Command Description; Segment driver direction select
*5: 7.Command Description; Common driver direction select
*6: 7.Command Description; LCD bias set
*7: Description of functions; Power supply circuit & Command description; V0-resistor ratio set
*8: Description of functions; Power supply circuit & Command description; Electronic volume
*9: 7.Command Description; Power saver
*10: Description of functions; Power supply circuit & Command description; Power control set

(2) Data display



Notes: Reference items
*11: 7.Command Description; Display start line address set
*12: 7.Command Description; Page address set
*13: 7.Command Description; Column address set
*14: 7.Command Description; Display data write
*15: 7.Command Description; Display ON/OFF

(3) Power OFF *16



Notes: Reference items
*16: After turning OFF the internal power supply, turn OFF the power supply of this IC.
(Function Description; Power supply circuit)
When the power of this IC is turned OFF with the internal power supply is held in the ON status, since the where the voltage is supplied, even though an only little, to on chip LCD drive circuit is still continued, it is featured to ill affect the display quality of the LCD panel. To avoid this, be sure to observe the power OFF sequence strictly.
*17: 7.Command Description; Power saver
*18: It is recommended to be $\overline{RES}$ pin=LOW. Only if it is not possible to be $\overline{RES}$ pin=LOW, ase reset command.
*19: Set the time t_L from reset active to turning off the V_{DD2}/V_{DD} power, longer then the time t_H when the potential of $V_0 \sim V_4$ becomes below the threshold voltage (approximately 1V) of the LCD panel. ($t_L > t_H$) If $t_L < t_H$, an irregular display may occur.
Refer to the < Reference Data > as below. When t_H is too long, insert a resis for between V_0 and V_{SS} to reduce it.

<Reference Data>
Condition: V_{DD}=V_{DD2}=1.8V, Quintuple boosting, Boosting Capacitance 1 µ F,
Set the V_0 voltage to 8V
t_H (µ s) is calculated the following equation.

$t_H = t_{H0} \times V_0 + \Delta t_H \times CL \times V_0$

CL :The capacitance of LCD panel connected between V_0 and V_{SS}
t_{H0} :t_H at the CL=0
Δt_H :t_H when the V_0 drops 1V per the CL=1pF.

This is reference data, so it is needed to estimate a real LCD module since t_H is depends on the V_{DD}/V_{DD2} voltage and the capacitance of LCD panel.

① In case of $\overline{RES}$ pin=LOW

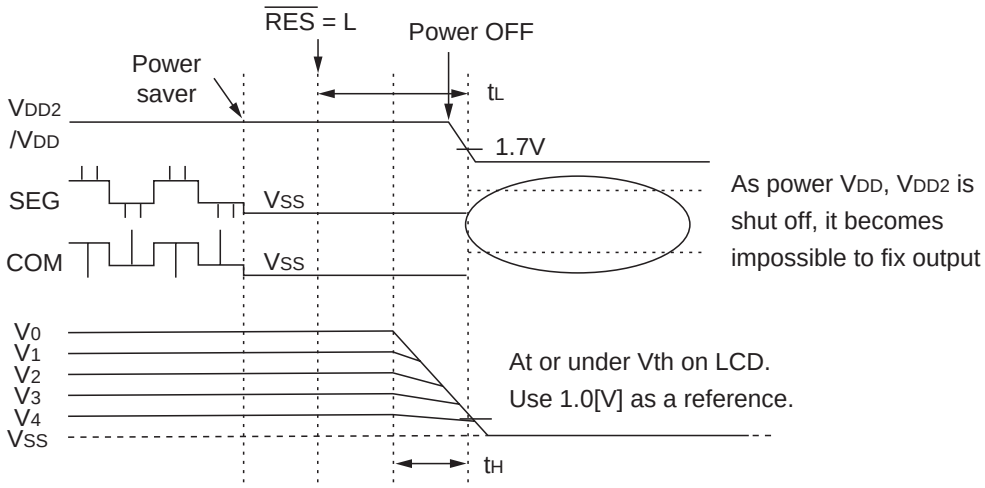


Figure 22

S1D15B01D00B∗ has the discharge faculty that is shorted V_{OUT} to V_{DD2}, when $\overline{RES}$ pin=LOW.
As t_{H0}=70(µs/V), Δt_H=0.079(µs/V/nF) by measurement, t_H is calculated as follows, when V_0=7V and CL=100pF.

$t_H = t_{H0} \times V_0 + \Delta t_H \times CL \times V_0 = 70 \times 7 + 0.079 \times 100 \times 7 = 545 \mu s$

② In case of reset command

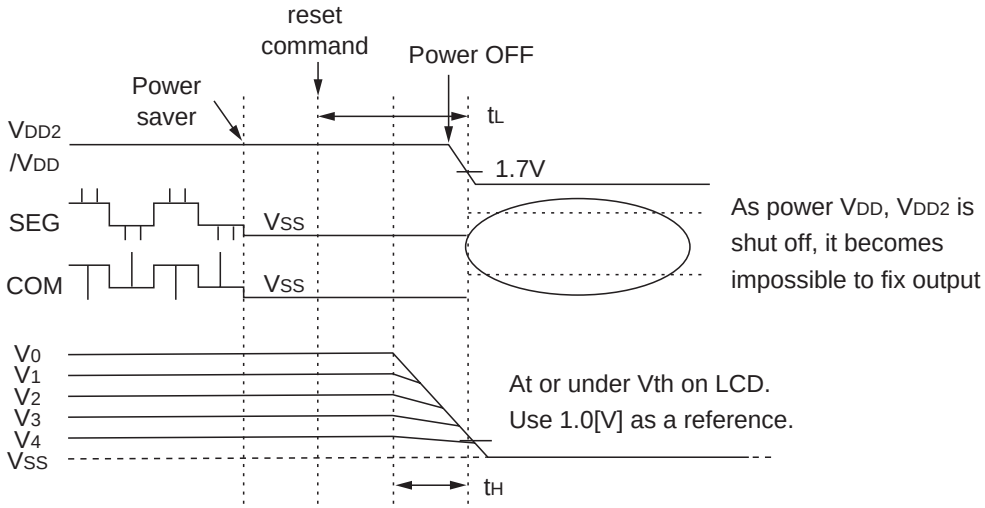


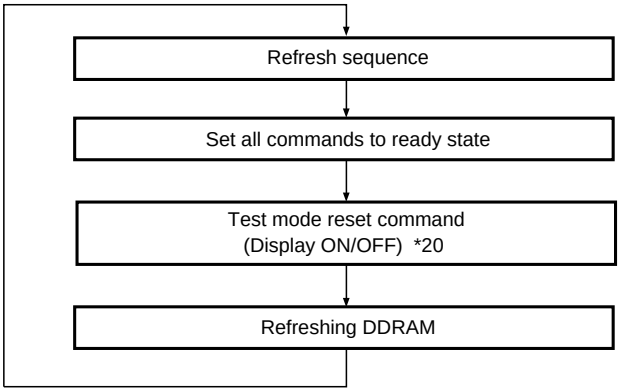
Figure 23

V_{OUT} is not shorted to V_{DD2} by reset command, so t_H is longer than the case of $\overline{RES}$ pin=LOW.
As t_{H0}=175(µs/V), Δt_H=0.23(µs/V/nF) by measurement, t_H is calculated as follows, when V_0=7V and CL=100pF.

$t_H = t_{H0} \times V_0 + \Delta t_H \times CL \times V_0 = 175 \times 7 + 0.23 \times 100 \times 7 = 1386 \mu s$

(3) Refresh

It is recommended that the operating modes and display contents be refreshed periodically to prevent the effect of unexpected noise.



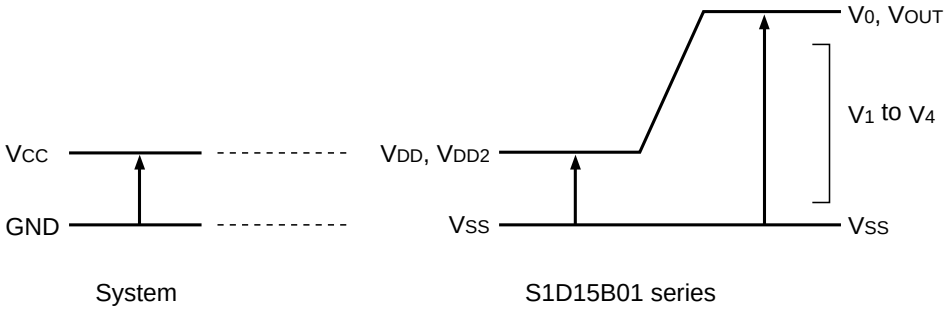
Notes: Reference items
*20: 7.Command description; Display ON/OFF

9. ABSOLUTE MAXIMUM RATING

Unless otherwise noted, V_{SS} = 0V.

Table 15

Parameter		Symbol	Conditions	Unit
Power supply voltage (1)		V_{DD}	–0.3 to 7.0	V
Power supply voltage (2)		V_{DD2}	–0.3 to 7.0	V
	Double boosting		–0.3 to 7.0	
	Triple boosting		–0.3 to 6.0	
	Quadruple boosting		–0.3 to 4.5	
	Quintuple boosting		–0.3 to 3.6	
Power supply voltage (3)		V_0, V_{OUT}	–0.3 to 18.0	V
Power supply voltage (4)		V_1, V_2, V_3, V_4	–0.3 to V_0	V
Input voltage		V_{IN}	–0.3 to V_{DD}+0.3	V
Output voltage		V_O	–0.3 to V_{DD}+0.3	V
Operating temperature		T_{OPR}	–40 to 85	°C
Storage temperature	TCP	T_{STR}	–55 to 100	°C
	Bare chip		–55 to 125	



Notes and Conditions

1. Voltage $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$ must always be satisfied.
2. If the LSI exceeds its absolute maximum rating, it may be damage permanently. It is desirable to use it under electrical characteristics conditions during general operation. Otherwise, a malfunction of the LSI may be caused and LSI reliability may be affected.

10. ELECTRICAL CHARACTERISTICS

DC Characteristics

Table 16 V_{SS}=0V, V_{DD}=3V±10%, Ta=–40 to 85°C unless otherwise noted.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Power voltage(1)	Recommended operation	V_{DD}	(Relative to V_{SS})	1.8	–	3.6	V	V_{DD} *1
	Operational			1.7	–	5.5	V	
Power voltage(2)	Recommended operation	V_{DD2}	(Relative to V_{SS})	1.8	–	3.6	V	V_{DD2} *1
	Operational			1.7	–	5.5		
	Booster circuit operatinal voltage		Double boosting	3.0	–	5.5		
			Triple boosting	2.0	–	5.0		
			Quadruple boosting	1.7	–	4.0		
			Quintuple boosting	1.7	–	3.0		
Voltage regulator operational voltage		V_{OUT}	(Relative to V_{SS})	6.0	–	16.0	V	V_{OUT}
Voltage follower operational voltage		V_0		4.5	–	16.0	V	V_0 *2
		V_1, V_2		0.6×V_0	–	V_0		V_1,V_2
		V_3, V_4		V_{SS}	–	0.4×V_0		V_3,V_4
Reference voltage		V_{REG}	Ta=25°C	1.26	1.30	1.34	V	*3
High-level input voltage		V_{IH}		0.8×V_{DD}	–	V_{DD}	V	*4
Low-level input voltage		V_{IL}		V_{SS}	–	0.2×V_{DD}	V	
High-level output voltage		V_{OH}	I_{OH}=-0.5mA	0.8×V_{DD}	–	V_{DD}	V	*5
Low-level output voltage		V_{OL}	I_{OL}=0.5mA	V_{SS}	–	0.2×V_{DD}	V	
Input leakage current		I_{LI}		–1.0	–	–1.0	µA	*6
Output leakage current		I_{LO}		–3.0	–	–3.0	µA	*7
LCD driver ON resistance		R_{ON}	V_0=8V Ta=25°C		2.0	5.0	kΩ	SEGn, COMn *8
Static current consumption		I_{DDQ}	Ta=25°C	–	0.01	5	µA	V_{DD}, V_{DD2}
		I_{0Q}	V_0=16V Ta=25°C	–	0.01	15	µA	V_5
Input terminal capacitance		C_{IN}	f =1MHz Ta=25°C		20	35	pF	
Oscillation frequency		f_{OSC}	Ta=25°C	4.55	5.2	5.85	kHz	*9

Relationship between oscillation frequency f_{osc} and frame rate frequency f_{FR} : $f_{FR} = f_{osc}/ 65$
Relationship between external clock (CL) frequency f_{CL} and frame rate frequency f_{FR} : $f_{FR} = f_{CL}/ 8/ 65$

Current consumption

Dynamic current consumption (1) : During display, when the internal power supply circuit is OFF (external power supply is used).

Table 17 Display Pattern OFF Ta=25˚C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Notes
S1D15B01*****	I_0(1)	V_{DD}=V_{DD2}=2.7V, V_0=8.0V	–	20	33	µA	*10
		V_{DD}=V_{DD2}=2.7V, V_0=11.0V	–	29	48		

Table 18 Display Pattern Checker Ta=25˚C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Notes
S1D15B01*****	I_0(1)	V_{DD}=V_{DD2}=2.7V, V_0=8.0V	–	24	40	µA	*10
		V_{DD}=V_{DD2}=2.7V, V_0=11.0V	–	33	55		

Dynamic current consumption (2) : During display, when the internal power supply circuit is ON.

Table 19 Display Pattern OFF Ta=25˚C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Notes
S1D15B01*****	I_{DD}+I_{DD2} (2)	V_{DD}=V_{DD2}=2.7V, V_0=8.0V Triple boosting	–	75	125	µA	*9
		V_{DD}=V_{DD2}=2.7V, V_0=8.0V Quadruple boosting	–	96	160		
		V_{DD}=V_{DD2}=2.7V, V_0=8.0V Quadruple boosting	–	119	198		

Table 20 Display Pattern Checker Ta=25˚C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Notes
S1D15B01*****	I_{DD}+I_{DD2} (2)	V_{DD}=V_{DD2}=2.7V, V_0=8.0V Triple boosting	–	86	143	µA	*9
		V_{DD}=V_{DD2}=2.7V, V_0=8.0V Quadruple boosting	–	110	183		
		V_{DD}=V_{DD2}=2.7V, V_0=8.0V Quadruple boosting	–	136	227		

Table 21 Power saver Ta=25˚C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Notes
S1D15B01*****	I_{DD}(2)	V_{DD}=V_{DD2}=1.7V to 3.6V	–	0.01	5	µA	*9

Reference data

Dynamic current consumption (1) : During display, when the internal power supply circuit is OFF (external power supply is used).

Conditions : Internal power supply OFF. External supply in use.
V_0=8.0V, Display pattern : OFF, Ta=25˚C

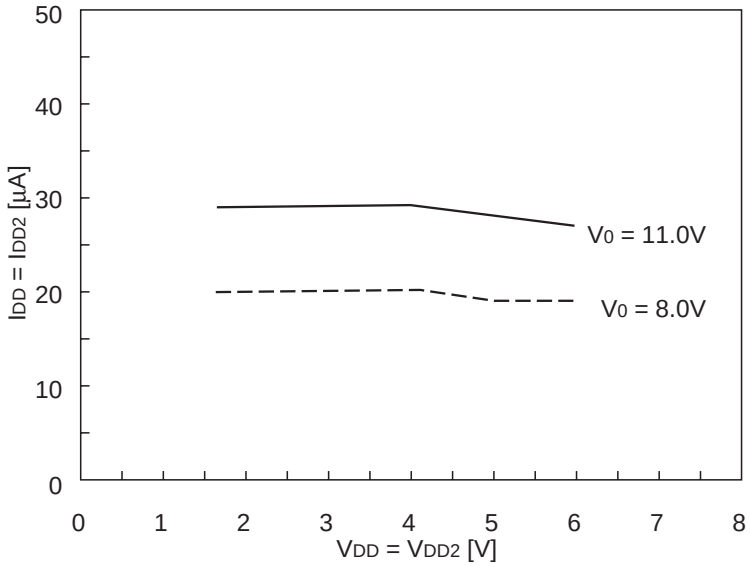


Figure 24

Conditions : Internal power supply OFF. External supply in use.
V_0=8.0V, Display pattern : Checker, Ta=25˚C

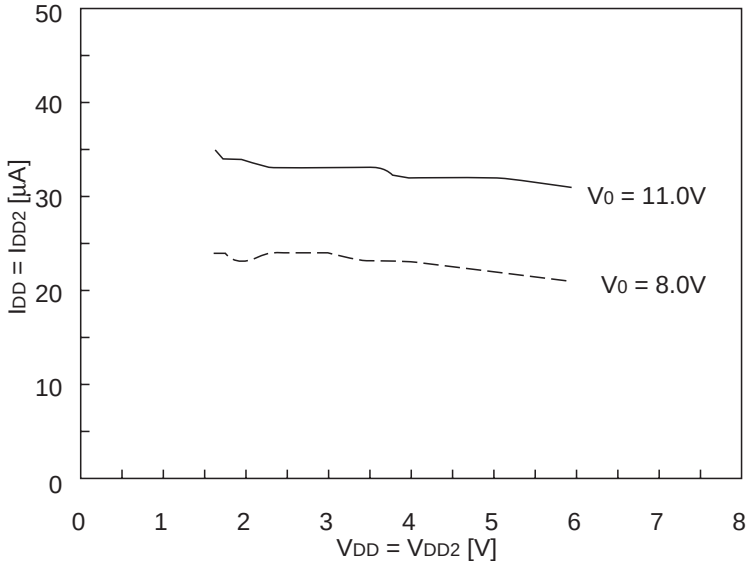


Figure 25

Dynamic current consumption (2) : During display, when the internal power supply circuit is ON.

Conditions : Internal power supply ON.
V_0=8.0V, Display pattern : OFF, Ta=25˚C

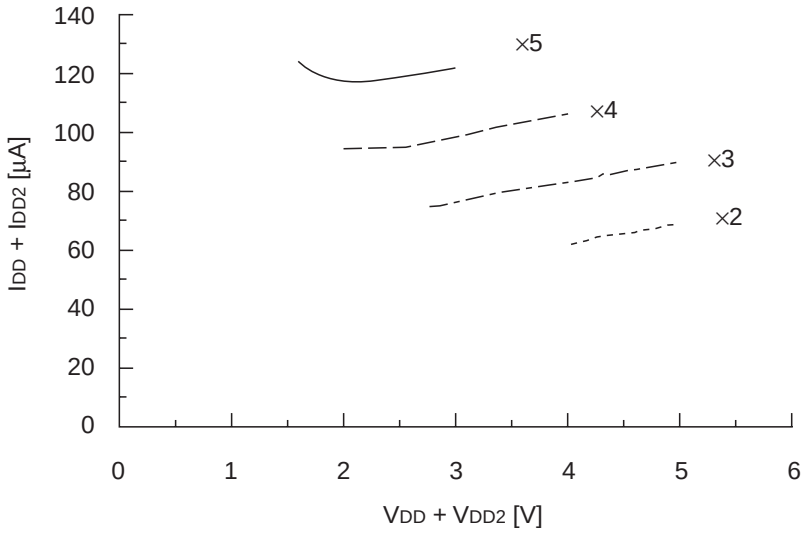


Figure 26

Conditions : Internal power supply ON.
V_0=8.0V, Display pattern : Checker, Ta=25˚C

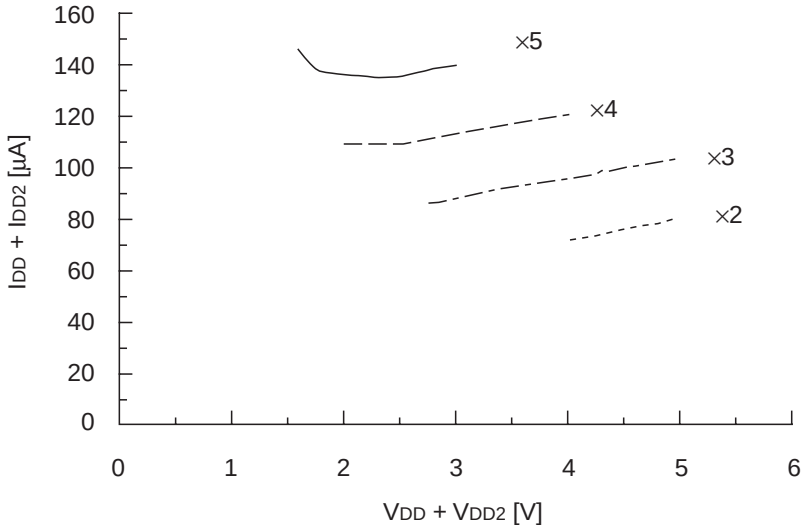


Figure 27

Dynamic current consumption (3) : During access and display (Checker pattern is constantly written at f_{CYC} and displayed), when the on-chip power supply circuit is ON.

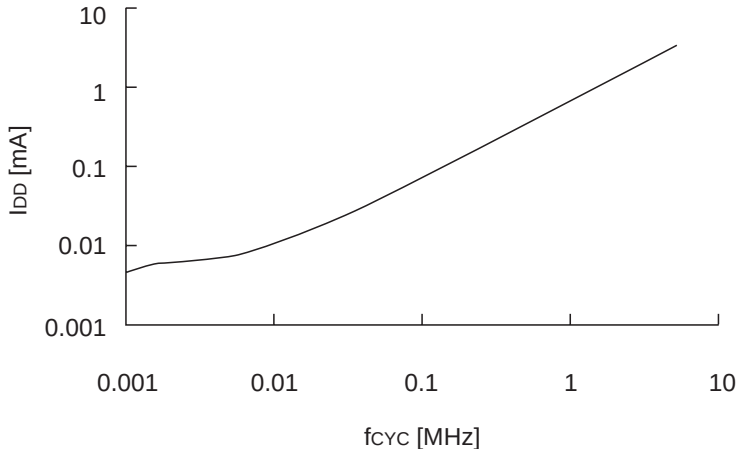


Figure 28

V_{DD}, V_{DD2} and V_0 (V_{OUT}) operation voltage range

(1) S1D15B01D00B∗

① $V_{DD}=V_{DD2}$

In the range of $V_{DD}=V_{DD2}<3.2V$, the maximum V_0 voltage is determined by V_{OUT} voltage of the quintuple boosting. It is necessary to keep $V_{OUT} > V_0$ for preventing irregular display. The voltage of $|V_{OUT} - V_0|$ is determined by LCD panel, so it is recommended to check the actual LCD module and set them.

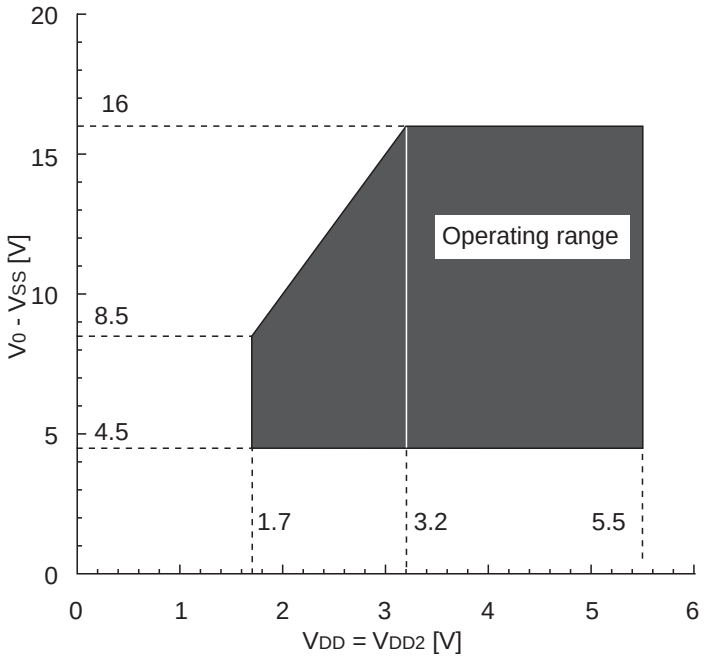


Figure 29

② $V_{DD}<V_{DD2}$

In the case, it is necessary to keep $1.7V \le V_{DD} \le V_{DD2} \le 3.6V$. And the V_{DD2} should be set to keep $V_{OUT}>V_0$.

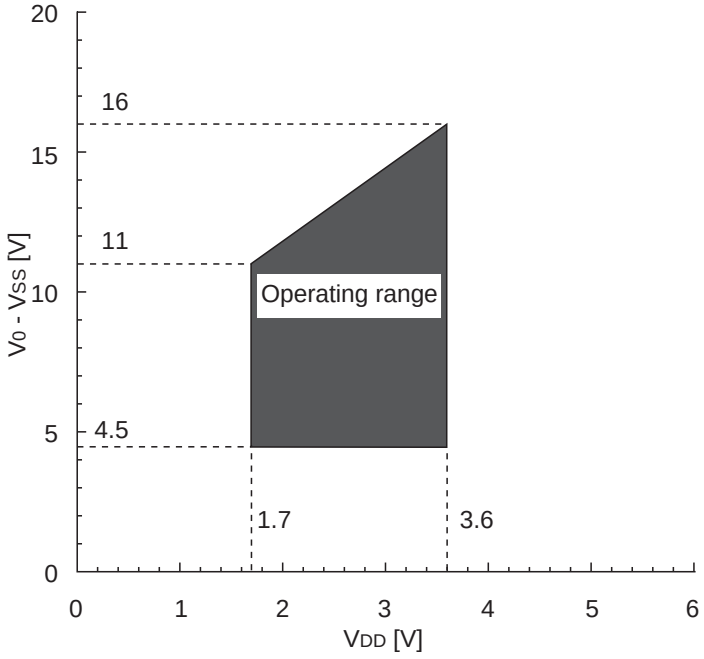


Figure 30

(2) S1D15B01D01B∗
If $V_{DD}=V_{DD2}$, the operating range of V_{DD}/V_{DD2} is $1.7V \le V_{DD}=V_{DD2} \le 4.5V$. And if $V_{DD}<V_{DD2}$, the operating range of V_{DD}/V_{DD2} is $1.7V \le V_{DD}<V_{DD2} \le 3.6V$
① Eternal voltage : V_{OUT}
In this case, the relationship between V_{OUT} and V_{DD}/V_{DD2} is required as shown in Figure 31.

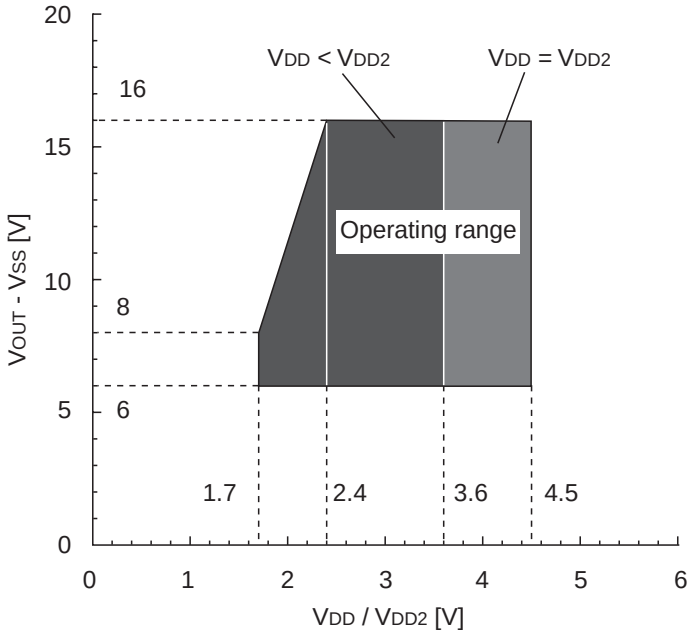


Figure 31

② Eternal voltage : V_0
In this case, the relationship between V_0 and V_{DD}/V_{DD2} is required as shown in Figure 32.

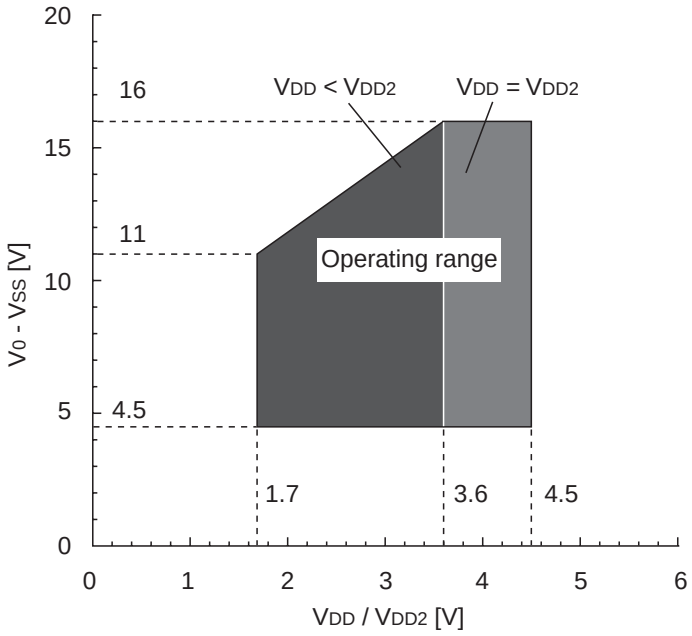


Figure 32

(3) S1D15B01D02B∗
Eternal voltage: V_0, V_1 to V_4
In this case, V_0 operating range is same as Figure 32, and $V_0 \ge V_1 \ge V_2 \ge V_3 \ge V_4 \ge V_{SS}$ is required.

*1. Though the wide range of operating voltage is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage during being accessed from MPU.
This V_{DD}, V_{DD2} operational voltage range (1.7V to 5.5V) is in case of $V_{DD}=V_{DD2}$. If $V_{DD}\neq V_{DD2}$, it becomes to be $1.7V\leq V_{DD}<V_{DD2}\leq 3.6V$.
*2. V_{DD}, V_{DD2} and V_0 operating voltage range is shown in Figure.
*3. V_{REG} is internal constant voltage source for V_0 voltage regulator circuit.
*4. D7 (SI), D6 (SCL), D5 to D0, A0, $\overline{CS}$, $\overline{RES}$, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$),C86, P/S and CL pins
*5. D7 to D0 pins
*6. A0, $\overline{CS}$, $\overline{RES}$, $\overline{RD}$ (E), $\overline{WE}$ (R/$\overline{W}$), C86, P/S and CL pins
*7. D7 (SI), D6 (SCL) and D5 to D0 pins
*8. Resistance value when 0.1V is applied between the output pin SEGn or COMn and each power supply pin (V_0, V_1, V_2, V_3, V_4, V_{SS}). This is specified in the "Voltage follower operating voltage" range. $R_{ON} = 0.1V/\Delta I$ (ΔI : Current flowing when 0.1V is applied between that output pin and those power supply pin).
*9. Current that each IC unit consumes. It does not include the current of the LCD panel capacity, wiring capacity, etc.

Timing Characteristics

System Bus Read/Write Characteristics 1 (For the 8080-series MPU)

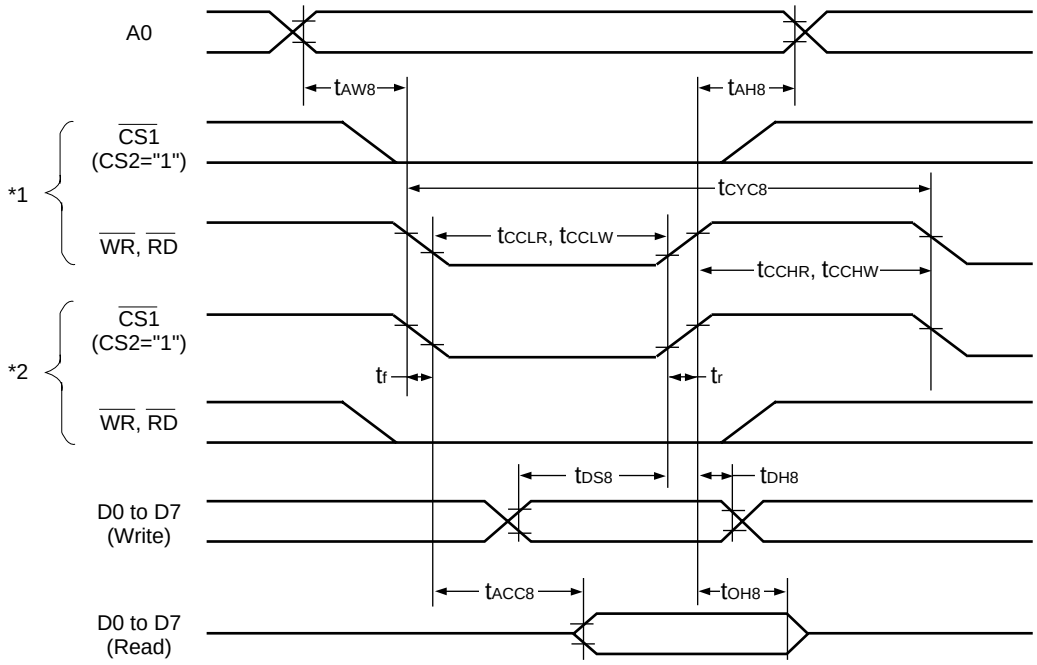


Figure 33

Table 22 [V_{DD}=4.5V to 5.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Min.	Max.	Units
Address hold time	A0	t_{AH8}		0	–	ns
Address setup time		t_{AW8}		0	–	
System cycle time		t_{CYC8}		160	–	
Control LOW pulse width(Write)	$\overline{WR}$	t_{CCLW}		30	–	
Control LOW pulse width(Read)	$\overline{RD}$	t_{CCLR}		70	–	
Control HIGH pulse width(Write)	$\overline{WR}$	t_{CCHW}		30	–	
Control HIGH pulse width(Read)	$\overline{RD}$	t_{CCHR}		30	–	
Data setup time	D7 to D0	t_{DS8}		20	–	
Data hold time		t_{DH8}		0	–	
Access time		t_{ACC8}	CL=100pF	–	70	
Output disable time		t_{OH8}		5	50	

Table 23 [V_{DD}=2.7V to 4.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Min.	Max.	Units
Address hold time	A0	t_{AH8}		0	–	ns
Address setup time		t_{AW8}		0	–	
System cycle time		t_{CYC8}		260	–	
Control LOW pulse width(Write)	$\overline{WR}$	t_{CCLW}		60	–	
Control LOW pulse width(Read)	$\overline{RD}$	t_{CCLR}		120	–	
Control HIGH pulse width(Write)	$\overline{WR}$	t_{CCHW}		60	–	
Control HIGH pulse width(Read)	$\overline{RD}$	t_{CCHR}		60	–	
Data setup time	D7 to D0	t_{DS8}		35	–	
Data hold time		t_{DH8}		0	–	
Access time		t_{ACC8}	CL=100pF	–	120	
Output disable time		t_{OH8}		10	100	

Table 24 [V_{DD}=1.7V to 2.7V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Min.	Max.	Units
Address hold time	A0	t_{AH8}		0	–	ns
Address setup time		t_{AW8}		0	–	
System cycle time		t_{CYC8}		700	–	
Control LOW pulse width(Write)	$\overline{WR}$	t_{CCLW}		120	–	
Control LOW pulse width(Read)	$\overline{RD}$	t_{CCLR}		240	–	
Control HIGH pulse width(Write)	$\overline{WR}$	t_{CCHW}		120	–	
Control HIGH pulse width(Read)	$\overline{RD}$	t_{CCHR}		120	–	
Data setup time	D7 to D0	t_{DS8}		90	–	
Data hold time		t_{DH8}		0	–	
Access time		t_{ACC8}	CL=100pF	–	240	
Output disable time		t_{OH8}		10	200	

*1. This is in the case of making the access by $\overline{WR}$ and $\overline{RD}$, setting the $\overline{CS1}$=LOW.
*2. This is in the case of making the access by $\overline{CS1}$, setting the $\overline{WR}$, $\overline{RD}$=LOW.
*3. The rise and fall times (tr and tf) of the input signal are specified for less than 15 ns. When using the system cycle time at high speed, they are specified for (tr+tf) $\leqq$ (t_{CYC8}-t_{CCLW}) or (tr+tf) $\leqq$ (t_{CYC8}-t_{CCLR}-t_{CCHR}).
*4. All timings are specified based on the 20 and 80% of V_{DD}.
*5. t_{CCLW} and t_{CCLR} are specified for the overlap period when $\overline{CS1}$ is at LOW (CS2=HIGH) level and $\overline{WR}$,$\overline{RD}$ are at the LOW level.

System Bus Read/Write Characteristics 2 (For the 6800-series MPU)

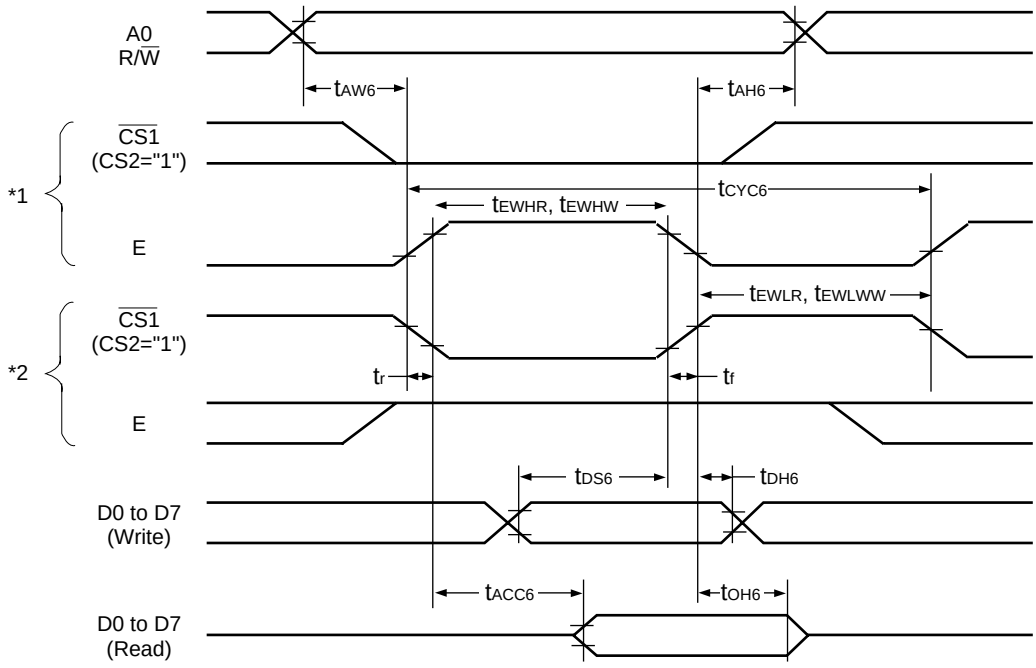


Figure 34

Table 25 [V_{DD}=4.5V to 5.5V, Ta=–40 to 85°C]

Item		Signal	Symbol	Condition	Min.	Max.	Units
Address hold time		A0, $\overline{WR}$	t_{AH6}		0	–	ns
Address setup time			t_{AW6}		0	–	
System cycle time			t_{CYC6}		160	–	
Enable HIGH pulse width	Width	E	t_{EWHW}		30	–	
	Read		t_{EWHR}		70	–	
Enable LOW pulse width	Width	E	t_{EWLW}		30	–	
	Read		t_{EWLR}		30	–	
Data setup time		D7 to D0	t_{DS6}		20	–	
Data hold time			t_{DH6}		0	–	
Access time			t_{ACC6}	CL=100pF	–	70	
Output disable time			t_{OH6}		5	50	

Table 26 [V_{DD}=2.7V to 4.5V, Ta=–40 to 85°C]

Item		Signal	Symbol	Condition	Min.	Max.	Units
Address hold time		A0,	t_{AH6}		0	–	ns
Address setup time		$\overline{WR}$	t_{AW6}		0	–	
System cycle time			t_{CYC6}		260	–	
Enable	Width	E	t_{EWHW}		60	–	
HIGH pulse width	Read		t_{EWHR}		120	–	
Enable	Width		t_{EWLW}		60	–	
LOW pulse width	Read		t_{EWLR}		60	–	
Data setup time		D7 to D0	t_{DS6}		35	–	
Data hold time			t_{DH6}		0	–	
Access time			t_{ACC6}	CL=100pF	–	120	
Output disable time			t_{OH6}		10	100	

Table 27 [V_{DD}=1.7V to 2.7V, Ta=–40 to 85°C]

Item		Signal	Symbol	Condition	Min.	Max.	Units
Address hold time		A0,	t_{AH6}		0	–	ns
Address setup time		$\overline{WR}$	t_{AW6}		0	–	
System cycle time			t_{CYC6}		700	–	
Enable	Width	E	t_{EWHW}		120	–	
HIGH pulse width	Read		t_{EWHR}		240	–	
Enable	Width		t_{EWLW}		120	–	
LOW pulse width	Read		t_{EWLR}		120	–	
Data setup time		D7 to D0	t_{DS6}		90	–	
Data hold time			t_{DH6}		0	–	
Access time			t_{ACC6}	CL=100pF	–	240	
Output disable time			t_{OH6}		10	200	

*1. This is in the case of making the access by E, setting the $\overline{CS1}$=LOW.
*2. This is in the case of making the access by $\overline{CS1}$, setting the E=HIGH.
*3. The rise and fall times (tr and tf) of the input signal are specified for less than 15 ns. When using the system cycle time at high speed, they are specified for (tr+tf) ≦ (t_{CYC6}-t_{EWLW}-t_{EWHW}) or (tr+tf) ≦ (t_{CYC6}-t_{EWLR}-t_{EWHR}).
*4. All timings are specified based on the 20 and 80% of V_{DD}.
*5. t_{EWLW} and t_{EWLR} are specified for the overlap period when $\overline{CS1}$ is at LOW (CS2=HIGH) level and E is at the HIGH level.

Serial interface

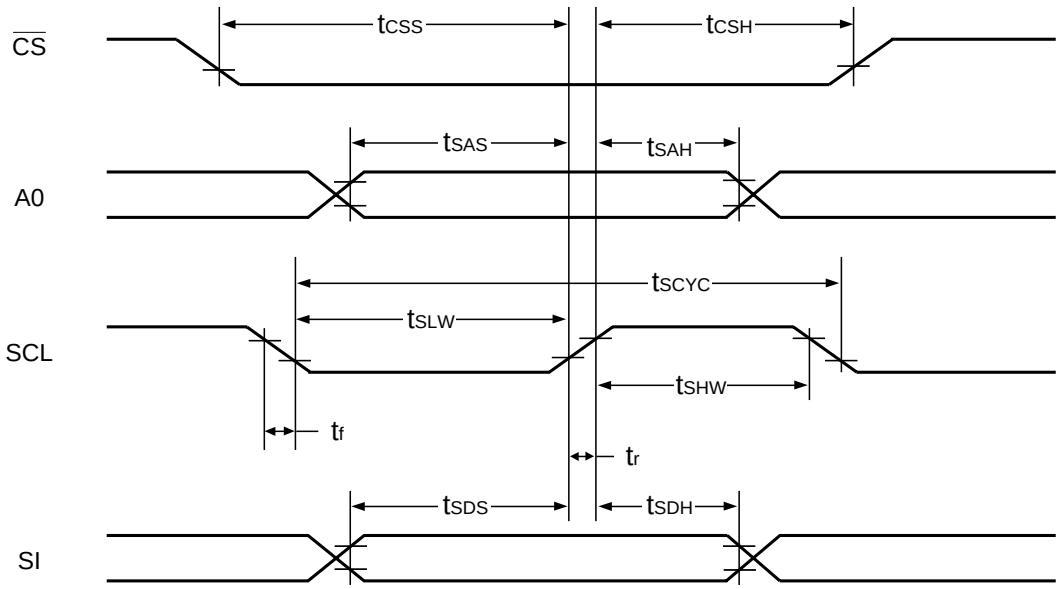


Figure 35

Table 28 VDD=4.5 to 5.5V, Ta=–40 to 85°C

Item	Signal	Symbol	Condition	Min.	Max.	Units
Serial clock cycle	SCL	tSCYC		40	–	ns
Serial clock HIGH pulse width		tSHW		15	–	
Serial clock LOW pulse width		tSLW		15	–	
Address setup time	A0	tSAS		10	–	
Address hold time		tSAH		20	–	
Data setup time	SI	tSDS		3	–	
Data hold time		tSDH		3	–	
$\overline{CS}$ serial clock time	$\overline{CS}$	tCSS		10	–	
		tCSH		25	–	

Table 29 VDD=2.7 to 4.5V, Ta=–40 to 85°C

Item	Signal	Symbol	Condition	Min.	Max.	Units
Serial clock cycle	SCL	tSCYC		70	–	ns
Serial clock HIGH pulse width		tSHW		25	–	
Serial clock LOW pulse width		tSLW		25	–	
Address setup time	A0	tSAS		20	–	
Address hold time		tSAH		40	–	
Data setup time	SI	tSDS		5	–	
Data hold time		tSDH		5	–	
$\overline{CS}$ serial clock time	$\overline{CS}$	tCSS		15	–	
		tCSH		50	–	

Table 30 V_{DD}=1.7 to 2.7V, Ta=–40 to 85°C

Item	Signal	Symbol	Condition	Min.	Max.	Units
Serial clock cycle	SCL	t_{SCYC}		150	–	ns
Serial clock HIGH pulse width		t_{SHW}		50	–	
Serial clock LOW pulse width		t_{SLW}		50	–	
Address setup time	A0	t_{SAS}		45	–	
Address hold time		t_{SAH}		90	–	
Data setup time	SI	t_{SDS}		10	–	
Data hold time		t_{SDH}		10	–	
$\overline{CS}$ serial clock time	$\overline{CS}$	t_{CSS}		50	–	
		t_{CSH}		100	–	

Note : 1. The input Signal rise and fall times must be with in 10ns.
2. Every timing is specified on the basis of 20% and 80% of V_{DD}.

Reset timing

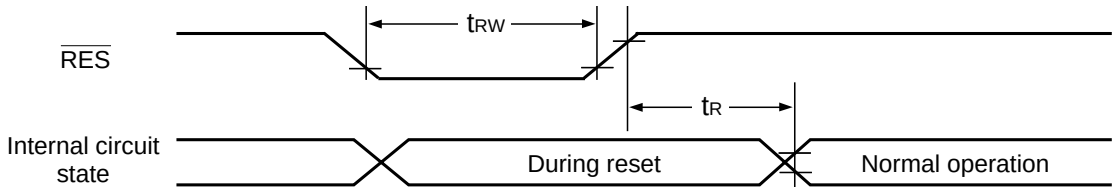


Figure 36

Table 31 V_{DD}=4.5 to 5.5V, Ta=–40 to 85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Units
Reset time		t_R		–	250	ns
Reset LOW pulse width	$\overline{RES}$	t_{RW}		250	–	

Table 32 V_{DD}=2.7 to 4.5V, Ta=–40 to 85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Units
Reset time		t_R		–	500	ns
Reset LOW pulse width	$\overline{RES}$	t_{RW}		500	–	

Table 33 V_{DD}=1.7 to 2.7V, Ta=–40 to 85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Units
Reset time		t_R		–	1000	ns
Reset LOW pulse width	$\overline{RES}$	t_{RW}		1000	–	

Note : 1. The input Signal rise and fall times must be with in 10ns.
2. Every timing is specified on the basis of 20% and 80% of V_{DD}.

Notes for Power on Sequence

It is preferable to turn on power supply V_{DD} and V_{DD2} at the same time, but if V_{DD} turn on after V_{DD2}, then it is necessary that the below 3 conditions are satisfied.

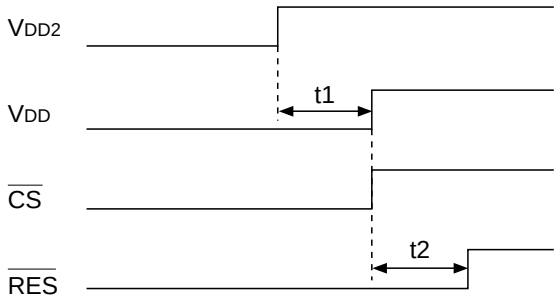


Figure 37

A. t1 < 1ms, during this timing, all input pins are fixed to V_{SS}.
B. $\overline{CS}$ becomes HIGH simultaneously with V_{DD}.
C. t2 > 100ns (Reset is canceled after V_{DD2} and rise up).

11. THE MPU INTERFACE (REFERENCE EXAMPLES)

The S1D15B01 series can directly be connected to the 80 system MPU and 68 series MPU. It can also be operated with a fewer signal lines by using the serial interface.
After the initialization using the RES pin, the respective input pins of the S1D15B01 series need to controlled normally.

(1) 80 series MPU

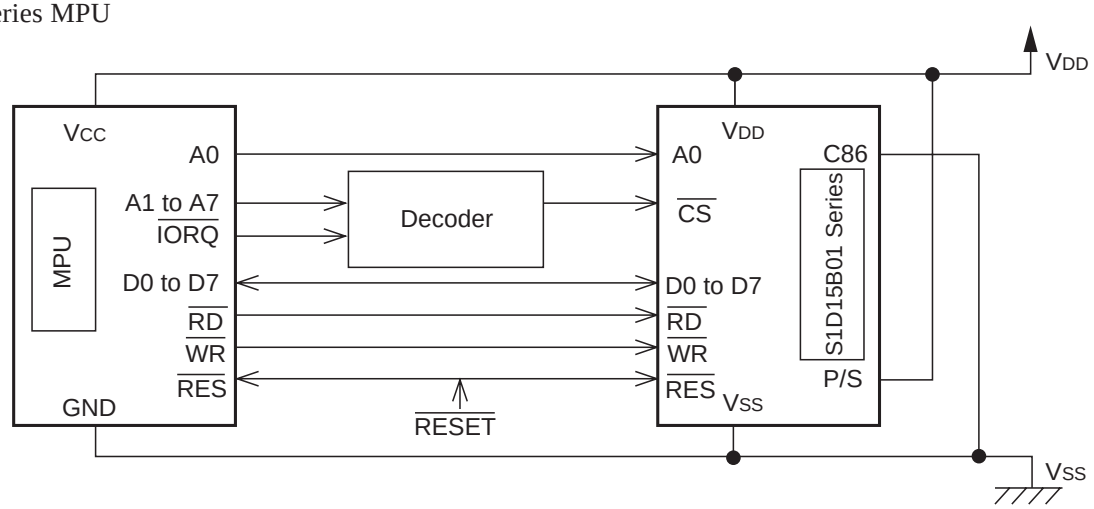


Figure 38

(2) 6800 series MPU

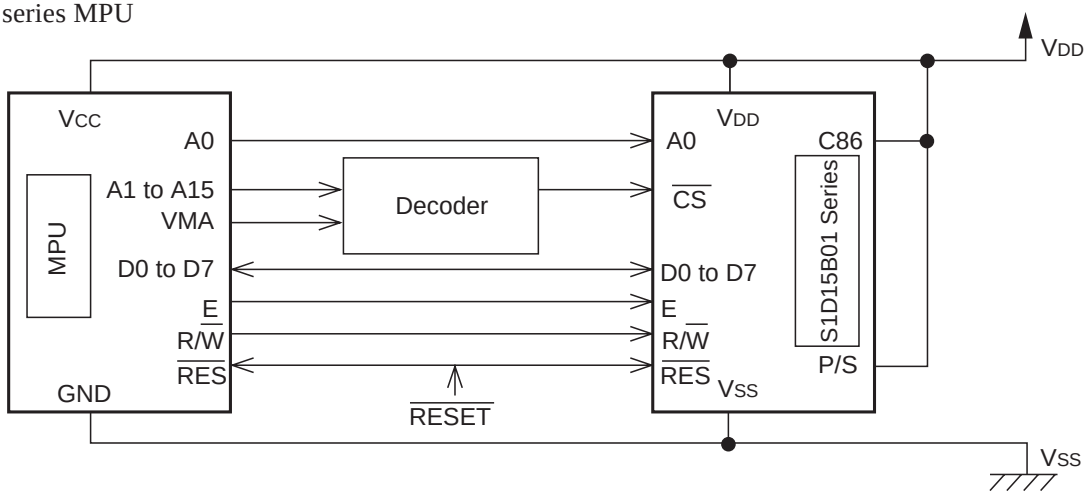


Figure 39

(3) Using serial interface

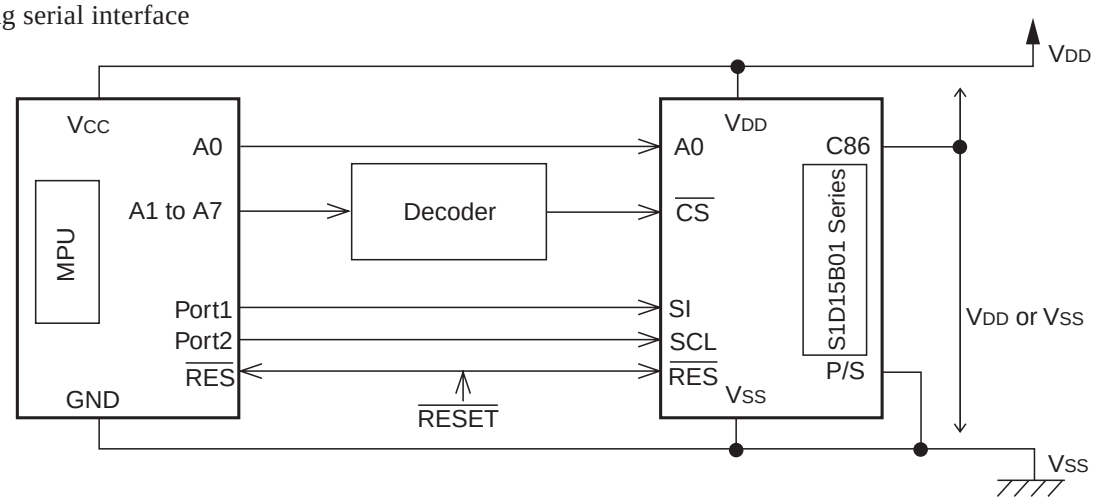


Figure 40

12. CAUTION

Please be advised on the following points in the use of this development specification.

1. This development specification is subject to change without previous notice.
2. This development specification does not guarantee or furnish the industrial property right not its execution.
   Application examples in this development specification are intended to ensure your better understanding of the product. Thus the manufacturer shall not be liable for any trouble arising in your circuits from using such application example.
   Numerical values provided in the property table of this manual are represented with their magnitude on the numerical line.
3. No part of this development specification may not be reproduced, copied or used for commercialpurpose without a written permission from the manufacturer.

In handling of semiconductor devices, your attention is required to following points.

[Precaution on light]

Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in malfunctioning of the ICs. To prevent such malfunctioning of the ICs mounted on the boards or products, make sure that:

(1) Your design and mounting layout done are so that the IC is not exposed to light in actual use.

(2) The IC is protected from light in the inspection process.

(3) The IC is protected from light in its front, rear and side faces.

[Precautions when installing the COG]

When installing the COG, it is necessary to duly consider the fact that there exists a resistance of the ITO wiring occurring between the driver chip and the externally connected parts (such as capacitors and resistors). By the influence of this resistance, non-conformity may occur with the indications on the liquid crystal display.

Therefore, when installing the COG design the module paying sufficient considerations to the following three points.

1. Suppress the resistance occurring between the driver chip pin to the externally connected parts as much as possible.
2. Suppress the resistance connecting to the power supply pin of the driver chip.
3. Make various COG module samples with different ITO sheet resistance to select the module with the sheet resistance with sufficient operation margin.

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