LH155BA

128-Segment and 64-Common Outputs LCD Driver IC with A Built-in RAM

DESCRIPTION

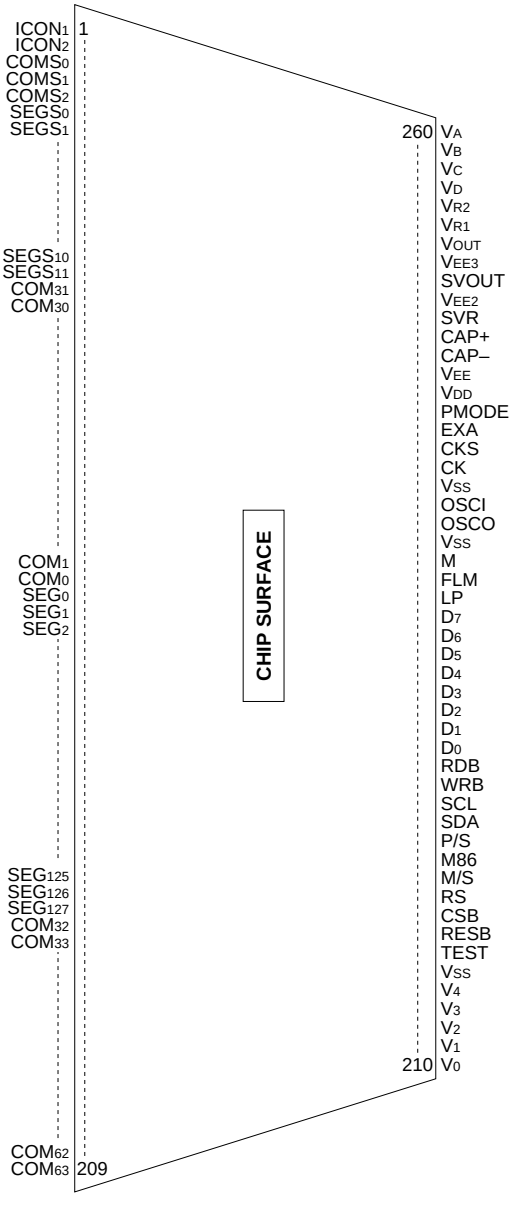
The LH155BA is an LCD driver with a built-in RAM suitable for driving medium/small scale dot-matrix LCD panels, and which is capable of being directly connected to the bus line of a microcomputer. The LH155BA stores in the RAM the 8-bit parallel or serial display data transferred from the microcomputer and generates LCD drive signals. Since the LH155BA features a bit-map type LCD driver that one bit of data in the display RAM corresponds to one dot in the LCD, there is a lot of freedom in displaying. The LH155BA has 128 segment outputs and 64 common outputs in a single chip, making it possible to create an LCD system with the fewest number of the chips. The LH155BA enables an LCD system for battery-operated, hand-carrying information equipment by securing lower power consumption and wider operating voltage range.

FEATURES

- Graphic display output pin : 64 x 128 pins
- Segment display output pin : 3 x 12 pins
- Icon display output pin : 1 x 1 pin
- LCD display by graphic display RAM
  - Normal mode : RAM data "0"→not lighted, RAM data "1"→lighted
  - Reverse mode : RAM data "1"→not lighted, RAM data "0"→lighted
- Display RAM memory capacity
  - 128 x 64 = 8 192 bits (For graphic display)
  - 12 x 3 = 36 bits (For segment display)
  - 1 x 1 = 1 bit (For icon display)
- General 8-bit MPU interface : Possible to directly connect 80-family and 68-family MPUs to bus line
- Possible to make serial interface
- Ratio of display duty cycle : 1/16, 1/32, 1/48 or 1/64 (selectable by command)
- 128-bit automatic transfer from display RAM to display data latch
- Abundant command functions
  - Display data read/write
  - Setting up LCD alternating signal cycle
  - Setting up display starting-line : per line
  - Display ON/OFF
  - Display control of normal and reverse modes
  - Increment control of display RAM address
  - Write control of read modifying
  - Internal register read
  - Power saving mode
- LCD drive power circuit
  - Built-in booster circuit : Two, three or four times voltage boost is possible
  - Built-in voltage converter : Generates LCD drive voltages (V_0, V_1, V_2, V_3 and V_4) based on the boosted voltage
  - Built-in power bias ratio : 1/7 or 1/9 bias (selectable by command)
  - Built-in electronic volume : Controllable in 16 steps
  - Supply voltages
    Logic system : +1.8 to +5.5 V
    LCD drive system : +4.0 to +14.0 V
- Operating temperature : –30 to +85 ˚C
- Package : 260-pin TCP (Tape Carrier Package)

PIN CONNECTIONS

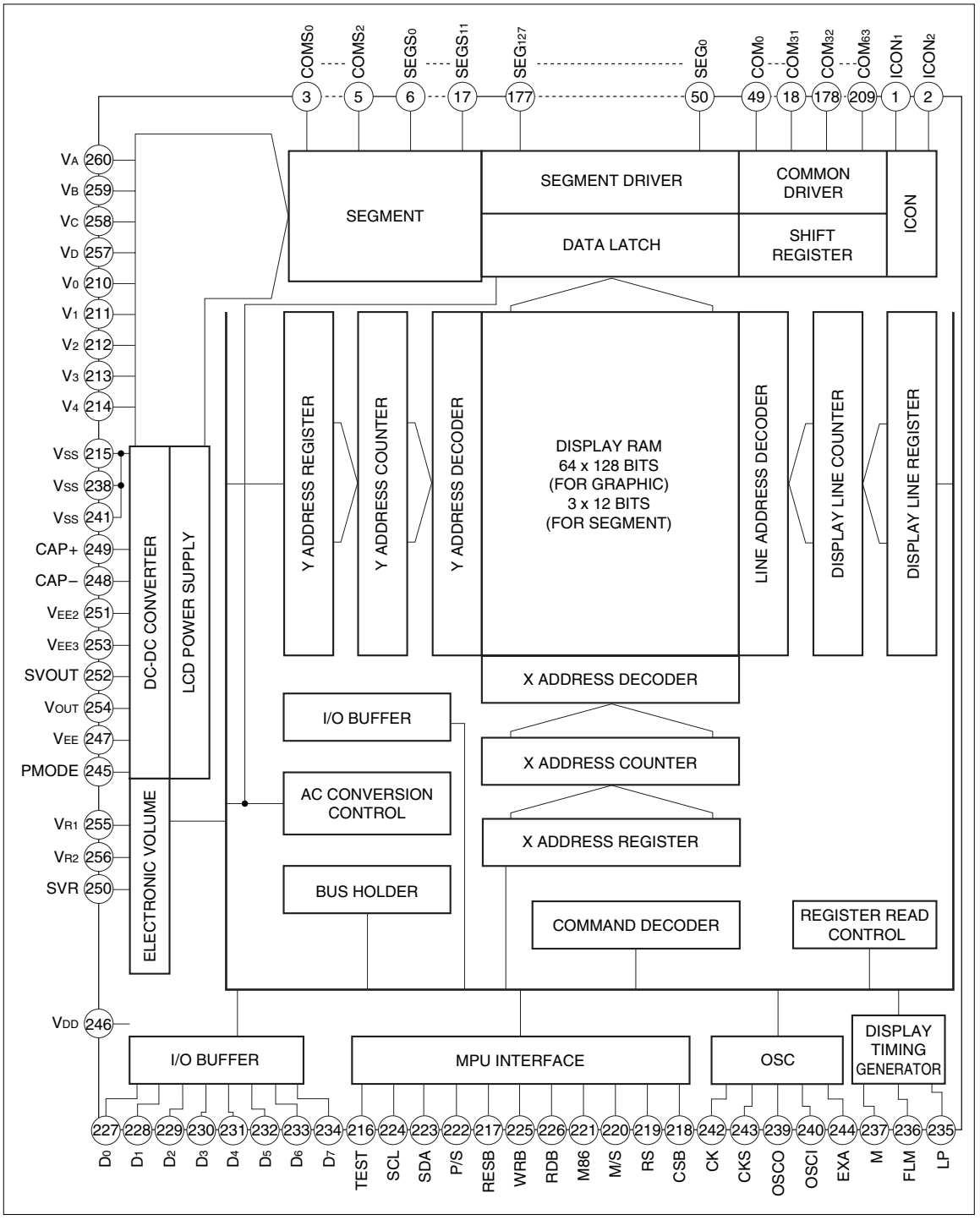
260-PIN TCP TOP VIEW



NOTE :

Doesn't prescribe TCP outline.

BLOCK DIAGRAM



1. PIN DESCRIPTION

1.1. Power Supply Pins

SYMBOL	I/O	DESCRIPTION
V_{DD}	Power Supply	Power supply pin for logic, connected to +1.8 to +5.5 V.
V_{SS}	Power Supply	Ground pin, connected to 0 V.
V_0 V_1 V_2 V_3 V_4 V_A V_B V_C V_D	Power Supply V_0-V_4 for Graphic Display V_A-V_D for Segment Display	Bias power supply pins for LCD drive voltage. • When using an external power supply, convert impedance by using resistance-division of LCD drive power supply or operational amplifier before adding voltage to the pins. • When using the external power supply, maintain the following power supply conditions. $V_{SS} < V_4 < V_3 < V_2 < V_1 < V_0$, $V_{SS} \leq V_D < V_C < V_B < V_A$ • When the power supply circuit is ON at master operation, LCD drive voltages of V_0 to V_4 are generated by the internal booster circuit and voltage converter. When using segment display, input V_A, V_B, V_C and V_D level externally. • When using the internal power supply, be sure to connect each capacitor between V_0 to V_4, V_A to V_D, and V_{SS}.

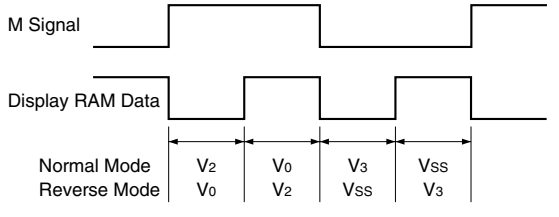
1.2. LCD Power Supply Circuit Pins

SYMBOL	I/O	DESCRIPTION
CAP+	O	Connecting pin for the internal booster's capacitor + side. The capacitor is connected between CAP− and CAP+.
CAP−	O	Connecting pin for the internal booster's capacitor − side. The capacitor is connected between CAP+ and CAP−.
V_{EE2}	O	Connecting pin for the internal booster's capacitor + side. The capacitor is connected between V_{SS} and V_{EE2}.
V_{EE3}	O	Connecting pin for the internal booster's capacitor + side. The capacitor is connected between V_{SS} and V_{EE3}.
V_{EE}	Power supply	Voltage supply pin for generating boosted voltage in the internal booster circuit. Usually the same voltage level as V_{DD}.
V_{OUT}	Power supply/ O	Output pin of boosted voltage in the internal booster circuit. The capacitor must be connected between V_{SS} and V_{OUT}.
SVOUT	–	Non-connected.
V_{R1} V_{R2}	I	Used as input pins for graphic display voltage converter. Voltage must be input between the V_{EE} and V_{OUT} pins by voltage divided by resistors.
SVR	–	Non-connected.
PMODE	I	Pin for controlling LCD power supply. A combination of PMODE pin and ON/OFF command of power supply (PON) enables selection of a specific drive operation.

1.3. System Bus Pins

<table>
<tr><th>SYMBOL</th><th>I/O</th><th>DESCRIPTION</th></tr>
<tr><td>D7-D0</td><td>I/O</td><td>8-bit bi-directional data bus, connected to 8-bit MPU data bus.</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip selection input pin that decoded address bus signal is input.</td></tr>
<tr><td>RS</td><td>I</td><td>Distinguishes display RAM data/commands of D7 to D0 data transferred from MPU.
0 : The data of D7 to D0 show the display RAM data.
1 : The data of D7 to D0 show the command data.</td></tr>
<tr><td>RESB</td><td>I</td><td>Initialized by setting to "L". The reset signals of the system are normally input. Reset operation is performed in accordance with RESB signal level.</td></tr>
<tr><td>RDB
(E)</td><td>I</td><td>• In connecting to 80-family MPU :
This RDB is a pin for connecting the RDB signal of 80-family MPU. When the signal enters in the "L" state, the data bus of this IC turns to the "output" state.
• In connecting to 68-family MPU :
This RDB becomes a pin for connecting the enable clock signal of 68-family MPU. When the signal enters in the "H" state, the data bus of this IC turns to the "active" state.</td></tr>
<tr><td>WRB
(R/W)</td><td>I</td><td>• In connecting to 80-family MPU :
This WRB is a pin for connecting the WRB signal of 80-family MPU, and when WRB signal is "L", this pin is "active".
The data bus signal is input at the rising edge of WRB signal.
• In connecting to 68-family MPU :
This WRB becomes a pin for connecting the R/W signal of controlling read/write of 68-family MPU.
R/W = "H" : Read
R/W = "L" : Write</td></tr>
<tr><td>M86</td><td>I</td><td>MPU interface-type shift pin.
M86 = "H" : 68-family interface
M86 = "L" : 80-family interface
Fixed to either "H" or "L".</td></tr>
<tr><td>SDA</td><td>I</td><td>Serial-data input pin at time of serial interface selection.</td></tr>
<tr><td>SCL</td><td>I</td><td>Serial clock pin at time of serial interface selection.
Used to shift the SDA data by using the rising edge of SCL.
Used to convert into 8-bit data by using the 8th clock at the rising edge of SCL in serial-to-parallel data processing.
After data-transferring, or when making no access, be sure to set to "L".</td></tr>
<tr><td>P/S</td><td>I</td><td>Used to shift between parallel interface and serial interface.
<table>
<tr><th>P/S</th><th>Chip selection</th><th>Data identification</th><th>Data</th><th>Read/Write</th><th>Serial clock</th></tr>
<tr><td>H</td><td>CSB</td><td>RS</td><td>D7-D0</td><td>RDB, WRB</td><td>–</td></tr>
<tr><td>L</td><td>CSB</td><td>RS</td><td>SDA</td><td>Write only</td><td>SCL</td></tr>
</table>
P/S = "H" for parallel input. Fix SDA and SCL pins to either "H" or "L".
P/S = "L" for serial input. Fix D7 to D0 pins to High-Z, RDB and WRB pins to either "H" or "L".</td></tr>
<tr><td>TEST</td><td>I</td><td>For testing. Fix to "L".</td></tr>
</table>

1.4. LCD Drive Circuit Signals

<table>
<tr><th>SYMBOL</th><th>I/O</th><th>DESCRIPTION</th></tr>
<tr><td>LP</td><td>I/O</td><td>The latching signal of display data to count up the display line counter at the rising, and to output the LCD drive signals at the falling.
M/S = "H" : Output for master mode
M/S = "L" : Input for slave mode</td></tr>
<tr><td>FLM</td><td>I/O</td><td>I/O pin for LCD synchronous signals (first line marker).
When FLM pin is set to "H", the display starting line address is preset in the display line counter.
M/S = "H" : Output for master mode
M/S = "L" : Input for slave mode</td></tr>
<tr><td>M</td><td>I/O</td><td>I/O pin for alternating signals of LCD drive output.
M/S = "H" : Output for master mode
M/S = "L" : Input for slave mode</td></tr>
<tr><td>M/S</td><td>I</td><td>Used to select either master or slave mode operation.
<table>
<tr><th>M/S</th><th>State</th><th>OSC</th><th>P.S.circuit</th><th>LP</th><th>FLM</th><th>M</th></tr>
<tr><td>H</td><td>Master</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Slave</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Input</td></tr>
</table>
Fix to "H" or "L" at this pin.</td></tr>
<tr><td>SEG0-SEG127</td><td>O</td><td>Segment output pins for graphic display.
According to the data of the display RAM data,
non-lighted at "0", lighted at "1" (Normal mode)
non-lighted at "1", lighted at "0" (Reverse mode)
and, by a combination of M signal and display data, one signal level among V0, V2, V3, and VSS is selected.

</td></tr>
<tr><td>COM0-COM63</td><td>O</td><td>Common output pins for graphic display.
By a combination of the scanning data and M signals, one signal level among V0, V1, V4 and VSS is selected.
<table>
<tr><th>Data</th><th>M</th><th>Output level</th></tr>
<tr><td>H</td><td>H</td><td>VSS</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
</table></td></tr>
</table>

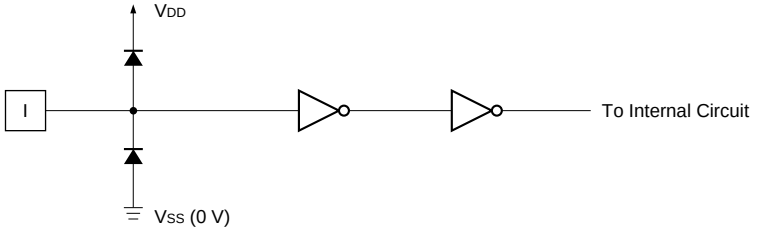
<table>
<tr><th>SYMBOL</th><th>I/O</th><th>DESCRIPTION</th></tr>
<tr><td>COMS0-COMS2</td><td>O</td><td>Common output pins for segment display.
When executing SEGON command, it functions as common output pin.
<table>
<tr><td></td><td>SEG ON</td><td>SEG OFF</td></tr>
<tr><td>COMS state</td><td>Display</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>SEGS0-SEGS11</td><td>O</td><td>Segment output pins for segment display.
When executing SEGON command, it functions as segment output pins.
<table>
<tr><td></td><td>SEGON = "1"</td><td>SEGON = "0"</td></tr>
<tr><td>SEGS state</td><td>Display</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>ICON1</td><td>O</td><td>Common output pin for icon display.
When executing ICON command, it functions as common icon display output pin.
<table>
<tr><td></td><td>ICON = "1"</td><td>ICON = "0"</td></tr>
<tr><td>ICON1 state</td><td>Display</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>ICON2</td><td>O</td><td>Data output pin for icon display.
When executing ICON command, it functions as data icon display output pin.
<table>
<tr><td></td><td>ICON = "1"</td><td>ICON = "0"</td></tr>
<tr><td>ICON2 state</td><td>Display</td><td>VSS</td></tr>
</table></td></tr>
</table>

1.5. Pins for Oscillation Circuit

SYMBOL	I/O	DESCRIPTION
OSCI OSCO	I O	Feedback-resistance connecting pin for the internal oscillation circuit.
EXA	I	Input pin of icon clock.
CK	I	Input pin of display master clock at master mode. When using CK pin as an input of the master clock, fix OSCI pin to VSS. When using the internal oscillation circuit as the display master clock, fix CK pin to VSS.
CKS	I	Selection input pin of display master clock at master mode. CKS = "H" : Input the external clock to CK pin. CKS = "L" : The internal oscillation circuit by using OSCI and OSCO pins is used.

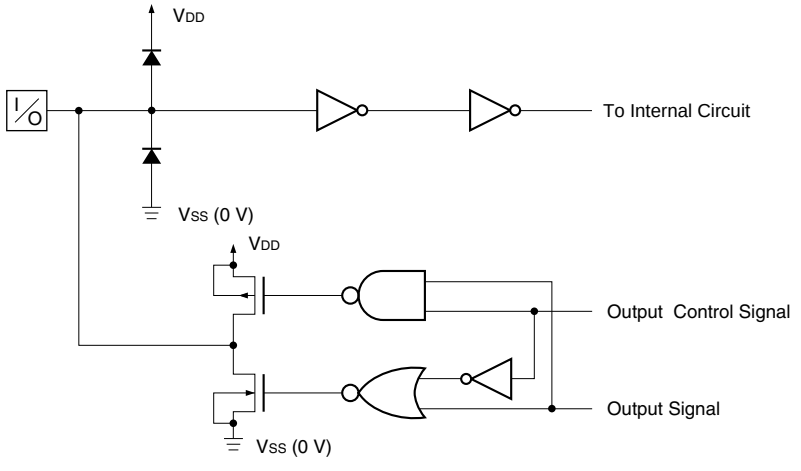
* Master clock : Clock for oscillation circuit or external clock.

1.6. Input/Output Circuits



【Applicable pins】
CSB, RS, RDB, WRB, M86, M/S, P/S, SDA, SCL, EXA, OSCI, CK, CKS, PMODE, RESB, TEST

Fig. 1 Input Circuit



【Applicable pins】
OSCO, FLM, LP, M

Fig. 2 Input/Output Circuit (1)

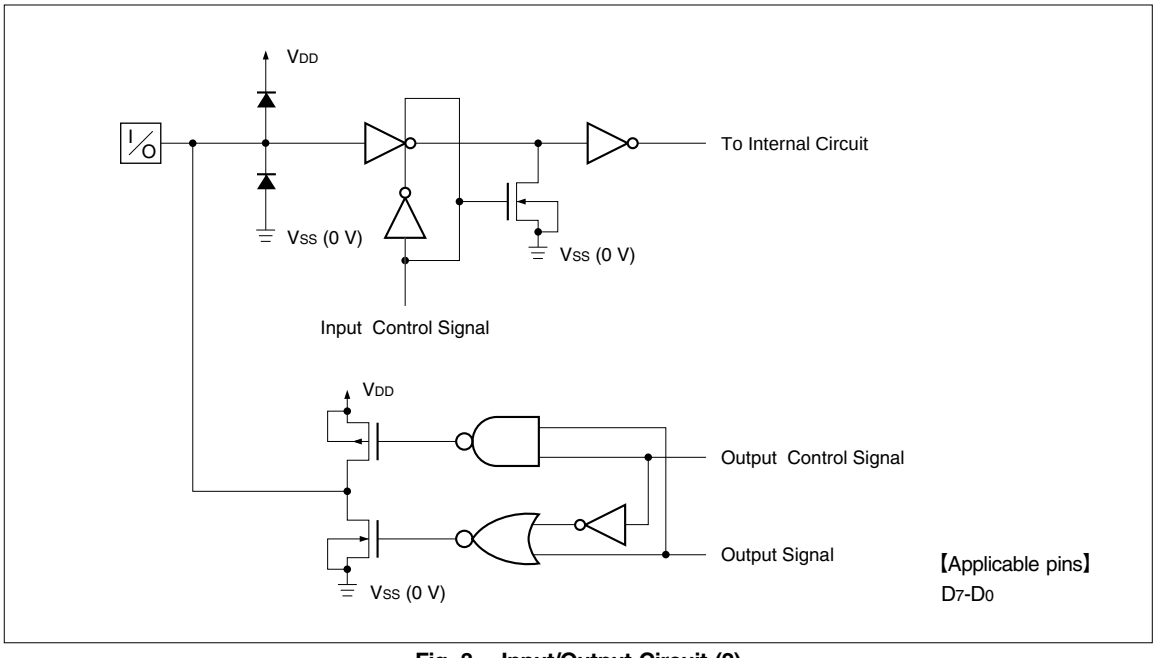


Fig. 3. Input/Output Circuit (2)

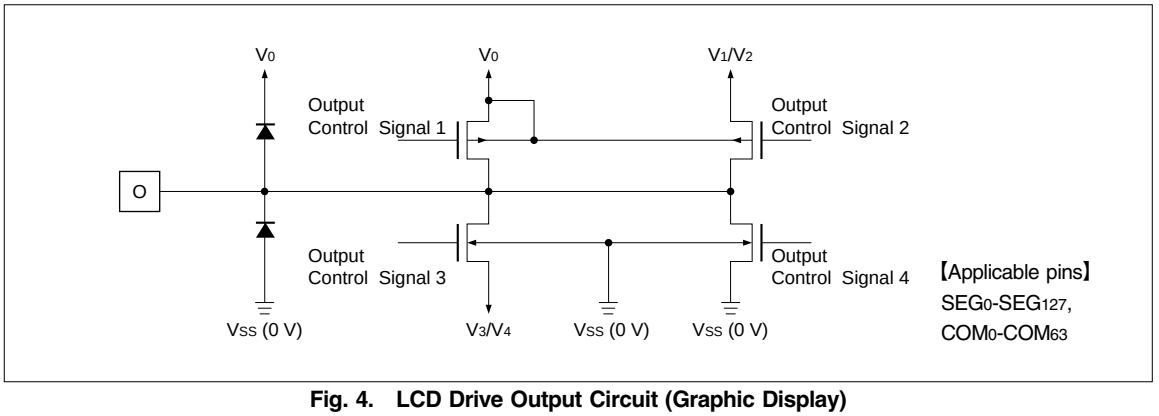


Fig. 4. LCD Drive Output Circuit (Graphic Display)

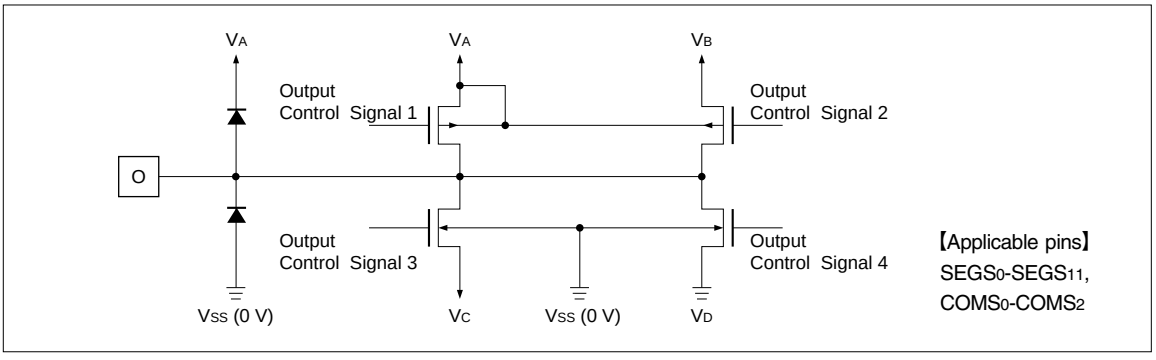


Fig. 5. LCD Drive Output Circuit (Segment Display)

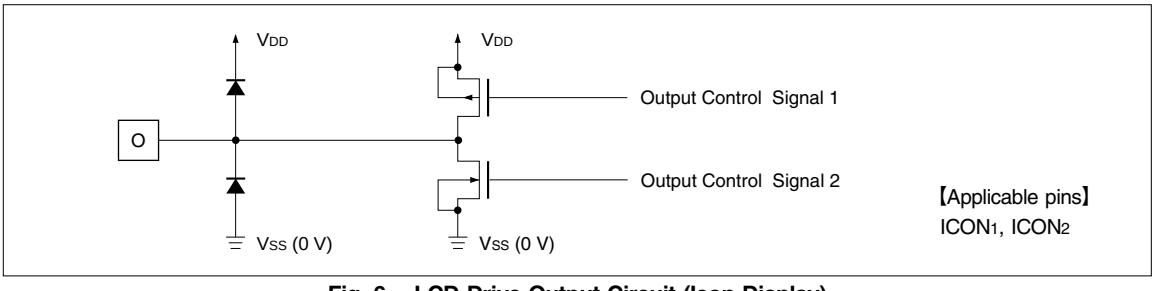


Fig. 6. LCD Drive Output Circuit (Icon Display)

2. FUNCTIONAL DESCRIPTION

2.1. MPU Interface

2.1.1. INTERFACE TYPE SELECTION

The LH155BA transfers data through 8-bit parallel I/O (D_7 to D_0) or serial data input (SDA, SCL).
The selection between parallel interface and serial interface is made by setting the state of P/S pin to "H" or "L".
When selecting serial interface, data-reading cannot be performed, but data-writing can.

P/S	I/F TYPE	CSB	RS	RDB	WRB	M86	SDA	SCL	DATA
H	Parallel	CSB	RS	RDB	WRB	M86	–	–	D_7 to D_0
L	Serial	CSB	RS	–	–	–	SDA	SCL	–

2.1.2. PARALLEL INPUT

The LH155BA can transfer data in parallel by directly connecting 8-bit MPU to the data bus when parallel interface is selected with P/S pin.
As an 8-bit MPU, either 80-family MPU interface or 68-family MPU interface is selected with M86 pin.

M86	MPU TYPE	CSB	RS	RDB	WRB	DATA
H	68-family MPU	CSB	RS	E	R/W	D_7 to D_0
L	80-family MPU	CSB	RS	RDB	WRB	D_7 to D_0

2.1.3. DATA IDENTIFICATION

The LH155BA can identify the data of 8-bit data bus by combinations of RS, RDB and WRB signals.

RS	68-FAMILY	80-FAMILY		FUNCTION
	R/W	RDB	WRB	
1	1	0	1	Reads from internal register
1	0	1	0	Writes to internal register
0	1	0	1	Reads from display data RAM
0	0	1	0	Writes to display data RAM

2.1.4. SERIAL INTERFACE

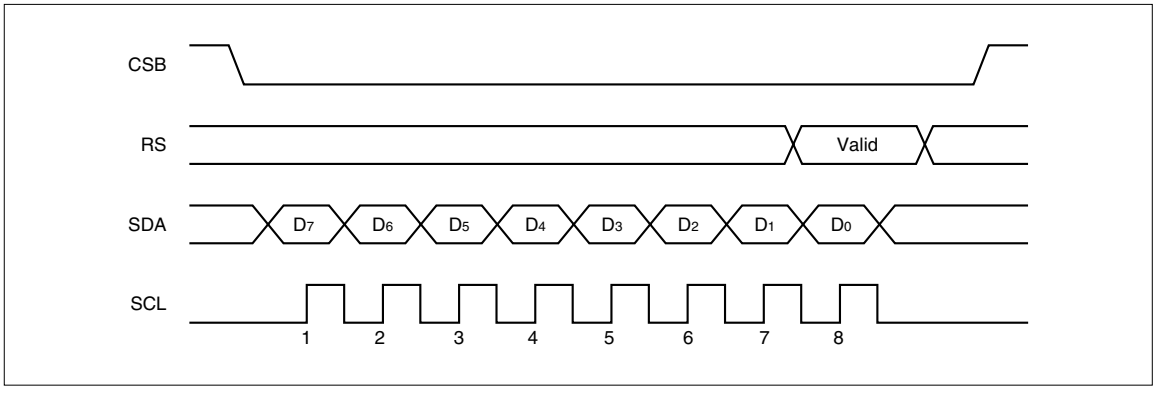
The serial interface of LH155BA can accept inputs of SDA and SCL in the chip selection state (CSB = "L"). When not in the chip selection state, the internal shift register and counter are reset to their initial condition.

Serial data SDA are input sequentially in order of D_7 to D_0 at the rising edge of serial clock (SCL) and are converted into 8-bit parallel data (by serial to parallel conversion) at the rising edge of the 8th serial clock, being processed in accordance with the data. The identification whether the serial data inputs (SDA) are display data or commands is judged by input to RS pin.

RS = "L" : Display data
RS = "H" : Commands

After completing 8-bit data transferring, or when making no access, be sure to set serial clock input (SCL) to "L".

Protection of SDA and SCL signals against external noise should be taken in actual wiring. To prevent the successive recognition errors of transferring data from external noise, release the chip selection state (CSB = "H") at every completion of 8-bit data transferring.



2.2. Access to Display RAM and Internal Register

The LH155BA makes access to display RAM, and internal register by data bus D_7 to D_0, chip selection CSB pin, display RAM/register shifting RS pin, and read/write control RDB and WRB pins. When CSB is at "H", it is in non-selective state and cannot access display RAM and internal registers. When making access to them, set CSB to "L".

The access to either display RAM or internal registers can be shifted by RS input.

RS = "L" : Display RAM data

RS = "H" : Internal command register

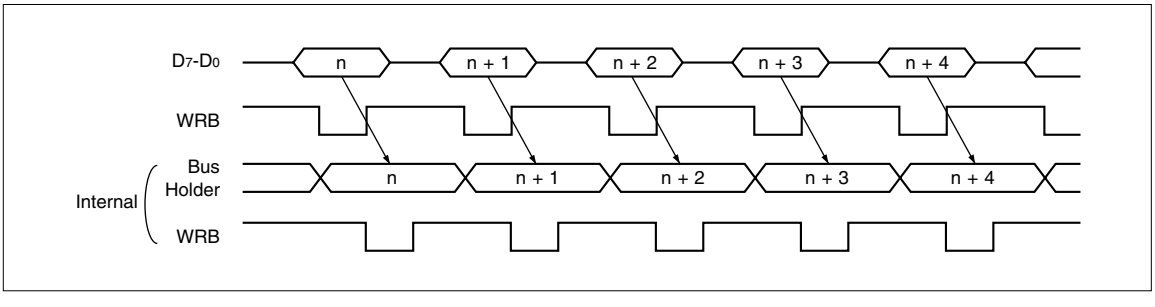
The data of 8-bit data bus D_7 to D_0 are written by write-operation after address setting through MPU. The timing of write is at the rising of WRB for 80-family MPU and at the falling of E for 68-family MPU respectively.

Write is internally processed by intermediately placing the bus holder in the internal data bus. During data writing from MPU, the data are temporally held in the bus holder, then they are written by the time of the next cycle.

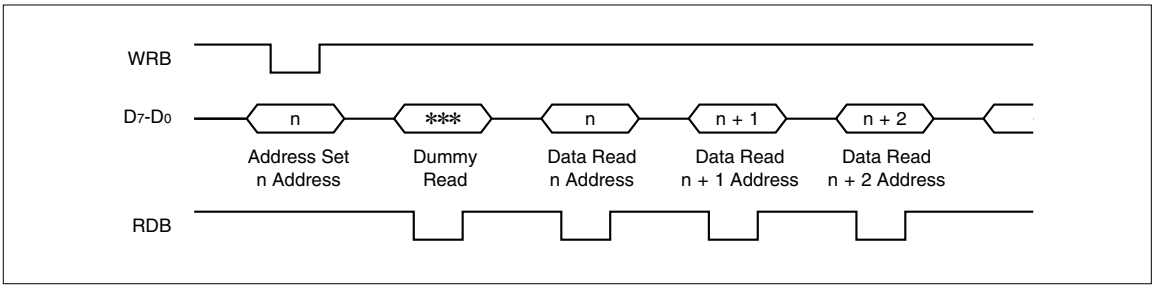
Since the read sequence of display RAM data is limited, note that when address set is made, the designated address data are not output to read command immediately after the address set, but are output when the second data are read, resulting in requiring one time dummy read.

Dummy read is always required one time after address set and write cycle.

Data Write Operation

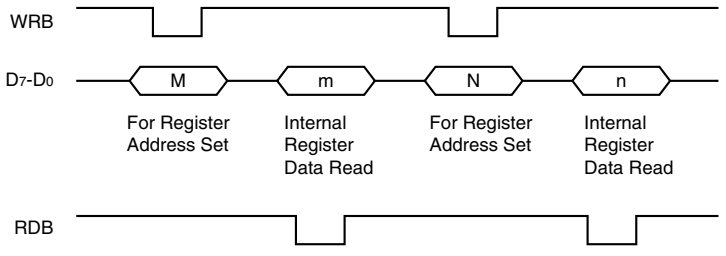


Data Read Operation



2.3. Read of Internal Register

The LH155BA reads not only display RAM, but also the internal registers. Read addresses (0H, 2H-EH) are allotted to each internal register. In reading the internal registers, the addresses of internal registers allotted to read are written in the registers for internal register read and then are read.



2.4. Display Mode

The LH155BA has 3 display modes.

One is for graphic display mode and one is for segment display mode and the other is for icon display mode. Since 3 modes can be used independently by command, the suitable display mode can be selected to drive the device with minimum circuit for lower supply current operation.

2.4.1. GRAPHIC DISPLAY MODE

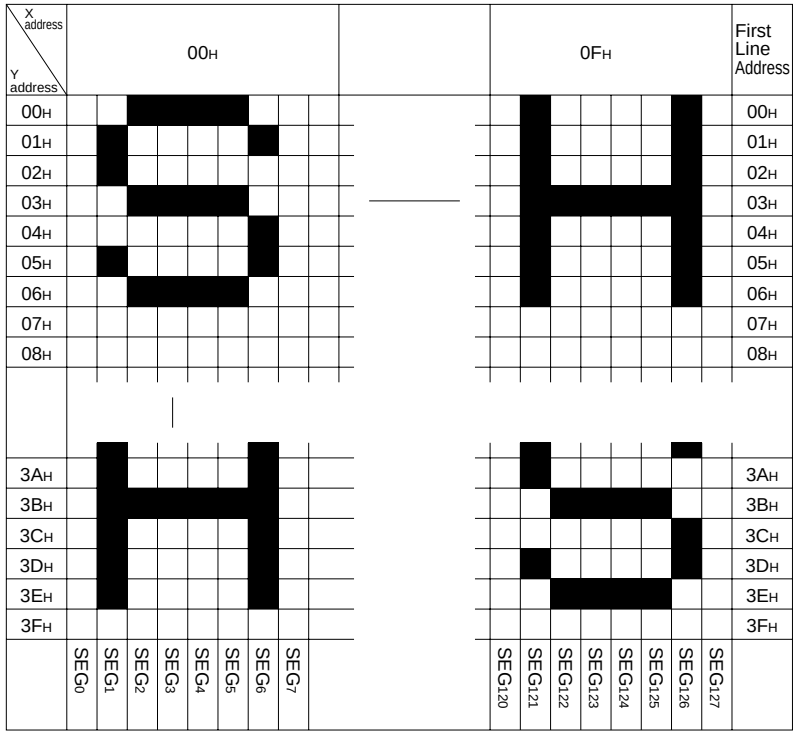
This mode is built in 64 x 128 bits SRAM and 64-common x 128-segment output.

Graphic display's memory map is shown below.

When standby mode and sleep mode, power supply circuit is stopped and output pin is specified V_{SS} level.

The memory for graphic display is accessed by 8 bits at one time.

X address is from 00H to 0FH and Y address is from 00H to 3FH.



2.4.2. SEGMENT DISPLAY MODE

This mode enables 3 x 12 bits memory and 3 COMS x 12 SEGS output.

Segment display's memory map is below.

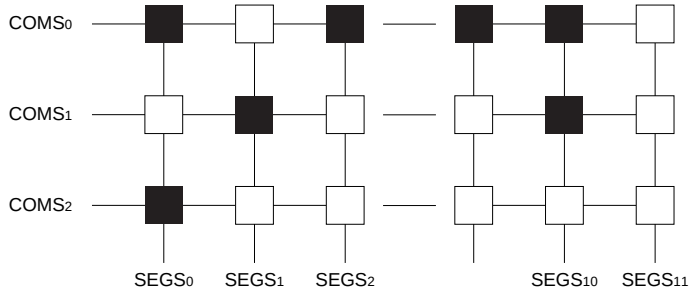
Bias is fixed to 1/3. When display OFF, each output pin is specified V_{SS} level.

X address is from 00_H to 01_H, and Y address is from 40_H to 42_H.

Segment display mode and graphic display mode are independent of each other.

When using segment display mode, lower power operation is possible.

When using slave mode, input clock for segment display at EXA pin (500 Hz : Duty 50%), and this time, EXA flag (E_H register : See **Section 4.14. "Power Control (3) Register Set"**) must be fixed to "H".



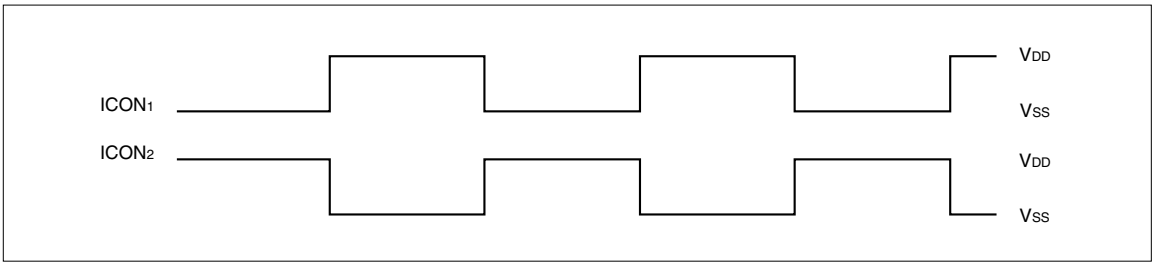
	00H								01H			
40H	■		■							■		
41H		■									■	
42H	■											
	SEGS0	SEGS1	SEGS2	SEGS3	SEGS4	SEGS5	SEGS6	SEGS7	SEGS8	SEGS9	SEGS10	SEGS11

X address is 00_H-01_H, and Y address is 40_H-42_H.

2.4.3. ICON DISPLAY MODE

This mode enables 2 output pins for icon display and this mode can display 1 icon.
Source are V_{DD} and V_{SS}. Since this mode is independent of other mode completely, when using this mode, lower power operation is possible. Waveform of this mode is below.

To display, use internal clock or external clock.
When using external clock, input clock pulse to EXA pin (120 Hz : Duty 50%).
When using icon display and segment display, input 500 Hz, duty 50% pulse.



2.5. Display Starting Line Register

This register is for determining display starting line (usually the most upper line) corresponding to COM_0 when displaying the display data RAM.
The register is also used in picture-scrolling.
The 6-bit display starting address is set in this register by display starting line setting command.
The register is preset every timing of FLM signal variation in the display line counter. The line counter counts up being synchronized with LP input and generates line addresses which sequentially read out 128-bit data from display RAM to LCD drive circuit.

2.6. Addressing of Display RAM

Display RAM consists of 128 x 64 bits memory, and enables access in 8-bit unit to an address specified by X address and Y address from MPU.
It is possible to set up the addresses X and Y so that they can increment automatically with the address control register. The increment is made every time display RAM is read or written from MPU. (See **Section 4. "COMMAND FUNCTION"**.)
Though the X direction side is selected by X address while the Y direction side by Y address, 10_H-FF_H in the X address are inhibited and do not have the X address set in these addresses.
In the Y direction side, the 128-bit display data are internally read into the display data latch circuit at the rising of LP every one line cycle, and are output from the display data latch circuit at the falling of LP. 43_H-FF_H in the Y address are inhibited and do not have the Y address set in these addresses.
When FLM signals being output in one frame cycle are at "H", the value in the display starting line register are preset in the line counter and the line counter counts up at the falling of LP signals.
The display line address counter is synchronized with each timing signal of the LCD system to operate and is independent of address counters X and Y.

2.7. Display RAM Data and LCD

One bit of display RAM data corresponds to one dot of LCD. Normal display and reverse display by REV register are set up as follows.

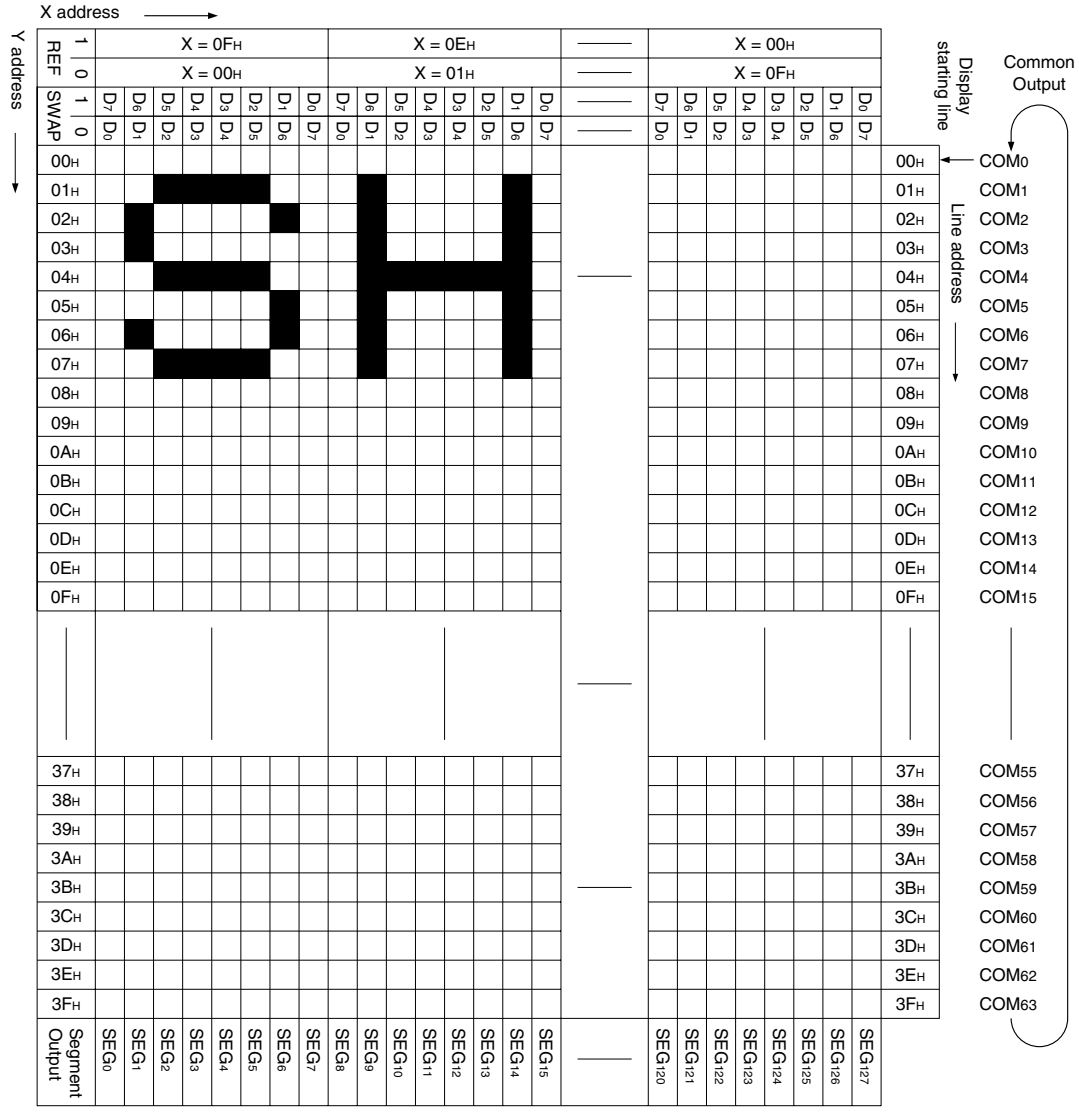
- Normal display (REV = 0) :
  RAM data = "0"; not lighted
  RAM data = "1"; lighted
- Reverse display (REV = 1) :
  RAM data = "0"; lighted
  RAM data = "1"; not lighted

2.8. Segment Display Output Order/ Reverse Set Up

The order of display outputs, SEG_0 to SEG_{127} can be reversed by reversing access to display RAM from MPU by using REF register, to lessen the limitation on placing IC when composing an LCD module.

2.9. Relationship between Display RAM and Address

(Configuration of display starting line address "00H")



2.10. Display Timing Generator

The display timing generator generates a timing clock necessary for internal operation and timing pulses (LP, FLM, and M) by inputting the master clock CK or by the oscillation circuit of OSCI and OSCO.

By setting up master/slave mode (M/S), the state of timing pulse pins and the timing generator changes.

Display Timing Pulse Pins and Timing Generator State

M/S PIN	MODE	LP PIN	M PIN	FLM PIN	STATE OF TIMING GENERATOR
L	Slave	Input	Input	Input	Stop of LP, M, FLM generation circuit
H	Master	Output	Output	Output	Operating state

2.11. Signal Generation to Display Line Counter, and Display Data Latching Circuit

Both the clock to the line counter and latching signals to display data latching circuit from the display clock (LP) are generated.

Synchronized with the display clock, the line addresses of display RAM are generated and 128-bit display data are latched to display-data latching circuit to output to the LCD drive circuit (SEG output).

Readout of the display data to the LCD drive circuit is completely independent of MPU. Therefore, a MPU that has no relationship the readout operation of the display data can access it.

2.12. Generation of The Alternating Signal (M) and The Synchronous Signal (FLM)

LCD alternating signal (M) and synchronous signal (FLM) are generated by the display clock (LP). The FLM generates alternated drive waveform to the LCD drive circuit. Normally, the FLM generates alternated drive waveform every frame unit (M-signal level is reversed every one frame).

But by setting up data (n – 1) in an n-line reverse register and n-line alternating command (NLIN) at "H", n-line reverse waveform is generated.

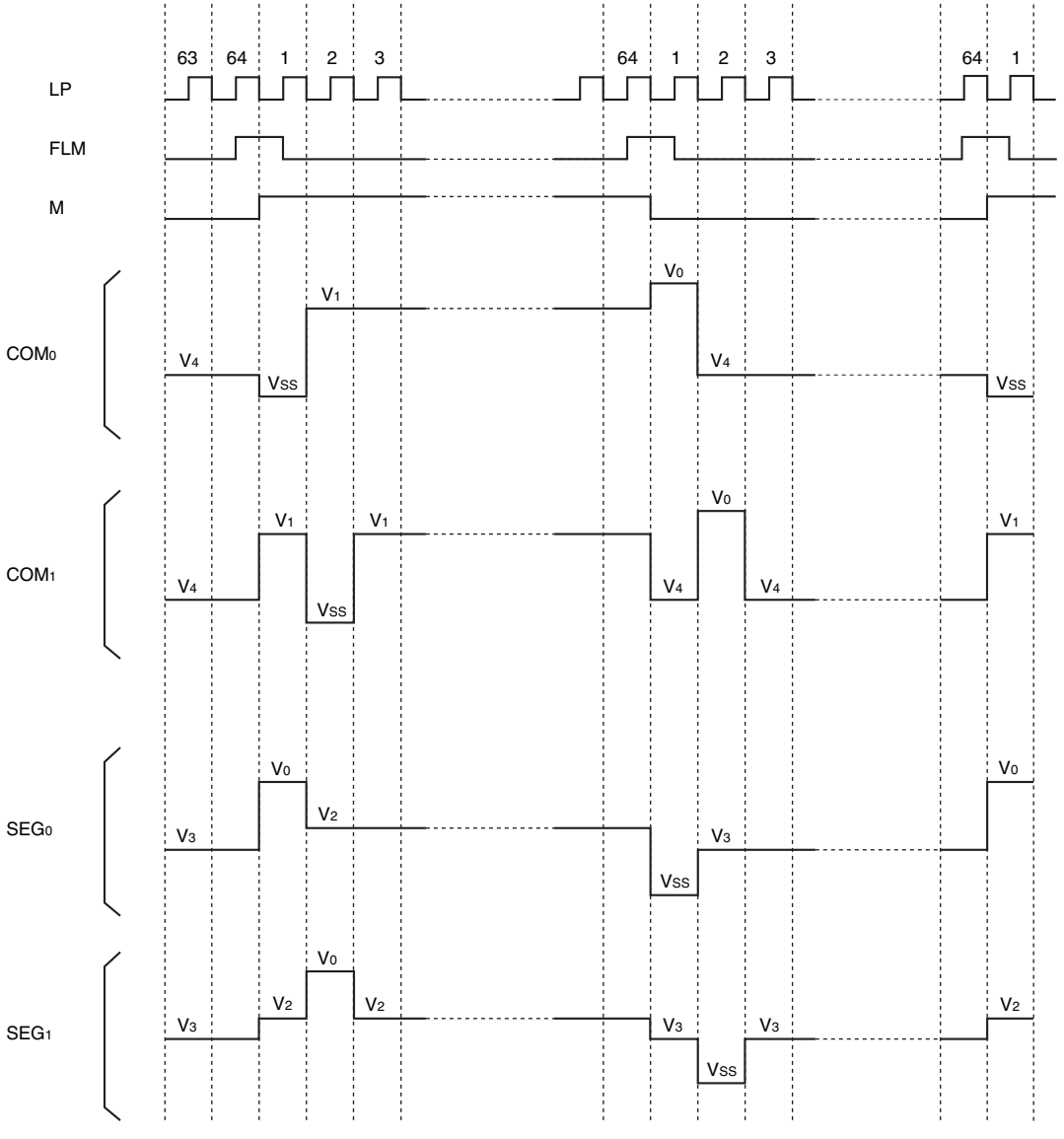
When the LH155BA is used in multi-chip, the signals of LP, FLM, and M must be sent from master side in the slave operation.

2.13. Display Data Latching Circuit

Display data latching circuit temporally latches display data that is output display data to LCD drive circuit from display RAM every one common period. Normal display/reverse display, display ON/OFF, and display all ON commands are operated by controlling data in the latch. And no data within display RAM changes.

2.14. Output Timing of LCD Driver

Display timing at normal mode, 1/64 duty



2.15. LCD Drive Circuit

This drive circuit generates 4 levels of LCD drive voltage. The circuit has 128 segment outputs and 64 common outputs and outputs combined display data and M signal. A common drive circuit that has a shift register sequentially outputs common scan signals.

2.16. Oscillation Circuit

The frequency of this CR oscillator is controlled by the feedback resistor R_F.

The output from this oscillator is used as the timing signal source of the display and the boosting clock to the booster circuit. This is valid only in the master operation mode.

During the slave operation mode, maintain OSCI pin at V_{SS} and OSCO pin open (NC).

When in the master operation mode and if external clock is used, maintain OSCI pin at V_{SS} and OSCO pin open (NC), and feed the clock to CK pin. The duty cycle of the external clock must be 50%.

The CKS pin selects either internal oscillation circuit or external clock.

CKS	MASTER MODE		SLAVE MODE	
	OSC	External Clock (CK)	OSC	External Clock (CK)
L	Enabled	Disabled	Disabled	Disabled
H	Disabled	Enabled	Disabled	Disabled

2.17. Power Supply Circuit

This circuit supplies voltages necessary to drive an LCD panel. This circuit is valid only in the master operation mode. The circuit consists of booster circuit and voltage converter.

Boosted voltage from the booster circuit is fed to the voltage converter which converts this high input voltage into V_0, V_1, V_2, V_3 and V_4 which are used for graphic display. This internal power supply should not be used to drive a large LCD panel containing many pixels or a large LCD panel that has large capacity consisting of more than one chip. Otherwise, display quality will degrade considerably. Instead, use an external power supply.

This internal power supply is controlled by the power supply circuit ON/OFF command (PON). When the internal power supply is turned off, the booster circuit and voltage converter are also turned off.

When using the external power supply, turn off the internal power supply, disconnect pins CAP+, CAP−, V_{EE2}, V_{EE3}, V_{OUT}, V_{EE}, V_{R1} and V_{R2}, and keep PMODE pin at V_{SS}. Then, feed external LCD drive voltages to pins V_0, V_1, V_2, V_3, and V_4.

This circuit can be changed by the state of PMODE pin.

PON	PMODE	BOOSTER CIRCUIT	VOLTAGE CONVERTER	EXTERNAL VOLTAGE INPUT	NOTE
0	0	Disabled	Disabled	V_0, V_1, V_2, V_3, V_4	1
0	1	Disabled	Disabled	V_0, V_1, V_2, V_3, V_4	1
1	0	Enabled	Enabled	–	
1	1	Disabled	Enabled	V_{OUT}, V_{R1}, V_{R2}	2

NOTES :

1. Because the booster circuit and voltage converter are not functioning, disconnect pins CAP+, CAP−, V_{EE2}, V_{EE3}, V_{OUT}, V_{EE}, V_{R1} and V_{R2}.
   Apply external LCD drive voltages to corresponding pins.
2. Because the booster circuit is not functioning, disconnect pins CAP+, CAP−, V_{EE2}, V_{EE3} and V_{EE}. Derive the voltage source to be supplied to the voltage converter from V_{OUT} pin and then output LCD drive voltage to V_{R1} and V_{R2} pins. The voltage level at V_{R1} and V_{R2} pins must be $V_{R2} \leq V_{R1} \leq V_{OUT}$.

2.18. Booster Circuit

Setting BS register, booster circuit multiple can be selected. Placing capacitor C_1 across CAP+ and CAP–, across V_{EE2} and V_{SS}, across V_{EE3} and V_{SS} and across V_{OUT} and V_{SS} boosts four times.

Placing capacitor C_1 across CAP+ and CAP–, across V_{EE2} and V_{SS}, across V_{OUT} and V_{SS}, and setting V_{EE3} to NC when boosting three times.

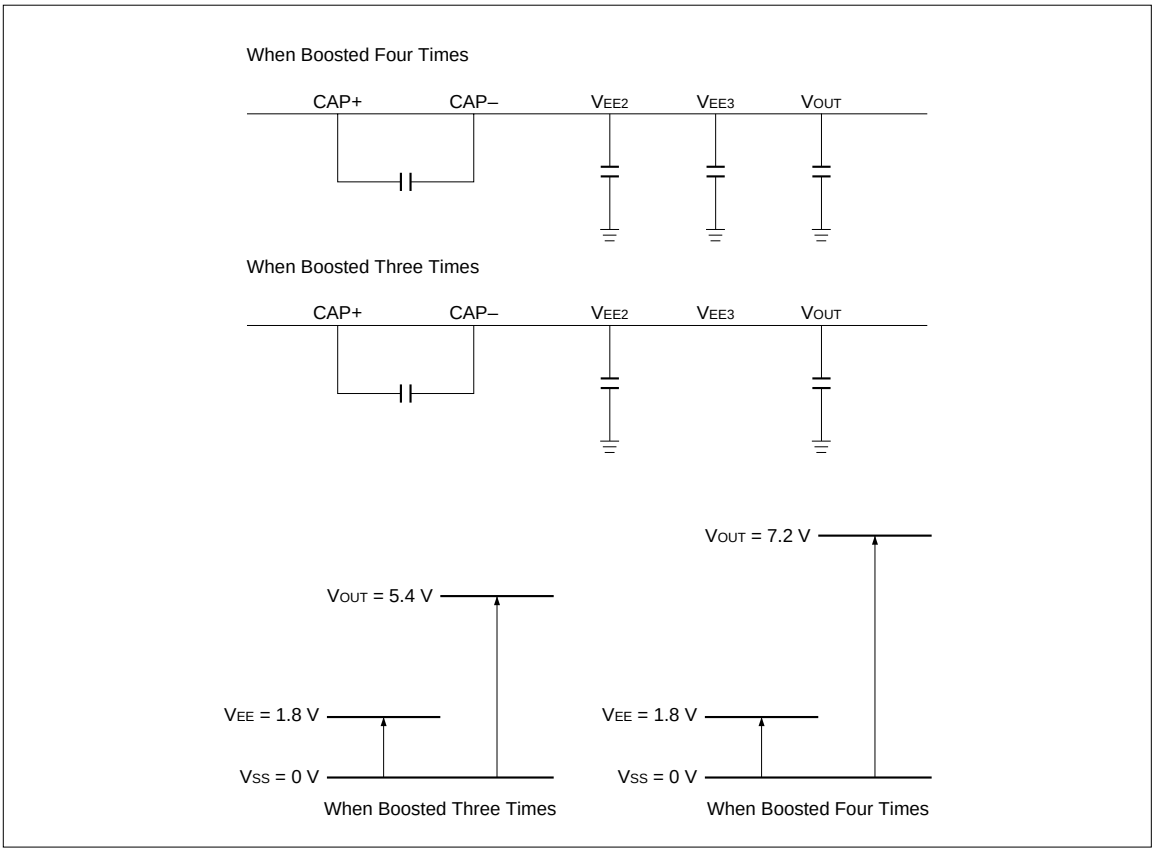
Placing C_1 across CAP+ and CAP–, across V_{OUT} and V_{SS}, and setting V_{EE2} and V_{EE3} to NC when boosting two times.

The boosted voltage is output to V_{OUT} pin.

Since the booster circuit uses the clock derived from the internal oscillation circuit or external clock as the boosting clock, the internal oscillation circuit must be enabled, or if external clock is selected, it must be fed to CK pin.

The output level at the V_{OUT} pin does not exceed the recommended maximum operating voltage (14.0 V) when the voltage is boosted. If this value is exceeded, the operation of the LH155BA is not covered by warranty.

When boosting four times and three times, placement of capacitor is as shown below.



If charge up of LCD drive voltage is not successful, check capacity, voltage dependency and temperature characteristics of external capacitor, and select appropriate device. When charge up is unsuccessful, it is advisable to charge up LCD drive voltage step by step (x 2, x 3, x 4) by inputting software from external microcontroller.

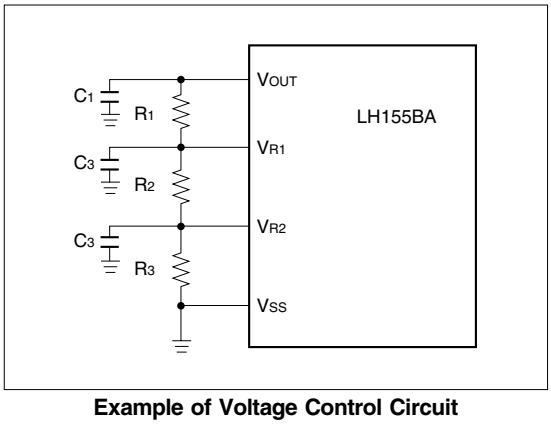
2.19. Voltage Control Circuit

The boosted voltage at the V_{OUT} pin is connected to the V_{R1} and V_{R2} pins and then the LCD drive voltages (V_0, V_1, V_2, V_3, and V_4) are generated via the voltage converter. The input level at the V_{R1} and V_{R2} must meet the electric potential condition of $V_{R1} \geq V_{R2}$. The internal electronic volume divides the electric potential between the V_{R1} and V_{R2} into 16 segments.

Since the V_{R1} and V_{R2} pins have high input impedance, the input voltage levels at the V_{R1} and V_{R2} are determined by the resistance ratio of R_1, R_2, and R_3. The current flowing between the V_{OUT} and V_{SS} pins is determined by the combined resistance of R_1, R_2, and R_3.

Therefore, R_1, R_2, and R_3 must be selected in accordance with the above current as well as the input voltage levels at the V_{R1} and V_{R2}.

The boosted voltage at the V_{OUT} pin originates from the voltage supplied at the V_{EE} pin. Thus, the DC path current generated with R_1, R_2, and R_3 connected between the V_{OUT} and V_{SS} pins is supplied as current at the V_{EE} pin. The electric current value, four times larger than the DC path current generated between the V_{OUT} and V_{SS} pins when the voltage is boosted four times, is added as supply current at the V_{EE} pin (three times larger current is added for tripled voltage). Take sufficient care that the input levels at the V_{R1} and V_{R2} pins do not fluctuate with external noise (connect capacitor C_3).



Example of Voltage Control Circuit

2.20. Electronic Volume

The voltage converter incorporates an electronic volume, which allows the LCD drive voltage level V_0 to be controlled with a command and also allows the tone of LCD to be controlled.

If 4-bit data is stored in the register of the electronic volume, one level can be selected among 16 voltage values for the LCD drive voltage V_0. The voltage control range of the electronic volume is determined by the input voltage levels at the V_{R1} and V_{R2}. This means that the voltage range of (V_{R1} to V_{R2}) for the graphic display voltage control circuit is the controllable voltage range of the electronic volume. The electric potential relation between the V_{R1} and V_{R2} pins must be $V_{R1} \geq V_{R2}$. The input voltage levels at the V_{R1} and V_{R2} must be selected in accordance with the voltage levels to be obtained with the electronic volume.

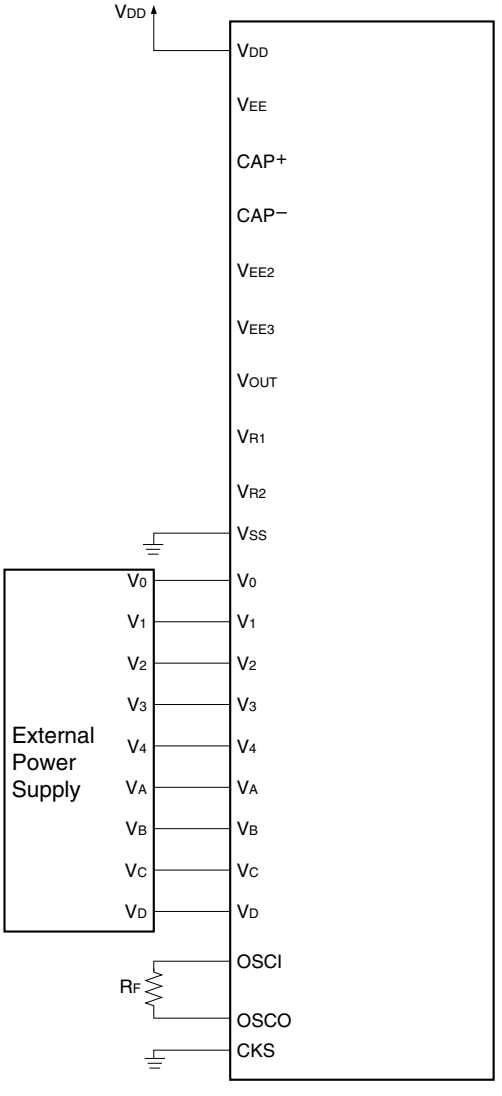
2.21. LCD Drive Voltage Generation Circuit

The voltage converter contains the voltage generation circuit. The LCD drive voltages other than V_0, that is, V_1, V_2, V_3 and V_4, are obtained by dividing V_0 through a resistor network. The LCD drive voltage from LH155BA is biased at 1/7 or 1/9 for the graphic display mode and at 1/3 (fixed) for the segment display mode.

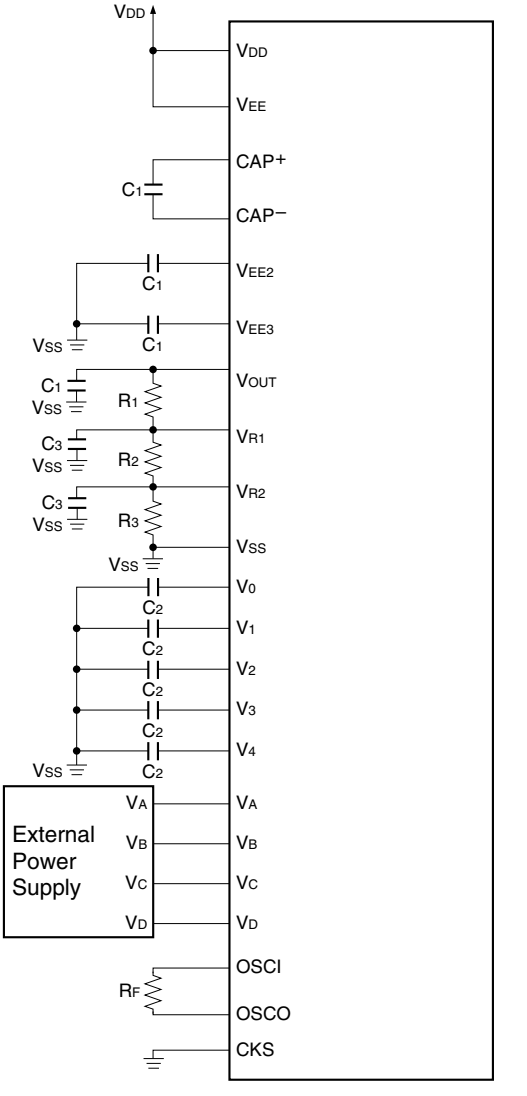
When using the internal power supply, connect a stabilizing capacitor C_2 to each of pins V_0 to V_4.

The capacitance of C_2 should be determined while observing the LCD panel to be used. In this case, connect a capacitor C_3 to stabilize input voltage to V_{R1} and V_{R2}. A value of C_3 can be defined selectively.

2.22. Example of Power Supply Circuit Connection



When Using The External Power Supply



When Using The Internal Power Supply

Recommended Values

C_1	1.0 to 5.0 µF (B)*
C_2	1.0 to 2.0 µF (B)*
C_3	0.01 to 0.1 µF
R_F	680 kΩ
$R_1 + R_2 + R_3$	2.0 to 4.0 MΩ

* B characteristics must be used with C_1 and C_2.

2.23. Initialization

The LH155BA is initialized by setting RESB pin to "L". Normally, RESB pin is initialized together with MPU by connecting to the reset pin of MPU.
When power is ON, be sure to reset operation.

PARAMETER	INITIAL STATE
Display RAM	Not fixed
X-address	00H set
Y-address	00H set
Display starting line	Set at the first line (0H)
Display ON/OFF	Display OFF
Display normal/reverse	Normal
Display duty	1/64
n-line alternating	Every frame unit
Common shift direction	$COM_0 \rightarrow COM_{63}$
Increment mode	Increment OFF
REF mode	Normal
Data SWAP mode	OFF
Register in electronic volume	(1, 1, 1, 1)
Power supply	OFF

3. PRECAUTIONS

Precautions when connecting or disconnecting the power supply

This IC may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. The details are as follows.

① When using an external power supply

- When connecting the power supply
  After connecting the logic system power supply, make reset operation and then apply external LCD drive voltages to corresponding pins. (V_0, V_1, V_2, V_3, V_4 or V_{OUT}, V_{R1} and V_{R2})
- When disconnecting the power supply
  After executing HALT command, disconnect external LCD drive voltages and then disconnect the logic system power supply.

② When using the internal power supply

- When connecting the power supply
  After connecting the logic system power supply, make reset operation and then execute PON command.
- When disconnecting the power supply
  After executing HALT command, disconnect the logic system power supply.

It is advisable to connect the serial resistor (50 to 100 Ω) or fuse to the LCD drive power V_{OUT} or V_0 of the system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

4. COMMAND FUNCTION

4.1. Command Function Table

INSTRUCTION	CODE					CODE								FUNCTION
	CSB	RS	WRB	RDB	RE	D7	D6	D5	D4	D3	D2	D1	D0	
Display data write	0	0	0	1	0	WRITE DATA								Writes to display RAM.
Display data read	0	0	1	0	0	READ DATA								Reads from display RAM.
X address set [0H]	0	1	0	1	0	0	0	0	0	X Address				Sets X direction address in display RAM.
Y address set (Lower) [2H]	0	1	0	1	0	0	0	1	0	Y Address				Sets Y direction address in display RAM.
Y address set (Upper) [3H]	0	1	0	1	0	0	0	1	1	*	Y Address			Sets Y direction address in display RAM.
Display starting line set (Lower) [4H]	0	1	0	1	0	0	1	0	0	Display Starting Line				Sets line address of RAM making COM0 display.
Display starting line set (Upper) [5H]	0	1	0	1	0	0	1	0	1	*	*	Display Starting Line		Sets line address of RAM making COM0 display.
n-line alternating set (Lower) [6H]	0	1	0	1	0	0	1	1	0	Alternating Line				Sets the number of alternating reverse line.
n-line alternating set (Upper) [7H]	0	1	0	1	0	0	1	1	1	*	*	Alternating Line		Sets the number of alternating reverse line.
Display control (1) set [8H]	0	1	0	1	0	1	0	0	0	SHIFT	SEGON	ALLON	ON/OFF	①
					1					*	*	ER	IR	ER : Segment's external source IR : Segment source mode
Display control (2) set [9H]	0	1	0	1	0	1	0	0	1	REV	NLIN	SWAP	REF	②
Increment control set [AH]	0	1	0	1	0	1	0	1	0	*	AIM	AYI	AXI	AIM : Increment mode selection AYI : Y increment, AXI : X increment
Power control (1) set [BH]	0	1	0	1	0	1	0	1	1	BIAS	HALT	PON	ACL	BIAS : 1/7 or 1/9, HALT : HALT ON PON : Power ON, ACL : reset
Power control (2) set [DH]	0	1	0	1	0	1	1	0	1	DVOL				Sets electronic volume for the graphic display.
Power control (3) set [EH]	0	1	0	1	0	1	1	1	0	SEGPON	*	EXA	ICON	③
					1					DUTY DU1	DUTY DU0	BS1	BS0	DUTY : Selects duty ratio. BS : Selects boosted voltage level.
RE set [FH]	0	1	0	1	0/1	1	1	1	1	*	*	*	RE	Sets RE flag.
Address set for internal register read	0	1	0	1	0	1	1	0	0	Address for Register Read				Sets address of internal register for reading.
Internal register read	0	1	1	0	0	*	*	*	*	Read Data				Reads out internal register.

① SHIFT : Common shift direction for the graphic display, SEGON : Segment display ON, ALLON : All graphic display ON, ON/OFF : Graphic display ON/OFF control

② REV : Graphic display normal/reverse, NLIN : n-line reverse ON, SWAP : Data for graphic display swap, REF : Segment output for graphic display normal/reverse

③ SEGPON : Power supply for segment display (Not available now. Set to "0".), EXA : Clock for segment display external/internal, ICON : Icon display ON

* mark means "Don't care".

Parenthesis [ ] shows address for internal register read.

The LH155BA has a lot of commands, as shown in the list of commands, and each command is explained in detail as follows.

Data codes and command codes are defined as follows and the execution of commands must be made in the chip selection state (CSB = "L").

(For example X address)

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
*	0	0	0	0	AX3	AX2	AX1	AX0
← Command Codes →					← Data Codes →			

* RS = "0" : RAM data access (Refer to **Sections 4.2. and 4.3.**.)
  RS = "1" : Register access (Refer to **Sections 4.4. through 4.17.**.)
  The undefined command codes are inhibited.

4.2. Data Write to Display RAM

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display RAM Write Data							

CSB	RS	WRB	RDB	RE
0	0	0	1	0

The display RAM data of 8-bit are written in the designated X and Y addresses.

4.3. Data Read to Display RAM

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display RAM Read Data							

CSB	RS	WRB	RDB	RE
0	0	1	0	0

The 8-bit contents of display RAM designated in X and Y addresses are read out.
Immediately after data are set in X and Y addresses, dummy read is necessary one time.

4.4. X Address Register Set

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	AX3	AX2	AX1	AX0

CSB	RS	WRB	RDB	RE
0	1	0	1	0

(At the time of reset : AX3 to AX0 = 0_H, read address : 0_H)

Addresses of display RAM's X direction are set. The values of AX3 to AX0 are usable up to 00_H-$0F_H$, but 10_H-FF_H are inhibited. When the register setting of SEG output normal/reverse is REF = "0", the data of AX3 to AX0 are addressed to display RAM as they are.
When REF = "1", the data of $0F_H$-(AX3 to AX0)$_H$ are addressed to the display RAM.

4.5. Y Address Register Set

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	AY3	AY2	AY1	AY0

CSB	RS	WRB	RDB	RE
0	1	0	1	0

(At the time of reset : AY3 to AY_0 = 0H, read address : 2H)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	AY6	AY5	AY4

CSB	RS	WRB	RDB	RE
0	1	0	1	0

* mark means "Don't care".

(At the time of reset : AY6 to AY4 = 0H, read address : 3H)

Addresses of display RAM's Y direction are set. In data-setting, lower place and upper place are divided with 4 bits and 3 bits respectively.
When data are set, lower place should be set first and upper place should be set second.

The values of AY6 to AY0 are usable up to 00H-42H, but 43H-FFH are inhibited.
The addresses of 40H to 42H are for the segment display RAM.

4.6. Display Starting Line Register Set

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	LA3	LA2	LA1	LA0

CSB	RS	WRB	RDB	RE
0	1	0	1	0

(At the time of reset : LA3 to LA0 = 0H, read address : 4H)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	LA5	LA4

CSB	RS	WRB	RDB	RE
0	1	0	1	0

* mark means "Don't care".

(At the time of reset : LA5, LA4 = 0H, read address : 5H)

The display line address is required to designate, and the designated address becomes the display line of COM_0.

The display of LCD is displayed from the designated display starting line address to the increment direction of the line address.

LA5	LA4	LA3	LA2	LA1	LA0	LINE ADDRESS
0	0	0	0	0	0	0
0	0	0	0	0	1	1
		|				|
1	1	1	1	1	1	63

4.7. n-line Alternating Register Set

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	N3	N2	N1	N0

CSB	RS	WRB	RDB	RE
0	1	0	1	0

(At the time of reset : N3 to N0 = 0H, read address : 6H)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	N5	N4

CSB	RS	WRB	RDB	RE
0	1	0	1	0

* mark means "Don't care".

(At the time of reset : N5, N4 = 0H, read address : 7H)

The reverse line number of LCD alternated drive is required to be set in the register. The line number possible to be set is 2 to 64 lines.

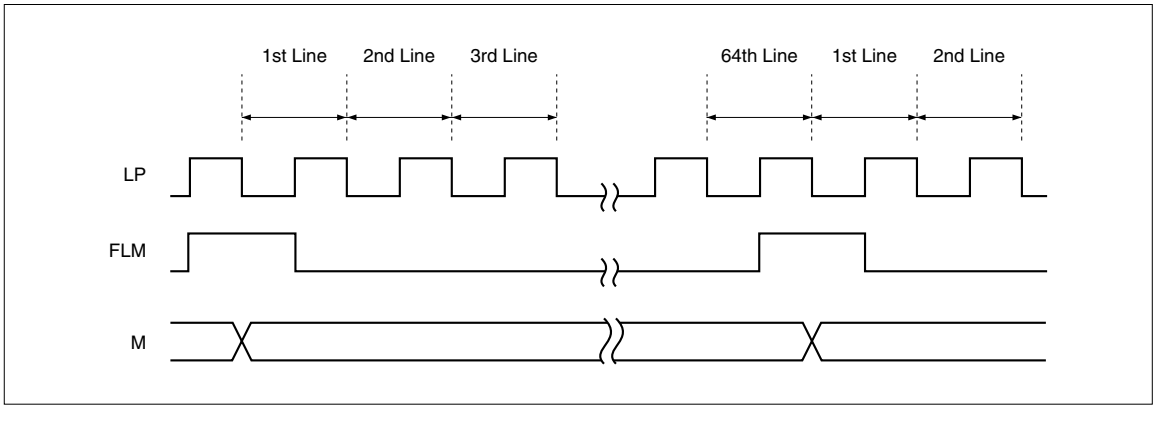
The values set up by the n-line alternating register become enabled when the n-line alternated drive command is ON (NLIN = "1").

When the n-line alternated drive command is OFF (NLIN = "0"), an alternated drive waveform which reverses by frame cycle is generated.

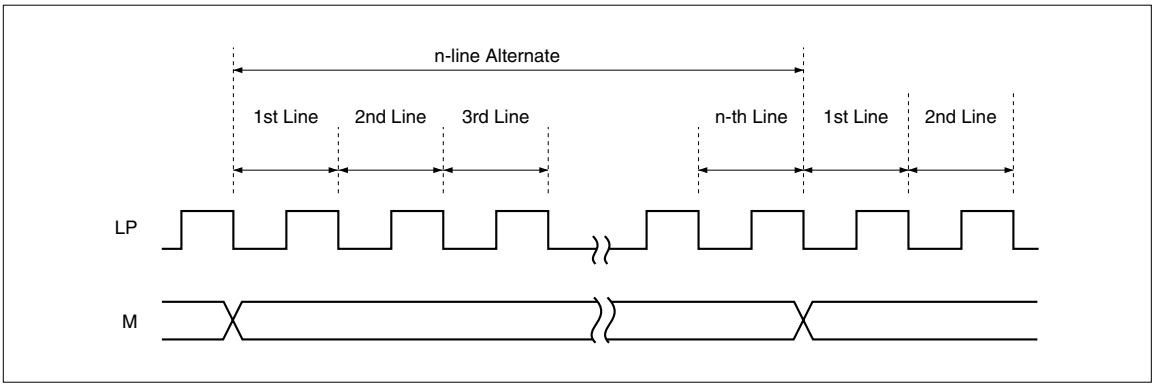
N5	N4	N3	N2	N1	N0	REVERSE LINE NUMBER
0	0	0	0	0	0	–
0	0	0	0	0	1	2
			|			|
1	1	1	1	1	1	64

4.8. Alternating Timing

(1) At The Time of n-line Alternating OFF (in case of 1/64 duty display)



(2) At The Time of n-line Alternating ON



4.9. Display Control (1) Register Set

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	SHIFT	SEGON	ALLON	ON/OFF

CSB	RS	WRB	RDB	RE
0	1	0	1	0

(At the time of reset : (SHIFT, SEGON, ALLON, ON/OFF) = 0_H, read address : 8_H)

Various controls of display are set up.

(1) ON/OFF Command (For the graphic display only)
To control ON/OFF of the graphic display.
ON/OFF = "0" : Display OFF
ON/OFF = "1" : Display ON

(2) ALLON Command (For the graphic display only)
Regardless of the data of the graphic display RAM, all the graphic displays are ON.
This command has priority over display normal/reverse commands.
ALLON = "0" : Normal display
ALLON = "1" : All displays lighted.

(3) SEGON Command (For the segment display only)
To control ON/OFF of the segment display.
SEGON = "0" : Display OFF
The pins are specified V_{SS} level.
SEGON = "1" : Display ON

(4) SHIFT Command (For the graphic display only)
The shift direction of the graphic display scanning data in the common drive output is selected.
SHIFT = "0" : $COM_0 \rightarrow COM_{63}$ shift-scan
SHIFT = "1" : $COM_{63} \rightarrow COM_0$ shift-scan

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	*	*	ER	IR

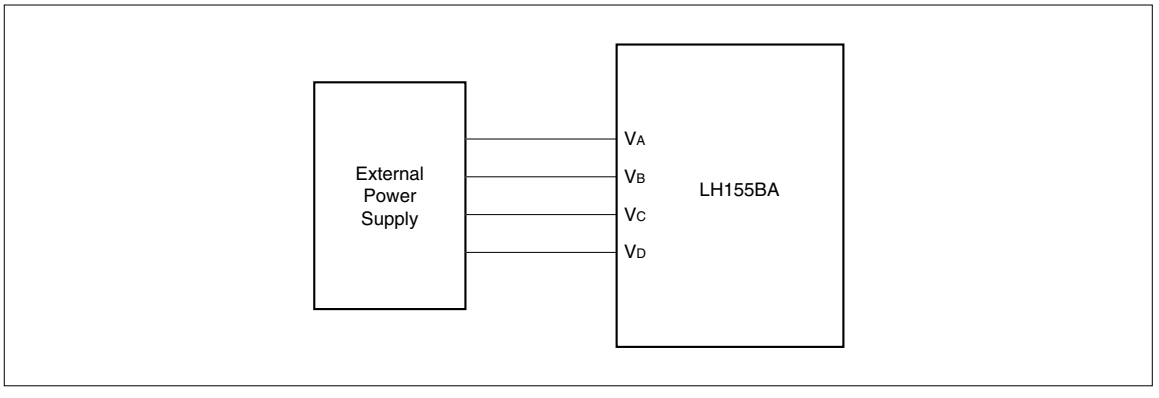
CSB	RS	WRB	RDB	RE
0	1	0	1	1

* mark means "Don't care".
(At the time of reset : (ER, IR) = 0_H, read address : 8_H)

(1) IR Command (For the segment display only)
IR command is not available now. When using the segment display, set to "0".

(2) ER Command (For the segment display only)
ER command is not available now. When using the segment display, set to "1".

And when using the segment display, input V_A, V_B, V_C and V_D level externally.



4.10. Display Control (2) Register Set

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	REV	NLIN	SWAP	REF

CSB	RS	WRB	RDB	RE
0	1	0	1	0

(At the time of reset : (REV, NLIN, SWAP, REF) = 0H, read address : 9H)

Various controls of display are set up.

(1) REF Command

When MPU accesses to the graphic display RAM, the relationship between X address and write data is normalized or reversed.

Therefore, the order of segment drive output can be reversed by register setting, to lessen the limitation on placing IC when composing an LCD module.

REF	ACCESS FROM MPU		INTERNAL ACCESS		CORRESPONDING SEG OUTPUT
	X ADDRESS	D7-D0	X ADDRESS	D7-D0	
0	nH	D0 (LSB) | D7 (MSB)	nH	(LSB) | (MSB)	SEG (8 x nH) output | SEG (8 x nH + 7) output
1	nH	D0 (LSB) | D7 (MSB)	0FH-nH	(MSB) | (LSB)	SEG (8 x (0FH – nH) + 7) output | SEG (8 x (0FH – nH)) output

When using this command, outputs of segment display circuits are set as below.
However the order of $D_0 \rightarrow D_7$ are not changed.

When REF = "1", set X address of segment display circuits described below.

$00_H \rightarrow 0F_H$

$01_H \rightarrow 0E_H$

REF	ACCESS FROM MPU		INTERNAL ACCESS		CORRESPONDING
	X ADDRESS	D_7-D_0	Y ADDRESS	D_7-D_0	SEGS OUTPUT
0	00_H	D_0 (LSB) | D_7 (MSB)	00_H	D_0 (LSB) | D_7 (MSB)	$D_0 \rightarrow D_7$ $SEGS_0 \rightarrow SEGS_7$
0	01_H	D_0 (LSB) | D_3 (MSB)	01_H	D_0 (LSB) | D_3 (MSB)	$D_0 \rightarrow D_3$ $SEGS_8 \rightarrow SEGS_{11}$
1	$0F_H$	D_0 (LSB) | D_7 (MSB)	00_H	D_0 (LSB) | D_7 (MSB)	$D_0 \rightarrow D_7$ $SEGS_0 \rightarrow SEGS_7$
1	$0E_H$	D_0 (LSB) | D_3 (MSB)	01_H	D_0 (LSB) | D_3 (MSB)	$D_0 \rightarrow D_3$ $SEGS_8 \rightarrow SEGS_{11}$

(2) SWAP Command (For the graphic display only)
When data to the graphic display RAM are written, the write data are swapped.
SWAP = "0" : Normal mode. In data-writing, the data of D_7 to D_0 can be written to the graphic display RAM.
SWAP = "1" : SWAP mode ON. In data-writing, the swapped data of D_7 to D_0 can be written to the graphic display RAM.

	SWAP = "0"	SWAP = "1"
EXTERNAL DATA	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
INTERNAL DATA	d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	d_0 d_1 d_2 d_3 d_4 d_5 d_6 d_7

(3) NLIN Command (For the graphic display only)
The ON/OFF control of n-line alternated drive is performed.
NLIN = "0" : n-line alternated drive OFF.
By using frame cycle, the alternating signals (M) are reversed.
NLIN = "1" : n-line alternated drive ON.
According to data set up in n-line alternating register, the alternation is made.

(4) REV Command (For the graphic display only)
Corresponding to the data of the graphic display RAM, the lighting or not-lighting of the display is set up.
REV = "0" : When RAM data are at "H", LCD at ON voltage (normal).
REV = "1" : When RAM data are at "L", LCD at ON voltage (reverse).

4.11. Increment Control Register Set

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	*	AIM	AYI	AXI

CSB	RS	WRB	RDB	RE
0	1	0	1	0

* mark means "Don't care".

(At the time of reset : (AIM, AYI, AXI) = 0_H, read address : A_H)

The increment mode is set up when accessing the graphic display RAM.

(The graphic display RAM only)

By AIM, AYI, and AXI registers, the setting-up of increment operation/non-operation for the X-address counter and the Y-address counter every write access or every read access to the graphic display RAM is possible.

In setting to this control register, the increment operation of address can be made without setting successive addresses for writing data or for reading data to the graphic display RAM from MPU.

After setting this register, be sure to set the X and Y address registers.

Because it is not assuring the data of X and Y address registers after setting increment control registers, the increment control of X and Y addresses by AIM, AYI and AXI registers is as follows.

AIM	SELECTION OF INCREMENT TIMING	REFERENCE
0	When writing to graphic display RAM or reading from graphic display RAM	①
1	Only when writing to graphic display RAM (read modify)	②

① This is effective when subsequently writing and reading the successive address areas.

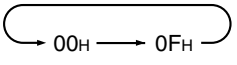
② This is effective in the case that, after reading and writing the successive address areas for every address, the read data are modified to write.

AYI	AXI	SELECTION OF INCREMENT ADDRESS	REFERENCE
0	0	Increment is not made	①
0	1	X address automatic increment	②
1	0	Y address automatic increment	③
1	1	X and Y addresses cooperative, automatic increment	④

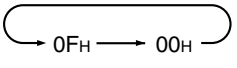
① Regardless of AIM, no increment for X and Y addresses.

② According to the setting-up of AIM, increment or decrement for only X address.
In accordance with the REF conditions of SEG normal/reverse output setting register, X address becomes as follows.

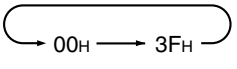
• At REF = "0" (normal output), increment by loop of



• At REF = "1" (reverse output), decrement by loop of



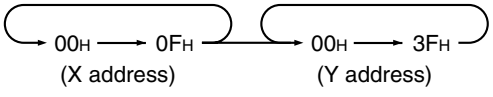
③ According to the setting-up of AIM, increment for only Y address.
Regardless of REF, increment by loop of



for Y address.

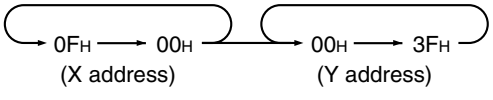
④ According to the setting-up of AIM, cooperative variation for X and Y addresses.
When the access of X address is made up to 0FH, Y address increment occurs.

• At REF = "0" (normal output)



vary in the above loops.

• At REF = "1" (reverse output)



vary in the above loops.

4.12. Power Control (1) Register Set

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	BIAS	HALT	PON	ACL

CSB	RS	WRB	RDB	RE
0	1	0	1	0

(At the time of reset : (BIAS, HALT, PON, ACL) = 0_H, read address : B_H)

(1) ACL Command

The internal circuit can be initialized. This command is enabled only at master operation mode.

ACL = "0" : Normal operation

ACL = "1" : Initialization ON

If the power control register is read out immediately after executing ACL command (ACL = 1), the D_0 bit is in the state of "1".

Therefore, if the reset operation is internally started, the D_0 bit becomes "0".

In executing ACL command, the internal reset signals are internally generated by using display master clock (oscillation by OSCI and OSCO, or clock input at CK pin).

Therefore, after executing ACL command, allow a waiting period having at least a two-cycle portion of the master clock before the next processing is made.

(2) PON Command

The internal power supply for the graphic display circuit is set ON/OFF.

PON = "0" : Power supply for the graphic display circuit OFF

PON = "1" : Power supply for the graphic display circuit ON

At PON = "1", the booster circuit and voltage converter for the graphic display circuit function.

In accordance with the setting conditions of PMODE pin, the operation circuit part changes. See **Table in Section 2.17.** for details.

(3)HALT Command

The conditions of power-saving are set ON/OFF by this command.

HALT = "0" : Normal operation

HALT = "1" : Power-saving operation

When setting in the power-saving state, the supply current can be reduced to a value near to that of the standby current.

The internal conditions at power-saving are as follows.

(a) The oscillation circuit and power supply circuit are stopped.

(b) The LCD drive is stopped, and outputs of the segment driver and common driver are V_{SS} level.

(c) The clock input from CK pin is inhibited.

(d) The contents of the display RAM data are maintained.

(e) The operation mode maintains the command execution state before executing power-saving command.

(4) BIAS Command

The internal bias value for the graphic display can be set by this command.

BIAS = "0" : 1/9 bias

BIAS = "1" : 1/7 bias

(Bias value for the segment display is 1/3 fixed.)

4.13. Power Control (2) Register Set

Electronic volume for the graphic display.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	MSB ·····			LSB

CSB	RS	WRB	RDB	RE
0	1	0	1	0

(At the time of reset : (DVOL) = 0_H, read address : D_H)

The LCD drive voltage V_0 output from the internal power supply circuit can be controlled and the display tone on the LCD can be also controlled.
The LCD drive V_0 takes one out of 16 voltage values by setting a 4-bit data register.
If the electronic volume is not used, specify (1, 1, 1, 1) in the 4-bit data register. After the LH155BA is reset, the 4-bit data register is automatically set to (1, 1, 1, 1).

MSB ·····			**LSB**	**V_0**
0	0	0	0	Smaller
		|		|
1	1	1	1	Larger

4.14. Power Control (3) Register Set

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	0	SEGPON	*	EXA	ICON

CSB	RS	WRB	RDB	RE
0	1	0	1	0

* mark means "Don't care".

(At the time of reset : (SEGPON, EXA, ICON) = 0_H, read address : E_H)

(1) ICON Command
Icon display ON/OFF.
ICON = "0" : ICON is OFF.
ICON = "1" : ICON is ON.
See **Section 2.4.3. "ICON DISPLAY MODE"** for details.

(2) EXA Command
Clock for icon display external/internal.
EXA = "0" : Internal clock
EXA = "1" : External clock from EXA pin

(3) SEGPON Command
A power supply for the segment display is set ON/OFF.
SEGPON = "0" : Power supply circuit is OFF.
SEGPON = "1" : Power supply circuit is ON.
SEGPON command is not available now.
Set SEGPON = "0".

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	0	DU1	DU0	BS1	BS0

CSB	RS	WRB	RDB	RE
0	1	0	1	1

(At the time of reset : (DU1, DU0, BS1, BS0) = 0H, read address : EH)

(1) BS Command

Command for bias setting.

Select boost voltage level below.

BS1	BS0	BOOSTED VOLTAGE LEVEL
0	0	4 times
0	1	3 times
1	0	2 times
1	1	Prohibition

Do not set BS1 = "1", BS0 = "0".

(2) DUTY Command

Command for duty setting.

Select duty ratio below.

DU1	DU0	DUTY RATIO
0	0	1/64
0	1	1/48
1	0	1/32
1	1	1/16

4.15. RE Register Set

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	1	*	*	*	RE

CSB	RS	WRB	RDB	RE
0	1	0	1	0/1

* mark means "Don't care".

(At the time of reset : (RE) = 0H, read address : FH)

RE Command

RE = "0" : The power supply selection for the segment display, duty ratio selection and boosted voltage level selection cannot be accessed.

RE = "1" : The extended function is set. The power supply selection for the segment display, duty ratio selection and boosted voltage level selection can be accessed.

4.16. Address Set for Internal Register Read

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	RA3	RA2	RA1	RA0

CSB	RS	WRB	RDB	RE
0	1	0	1	0

(At the time of reset : (RA3, RA2, RA1, RA0) = CH)

When data set up in the internal registers are read out, set the read address allotted to each register by this command before executing the read command of the internal registers.

For example, when the data of the command register in the display control (1) are read out, set the values of (RA3, RA2, RA1, and RA0) = 8H.

Refer to the functional description of each command or the list of commands for the read address allotted to each command register.

4.17. Internal Register Read

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
*	*	*	*	Internal Register Read Data			

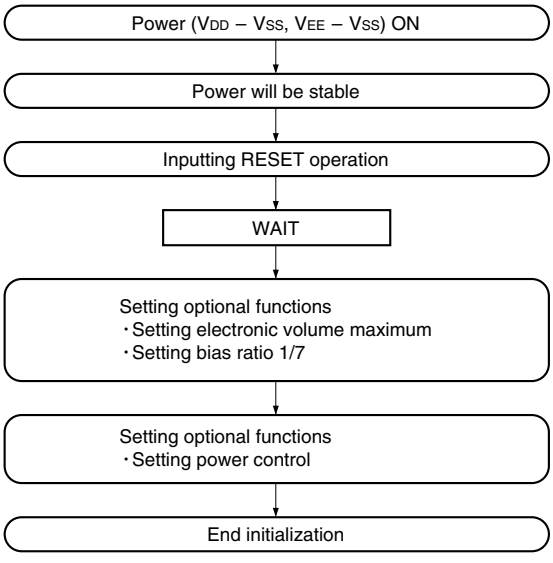
CSB	RS	WRB	RDB	RE
0	1	1	0	0

* mark means "Don't care".

Command for reading out the data of the internal registers. When this command is executed, the read address in the internal registers to be read must be preset.

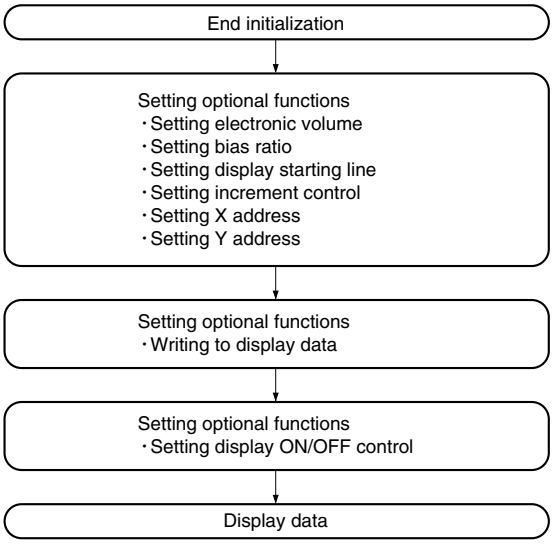
4.18. Example of Setting Commands

(1) Initialization

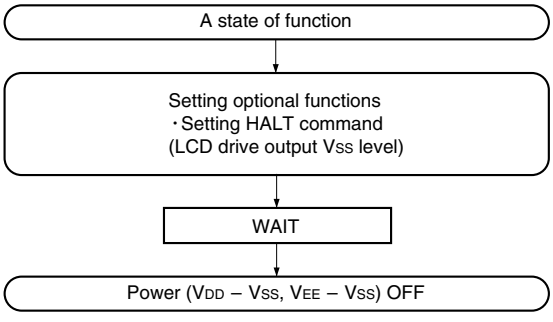


If V_{DD} and V_{EE} voltages are not same, connect the logic system power supply (V_{DD}) first.

(2) Display Data



(3) Power OFF



If V_{DD} and V_{EE} voltages are not same, disconnect the booster circuit power supply (V_{EE}) first. After V_{EE}, V_{OUT}, V_0, V_1, V_2, V_3 and V_4 voltages are below LCD ON voltage (threshold voltage for liquid crystal turns on), disconnect the logic system power supply (V_{DD}).

5. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	−0.3 to +6.0	V	1, 2
Supply voltage (2)	V_{EE}	V_{EE}	−0.3 to +6.0	V	
Supply voltage (3)	V_{OUT}	V_{OUT}	−0.3 to +15.0	V	
Supply voltage (4)	V_R	V_R	−0.3 to +15.0	V	
Supply voltage (5)	V_0	V_0	−0.3 to +15.0	V	
Supply voltage (6)	V_1, V_2, V_3, V_4	V_1, V_2, V_3, V_4	−0.3 to V_0 + 0.3	V	
Input voltage	V_I	D_7-D_0, CSB, RS, M/S, M86, RDB, WRB, CK, CKS, OSCI, LP, FLM, M, SDA, SCL, P/S, RESB, EXA, PMODE, TEST	−0.3 to V_{DD} + 0.3	V	
Storage temperature	T_{STG}		−45 to +125	°C	

NOTES :

1. T_A = +25 °C
2. The maximum applicable voltage on any pin with respect to V_{SS} (0 V).

6. RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{DD}	V_{DD}	+1.8		+5.5	V	1
	V_{EE}	V_{EE}	+2.4		+5.5	V	2
Operating voltage	V_0	V_0	+4.0		+14.0	V	3
	V_{OUT}	V_{OUT}			+14.0	V	
	V_{R1}, V_{R2}	V_{R1}, V_{R2}	+4.0		+14.0	V	4
Operating temperature	T_{OPR}		−30		+85	°C	

NOTES :

1. The applicable voltage on any pin with respect to V_{SS} (0 V).
2. When using the booster circuit, power supply, V_{EE} at the primary circuit must be used within the above-described range. If the drive voltage of LCD panel can be boosted by utilizing the voltage level of V_{DD}, usually connect this pin to V_{DD} power supply.
3. Ensure that voltages are set such that $V_{SS} < V_4 < V_3 < V_2 < V_1 < V_0$.
4. The operating range is adjusted by the external circuit constructed between V_{OUT} and V_{R1}, V_{R2}. The electric potential relation between the V_{R1}, V_{R2} and V_{OUT} pins must be $V_{R2} \leq V_{R1} \leq V_{OUT}$.

7. ELECTRICAL CHARACTERISTICS

7.1. DC Characteristics

(Unless otherwise specified, V_{SS} = 0 V, V_{DD} = +1.8 to +5.5 V, T_{OPR} = −30 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS		APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}			D_7-D_0, CSB, RS, M/S, M86, RDB, WRB, CK, CKS, OSCI, LP, FLM, M, SDA, SCL, P/S, RESB, EXA, PMODE	0		0.2V_{DD}	V	
Input "High" voltage	V_{IH}				0.8V_{DD}		V_{DD}	V	
Output "Low" voltage	V_{OL}	I_{OL} = 0.4 mA		D_7-D_0, LP, FLM, M			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = −0.4 mA			V_{DD} − 0.4			V	
Input leakage current	I_{LI}	V_I = V_{SS} or V_{DD}		CSB, RS, M/S, M86, RDB, WRB, CK, CKS, OSCI, SDA, SCL, P/S, RESB, EXA, PMODE	−10		10	µA	
Output leakage current	I_{LO}	V_I = V_{SS} or V_{DD}		D_7-D_0, LP, FLM, M	−10		10	µA	1
LCD drive output ON resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$ = 0.5 V	V_0 = 10 V	SEG_0-SEG_{127}, COM_0-COM_{63}			4	kΩ	2
			V_0 = 6 V				6		
Standby current	I_{STB}	CK = 0 V, CSB = V_{DD}	V_{DD} = 5 V	V_{DD}			20	µA	3
			V_{DD} = 3 V				10		
			V_{DD} = 2 V				5		
Supply current (1)	I_{DD1}	During sleep mode	V_{DD} = 5 V	V_{DD}			20	µA	4
			V_{DD} = 3 V				10		
			V_{DD} = 2 V				5		
Supply current (2)	I_{DD2}	During hold mode	V_{DD} = 5 V	V_{DD}, V_{EE}			240	µA	5
			V_{DD} = 3 V				120		
			V_{DD} = 2 V				80		
Supply current (3)	I_{DD3}	During active mode f_{CYC} = 100 kHz	V_{DD} = 5 V	V_{DD}			1 200	µA	6
			V_{DD} = 3 V				400		
			V_{DD} = 2 V				200		
Oscillation frequency	f_{OSC}	R_F = 680 kΩ±2%	V_{DD} = 5 V	OSCO		30		kHz	7
			V_{DD} = 3 V			28			
			V_{DD} = 2 V			24			
Reset ("L") pulse width	t_{RW}			RESB	10			µs	

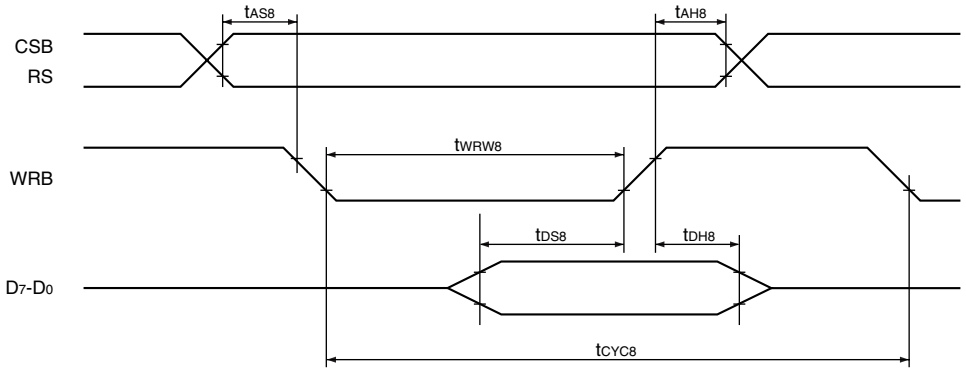
NOTES :

1. Applied when D_7 to D_0, LP, FLM, and M are in the high impedance state.
2. Resistance when 0.5 V is applied between each output pin and each power supply (V_0, V_1, V_2, V_3, V_4). Applied when power is supplied at power bias ratio of 1/9 in the external power supply mode.
3. Current at the V_{DD} pin when the master clock stops, the chip is not selected (CSB = V_{DD}), and no load is used. All circuits stop.
4. Sleep mode supply current.
   Stop internal oscillation clock, using external EXA signal. Without using booster circuits. Graphic and segment displays OFF. Icon display ON. No load.
5. Applied when no access is made by the MPU when the internal oscillation circuit (R_F = 680 kΩ) and power supply circuit (PMODE = "L") are used. The electronic volume is preset (the code is "1 1 1 1"). The display is OFF and the LCD drive pin is not loaded.
   Measuring conditions : V_{DD} = V_{EE}, V_{R1} = V_{R2}, C_1 = C_2 = 1 µF, R_1 + R_2 + R_3 = 4 MΩ.
6. Active mode supply current.
   Using internal oscillation clock.
   Writing at f_{CYC} the graphic display data which are reversed every one bit. No load.
7. Oscillation frequency when connecting a feedback resistor (R_F) of 680 kΩ between OSCI and OSCO.

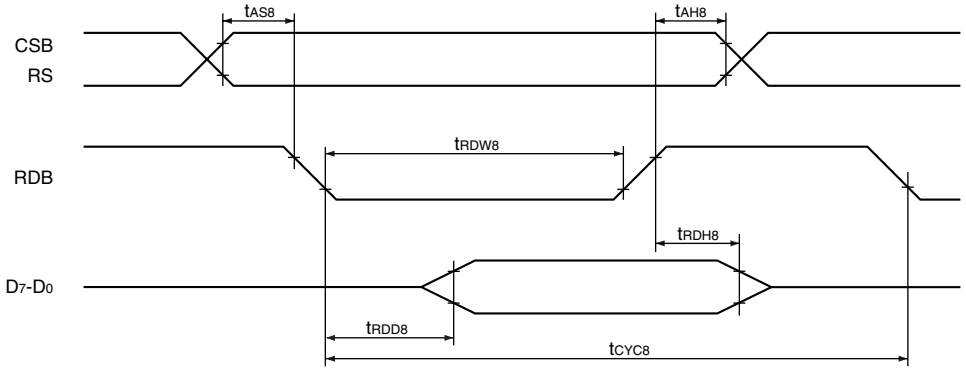
7.2. AC Characteristics

7.2.1. SYSTEM BUS READ/WRITE TIMING (80-FAMILY MPU)

(Write Timing)



(Read Timing)



(80-family MPU Timing Characteristics) (V_{DD} = 2.7 to 5.5 V, T_{OPR} = –30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t_{AH8}		CSB	60		ns
Address setup time	t_{AS8}		RS	40		ns
System cycle time	t_{CYC8}		RDB	450		ns
Read pulse width (READ)	t_{RDW8}		WRB	270		ns
Write pulse width (WRITE)	t_{WRW8}			100		ns
Data setup time	t_{DS8}		D_7-D_0	100		ns
Data hold time	t_{DH8}			40		ns
Read data output delay time	t_{RDD8}	C_L = 15 pF	D_7-D_0		220	ns
Read data hold time	t_{RDH8}			10		ns
Input signal rise and fall time	t_R, t_F		All of above pins		15	ns

(V_{DD} = 2.4 to 2.7 V, T_{OPR} = –30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t_{AH8}		CSB	80		ns
Address setup time	t_{AS8}		RS	80		ns
System cycle time	t_{CYC8}		RDB	900		ns
Read pulse width (READ)	t_{RDW8}		WRB	500		ns
Write pulse width (WRITE)	t_{WRW8}			200		ns
Data setup time	t_{DS8}		D_7-D_0	200		ns
Data hold time	t_{DH8}			80		ns
Read data output delay time	t_{RDD8}	C_L = 15 pF	D_7-D_0		320	ns
Read data hold time	t_{RDH8}			10		ns
Input signal rise and fall time	t_R, t_F		All of above pins		30	ns

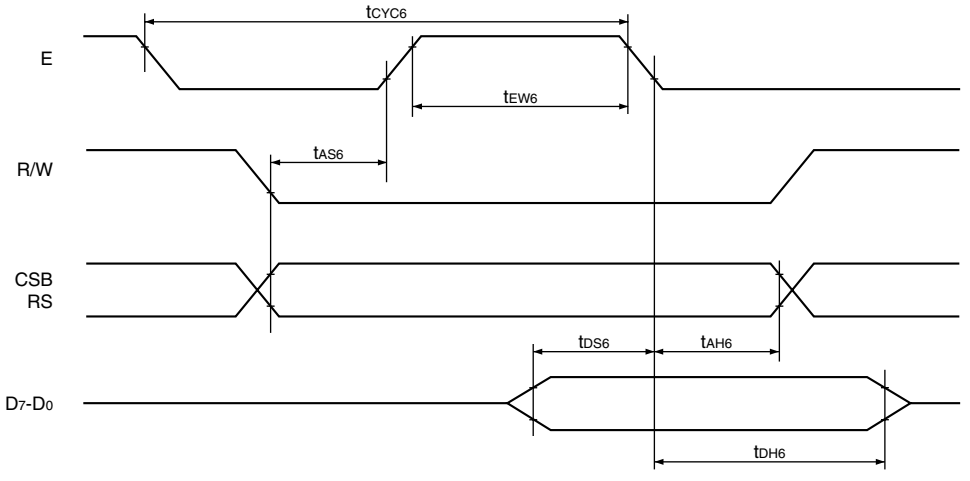
(V_{DD} = 1.8 to 2.4 V, T_{OPR} = –30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t_{AH8}		CSB	160		ns
Address setup time	t_{AS8}		RS	160		ns
System cycle time	t_{CYC8}		RDB	1 800		ns
Read pulse width (READ)	t_{RDW8}		WRB	1 000		ns
Write pulse width (WRITE)	t_{WRW8}			400		ns
Data setup time	t_{DS8}		D_7-D_0	400		ns
Data hold time	t_{DH8}			160		ns
Read data output delay time	t_{RDD8}	C_L = 15 pF	D_7-D_0		640	ns
Read data hold time	t_{RDH8}			10		ns
Input signal rise and fall time	t_R, t_F		All of above pins		30	ns

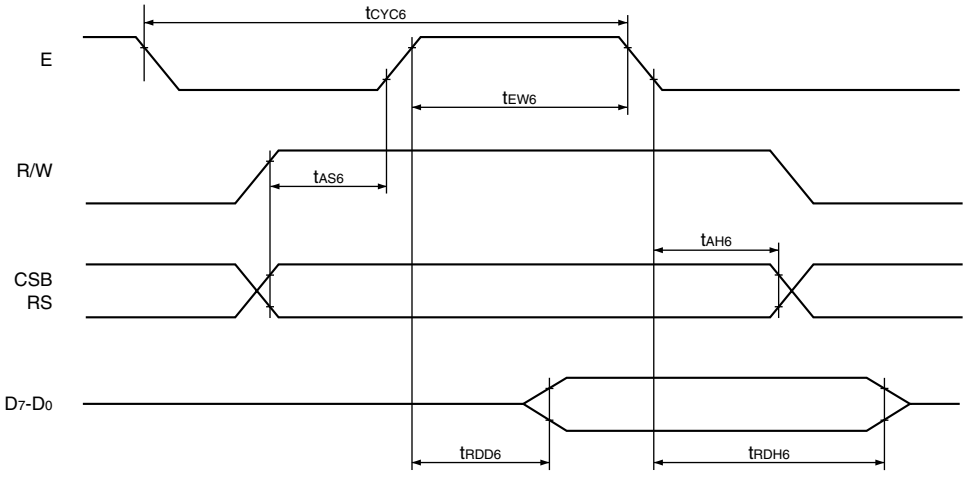
NOTE : All the timings must be specified relative to 20% and 80% of V_{DD} voltage.

7.2.2. SYSTEM BUS READ/WRITE TIMING (68-FAMILY MPU)

(Write Timing)



(Read Timing)



(68-family MPU Timing Characteristics) (V_{DD} = 2.7 to 5.5 V, T_{OPR} = –30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t_{AH6}		CSB	60		ns
Address setup time	t_{AS6}		RS	40		ns
System cycle time	t_{CYC6}		E	450		ns
Enable pulse width (READ)	t_{EW6}			270		ns
Enable pulse width (WRITE)				100		ns
Data setup time	t_{DS6}		D_7-D_0	100		ns
Data hold time	t_{DH6}			40		ns
Read data output delay time	t_{RDD6}	C_L = 15 pF	D_7-D_0		220	ns
Read data hold time	t_{RDH6}			10		ns
Input signal rise and fall time	t_R, t_F		All of above pins		15	ns

(V_{DD} = 2.4 to 2.7 V, T_{OPR} = –30 to +85 ˚C)

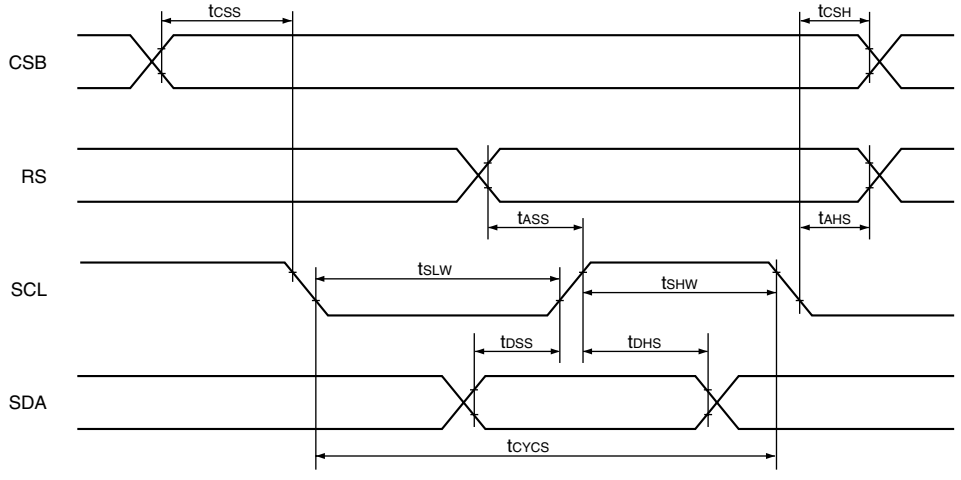
PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t_{AH6}		CSB	80		ns
Address setup time	t_{AS6}		RS	80		ns
System cycle time	t_{CYC6}		E	900		ns
Enable pulse width (READ)	t_{EW6}			500		ns
Enable pulse width (WRITE)				200		ns
Data setup time	t_{DS6}		D_7-D_0	200		ns
Data hold time	t_{DH6}			80		ns
Read data output delay time	t_{RDD6}	C_L = 15 pF	D_7-D_0		320	ns
Read data hold time	t_{RDH6}			10		ns
Input signal rise and fall time	t_R, t_F		All of above pins		30	ns

(V_{DD} = 1.8 to 2.4 V, T_{OPR} = –30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t_{AH6}		CSB	160		ns
Address setup time	t_{AS6}		RS	160		ns
System cycle time	t_{CYC6}		E	1 800		ns
Enable pulse width (READ)	t_{EW6}			1 000		ns
Enable pulse width (WRITE)				400		ns
Data setup time	t_{DS6}		D_7-D_0	400		ns
Data hold time	t_{DH6}			160		ns
Read data output delay time	t_{RDD6}	C_L = 15 pF	D_7-D_0		640	ns
Read data hold time	t_{RDH6}			10		ns
Input signal rise and fall time	t_R, t_F		All of above pins		30	ns

NOTE : All the timings must be specified relative to 20% and 80% of V_{DD} voltage.

7.2.3. SERIAL INTERFACE TIMING



(V_{DD} = 2.4 to 5.5 V, T_{OPR} = −30 to +85 ˚C)

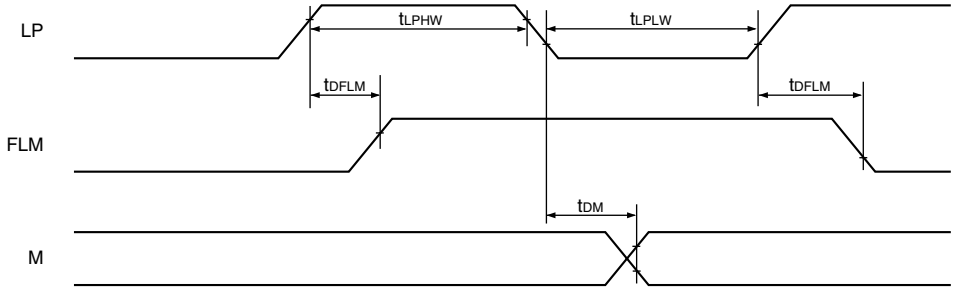
PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Serial clock period	t_{CYCS}		SCL	1 000		ns
SCL "H" pulse width	t_{SHW}			400		ns
SCL "L" pulse width	t_{SLW}			400		ns
Address setup time	t_{ASS}		RS	80		ns
Address hold time	t_{AHS}			80		ns
Data set up time	t_{DSS}		SDA	400		ns
Data hold time	t_{DHS}			400		ns
CSB to SCL time	t_{CSS}		CSB	80		ns
CSB hold time	t_{CSH}			80		ns
Input signal rise and fall time	t_R, t_F		All of above pins		30	ns

(V_{DD} = 1.8 to 2.4 V, T_{OPR} = −30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Serial clock period	t_{CYCS}		SCL	2 000		ns
SCL "H" pulse width	t_{SHW}			800		ns
SCL "L" pulse width	t_{SLW}			800		ns
Address setup time	t_{ASS}		RS	160		ns
Address hold time	t_{AHS}			160		ns
Data set up time	t_{DSS}		SDA	800		ns
Data hold time	t_{DHS}			800		ns
CSB to SCL time	t_{CSS}		CSB	160		ns
CSB hold time	t_{CSH}			160		ns
Input signal rise and fall time	t_R, t_F		All of above pins		30	ns

NOTE : All the timings must be specified relative to 20% and 80% of V_{DD} voltage.

7.2.4. DISPLAY CONTROL TIMING



Input Timing Characteristics (Slave Mode) (V_{DD} = 2.4 to 5.5 V, T_{OPR} = –30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
LP "H" pulse width	t_{LPHW}		LP	80		µs
LP "L" pulse width	t_{LPLW}			80		µs
FLM delay time	t_{DFLM}		FLM	–1.0	1.0	µs
M delay time	t_{DM}		M	–1.0	1.0	µs
Input signal rise and fall time	t_R, t_F		All of above pins		15	ns

(V_{DD} = 1.8 to 2.4 V, T_{OPR} = –30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
LP "H" pulse width	t_{LPHW}		LP	80		µs
LP "L" pulse width	t_{LPLW}			80		µs
FLM delay time	t_{DFLM}		FLM	–1.0	1.0	µs
M delay time	t_{DM}		M	–1.0	1.0	µs
Input signal rise and fall time	t_R, t_F		All of above pins		30	ns

Output Timing Characteristics (Master Mode) (V_{DD} = 2.4 to 5.5 V, T_{OPR} = –30 to +85 ˚C)

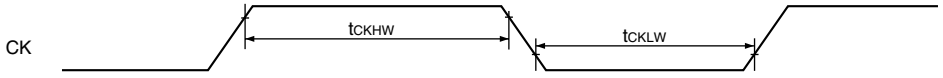
PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
FLM delay time	t_{DFLM}	C_L = 15 pF	FLM	10	1 000	ns
M delay time	t_{DM}		M	10	1 000	ns

(V_{DD} = 1.8 to 2.4 V, T_{OPR} = –30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
FLM delay time	t_{DFLM}	C_L = 15 pF	FLM	10	2 000	ns
M delay time	t_{DM}		M	10	2 000	ns

NOTE : All the timings must be specified relative to 20% and 80% of V_{DD} voltage.

7.2.5. MASTER CLOCK INPUT TIMING



(V_{DD} = 2.4 to 5.5 V, T_{OPR} = –30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PIN	MIN.	MAX.	UNIT
CK "H" pulse width	t_{CKHW}		CK	10	32	µs
CK "L" pulse width	t_{CKLW}			10	32	µs
Input signal rise and fall time	t_R, t_F				15	ns

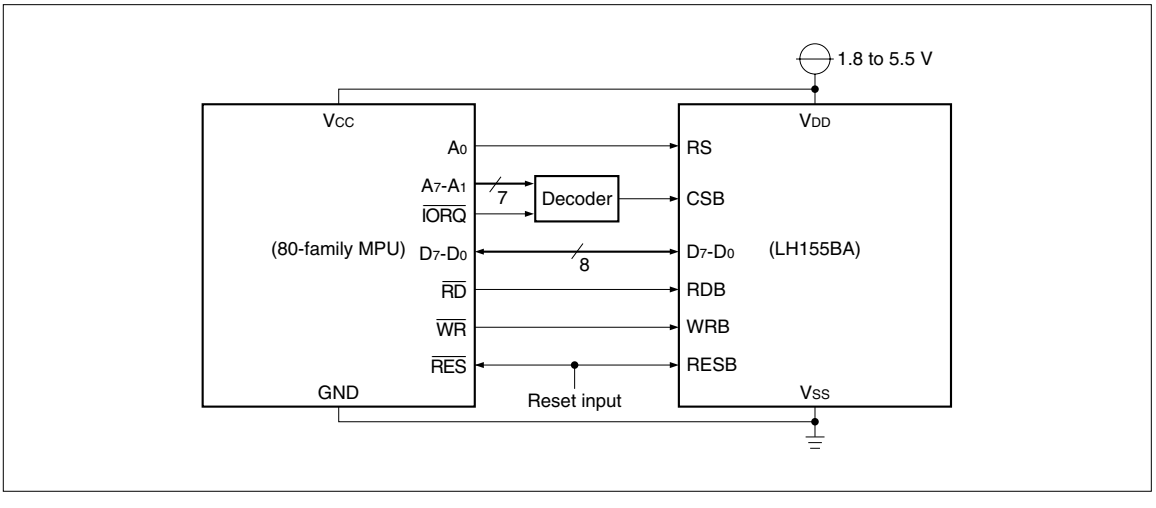
(V_{DD} = 1.8 to 2.4 V, T_{OPR} = –30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PIN	MIN.	MAX.	UNIT
CK "H" pulse width	t_{CKHW}		CK	10	32	µs
CK "L" pulse width	t_{CKLW}			10	32	µs
Input signal rise and fall time	t_R, t_F				30	ns

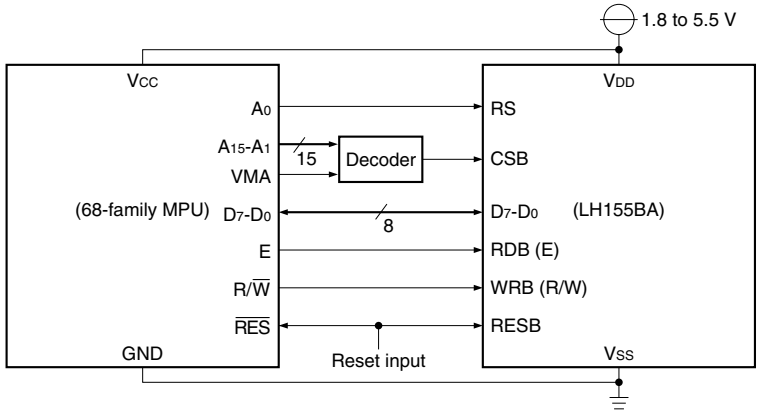
NOTE : All the timings must be specified relative to 20% and 80% of V_{DD} voltage.

8. CONNECTION EXAMPLES OF REPRESENTATIVE APPLICATIONS

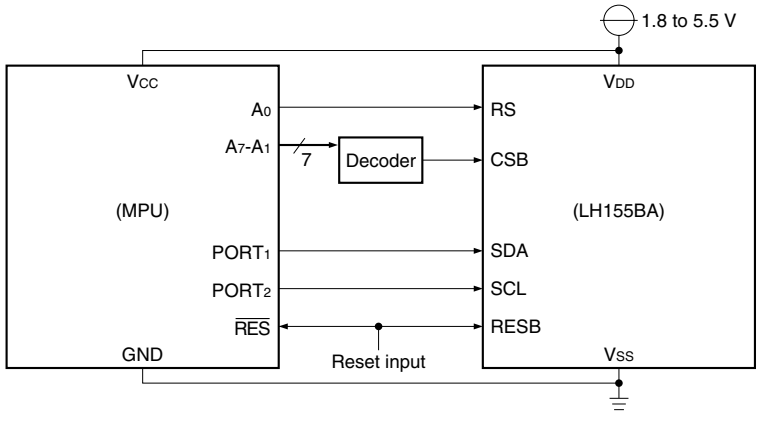
(a) Connection to The 80-family MPU



(b) Connection to The 68-family MPU



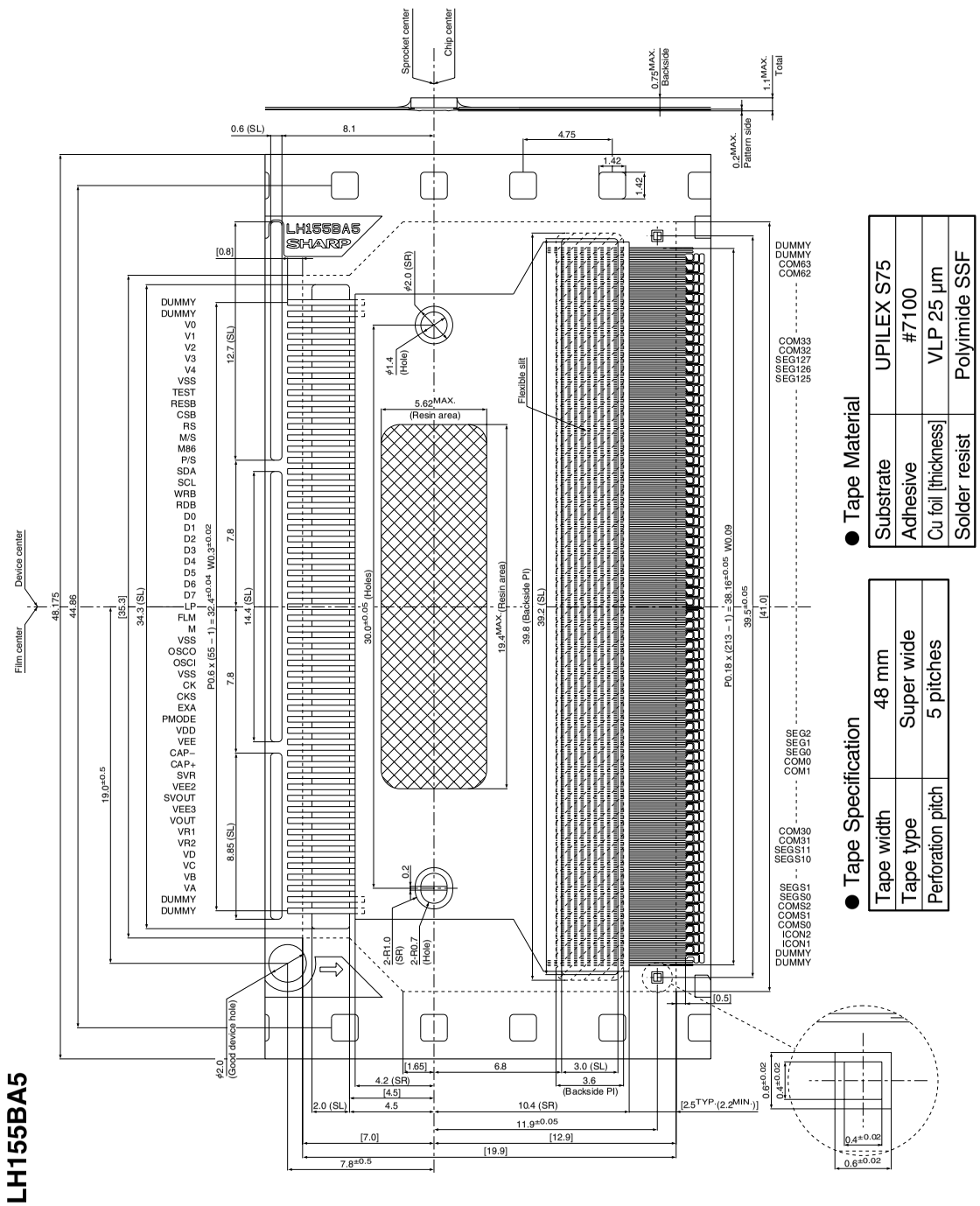
(c) Connection to The MPU with Serial Interface



* When connecting multiple LH155BAs, input to each CSB pin by varying the decoder conditions of address signals.

9. PACKAGES

(Unit : mm)



LH155BA5

● Tape Material

Substrate	UPILEX S75
Adhesive	#7100
Cu foil [thickness]	VLP 25 µm
Solder resist	Polyimide SSF

● Tape Specification

Tape width	48 mm
Tape type	Super wide
Perforation pitch	5 pitches

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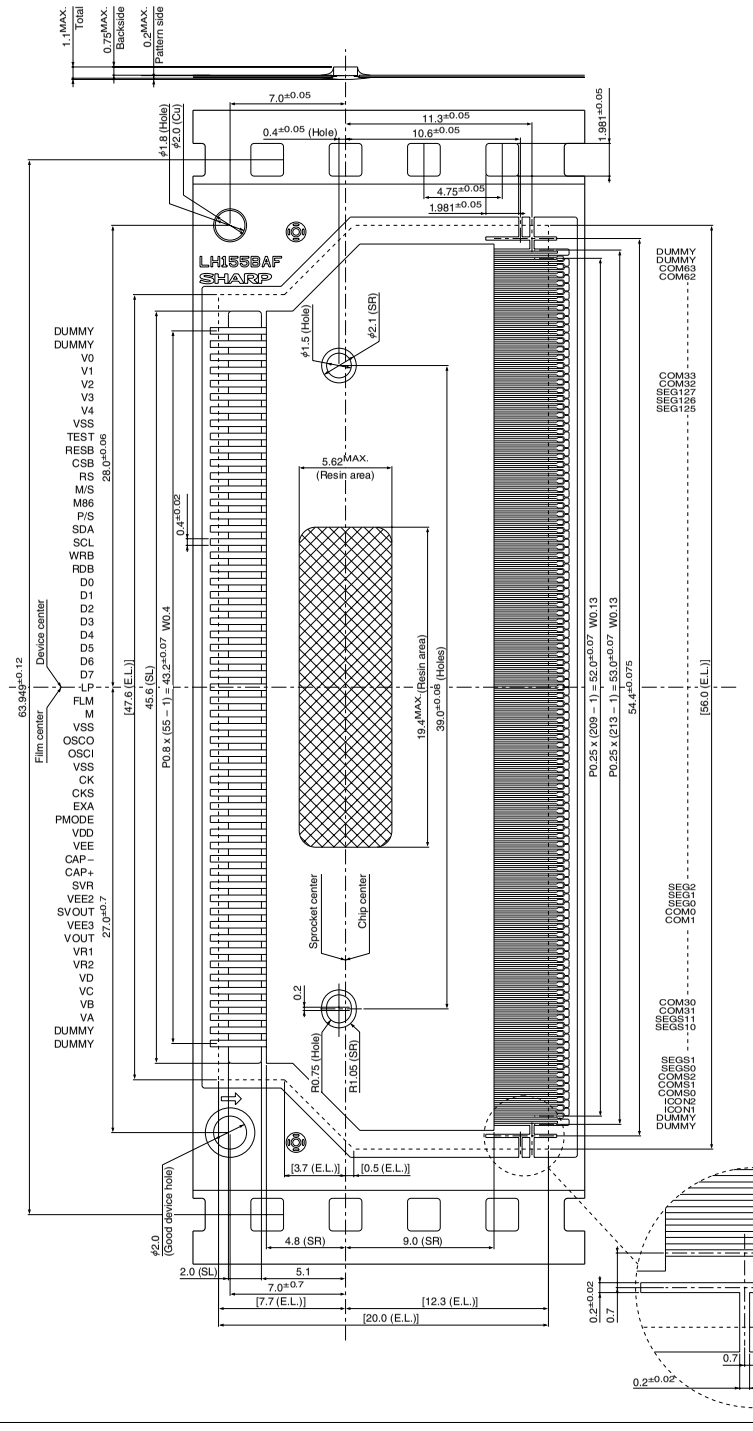
LH155BAF



● Tape Material

Substrate	UPILEX S75
Adhesive	E type
Cu foil [thickness]	VLP 25 µm
Solder resist	Epoxy resin

● Tape Specification

Tape width	70 mm
Tape type	Wide
Perforation pitch	5 pitches