Ordering number: EN 3255C

CMOS LSI

LC7985NA, LC7985ND

LCD Controller/Driver

Overview

The LC7985 series devices are low-power CMOS ICs that incorporate dot-matrix character generator, display controller and driver functions in a single device, making them ideal for use in portable equipment containing LCD displays.

The LC7985 series feature 5 × 7-pixel and 5 × 10-pixel character fonts including either eight or four user-defined characters, single-line and two-line display modes, built-in drivers for displays up to eight characters in size, and easy expansion to control displays of up to 80 characters by adding LC7930N display drivers.

The LC7985 series interface directly to both 4-bit and 8-bit microcontrollers. The instruction set includes display clear, cursor home, display ON/OFF, character blink, and cursor and display shift instructions. The built-in reset circuit automatically initializes the devices at power-ON.

The LC7985 series operate from a 5V supply and are available in 80-pin QIPs.

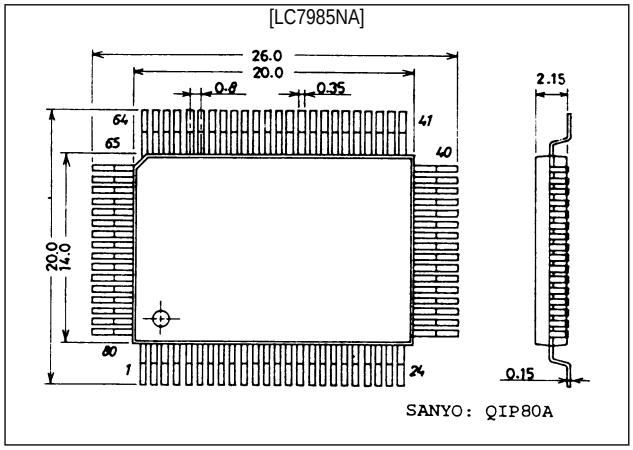
Features

- Controller and driver for dot-matrix LCD displays
- 5 × 7-pixel and 5 × 10-pixel character fonts
- 160, 5 × 7-pixel characters and 32, 5 × 10-pixel characters in character generator ROM
- Eight, 5 × 7-pixel characters or four, 5 × 10-pixel characters in character generator RAM
- 80-character display data RAM
- Built-in drivers for 1-line × 8-character and 2-line × 8-character displays
- Easy expansion to 1-line × 80-character or 2-line × 40-character displays
- 4-bit or 8-bit microcontroller interface
- 11 microcontroller instructions
- Built-in reset circuit
- Built-in oscillator
- 5V supply
- 80-pin QIP

Package Dimensions

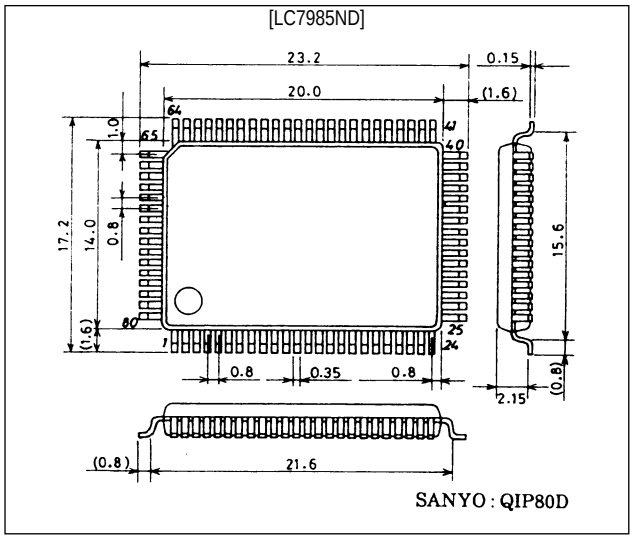
unit: mm

3044B - QFP80A

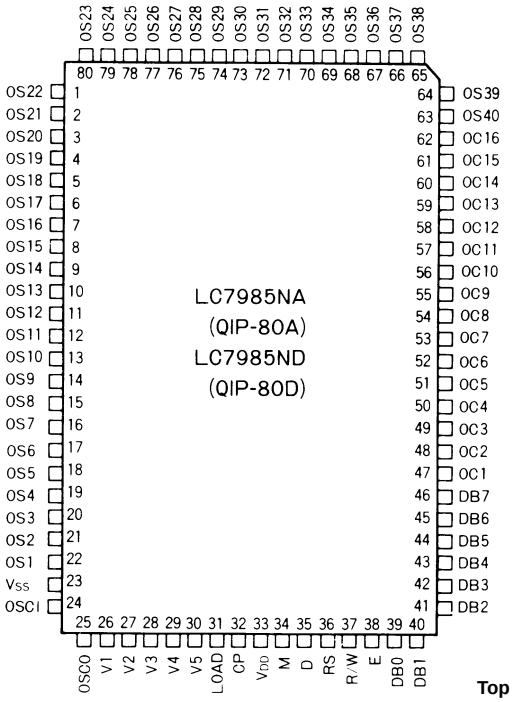


unit: mm

3177 - QFP80D

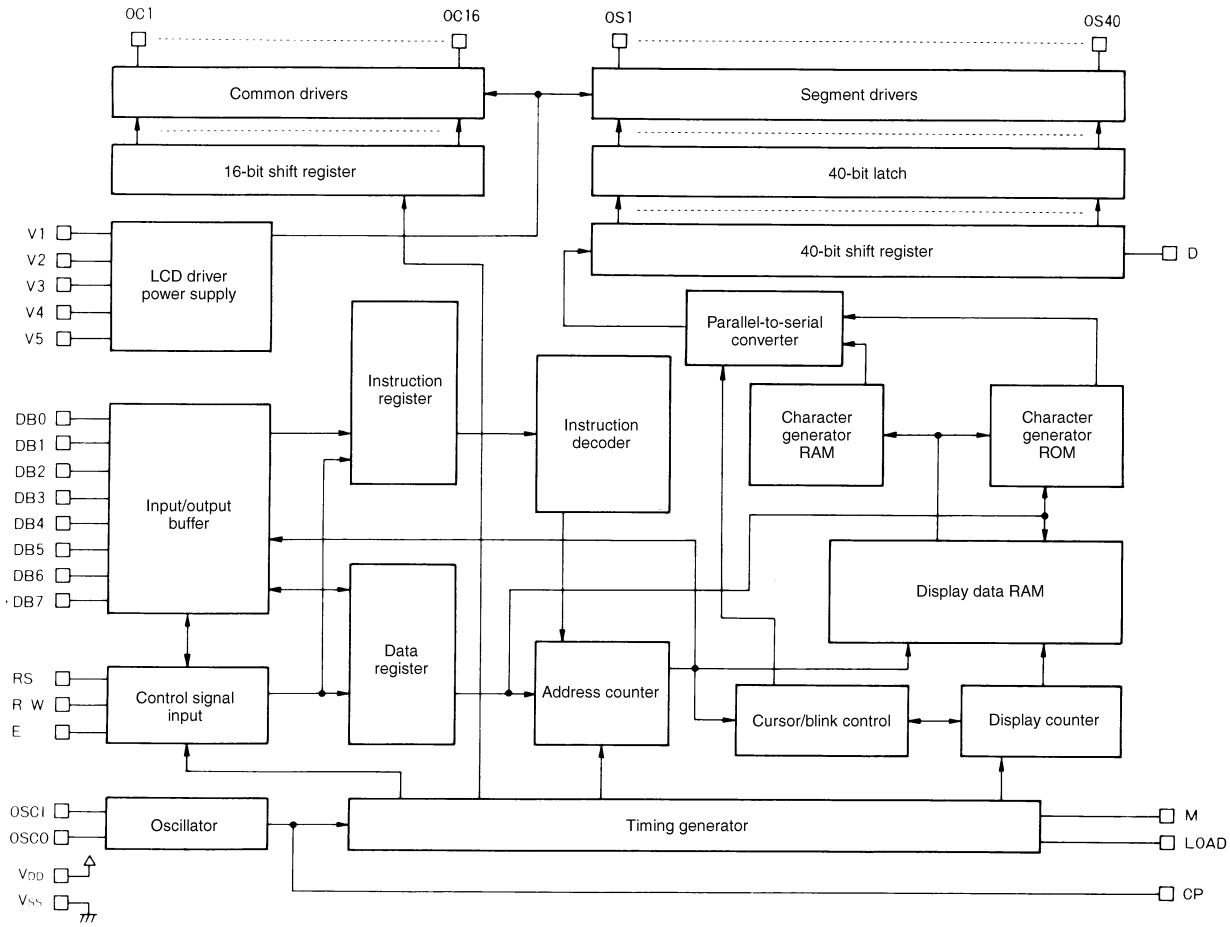


Pin Assignment



Top view

Block Diagram



Specifications

Absolute Maximum Ratings at Ta = 25 ± 2°C, V_{SS} = 0V

Parameter	Symbol	Ratings	Unit
Supply voltage range	V_{DD}	–0.3 to +7.0	V
LCD drive supply voltage range*1	V_1 to V_5	V_{DD} – 13.5 to V_{DD} + 0.3	V
Input voltage range	V_I	–0.3 to V_{DD} + 0.3	V
Operating temperature range	Topr	–20 to +75	°C
Storage temperature range	Tstg	–55 to +125	°C

Note: *1. V_{DD} must obey the relationship : $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$

Allowable Operating Ranges at Ta = –20 to +75°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage range	V_{DD}		4.5		5.5	V
Supply voltage*1	V_{D5}	$V_{D5} = V_{DD} - V_5$	1.5			V
	V_{D1}	$V_{D1} = V_{DD} - V_1$			V_{D5} x 0.25	V
Input high level voltage	V_{IH1}	except OSCI	2.2		V_{DD}	V
	V_{IH2}	OSCI only	V_{DD} - 1.0		V_{DD}	V
Input low level voltage	V_{IH1}	except OSCI			0.6	V
	V_{IH2}	OSCI only			1.0	V

Note: *1. These voltages guarantee correct operation of the LC7985NA and LC7985ND. They do not guarantee correct operation of the LCD panel. V_{LCD} must also be observed.

Electrical Characteristics at Ta = –20 to +75°C, V_{SS} = 0V, V_{DD} = 5V ± 10%, unless otherwise noted

Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Output high-level voltage		V_{OH1}	I_{OH} = –0.205mA Input / Output pins	2.4	–	–	V
		V_{OH2}	I_{OH} = –0.04mA Output pins	0.9V_{DD}	–	–	V
Output low-level voltage		V_{OL1}	I_{OL} = 1.2mA Input / Output pins	–	–	0.4	V
		V_{OL2}	I_{OL} = 0.04mA Output pins	–	–	0.1V_{DD}	V
Driver fall voltage*1		V_{COM}	I_d = 0.05mA All common pins	–	–	2.9	V
		V_{SEG}	I_d = 0.05mA All segment pins	–	–	3.8	V
Leakage current		I_L	$V_I = V_{SS}$ to V_{DD}	–	–	1	µA
Pull-up current*2		I_P	V_{DD} = 5V	50	125	250	µA
Current drain		I_{DD1}	Ceramic resonator oscillator, V_{DD} = 5V, f_{OSC} = 250kHz, no output load	–	0.55	0.8	mA
		I_{DD2}	Feedback resistor oscillator, V_{DD} = 5V, f_{OSC} = 270kHz, no output load	–	0.35	0.6	
External clock*3	Frequency	f_{CP}		125	250	350	kHz
	Duty cycle	DUTY		45	50	55	%
	Rise time	t_R		–	–	0.2	µs
	Fall time	t_F		–	–	0.2	µs

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Internal oscillator frequency	f_{OSC1}	Ceramic filter oscillator	245	250	255	kHz
	f_{OSC2}	Feedback resistor oscillator, R_f = 91kΩ ±3%	190	270	350	
LCD display voltage	V_{LCD1}	1/5 bias, $V_{LCD} = V_{DD} - V_5$	4.6	–	11	V
	V_{LCD2}	1/4 bias, $V_{LCD} = V_{DD} - V_5$	3.0	–	11	

Note: *1. V_{COM} is the voltage from VDD, V1, V4 and V5 to the LCD common drive pins OC1 to OC16.
V_{SEG} is the voltage from VDD, V2, V3 and V5 to the LCD segment drive pins OC1 to OC40.
Note: *2. Applied pins are RS, R/W, and DB0 to DB7.
Note: *3. External clock

Switching Characteristics at Ta = -20 to +75°C, VDD = 5V ± 10%, VSS = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
E cycle time	t_{ECYC}		1000	–	–	ns
E high-level pulsewidth	t_{EW}		450	–	–	ns
E rise time	t_{ER}		–	–	25	ns
E fall time	t_{EF}		–	–	25	ns
RS and R/W to E setup time	t_{SU}		140	–	–	ns
E to RS and R/W address hold time	t_{AH}		10	–	–	ns
DB0 to DB7 to E data setup time	t_{DSU}		195	–	–	ns
Write cycle E to DB0 to DB7 data hold time	t_{DHW}		10	–	–	ns
Read cycle E to data valid delay time	t_{DD}	See measurement circuit.	–	–	320	ns
Read cycle E to DB0 to DB7 data hold time	t_{DHR}		20	–	–	ns
CP low-level pulsewidth	t_{WL}		800	–	–	ns
CP high-level pulsewidth	t_{WH}		800	–	–	ns
CP to LOAD setup time	t_{CSU}		500	–	–	ns
D to CP data setup time	t_{DSU}		300	–	–	ns
CP to D data hold time	t_{DH}		300	–	–	ns
LOAD to M delay time	t_{DM}		–1000	–	1000	ns

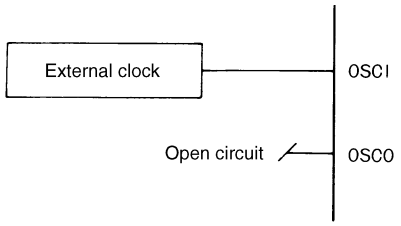
Reset characteristics at Ta = -20 to +75°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
V_{DD} rise time	t_{DDR}		0.1	–	10	µs
V_{DD} off time	t_{DDOFF}		1	–	–	ms

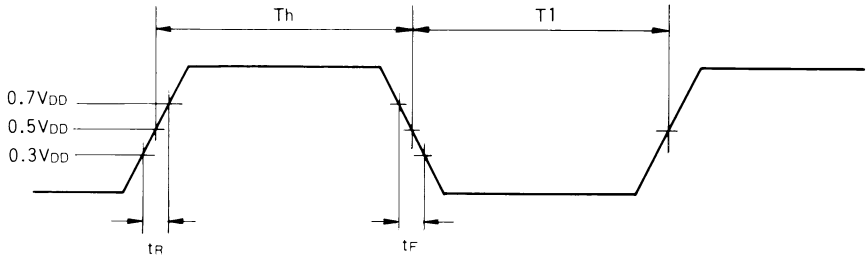
Clock Generator

The internal oscillator that generates the clock for the internal circuit requires an external filter, a feedback resistor or an external clock input as shown in the following sections.

External clock

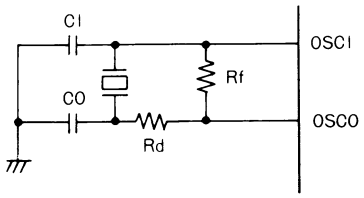


The input duty cycle should be between 45 and 55% as shown in the following figure.



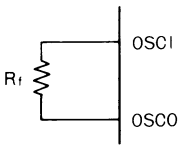
Note. $\text{Duty} = \dfrac{T_h}{T_h + T_l} \times 100\%$

Ceramic filter



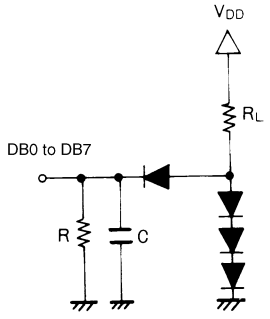
Note. Rf = 1MΩ ±10%, CI = CO = 680pF ±10%, Rd = 3.3kΩ ±5%

Feedback resistor



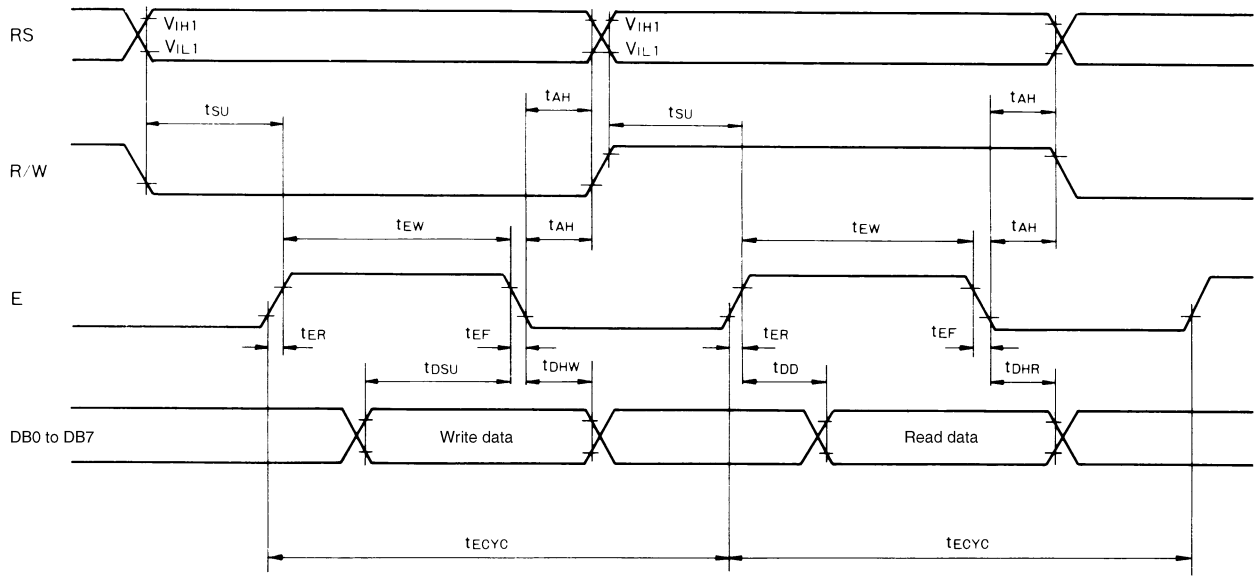
Note. The resistor should be mounted as close as possible to OSCI and OSCO.

Measurement Circuit

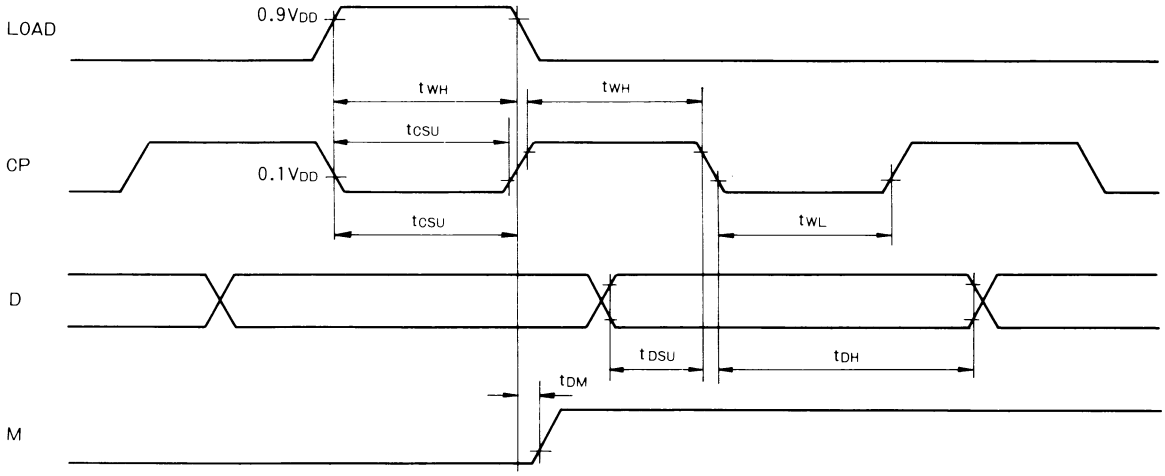


Note. R_L = 2.4kΩ, C = 130pF, R = 11kΩ

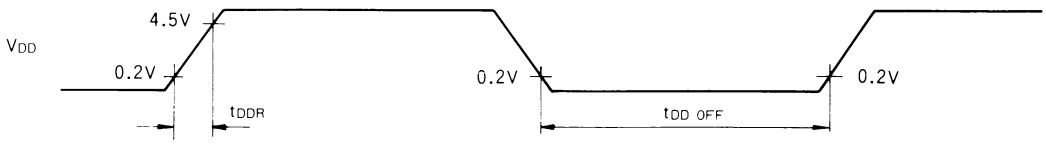
Read/write cycle timing



LC7930N interface timing



Power supply



Pin Description

Name	Num	I/O	Connect to	Functions
RS	1	I	MPU	Data register or instruction register select input. Data register when "1" and instruction register when "0".
R/W	1	I	MPU	Read or write select input "0" indicates write, "1" ; read
E	1	I	MPU	Execution start input to write or read
DB_4 to DB_7	4	I/O	MPU	4-bit microcontroller interface data bus and 8-bit microcontroller interface high-order four bits data bus connections. Three-state bidirectional. DB_7 can be used as a busyflag.
DB_0 to DB_3	4	I/O	MPU	8-bit microcontroller interface low-order four bits data bus connections. No connection when 4-bit interface size is selected. Three-state bidirectional.
LOAD	1	O	LC7930N	Clock to latch the D serial data output to LC 7930N
CP	1	O	LC7930N	Clock to shift the D serial data
M	1	O	LC7930N	Output to shift the LCD drive signal to alternating current signal
D	1	O	LC7930N	Display expansion serial data output "0" indicates unselected, "1" ; selected
OC_1 to OC_{16}	16	O	LCD	LCD common driver outputs. All common signals unused are unselected wave forms.
OS_1 to OS_{40}	40	O	LCD	LCD segment driver outputs
V_1 to V_5	5		source	Supply voltage for LCD display drive
V_{DD}, V_{SS}	2		source	V_{DD} : +5V, V_{SS} : 0V
OSCI, OSCO	2			Oscillator feedback resistor and ceramic filter connection, and external clock input

Functional Description

Registers

The LC7985 has two 8-bit registers—instruction register (IR) and data register (DR)—that are selected as shown in the following table.

RS	R/W	Operation
0	0	IR write, instruction execution
0	1	Busy flag (DB7) and address counter (DB0 to DB6) output
1	0	DR write, internal DR to DD RAM or CG RAM data transfer
1	1	DR read, internal DD RAM or CG RAM to DR data transfer

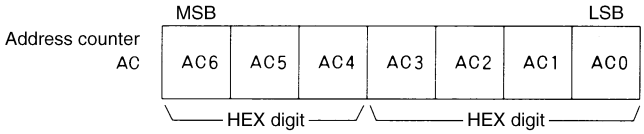
The instruction register is write-only. It contains instruction codes or DD RAM and CG RAM addresses written by the microcontroller.

Busy Flag

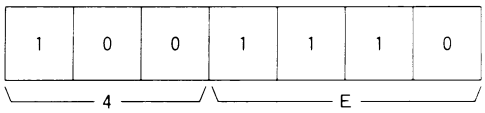
When busy flag is 1, the previous instruction is executing, and when 0, the instruction has completed. The next instruction cannot be received until BF is 0. The microcontroller should, therefore, confirm that BF is 0 before writing the next instruction.

Display Data RAM (DD RAM)

The display data RAM stores 80, 8-bit character codes, and the LC7985 can display a maximum of 80 characters. The address counter contains the location for the next display memory read or write operation as shown in the following figure.



Display data addresses are in hexadecimal. For example, the address counter contents for location 4E are shown in the following figure.



To prevent undesirable effects such as display flicker during DD RAM accesses, the internal memory and the microprocessor interface have separate timing signals.

The data register holds data read from or written to either DD RAM or CG RAM. Data written to the data register by the microcontroller is automatically transferred to the current DD RAM or CG RAM address. Data read from DD RAM or CG RAM is buffered in the data register.

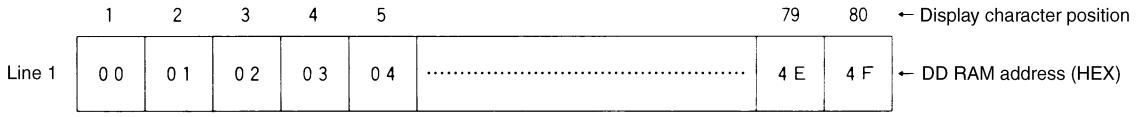
When the microcontroller writes a DD RAM or CG RAM address to the instruction register, the data at that address is copied into the data register. The microcontroller then reads the data in the data register to complete the transfer. Once that data is read, the data from the next DD RAM or CG RAM address is copied into the data register in preparation for the next data read.

Address Counter

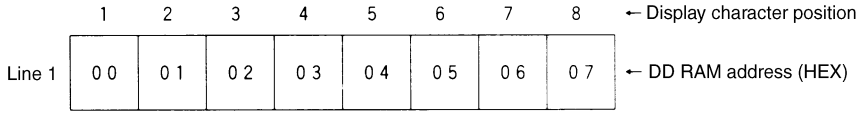
The address counter is used for both the DD RAM and the CG RAM. The address output on DB0 to DB7 is the counter value before the currently executing instruction began.

Single-line display mode (N = 0)

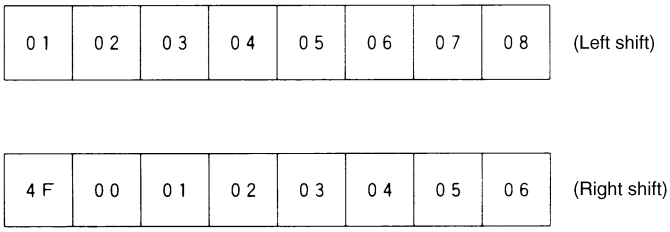
The DD RAM addresses and their corresponding display positions for an 80-character display are shown in the following figure.



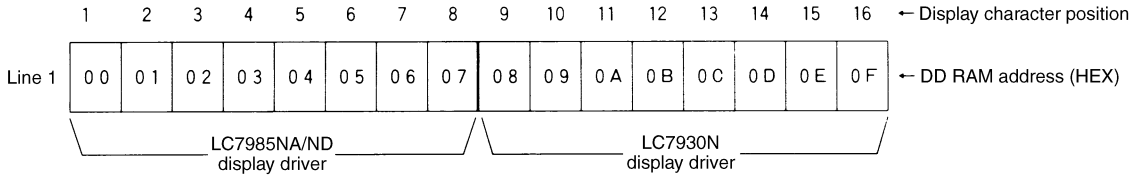
A single LC7985, however, can drive up to eight characters. The display positions and DD RAM addresses for an unshifted 8-character display are shown in the following figure.



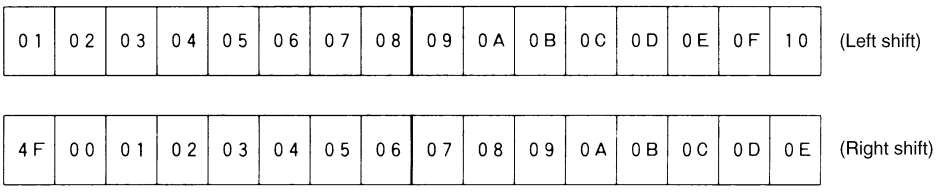
The DD RAM addresses following left and right display shifts are shown in the following figure. Note that the displayed characters wrap around from addresses $4F_H$ to 00_H.



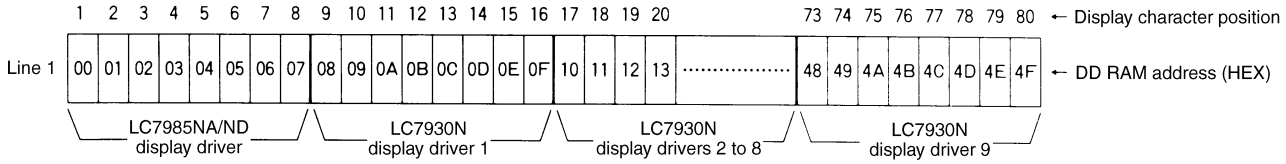
An LC7985 and a single LC7930N can drive a 16-character display. The display positions and DD RAM addresses for an unshifted display are shown in the following figure.



The DD RAM addresses following left and right display shifts are shown in the following figure.



The number of displayed characters can be increased by adding more LC7930Ns. An LC7985 and nine LC7930Ns can drive an 80-character display as shown in the following figure.



Two-line display mode (N = 1)

The DD RAM addresses and their corresponding display positions for a 2-line × 40-character display are shown in the following figure. Note that the address counter automatically increments from 27_H to 40_H.

	1	2	3	4	5	.....	39	40	← Display character position
Line 1	00	01	02	03	04	.....	26	27	← DD RAM address (HEX)
Line 2	40	41	42	43	44	.....	66	67	

A single LC7985, however, can drive up to eight characters per line. The display positions and DD RAM addresses for an unshifted, 2-line × 8-character display are shown in the following figure.

	1	2	3	4	5	6	7	8	← Display character position
Line 1	00	01	02	03	04	05	06	07	← DD RAM address (HEX)
Line 2	40	41	42	43	44	45	46	47	

The display positions following a left or right display shift are shown in the following figure. Note that the display shift is simultaneous for both lines, regardless of which line the cursor is in.

01	02	03	04	05	06	07	08	(Left shift)
41	42	43	44	45	46	47	48	

27	00	01	02	03	04	05	06	(Right shift)
67	40	41	42	43	44	45	46	

An LC7985 and a single LC7930N can drive a 2-line × 16-character display. The display positions and DD RAM addresses for an unshifted, 2-line × 16-character display are shown in the following figure.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display character position
Line 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM address (HEX)
Line 2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

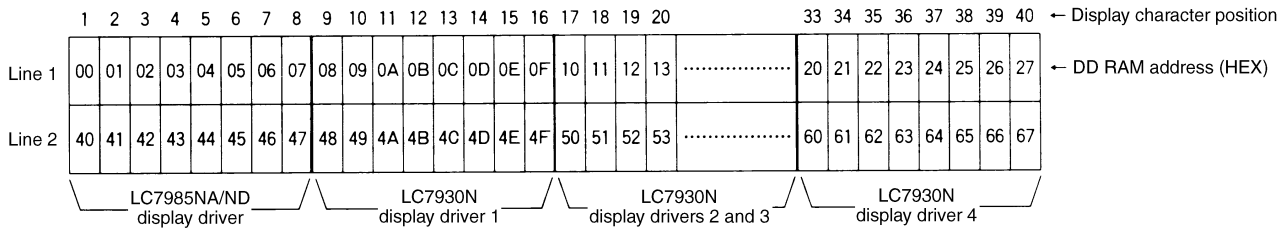
LC7985NA/ND display driver | LC7930N display driver

The DD RAM addresses following left and right display shifts are shown in the following figure.

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	(Left shift)
41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	

27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	(Right shift)
67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	

The number of displayed characters can be increased by adding more LC7930Ns. An LC7985 and four LC7930Ns can drive a 2-line × 40-character display as shown in the following figure.



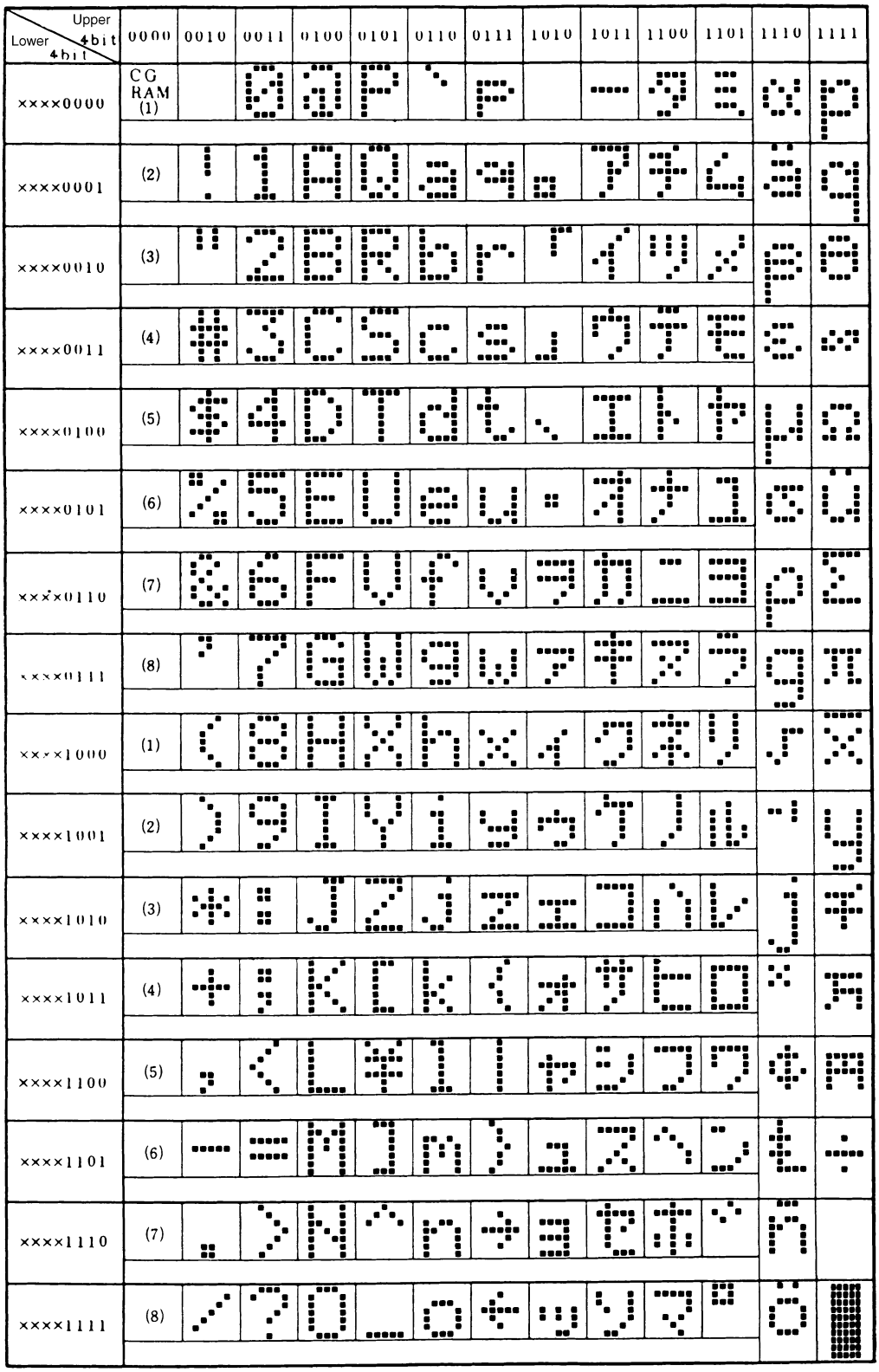
Character Generator ROM (CG ROM)

The character generator ROM contains 160, 5 × 7-pixel bitmaps and 32, 5 × 10-pixel bitmaps as shown in the following figure. The characters are selected by their 8-bit character code.

Character Generator RAM (CG RAM)

The character generator RAM stores user-defined bitmaps for either eight, 5 × 7-pixel characters or four, 5 × 10-pixel characters. To display character patterns stored in CG RAM, write the character codes, shown in the leftmost column of the following figure, on DD RAM.

Character cord and the character bitmap



5 × 7-pixel characters

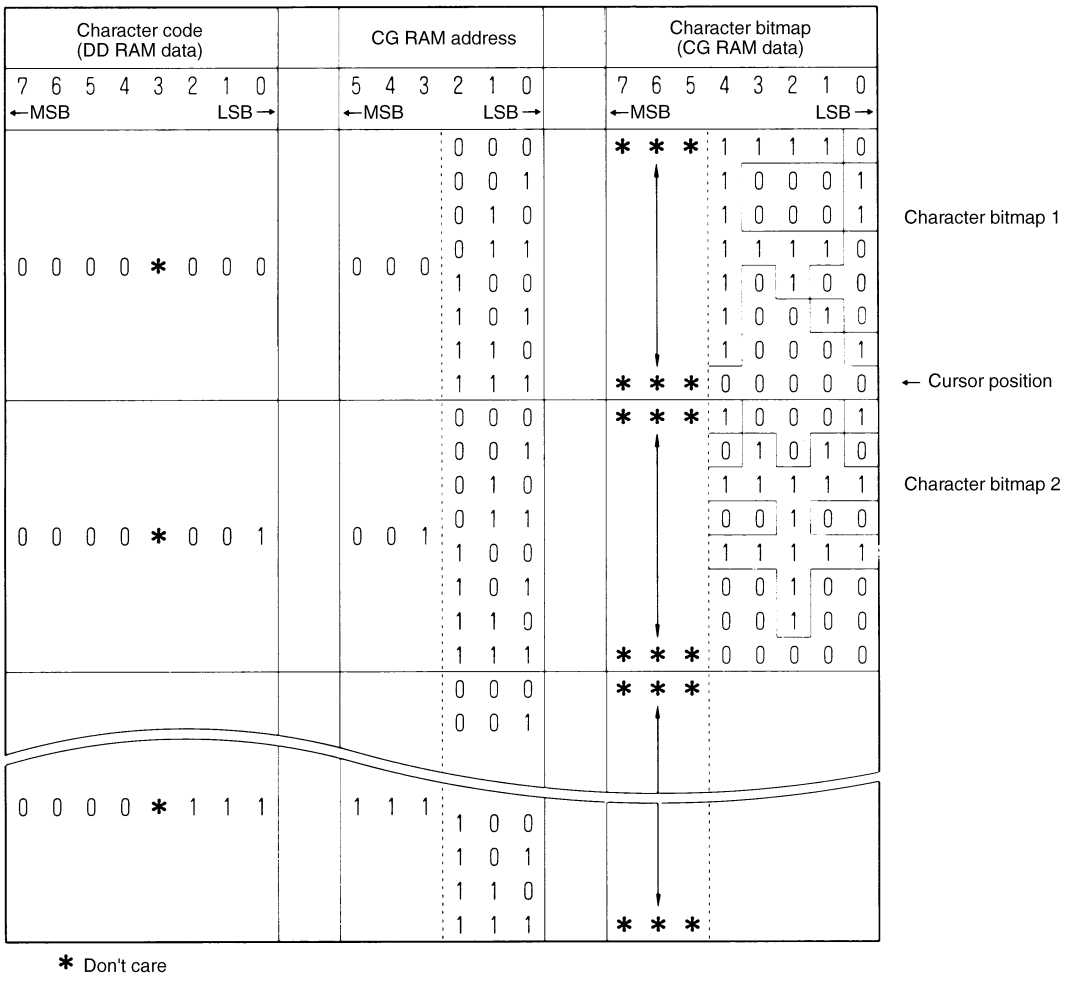
The layout and addressing for 5 × 7-pixel characters is shown in the following figure. Each character occupies eight bytes, where bits 3 to 5 of the CG RAM address correspond to bits 0 to 2 of the character code. Note that bit 3 of the character code is not significant so, for example, codes 00_H and 08_H select the same character.

Bits 0 to 2 of the CG RAM address are the bitmap row address, where row 000 is the topmost displayed row.

The cursor, when displayed, is formed by ORing the bottom row with all 1s. If the cursor is used, row 111 should contain all 0s so the cursor does not obscure the bottom row of the character.

Bits 0 to 4 of the CG RAM data contain the character bitmaps. When a bit is 1, the corresponding pixel is ON, and when 0, the pixel is OFF.

Bits 5 to 7 of the CG RAM data are present in memory, but are not used by the display circuit. These bits can be used as general-purpose RAM.



5 × 10-pixel characters

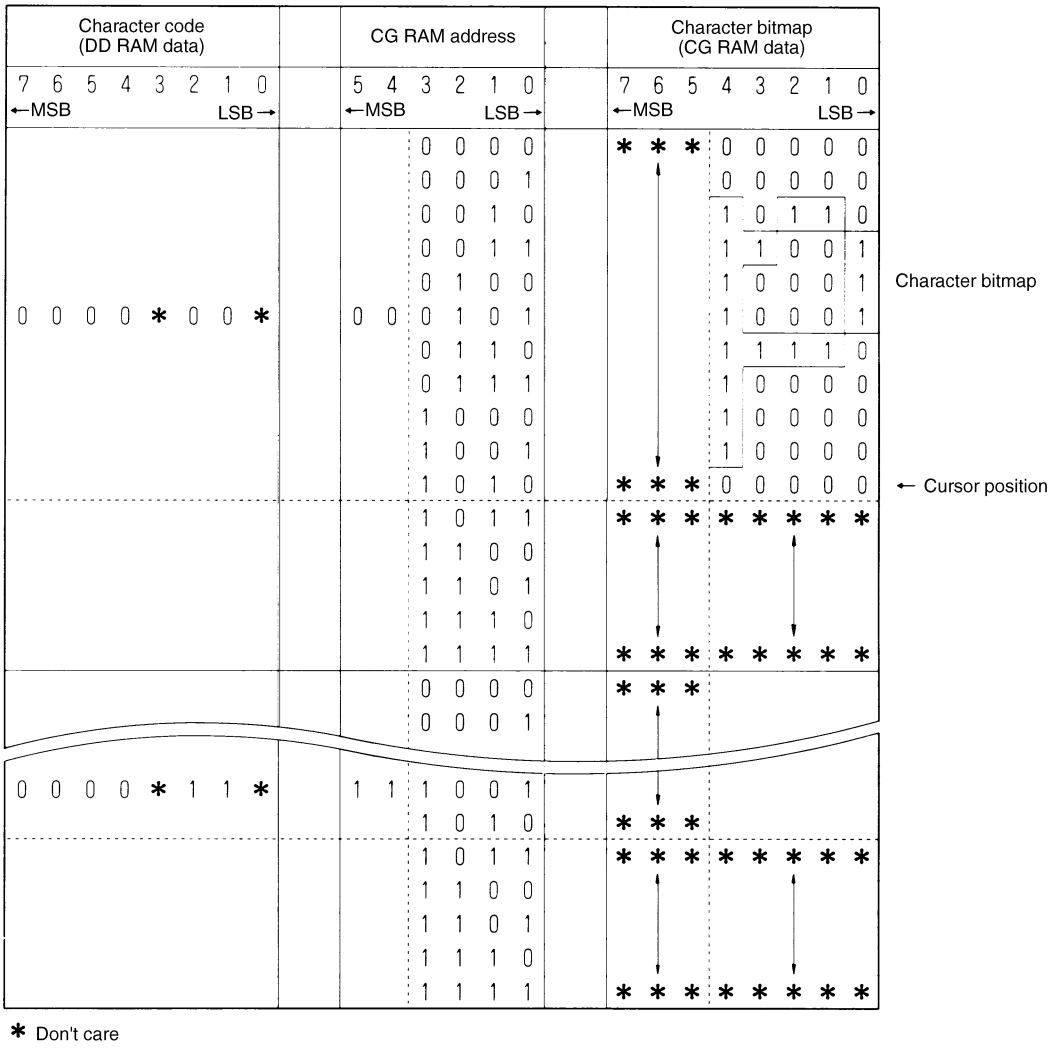
The layout and addressing for 5 × 10-pixel characters is shown in the following figure. Each character occupies eleven bytes, where bits 4 and 5 of the CG RAM address correspond to bits 1 and 2 of the character code. Note that bits 0 and 3 of the character code are not significant so, for example, codes 00_H, 01_H, 08_H and 09_H all select the same character.

Bits 0 to 3 of the CG RAM address are the bitmap row address where row 000 is the topmost displayed row.

The cursor, when displayed, is formed by ORing the bottom row with all 1s. If the cursor is used, row 1010 should contain all 0s so the cursor does not obscure the bottom row of the character.

Bits 0 to 4 of the CG RAM data contain the character bitmaps. When a bit is 1, the corresponding pixel is ON, and when 0, the pixel is OFF.

Bits 5 to 7 of the CG RAM data are present in memory, but are not used by the display circuit. These bits and the CG RAM bytes, rows 1011 to 1111 that are not used by the display circuit, can be used as general-purpose RAM.



Timing Generator

This circuit generates timing signals both for internal circuit operation and for driving external LC7930Ns. The timing signals for the DD RAM, CG ROM and CG RAM are independent of the microcontroller interface so that memory accesses by the microcontroller do not cause interference with the display drive signals.

Display Drivers

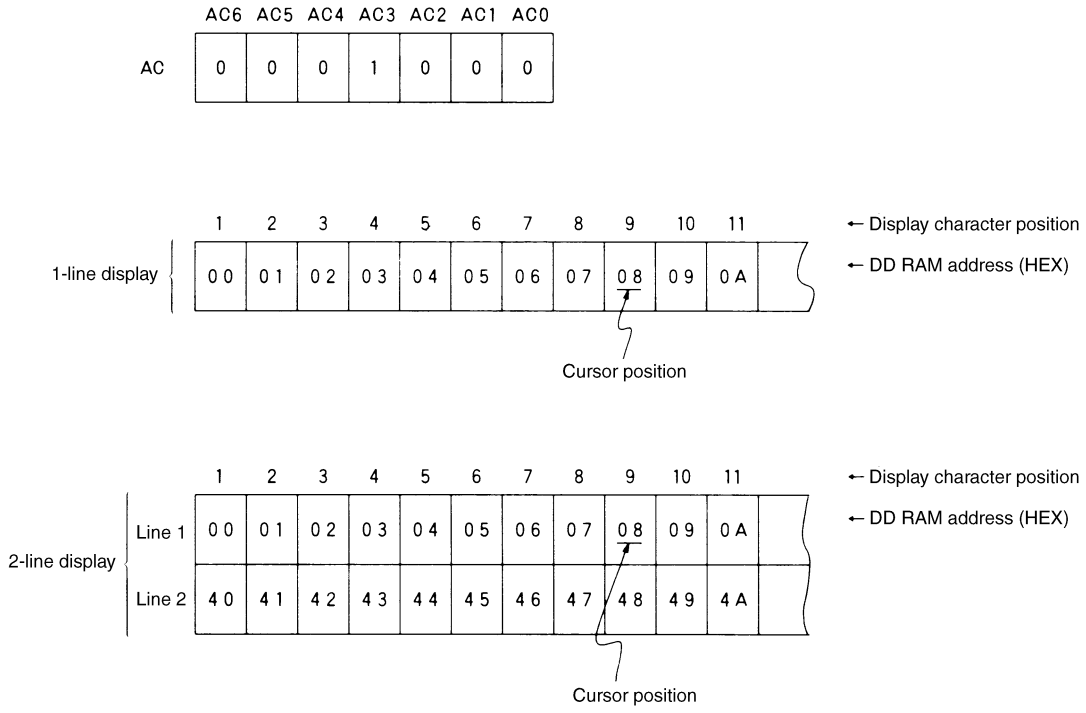
The LC7985 incorporates 16 LCD common driver outputs and 40 LCD segment driver outputs. The character font and the number of display lines determine the number of active common outputs.

The segment drivers function identically to the LC7930N display drivers. The character bitmap data to be displayed is latched in the internal 40-bit shift register before being output on the segment drivers.

The display bitmap data for each pixel-row is generated starting with the right-most character position. The data shifts through the shift register and is output on the shift register serial data output. The shift register latches the last 40 bits in the row so the LC7985 displays the left-most eight characters. External LC7930Ns connect in series to the serial data output and each one latches and displays bitmap data for eight additional characters.

Cursor Display and Blinking

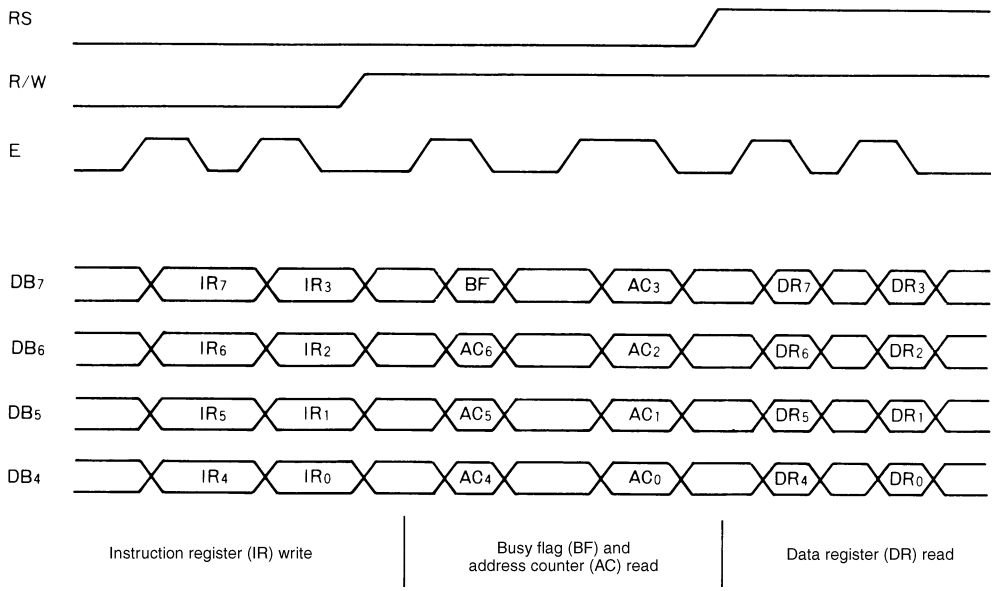
Cursor display and blinking of the character at the cursor position are controlled using the Display ON/OFF instruction. The cursor position is at the character corresponding to the address counter value as shown in the following figure. Note that the cursor and blinking character are also displayed at the address counter value when CG RAM is selected.



Microcontroller Interface

The LC7985 interfaces to both 4-bit and 8-bit microcontrollers.

DB0 to DB7 are used for the 4-bit data bus. Two read or write cycles, therefore, are required to transfer each data, status or instruction byte. The high-order four bits—bits DB4 to DB7 in 8-bit interface mode—are transferred first. The low-order four bits are then transferred as shown in the following figure.



Reset Circuit

The internal reset circuit initializes the LC7985 at power-ON. The busy flag remains ON from power-ON until initialization is complete 10ms after V_{DD} reaches 4.5V. Note that if power supply conditions are such that the internal reset circuit does not operate to initialize the device, the LC7985 must be initialized using commands from the microcontroller.

The initialization sequence is as follows.

1. Clear Display
2. Set Function (D/L = 1, N = 0, F = 0)
   Sets 8-bit interface size, 1-line display size and 5 × 7-pixel character font.
3. Cursor/Display Control (D = 0, C = 0, B = 0)
   Sets the display, the cursor and character blinking OFF.
4. Set Entry Mode (I/D = 1, S = 0)
   Sets address counter auto-increment and sets display shift OFF.