HIGH-VOLTAGE MIXED-SIGNAL IC

UC1611s

160COM x 256SEG Matrix LCD Controller-Driver
w/ 16-shade per pixel

MP Specifications
Revision 1.0

June 11, 2008

ULTRACHIP

The Coolest LCD Driver. Ever!!

TABLE OF CONTENT

UC1611s

Single-Chip, Ultra-Low Power
160COM x 256SEG Matrix
Passive LCD Controller-Driver

INTRODUCTION

UC1611s is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

UC1611s employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture and LRM (Line Rate Modulation) gray-shade modulation scheme to achieve near crosstalk free images, with well balanced gray shades.

In addition to low power SEG and COM drivers, UC1611s contains all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation, and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Cellular Phones, Smart Phones, PDA, and other battery-operated palmtop devices and/or portable instruments.

FEATURE HIGHLIGHTS

- Single-chip controller-driver supports 160x256 STN LCD, 16-shade-per-pixel with gamma compensated modulation.
- Soft-ICON: Partial scroll function to support programmable graphics ICON or scroll bar.
- Support both row ordered and column ordered display buffer RAM access
- Support industry standard 4-wire, 3-wire, and 2-wire serial buses (S8, S9, I^2C), and 16- /8- /4-bit parallel buses (8080 or 6800).
- Special driver structure and gray shade modulation scheme produce near crosstalk free image, with low power consumption for all display patterns.
- Fully programmable Mux Rate, partial display window, Bias Ratio, and Line Rate allow many flexible power management options.
- 4 software programmable frame rates (25Hz, 30Hz, 35Hz, and 40Hz). Support the use of fast Liquid Crystal material for speedy LCD response.
- 4 software-programmable temperature compensation coefficients.
- On-chip Power-ON Reset and Software RESET command make RST pin optional.
- Self-configuring 11x charge pump with on-chip pumping capacitor requires only 5 external capacitors to operate.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- V_{DD} (digital) range (Typ.): 1.8 V ~ 3.3V
  V_{DD} (analog) range (Typ.): 2.8 V ~ 3.3V
  LCD V_{OP} range: 5.65V ~ 17.5V
- Available in gold bump dies
  Bump pitch: 38 μM (Typ.)
  Bump gap: 13 μM (Typ.)
  Bump surface: 1887.5 $μM^2$

ORDERING INFORMATION

Product ID	Description
UC1611sGAA	Gold bumped die.

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and quality their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

USE OF I^2C

The implementation of I^2C is already included and tested in all silicon.

MTP LIGHT & ESD SENSITIVITY

The MTP memory cell is sensitive to photon excitation and ESD. Under extended exposure to strong ambient light, or when TST4 pin is exposed to ESD strikes, the MTP cells can lose its content before the specified memory retention time span. The system designer is advised to provide proper light & ESD shields to realize full MTP content retention performance.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

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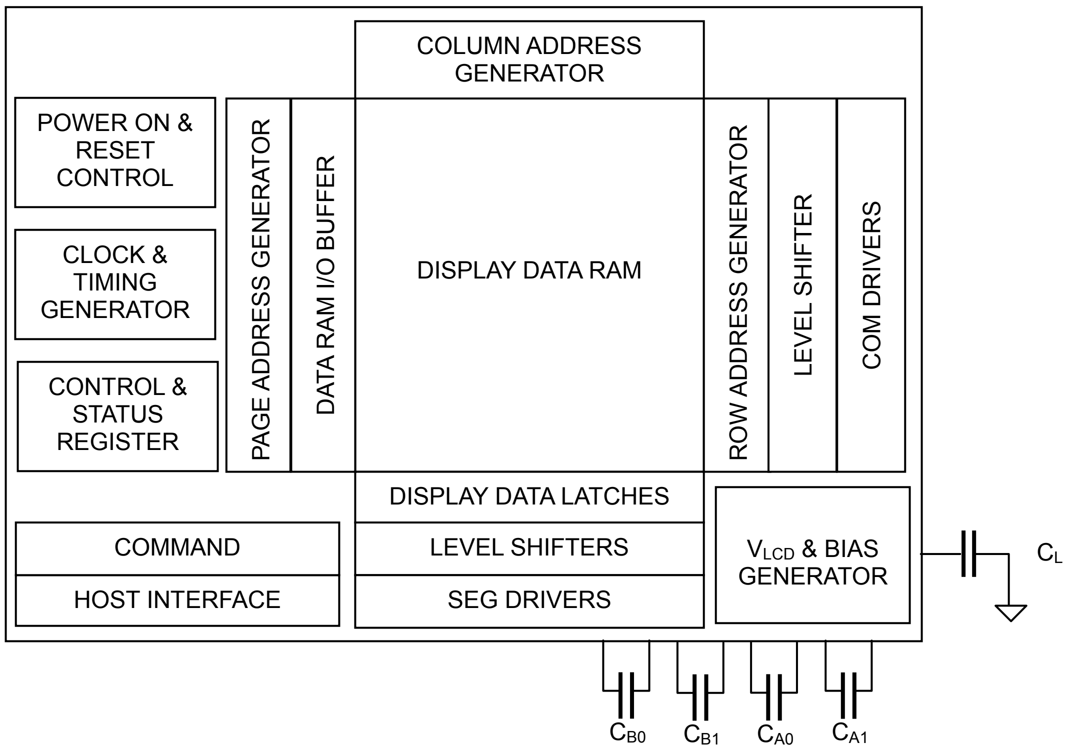
Block Diagram



PIN DESCRIPTION

Name	Type	Pins	Description
			MAIN POWER SUPPLY
V_{DD} V_{DD2} V_{DD3}	PWR	11 10 4	V_{DD2}/V_{DD3} is the analog power supply and it should be connected to the same power source. V_{DD} is the digital power supply and it should be connected to a voltage source that is no higher than V_{DD2}/V_{DD3}. Please maintain the following relationship: $V_{DD}+1.5\text{ V} \geqslant V_{DD2/3} \geqslant V_{DD}$ Minimize the trace resistance for V_{DD} and V_{DD2}/V_{DD3}.
V_{SS} V_{SS2}	GND	11 11	Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. Minimize the trace resistance for V_{SS} and V_{SS2}.
			LCD POWER SUPPLY
V_{A0+}, V_{A0-} V_{A1+}, V_{A1-} V_{B0+}, V_{B0-} V_{B1+}, V_{B1-}	PWR	4, 4 4, 4 4, 4 4, 4	LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C_{AX} / C_{BX} value between V_{AX+} / V_{BX+} and V_{AX-} / V_{BX-}, respectively. The resistance of these traces directly affects the driving strength of SEG electrodes and impacts the image of the LCD module. Minimize the trace resistance is critical in achieving high quality image.
$V_{LCD\text{-}IN}$ $V_{LCD\text{-}OUT}$	PWR	2 2	High voltage LCD Power Supply. Connect these pins together. A bypass capacitor C_L should be connected between V_{LCD} and V_{SS}. Keep the trace resistance under 30 Ω ~ 50 Ω.

Note:

Recommended capacitor values:

C_B: 100~250 x LCD load capacitance or 5 μF (5V), whichever is higher.
C_L: 0.1μF ~0.5 μF (25V) is appropriate for most applications.

<table>
<tr><th>Name</th><th>Type</th><th>Pins</th><th>Description</th></tr>
<tr><td colspan="4">HOST INTERFACE</td></tr>
<tr><td>BM1~0</td><td>I</td><td>2</td><td>Bus Mode: The interface bus mode is determined by BM[1:0] and D[15, 13] with the following relationship:
<table>
<tr><td>BM[1:0]</td><td>DB15, DB13</td><td>Mode</td></tr>
<tr><td>00</td><td>Data</td><td>8080/16-bit</td></tr>
<tr><td>01</td><td>Data</td><td>6800/16-bit</td></tr>
<tr><td>10</td><td>00</td><td>8080/8-bit</td></tr>
<tr><td>11</td><td>00</td><td>6800/8-bit</td></tr>
<tr><td>10</td><td>01</td><td>8080/4-bit</td></tr>
<tr><td>11</td><td>01</td><td>6800/4-bit</td></tr>
<tr><td>10</td><td>10</td><td>4-wire SPI (S8)</td></tr>
<tr><td>11</td><td>10</td><td>3-wire SPI (S9)</td></tr>
<tr><td>11</td><td>11</td><td>2-wire SPI (I^2C)</td></tr>
</table></td></tr>
<tr><td>CS1/A3
CS0/A2</td><td>I</td><td>2</td><td>Chip Selection. Chip is selected when CS1=”H” and CS0 = “L”. When the chip is not selected, D[15:0] will be high impedance.</td></tr>
<tr><td>RST</td><td>I</td><td>1</td><td>When RST=”L”, all control registers are re-initialized with their default states.

An RC filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to V_{DD}.</td></tr>
<tr><td>CD</td><td>I</td><td>1</td><td>Control data or Display data Selection for read/write operation.
In S9 and I^2C modes, CD pin is not used, connect CD pin to V_{SS}.
”L”: Control data ”H”: Display data</td></tr>
<tr><td>WR0
WR1</td><td>I</td><td>1
1</td><td>WR[1:0] controls the read/write operation of the host interface. See Host Interface section for more detail.

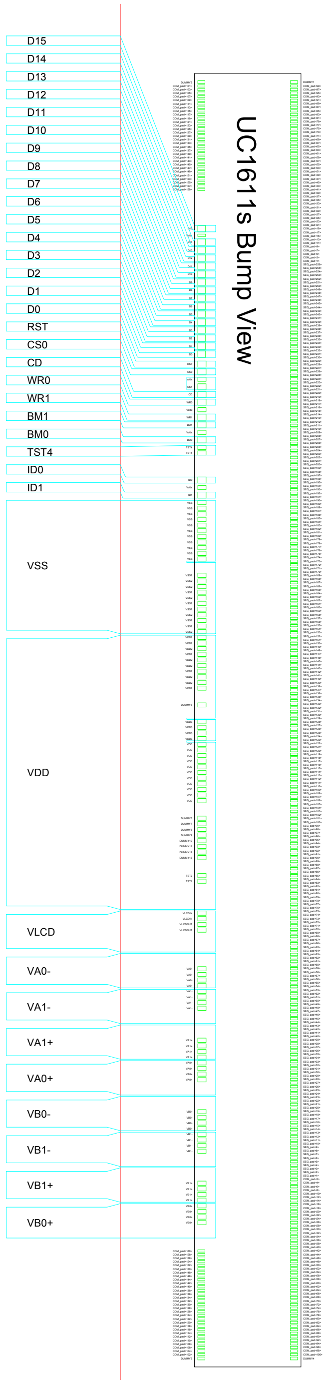
In parallel mode, WR[1:0] meaning depends on whether the interface is in 6800 mode or 8080 mode. In serial interface modes, these two pins are not used. Connect them to V_{SS}.</td></tr>
</table>

<table>
<tr><th>Name</th><th>Type</th><th>Pins</th><th>Description</th></tr>
<tr><td>D15~D0</td><td>I/O</td><td>16</td><td>Bi-directional bus for parallel host interface. In serial modes, connect D[0] to SCK, D[3] to SDA, and D[15, 13] to V_{DD} or V_{SS}.
<table>
<tr><th></th><th>D15</th><th>D14</th><th>D13</th><th>D12</th><th>D11</th><th>D10</th><th>D9</th><th>D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>16-bit (BM=0x)</td><td colspan="16">DB[15:0]</td></tr>
<tr><td>8-bit (BM=1x)</td><td>0</td><td>–</td><td>0</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td colspan="8">DB[7:0]</td></tr>
<tr><td>4-bit (BM=1x)</td><td>0</td><td>–</td><td>1</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td colspan="4">DB[3:0]</td></tr>
<tr><td>S8/S9 (BM=1x)</td><td>1</td><td>–</td><td>0</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>SDA</td><td>–</td><td>–</td><td>SCK</td></tr>
<tr><td>I^2C (BM=11)</td><td>1</td><td>–</td><td>1</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>SDA</td><td>–</td><td>–</td><td>SCK</td></tr>
</table>
Connect unused pins to V_{SS} or V_{DD}.
For connection details, refer to the table in the Host Interface section.</td></tr>
<tr><td>ID0</td><td>I</td><td>1</td><td>Production control. The connection will affect the content of ID when using the <code>Get Status</code> command. Connect to V_{DD} for “H” or V_{SS} for “L”.</td></tr>
<tr><td>ID1</td><td>I</td><td>1</td><td>SEG selection. Window commands will adjust its upper bound of column accordingly.
0 : number of column is set to 256 (SEG0~255)
1 : use SEG0~239 only and leave SEG240~255 open.</td></tr>
</table>

Name	Type	Pins	Description
HIGH VOLTAGE LCD DRIVER OUTPUT			
SEG1 ~ SEG256	HV	256	SEG (column) driver outputs. Support up to 256 columns. Leave unused drivers open-circuit.
COM1~ COM160	HV	160	COM (row) driver outputs. Support up to 160 rows. Leave unused drivers open-circuit.
MISC. PINS			
V_{DDX}	O	5	Auxiliary V_{DD}. These pins are connected to the main V_{DD} bus on chip. They are provided to facilitate chip configurations in COG application. These pins should not be used to provide V_{DD} power to the chip. It is not necessary to connect V_{DDX} to main V_{DD} externally.
TST4	I/HV	2	TST4 controls test mode and is also used to supply one of the high voltage required for MTP Program operation. Leave TST4 open during normal LCD operation. In COG applications keep TST4 trace resistance between 30 Ω ~ 50 Ω.
TST2 TST1	I/O	1 1	Test I/O pins. Leave these pins open during normal use.
Dummy		13	Dummy pins are *NOT* connected inside the IC.

Note: Several control registers will specify "0-based index" for COM and SEG electrodes. In those situations, COM_X or SEG_X will correspond to index *X*-1, and the value ranges for those index registers will be 0~159 for COM and 0~255 for SEG.

RECOMMENDED COG LAYOUT



Note for V_{DD} and V_{SS} with COG:
The operation condition, V_{DD}=1.8V (typical), should be satisfied under all operating conditions. UC1611s' peak current (I_{DD}) can be up to ~15mA during high speed data-write to UC1611s' on-chip SRAM. Such high pulsing current mandates very careful design of V_{DD} and V_{SS} ITO trances in COG modules. When V_{DD} and V_{SS} trace resistance is not low enough, the pulsing I_{DD} current can cause the actual on-chip V_{DD} to drop to below 1.65V and cause the IC to malfunction.

CONTROL REGISTERS

UC1611s contains registers that control the chip operation. These registers can be modified by commands. The following table is a summary of the control registers, their meaning and their default value. Commands supported by UC1611s will be described in the next two sections. A summary table comes first and then followed by a detailed instruction-by-instruction description.

Name: The symbolic reference of the register.
Note that, some symbol names refer to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after *Power-Up-Reset* and *System-Reset*.

Name	Bits	Default	Description
SL	8	00H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value are between 0 (for no scrolling) and (159 – FL). Setting SL outside of this range causes undefined effect on the displayed image.
FL	4	0H	Fixed lines. The first (FLx2) lines of each frame are fixed and are not affected by scrolling (SL). When FL is non-zero, the screen is effectively separated into two regions: one scrollable, one non-scrollable.
CA	8	00H	Display Data RAM Column Address (Used in Host to Display Data RAM access)
PA	7	00H	Display Data RAM Page Address (Used in Host for Display Data RAM access) When DC[5:3] = 100b, PA[6:5] : used to select Write Pattern 0~3. PA[4:0] : set SRAM page address
BR	2	2H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS}. 00b: 5 01b: 10 **10b: 11** 11b: 12
TC	2	0H	Temperature Compensation (per ^{o}C). **00b: -0.05%** 01b: -0.10% 10b: -0.15% 11b: 0.00%
PM	8	EAH	Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD}
PMO	6	00H	PM offset. the effective PM value, PMV = PM - PMO[4:0] when PMO[5]=1 the effective PM value, PMV = PM + PMO[4:0] when PMO[5]=0
PC	4	FH	Pump Control. PC[1:0]: Panel Loading 00b: LCD: ≤33nF **11b: 33nF ≤ LCD≤55nF** PC[3:2]: Pump Control 00b: External V_{LCD} **11b: Internal V_{LCD}** (11x charge pump) (Setting to 01 or 10 will be invalid and default value will be used instead.)
AC	4	1H	Address Control: AC[0]: WA: Automatic column/page Wrap Around (Default **1:ON**) AC[1]: Auto-Increment order **0: Column (CA) first** 1: Page (PA) first AC[2]: PID: PA (page address) auto increment direction (**0:+1**, 1:-1) AC[3]: Window Program Mode **0 : Inside Mode:** Write to SRAM within the window defined by (WPC0,WPP0), (WPC1,WPP1) 1 : Outside Mode: Write to SRAM but skip the window defined by (WPC0,WPP0), (WPC1,WPP1)

<table>
<tr><th>Name</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>DC</td><td>8</td><td>18H</td><td>Display Control:
DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default 0:OFF)
DC[1]: APO: All Pixels ON (Default 0:OFF)
DC[2]: Display ON/OFF (Default 0:OFF)
DC[4:3]: Gray-shade Modulation mode.
00 : On/Off mode   01: 8-shade Mode
10 : 4-shade Mode   11: 16-shade mode
DC[5]: Input Type of On/Off Mode (enable only when DC[4:3]=00b)
0: 4-bit per 1-pixel   1: 1-bit per 1-pixel
DC[7:6]: Display Pattern Selection (enable only when DC[5:3]=100b)
00: Pattern0   01: Pattern1
10: Pattern2   11: Pattern3</td></tr>
<tr><td>LC</td><td>10</td><td>020H</td><td>LCD Control:
LC[0]: MSF: MSB First mapping Option (Default: 0:OFF)
LC[1]: MX, Mirror X. SEG/Column sequence inversion (Default: 0:OFF)
LC[2]: MY, Mirror Y. COM/Row sequence inversion (Default: 0:OFF)
LC[3]: Enable FL lines in partial display mode.(Default: 0:OFF)
LC[5:4]: Line Rate (= Frame-Rate x Mux-Rate)
<table>
<tr><th></th><th>LC[5:4]=00b</th><th>01b</th><th>10b</th><th>11b</th></tr>
<tr><td>16-shade</td><td>20.0 Klps</td><td>24.0</td><td>28.0</td><td>32.0</td></tr>
<tr><td>8-shade</td><td>14.1</td><td>16.9</td><td>19.7</td><td>22.5</td></tr>
<tr><td>4-shade</td><td>13.3</td><td>16.0</td><td>18.7</td><td>21.4</td></tr>
<tr><td>On/Off mode</td><td>5.9</td><td>7.1</td><td>8.2</td><td>9.4</td></tr>
</table>
(Klps: Kilo-Line-per-second)
LC[7:6] : Reserved (Default : 00b)
LC[9:8] : Partial Display Control
0xb: Disable   Mux-rate = CEN+1 (DST and DEN are not used.)
11b: Enabled   Mux-rate = DEN-DST+1+LC[3]xFLx2</td></tr>
<tr><td>NIV</td><td>7</td><td>00H</td><td>N-Line Inversion
NIV[5:0] : 000000b : Disable N-line Inversion
NIV[6] : 0b: no-XOR   1b: XOR</td></tr>
<tr><td>CEN
DST
DEN</td><td>8
8
8</td><td>9FH
00H
9FH</td><td>COM scanning ENd (the last COM with full line cycle, 0-based index)
Display STart (the first COM with active scan pulse, 0-based index)
Display EDd (the last COM with active scan pulse, 0-based index)
Please maintain the following relationship:
CEN = (the actual number of pixel rows on the LCD) – 1
CEN ⩾ DEN ⩾ DST+ 9</td></tr>
<tr><td>ISOF</td><td>4</td><td>1H</td><td>Set the ISOlation clock in Front of COM pulse.</td></tr>
<tr><td>ISOB</td><td>4</td><td>0H</td><td>Set the ISOlation clock in Back of COM pulse.</td></tr>
<tr><td>WPC0</td><td>8</td><td>00H</td><td>Window program starting column address. Value range: 0 ~255.</td></tr>
<tr><td>WPP0</td><td>6</td><td>00H</td><td>Window program starting row address. Value range: 0~79.
When DC[5:3]=100b, value range: 0~19</td></tr>
<tr><td>WPC1</td><td>8</td><td>FFH</td><td>Window program ending column address. Value range: 0~255.</td></tr>
<tr><td>WPP1</td><td>6</td><td>4FH</td><td>Window program ending row address. Value range: 0~79.
When DC[5:3]=100b, value range: 0~19</td></tr>
</table>

Name	Bits	Default	Description
MTPC	5	10H	MTP Programming Control: MTPC[2:0] : MTP command **000** : **Idle** 001 : Read 010 : Erase 011 : Program 1xx : For UltraChip debug use only MTPC[3] : MTP Enable (automatically cleared after each MTP command) MTPC[4] : Ignore/Use MTP. 0: Ignore **1: Use**
MTPM	6	00H	MTP Write Mask.. 0: no action 1: program
APC	1	N/A	Advanced Product Configuration. For UltraChip only. Please do not use.
Status Registers			
OM	2	–	Operating Modes (Read Only) 00b: Reset 01b: (Not used) 10b: Sleep 11b: Normal
MD	1	–	MTP option flag. 0 : for non-MTP version. 1 : for MTP version
MS	1	–	MTP programming in-progress
WS	1	–	MTP Operation Succeeded

COMMAND TABLE

The following list of host commands is supported by UC1611s

C/D: 0: Control 1: Data
W/R: 0: Write cycle 1: Read cycle

\# Effective Data bits
– Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1.	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2.	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3.	Get Status	0	1	Ver	MX	MY	WA	DE	WS	MD	MS	Get Status	N/A
				ID[1:0]		PMO[5:0]							
				Product Code				0	0	0	EF		
4.	Set Column Addr. LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Addr. MSB	0	0	0	0	0	1	#	#	#	#	Set CA[7:4]	0
5.	Temp. Compensation.	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b: -0.05%/°C
6.	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC [1:0]	11b: 33~55 nF
7.	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC [3:2]	11b
8.	Set Adv. Program Control (double-byte command)	0	0	0	0	1	1	0	0	R	R	Set APC[R][7:0] R = 0~3	N/A
				#	#	#	#	#	#	#	#		
9.	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB			0	1	0	1	#	#	#	#	Set SL[7:4]	0
10.	Set Page Address LSB	0	0	0	1	1	0	#	#	#	#	Set PA[3:0]	0
	Set Page Address MSB			0	1	1	1	0	#	#	#	Set PA[6:4]	0
11.	Set Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	PM=EAH
				#	#	#	#	#	#	#	#		
12.	Set Isolation Clock Front	0	0	1	0	0	0	0	0	1	0	Set ISOF[3:0]	1H
				0	0	0	1	0	0	1	1		
				-	-	-	-	#	#	#	#		
13.	Set Isolation Clock Back	0	0	1	0	0	0	0	0	1	0	Set ISOB[3:0]	0H
				0	0	0	1	0	1	0	0		
				-	-	-	-	#	#	#	#		
14.	Set Partial Display Control	0	0	1	0	0	0	0	1	#	#	Set LC[9:8]	00b: Disable
15.	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
16.	Set Fixed Lines	0	0	1	0	0	1	#	#	#	#	Set FL[3:0]	0
17.	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[5:4]	10b:28klps
18.	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0
19.	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0
20.	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	110b
21.	Set LCD Mapping Control (double-byte command)	0	0	1	1	0	0	0	0	0	0	Set LC[3:0]	0
				0	0	0	0	#	#	#	#		
22.	Set N-line Inversion (double-byte command)	0	0	1	1	0	0	1	0	0	0	Set NIV[6:0]	00H
				-	#	#	#	#	#	#	#		
23.	Set Display Pattern	0	0	1	1	0	1	0	#	#	#	Set DC[7:5]	000b
24.	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
25.	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
26.	Set test control (double-byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
		0	0	#	#	#	#	#	#	#	#		
27.	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	10b: 11
28.	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[7:0]	159
		0	0	#	#	#	#	#	#	#	#		
29.	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[7:0]	0
		0	0	#	#	#	#	#	#	#	#		
30.	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[7:0]	159
		0	0	#	#	#	#	#	#	#	#		

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action		Default
31.	Set Window Program Starting Column Address	0	0	1	1	1	1	0	1	0	0	Shared with MTP Commands	Set WPC0	0
				#	#	#	#	#	#	#	#			
32.	Set Window Program Starting Row Address	0	0	1	1	1	1	0	1	0	1		Set WPP0	0
				-	-	#	#	#	#	#	#			
33.	Set Window Program Ending Column Address	0	0	1	1	1	1	0	1	1	0		Set WPC1	255
				#	#	#	#	#	#	#	#			
34.	Set Window Program Ending Column Address	0	0	1	1	1	1	0	1	1	1		Set WPP1	79
				-	-	#	#	#	#	#	#			
35.	Window Program Mode	0	0	1	1	1	1	1	0	0	#	Set AC[3]		0:Inside
36.	Set MTP Operation Control	0	0	1	0	1	1	1	0	0	0	Set MTPC[5:0]		10H
				-	-	#	#	#	#	#	#			
37.	Set MTP Write Mask	0	0	1	0	1	1	1	0	0	1	Set MTPM[5:0]		0
				-	-	#	#	#	#	#	#			
38.	Set V_{MTP1} Potentiometer	0	0	1	1	1	1	0	1	0	0	Shared with Window Program Commands	Set MTP1	N/A
				#	#	#	#	#	#	#	#			
39.	Set V_{MTP2} Potentiometer	0	0	1	1	1	1	0	1	0	1		Set MTP2	N/A
				#	#	#	#	#	#	#	#			
40.	Set MTP Write Timer	0	0	1	1	1	1	0	1	1	0		Set MTP3	N/A
				#	#	#	#	#	#	#	#			
41.	Set MTP Read Timer	0	0	1	1	1	1	0	1	1	1		Set MTP4	N/A
				#	#	#	#	#	#	#	#			
	SERIAL READ COMMAND (ENABLE IN S8 OR S9 BUS MODES ONLY)													
42.	Get Status	0	0	1	1	1	1	1	1	1	0	Get Status till Chip Disable		N/A
		-	1	Ver	MX	MY	WA	DE	WS	MD	MS			
				ID[1:0]		PMO[5:0]								
				Product Code				0	0	0	EF			

Notes:

- All bit patterns other than commands listed above may result in undefined behavior.
- Commands (38)~(41) are shared with commands (31)~(34), and have exactly the same code.
  When MTPC[3]=0, commands (37)~(41) are interpreted as Window Programming commands.
  When MTPC[3]=1, they are MTP Control commands.
- MTPM and PM are actually the same register. Only one of the commands (36) is valid at any time, and it is determined by MTPC[3].
- After MTP-ERASE or MTP-PROGRAM operation, please always perform the following steps,
  a) Disconnect TST4 power source.
  b) Do a full V_{DD} ON-OFF cycle (make sure V_{DD} drops below 50mV).
  before resuming normal operation.

COMMAND DESCRIPTIONS

(1) WRITE DATA TO DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8-bit Data-Write to SRAM							

(2) READ DATA FROM DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8-bit Data-Read from SRAM							

Write/Read Data Byte (command 1, 2) operation accesses display buffer RAM based on Page Address (PA) register and Column Address (CA) register. To minimize bus interface cycles, PA and CA will increase or decrease automatically after each bus cycle, depending on the setting of Access Control (AC) register. PA and CA can also be programmed directly by issuing `Set Page Address` and `Set Column Address` commands.

If Wrap-Around (WA) is OFF (AC[0] = 0), CA will stop increasing after reaching the end of page, and system programmers need to set the values of PA and CA explicitly. If WA is ON (AC[0]=1), when CA reaches end of page, CA will be reset to 0 and PA will be increased or decreased by 1, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 79), PA will be wrapped around to the other end of RAM and continue.

For both 8-bit and 16-bit interfaces, the first 1 byte and 2 bytes Read respectively is a dummy Read. Please ignore the data read out.

(3) GET STATUS SUMMARY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	Ver	MX	MY	WA	DE	WS	MD	MS
			ID[1:0]		PMO[5:0]					
			Product Code				**0**	**0**	**0**	EF

Status 1 definitions:

- *Ver* : Version Code. **1**
- *MX*: Status of register LC[1], mirror X.
- *MY*: Status of register LC[2], mirror Y.
- *WA:* Status of register AC[0]. Automatic column/row wrap around.
- *DE*: Display enable flag. DE=1 when display is enabled
- *WS*: MTP Command Succeeded
- *MD*: MTP Option (Yes/No)
- *MS*: MTP action status

Status 2 definitions:

- *ID*: Connection Status of the ID pin, could be used for production identifying.
- *PMO[5:0] :* PM offset value

Status 3 definitions:

- *Product Code :* 1h
- *EF:* ESD Flag. EF=1 when ESD strikes.

If multiple `Get Status` commands are issued consecutively within one single CD 1⇨0⇨1 transaction, the `Get Status` command will return {Status1, Status2, Status3, Status1, Status2, Status3, Status1..} alternately.

(4) SET COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB CA[3:0]	0	0	**0**	**0**	**0**	**0**	CA3	CA2	CA1	CA0
Set Column Address MSB CA[4:7]	0	0	**0**	**0**	**0**	**1**	CA7	CA6	CA5	CA4

Set the SRAM column address for read/write access.

CA possible value: **0** ~ 255

(5) SET TEMPERATURE COMPENSATION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Compensation TC[1:0]	0	0	**0**	**0**	**1**	**0**	**0**	**1**	TC1	TC0

Set V_{BIAS} Temperature compensation coefficient (%-per-degree-C) for all 4 temperature compensation curves.

Temperature compensation curve definition:
00b= -0.05%/°C 01b= -0.10%/°C 10b= -0.15%/°C 11b= 0.00%/°C

(6) SET PANEL LOADING

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading PC[1:0]	0	0	**0**	**0**	**1**	**0**	**1**	**0**	PC1	PC0

Set PC[1:0] according to the capacitance loading of LCD panel.

Panel loading definition: 00b : LCD ≤ 33nF **11b : 33 nF ≤ LCD ≤ 55 nF**

(7) SET PUMP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Pump Control PC[3:2]	0	0	**0**	**0**	**1**	**0**	**1**	**1**	PC3	PC2

Set PC[3:2] to program the build-in charge pump stages.

00b=External V_{LCD} **11b= Internal V_{LCD}** (11x charge pump)

(8) SET ADVANCED PROGRAM CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set APC[R][7:0] (Double byte command)	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	R
	0	0	APC[R] register parameter							

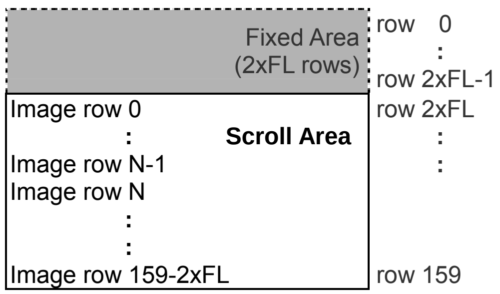
For UltraChip only. Please do NOT use.

(9) SET SCROLL LINE

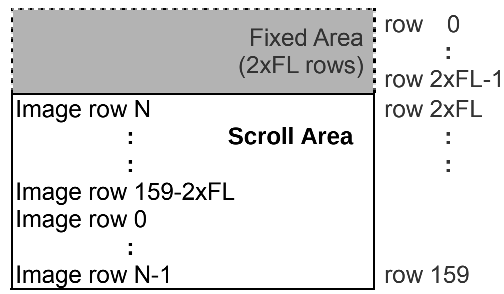
Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line LSB SL[3:0]	0	0	**0**	**1**	**0**	**0**	SL3	SL2	SL1	SL0
Set Scroll Line MSB SL[7:4]	0	0	**0**	**1**	**0**	**1**	SL7	SL6	SL5	SL4

Set the number of lines for scroll area.

The scroll line setting will scroll the displayed image up by SL rows. The valid value for SL is between 0 (no scrolling) and 159-2x(FL) (full scrolling). FL is the register value programmed by the Set Fixed Lines command.



SL=0



SL=N

(10) SET PAGE ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page Address LSB PA [3:0]	0	0	**0**	**1**	**1**	**0**	PA3	PA2	PA1	PA0
Set Page Address MSB PA [6:4]	0	0	**0**	**1**	**1**	**1**	0	PA6	PA5	PA4

Set SRAM page address for read/write access. UC1611s can store 4 B/W mode pictures in SRAM. Set PA[6:5] to specify which one to store. (Also refer to command "Set Display Mode".)

Possible value = **0** ~ 79

When On/Off mode and DC[5]=1
  PA[6:5] : select Write Pattern0(00b) ~ Write Pattern3(11b)
  PA[4:0] : set SRAM page address

(11) SET POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Potentiometer PM [7:0] (Double-byte command)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	0	0	PM[7:0]							

Program V_{BIAS} Potentiometer (PM[7:0]). See section *LCD VOLTAGE SETTING* for more detail.

Effective range of PM value = 0 ~ 255 (Default : **234**)

(12) SET ISOLATION CLOCK FRONT

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Isolation Clock Front ISOF [3:0] (Triple-byte command)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
	0	0	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**1**
	0	0	-	-	-	-	ISOF[3:0]			

Program isolation clock in front of COM pulse.

Effective range of ISOF value = 0 ~ 15 (Default : **1**)

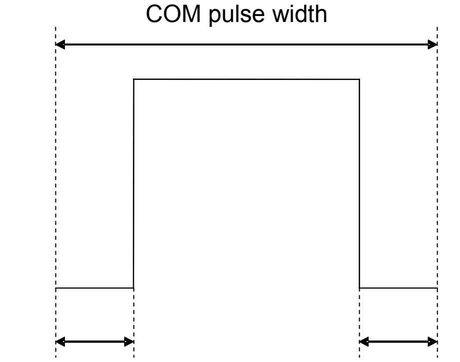
(13) SET ISOLATION CLOCK BACK

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Isolation Clock Back ISOB [3:0] (Triple-byte command)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
	0	0	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**
	0	0	-	-	-	-	ISOB[3:0]			

Program isolation clock in back of COM pulse.

Effective range of ISOB value = 0 ~ 15 (Default : **0**)

Note: Use higher V_{LCD} when increase isolation clock.



(14) SET PARTIAL DISPLAY CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Control LC [9:8]	0	0	**1**	**0**	**0**	**0**	**0**	**1**	LC9	LC8

This command is used to control partial display function.

LC[9:8] : **0xb: Disable Partial Display**, Mux-Rate = CEN+1 (DST and DEN are not used.)
11b: Enable Partial Display, Mux-Rate = DEN-DST+1+LC[3]xFLx2

(15) SET RAM ADDRESS CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	**1**	**0**	**0**	**0**	**1**	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0]: WA, Automatic column/page wrap around.
0: CA or PA (depends on AC[1]= 0 or 1) will stop incrementing after reaching boundary
1: CA or PA (depends on AC[1]= 0 or 1) will restart, and PA or CA will increment by one step.

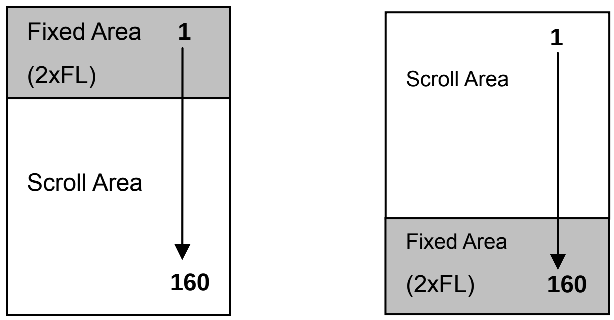
AC[1]: Auto-Increment order
0 : column (CA) increases (+1) first until CA reach CA boundary, then PA will increase by (+/-1).
1 : page (PA) increases (+/-1) first until PA reach PA boundary, then CA will increase by (+1).

AC[2]: PID, page address (PA) auto increment direction (**0**/1 = +/- 1)
When WA=1 and CA reaches CA boundary(CA=MC), PID controls whether page address will be adjusted by increasing +1 or -1. If WA is 0, the column address will stay in MC value and the page address will stay unchanged.

(16) SET FIXED LINES

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Fixed Lines FL [3:0]	0	0	**1**	**0**	**0**	**1**	FL3	FL2	FL1	FL0

The Fixed Lines function is used to implement the partial scroll function by dividing the screen into scroll and fixed area. The `Set Fixed Lines` command will define the fixed area, which will not be affected by the SL scroll function. When MY= 0, the fixed area covers the top 2xFL rows; when MY=1, the bottom 2xFL rows. One example of the visual effect on LCD is illustrated in the figure below. Default : **0**.



MY = 0 MY = 1

(17) SET LINE RATE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate LC [5:4]	0	0	**1**	**0**	**1**	**0**	**0**	**0**	LC5	LC4

Program LC [5:4] for line rate setting (Line-Rate = Frame-Rate x Mux-Rate)

In 16-shade mode:	00b : 20.0 Klps	01b : 24.0 Klps	**10b : 28.0 Klps**	11b : 32.0 Klps
In 8-shade mode:	00b : 14.1 Klps	01b : 16.9 Klps	**10b : 19.7 Klps**	11b : 22.5 Klps
In 4-shade mode:	00b : 13.3 Klps	01b : 16.0 Klps	**10b : 18.7 Klps**	11b : 21.4 Klps
In On/Off mode:	00b : 5.9 Klps	01b : 7.1 Klps	**10b : 8.2 Klps**	11b : 9.4 Klps

(Klps: Kilo-line per second)

(18) SET ALL PIXEL ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM. Default: **0**.

(19) SET INVERSE DISPLAY (PXV)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM. Default: **0**.

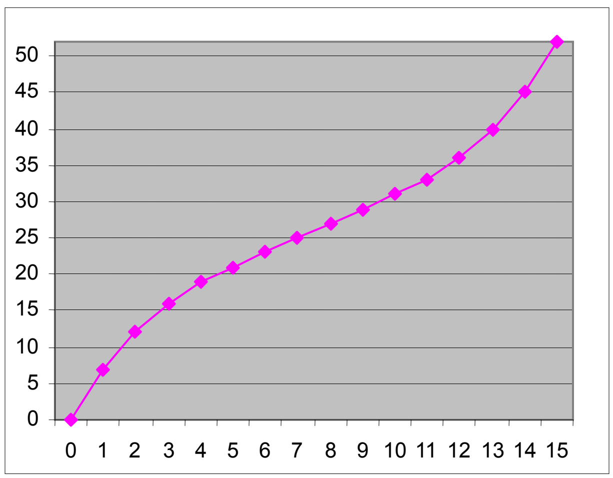
(20) Set Display Enable

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC[4:2]	0	0	**1**	**0**	**1**	**0**	**1**	DC4	DC3	DC2

This command is for programming register DC[4:2]. Default : **110b**.

When DC[2] is set to **0**, the IC will put itself into Sleep mode. All drivers, voltage generation circuit and timing circuit will be halted to conserve power. When DC[2] is set to 1, UC1611s will first exit from Sleep mode, restore the power and then turn on COM drivers and SEG drivers. There is no other explicit user action or timing sequence required to enter or exit the Sleep mode.

DC[4:3] controls the gray shade modulation modes. UC1611s has four gray shade modulation modes: an On/Off mode 8-shade mode, 4-shade mode and a 16-shade mode. The modulation curves are shown below. Horizontal axes are the gray shade data. The vertical axes are the ON-OFF ratio.



Effective range:

DC[4:3]		Gray-Scale	D7	D6	D5	D4	D3	D2	D1	D0
00	DC[5]=1	B/W Mode	1	0	1	0	1	0	1	0
	DC[5]=0		1	-	-	-	0	-	-	-
01		8-shade	1	1	1	-	0	0	0	-
			1	1	0	-	0	0	1	-
			1	0	1	-	0	1	0	-
			1	0	0	-	0	1	1	-
10		4-shade	1	1	-	-	0	0	-	-
			1	0	-	-	0	1	-	-
11		**16-shade**	1	1	1	1	0	0	0	0
			1	1	1	0	0	0	0	1
			1	1	0	1	0	0	1	0
			1	1	0	0	0	0	1	1
			1	0	1	1	0	1	0	0
			1	0	1	0	0	1	0	1
			1	0	0	1	0	1	1	0
			1	0	0	0	0	1	1	1

MSF=0 : RAM_D[7:4] = B[7:4], RAM_D[3:0] = B[3:0]
MSF=1 : RAM_D[7:4] = B[3:0], RAM_D[3:0] = B[7:4]

(21) Set LCD Mapping Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC[3:0] (Double-byte command)	0	0	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**
			0	**0**	**0**	**0**	LC3	MY	MX	MSF

Set LC[2:0] for COM (row) mirror (MY), SEG (column) mirror (MX) and MSB first or LSB first options (MSF).

MY is implemented by reversing the mapping order between RAM and COM (row) electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

MX is implemented by selecting the CA or 255-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

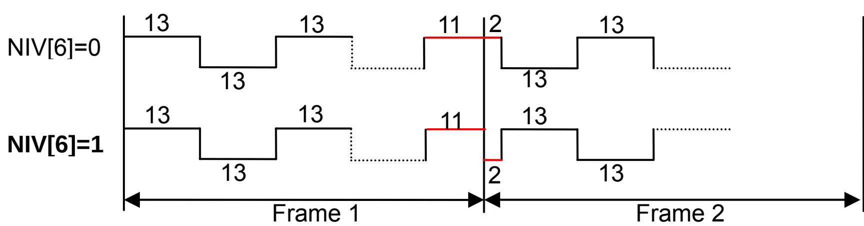
MSF is implemented by MSB-LSB swapping. The operation is determined by DC[4:3], as described in Set Gray Scale Mode command below.

LC[3] controls whether the soft icon section (FL on the top) will be displayed during partial display mode.

(22) Set N-Line Inversion

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set N-line Inversion NIV [6:0] (Double-byte command)	0	0	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**
			-	NIV [6:0]						

Set N-Line inversion:
NIV[5:0]: the number of lines to invert. **Default: 000000b**
NIV[6] : **0b: non-XOR** 1b: XOR



(23) Set Display Pattern

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Pattern	0	0	**1**	**1**	**0**	**1**	**0**	DC[7:5]		

Set Display Pattern Selection: (enabled only when DC[4:3]=00b)

DC[5]: Input type for On/Off mode
0 : 4 bits for 1 pixel 1 : 1 bit for 1 pixel

DC[7:6]: Select Display Pattern (Only enable when On/Off mode and DC[5:3] =100b)
00 : Pattern0 01 : Pattern1 10 : Pattern2 11 : Pattern3

UC1611s can store 4 different patterns in SRAM when DC[5:3]=100. Set PA[6:5] and DC[7:6] to select which pattern to store / display, respectively.

(24) System Reset

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This command will activate the system reset. Control register values will be reset to their default values. Data stored in RAM will not be affected.

(25) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No operation	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**

This command is used for "no operation".

(26) Set Test Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT (Double byte command)	0	0	**1**	**1**	**1**	**0**	**0**	**1**	**TT**	
	0	0	Testing parameter							

This command is used for UltraChip production testing. For UltraChip only. Please do NOT use.

(27) Set LCD Bias Ratio

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	**1**	**1**	**1**	**0**	**1**	**0**	BR1	BR0

Bias ratio definition: 00b= 5 01b=10 **10b**=11 11b=12

(28) Set COM End

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN [7:0] (Double byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**
	0	0	*CEN* register parameter							

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-rows in the LCD.

(29) Set Display Start

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST [7:0] (Double byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**0**
	0	0	*DST* register parameter							

This command programs the starting COM electrode, which has been assigned a full scanning period, and which will output active COM scanning pulses.

(30) Set Display End

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN [7:0] (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**
			DEN register parameter							

This command programs the ending COM electrode, which has been assigned a full scanning period, and which will output an active COM scanning pulse.

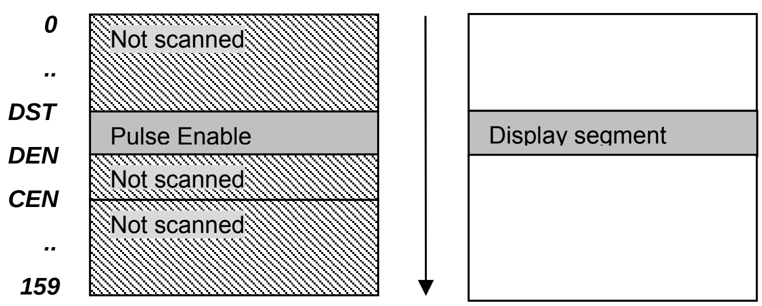
CEN, DST, and DEN are 0-based indexes of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

When LC[8:7]=11b, the Mux-Rate is narrowed down to DST-CEN+1+(LC[3]xFLx2). When MUS rate is reduced, reduce the line rate accordingly to reduce power. Changing MUX rate also require BR and V_{LCD} to be reduced.

For minimum power consumption, set LC[8:7]=11b, set (DST, DEN, FL, CEN) to minimize MUX rate, use slowest line rate which satisfies the flicker requirement, use On/Off mode, set PC[1:0]=00b, disable N-line Inversion, and use lowest BR, lowest V_{LCD} which satisfies the contrast requirement. When Mux-Rate is under 40, it is recommended to set BR=5 for optimum power saving.

In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.

Scan Method when LC[8:7]=11b: **Display Result:**



(31) Set Window Program Starting Column Address

<table>
<tr><th>Action</th><th>C/D</th><th>W/R</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td rowspan="2">Set WPC0 [7:0]
(Double-byte command)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td colspan="8">WPC0 register parameter</td></tr>
</table>

This command is to program the starting column address of RAM program window.

(32) Set Window Program Starting Row Address

<table>
<tr><th>Action</th><th>C/D</th><th>W/R</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td rowspan="2">Set WPP0 [5:0]
(Double-byte command)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>-</td><td>-</td><td colspan="6">WPP0 register parameter</td></tr>
</table>

This command is to program the starting row address of RAM program window.

(33) Set Window Program Ending Column Address

<table>
<tr><th>Action</th><th>C/D</th><th>W/R</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td rowspan="2">Set WPC1 [7:0]
(Double-byte command)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td colspan="8">WPC1 register parameter</td></tr>
</table>

This command is to program the ending column address of RAM program window.

(34) Set Window Program Ending Row Address

<table>
<tr><th>Action</th><th>C/D</th><th>W/R</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td rowspan="2">Set WPP1 [5:0]
(Double-byte command)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>-</td><td>-</td><td colspan="6">WPP1 register parameter</td></tr>
</table>

This command is to program the ending row address of RAM program window.

(35) SET WINDOW PROGRAM ENABLE

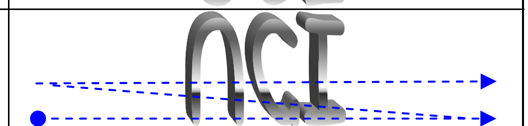
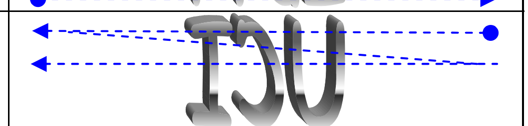
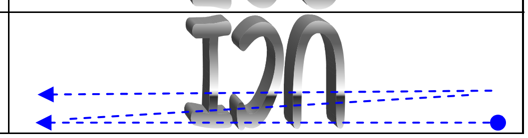
Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Window Program Enable AC[3]	0	0	**1**	**1**	**1**	**1**	**1**	**0**	**0**	AC3

This command controls the Window Program function.

0: Inside Mode 1: Outside Mode

Setting or resetting AC[3] does not affect the values of CA and RA. So, always remember to reposition CA and RA properly after changing the setting of AC[3].

When using Outside mode, the data inside window will be ignored, that is, users can send data of full screen.

Display Data Direction	Function Setting		Image in Display Data RAM (Physical origin: upper left corner)
	MX, LC[1]	RID, AC[2]	
Normal	0	0	
Y-mirror	0	1	
X-mirror	1	0	
X-mirror Y-mirror	1	1	

(36) SET MTP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPC[5:0] (Double-byte command)	0	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**0**
	0	0	**-**	**-**	MTPC register parameter					

This command is for MTP operation control:

MTPC[2:0] : MTP command

000 : Idle 001 : MTP Read
010 : MTP Erase 011 : MTP Program
1xx : For UltraChip use only.

MTPC[3] : MTP Enable (Automatically cleared each time after MTP command is done)
MTPC[4] : MTP value valid (Ignore MTP value when L)
MTPC[5] : For testing only. Set to 0 for normal operation

The following commands (34)~(38) are only valid when MTPC[3]=1.

DC[2] and MTPC[3] are mutually exclusive. Only one of these two control flags can be set to ON at any time. In other words, when DC[2] is ON, all MTP operations will be blocked, and, when MTP operation is active, set DC[2] to 1 will be blocked.

(37) SET MTP WRITE MASK

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPM[5:0] (Double-byte command)	0	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**1**
	0	0	-	-	MTPM register parameter					

This command enables Write to each individual MTP bits.

When MTPM[x]=1, the x-th bit of the MTP memory will be programmed to “1”. MTPM[x]=0 means no write action for x-th bit. And the content of this bit will not change.

The amount of “programming current” increases with the number of 1’s in MTPM. If the “programming current” appears to be too high for the LCM design (e.g. TST4 ITO trace is not wide enough to supply the current), use multiple write cycles and distribute the 1’s evenly into these cycles.

MTPM[5:0]: Set PMO value

(38) SET V_{MTP1} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP1 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**
	0	0	Shared register parameter							

This command is for fine tuning V_{OPT1} setting (use with BR=00) and is valid only when MTPC[3]=1.

(39) SET V_{MTP2} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP2 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**1**
	0	0	Shared register parameter							

This command is for fine tuning V_{MTP2} PM setting (use with BR=11) and is valid only when MTPC[3]=1.

(40) SET MTP WRITE TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP3 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**
	0	0	Shared register parameter							

(41) SET MTP READ TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP4 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**
	0	0	Shared register parameter							

Serial Read Commands (for S8 or S9 Bus mode only):

(42) GET STATUS

<table>
<tr><th>Action</th><th>C/D</th><th>W/R</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td rowspan="4">Get Status</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td rowspan="3">-</td><td rowspan="3">1</td><td>Ver</td><td>MX</td><td>MY</td><td>WA</td><td>DE</td><td>WS</td><td>MD</td><td>MS</td></tr>
<tr><td colspan="2">ID[1:0]</td><td colspan="6">PMO[5:0]</td></tr>
<tr><td colspan="4">Product Code</td><td>0</td><td>0</td><td>0</td><td>EF</td></tr>
</table>

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate (*MR*) is completely software programmable in UC1611s via the register CEN.

Combined with low power partial display mode and a low bias ratio of 5, UC1611s can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_{REF}, i.e.

$BR = V_{LCD}/V_{REF}$,
where $V_{REF} = V_{A1P} - V_{A1N}$

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux}+1$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

Due to the nature of STN operation, an LCD designed for good gray-shade performance at high Mux Rate (e.g. MR=160), can generally perform very well as a black and white display, at lower Mux Rate. However, it is also true that such technique generally cannot maintain LCD's quality of gray shade performance, since the contrast of the LCD will increase as Mux Rate decreases, and the shades near the two ends of the spectrum will start to lose visibility.

UC1611s supports four *BR* as listed below. BR can be selected by software program.

BR	0	1	2	3
Bias Ratio	5	10	**11**	12

Table 1: Bias Ratios

TEMPERATURE COMPENSATION

Four (4) different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per °C	–0.05	–0.10	–0.15	0.00

Table 2: Temperature Compensation

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[3:2]. For good product reliability, it is recommended to keep V_{LCD} under 17.5V over the entire operating range.

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and TC (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T \%)$$

where

C_{V0} and C_{PM} are two constants, whose value depends on the BR register setting. The values are provided in the table in the next page,

PM is the numerical value of PM register,

T is the ambient temperature in °C, and

C_T is the temperature compensation coefficient as selected by TC register.

V_{LCD} FINE TUNING

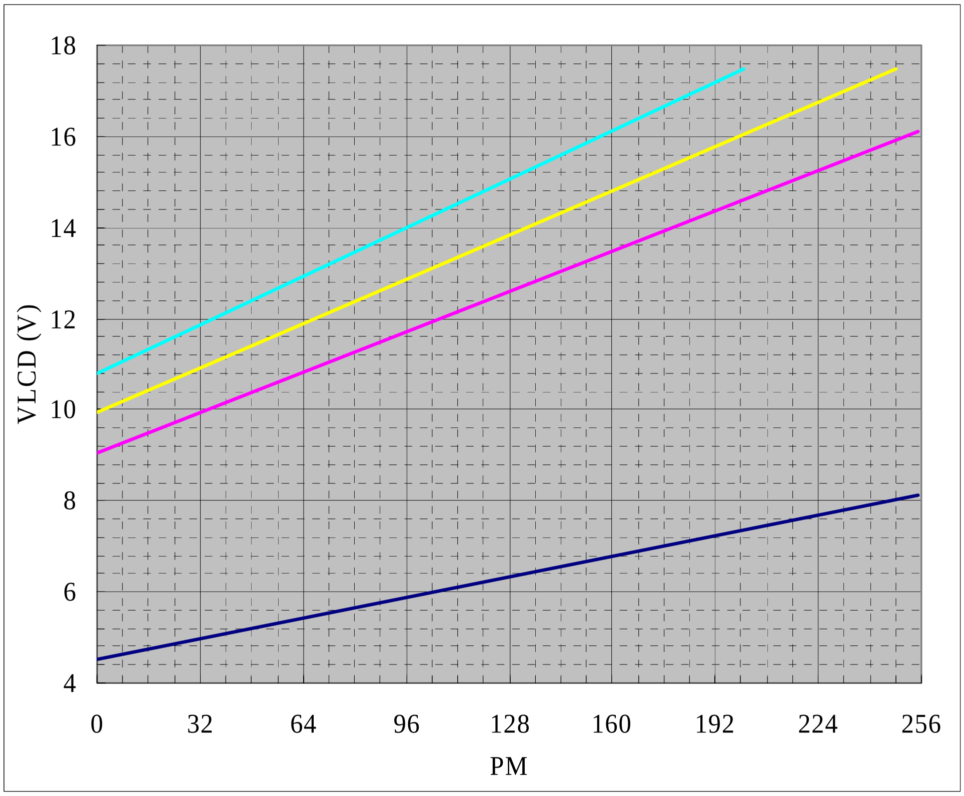
Gray shade and color STN LCD is sensitive to even a 1% mismatch between IC driving voltage and the V_{OP} of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to match the actual V_{OP} of the LCD.

For best result, software or MTP based V_{LCD} adjustment is the recommended method for V_{LCD} fine-tuning. System designers should always consider the contrast fine tuning requirement before finalizing on the LCM design.

LOAD DRIVING STRENGTH

The power supply circuits of UC1611s are designed to handle LCD panels with load capacitance up to 40nF at V_{LCD}=17V when V_{DD2} = 2.8V. For larger LCD panels or higher V_{LCD}, use higher $V_{DD2/3}$.

V_{LCD} QUICK REFERENCE



V_{LCD}-PM relationship for different BR setting at 25°C.

BR	C_{V0} (V)	C_{PM} (mV)	PM_reg	V_{LCD} (V)
5	4.518	14.19	0	4.52
			255	8.14
10	9.048	27.68	0	9.05
			255	16.11
11	9.925	30.48	0	9.92
			248	17.48
12	10.791	33.25	0	10.79
			201	17.47

NOTE:

1. For good product reliability, keep V_{LCD} (max) under **17.5V** under all operating temperature.
2. The integer values of BR above are for reference only and may have slight shift.

HI-V GENERATOR AND BIAS REFERENCE CIRCUIT

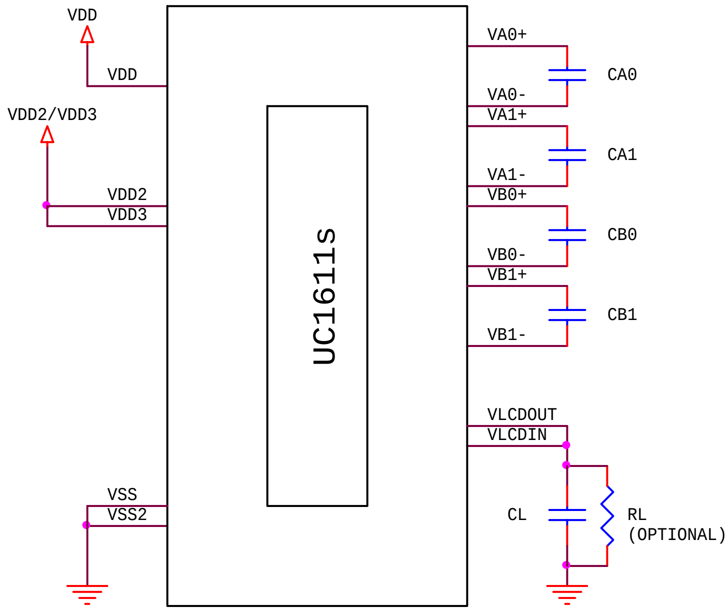


FIGURE 1: Reference circuit using internal Hi-V generator circuit

Note

- Recommended component values:
  - C_B: 100~250 x LCD load capacitance or 5μF (5V), whichever is higher.
  - C_L: 0.1μF ~0.5μF (25V) is appropriate for most applications.
  - R_L: 3.3M ~ 10MΩ Acts as a draining circuit when the power is abnormally shut down.

LCD Display Controls

Clock & Timing Generator

UC1611s contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Eight different line rates are provided for system design flexibility. The line rate is controlled by register LC[5:4]. When Mux-Rate is above 108, frame rate is calculated as:

Frame rate = Line-Rate / Mux-Rate.

When Mux-Rate is under 107, 80, 53, 40, Line rate will automatically be scaled down by 1.5, 2, 3, 4 respectively to reduce power consumption.

Flicker-free frame rate is dependent on LC material and gray-shade modulation scheme. Frame rate ⩾ 150Hz is recommended for 16-shade mode. Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

Driver Modes

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When SEG drivers are in idle mode, they will be connected together to ensure zero DC condition on the LCD.

Driver Arrangements

The naming conventions are: COM(x), where x = 1~160, refers to the COM driver for the x-th row of pixels on the LCD panel.
The mapping of COM(x) to LCD pixel rows is fixed and it is not affected by SL, CST, CEN, DST, DEN, MX or MY settings.

Display Controls

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO), and Inverse (PXV). DE has the overriding effect over PXV and APO.

Driver Enable (DE)

Driver Enable is controlled by the value of DC[2] via *Set Display ON* command. When DC[2] is set to OFF (logic “0”), both COM and SEG drivers will become idle and UC1611s will put itself into Sleep mode to conserve power.

When DC[2] is set to ON, the DE flag will become “1”, and UC1611s will first exit from Sleep mode, restore the power (V_{LCD}, V_D, etc.) and then turn on COM and DEG drivers.

All Pixels On (APO)

When set, this flag will force all active SEG drivers to output On signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

Inverse (PXV)

When this flag is set to ON, active SEG drivers will output the inverse of the value it received from the display buffer RAM. This flag has no impact on data stored in RAM.

Partial Scroll

The control register FL specifies a region of rows those are not affected by the SL register. Since SL register can be used to implement scroll function. The FL register can be used to implement fixed region when the other part of the display is scrolled by SL.

Partial Display

UC1611s provides flexible control of Mux Rate and active display area. Please refer to command Set COM End, Set Partial Display Start, and Set Partial Display End for more detail.

Gray-shade Modulation Mode

UC1611s has two gray-shade modulation modes: 16-shade, 8-shade, 4-shade and On/Off mode.

The On/Off mode will consume roughly 40~45% less power than the 16-shade mode, and can be used for situations where power consumption is more critical than color fidelity.

Changing gray-shade modulation mode does not affect the content of SRAM display buffer, and the image data will remain the same after switching back and forth between On/Off mode and 16-shade mode.

LAYOUT CONSIDERATIONS FOR COM SIGNALS

Under 16-gray-shade mode, the COM scanning pulses of UC1611s can be as short as 17µs. Since COM distortion can lead to reduction of effective duty factor of the LCM, it is critical to control the RC delay of COM signal to minimize distortion of COM scanning pulse.

For the best image quality, limit the worst case RC delay of COM signal as calculated below.

$RC_{COM} = (R_{ROW} / 3 + R_{COM} + R_{OUT}) \times C_{ROW}$
$RC_{COM\text{-}MAX} \leqslant 1.2\mu S$

where

- C_{ROW}: LCD loading capacitance of one row of pixels. It can be calculated by C_{LCD}/Mux-Rate, where C_{LCD} is the LCD panel capacitance.
- R_{ROW}: ITO resistance over one row of pixels within the active area
- R_{COM}: COM routing resistance from IC to the active area (COF+ITO routing)
- R_{OUT}: COM driver output impedance

In case $RC_{COM\text{-}MAX}$ exceed the above constraint significantly, please make sure

$| RC_{COM\text{-}MAX} – RC_{COM\text{-}MIN} | < 0.6\mu S$

so that the COM scan pulse distortions from the top of the screen to the bottom of the screen are uniform.

For 8-gray-shade mode, the COM scanning pulse is about 35% slower than the 16-gray-shade mode. Therefore, the two constraints described above can be relaxed by 1/3 respectively to

$RC_{COM} \leqslant 1.6uS$
$| RC_{COM\text{-}MAX} – RC_{COM\text{-}MIN} | < 0.8\mu S$

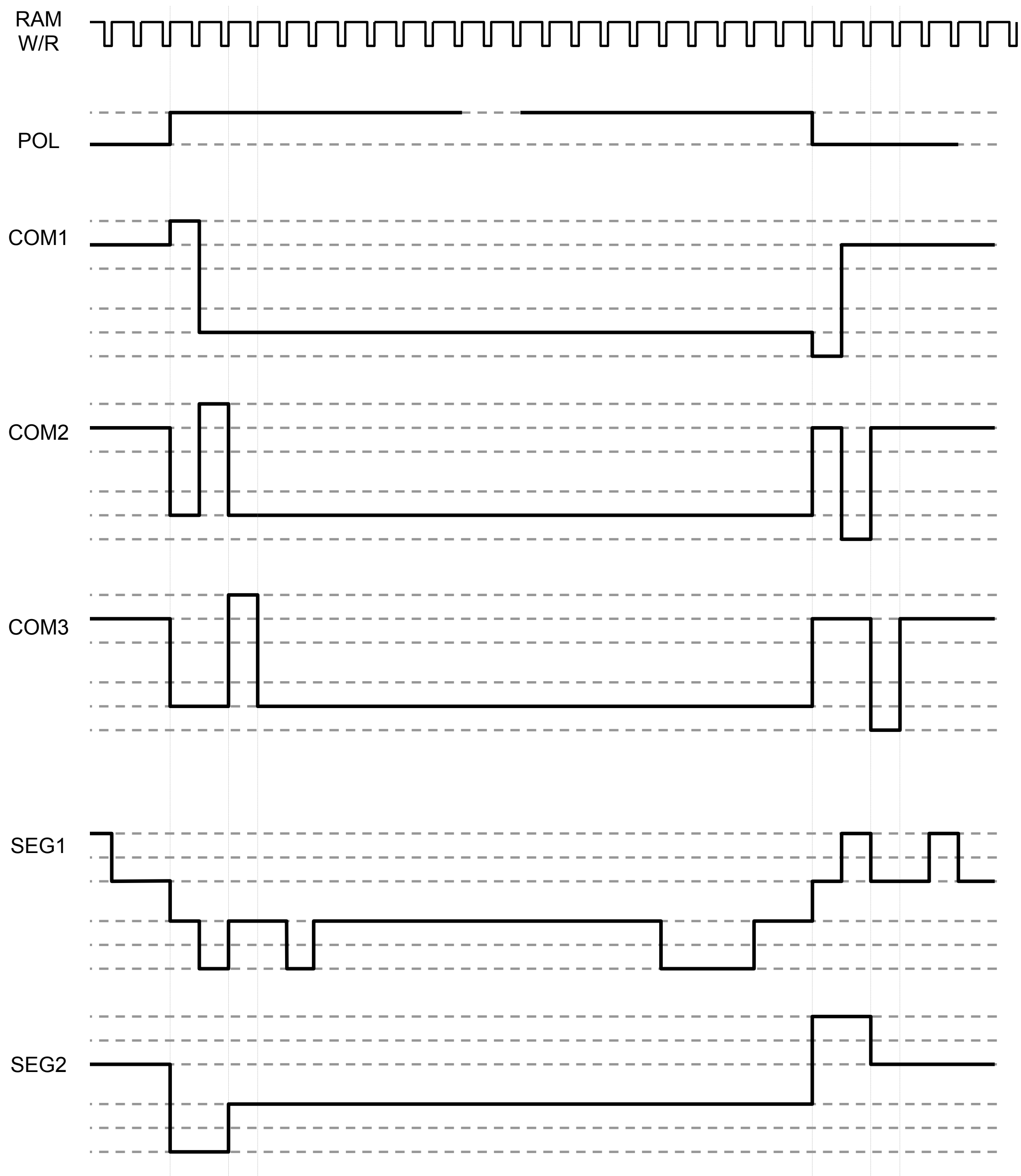


FIGURE 2: COM and SEG Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1611s supports 2 parallel bus protocols, 8080 and 6800 (in 16-bit, 8-bit, or 4-bit bus width), and 3 serial bus protocols (4-wire, 3-sire, and 2-wire).

Designers can either use parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules.

		Bus Type								
		Parallel						**Serial**		
		8080			**6800**			**S8**	**S9**	**I²C**
Width		16-bit	8-bit	4-bit	16-bit	8-bit	4-bit	4-wire	3-wire	2-wire
Access		Read/Write								
Control & Data Pins	BM[1:0]	00	10	10	01	11	11	10	11	11
	D[15, 13]	Data	00	01	Data	00	01	10	10	11
	CS[1:0]	Chip Select								A[3:2]
	CD	Control/Data							–	
	WR0	$\overline{WR}$			R/$\overline{W}$			0		
	WR1	$\overline{RD}$			EN			0		
	D[14, 12:8]	Data	–	–	Data	–	–	–		
	D[7:4]	Data		–	Data		–	–		
	D[3:0]	Data		Data	Data		Data	D3=SDA, D0=SCK		

* Connect unused control pins and data bus pins to V_{DD} or V_{SS}

Table 3: Host interfaces Choices

PARALLEL INTERFACE

The timing relationship between UC1611s' internal control signals, RD and WR, and their associated bus actions are shown in the figure below.

The Display RAM Read Interface is implemented as a two-stage pipe-line. This architecture requires a dummy read cycle to be performed before the actual data can propagate through the pipe-line and be read from data port D[7:0], every time memory address is modified (in 16-bit, 8-bit, or 4-bit mode) by either *Set CA,* or *Set PA* command.

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

16-BIT, 8-BIT & 4-BIT BUS OPERATION

UC1611s supports 16-bit, 8-bit, and 4-bit bus widths. The bus width is determined by pins BM[1:0] and {D15, D13}.

UC1611s SARM read/write is based on 8-bit.

8-bit bus operation exactly doubles the clock cycles of 16-bit bus operation, while 4-bit doubles the clock cycles of 8-bit, MSB followed by LSB, including the dummy read, which also requires two clock cycles. For 16-bit bus operation, SRAM will perform read/write twice successively to finish a complete Read/Write.

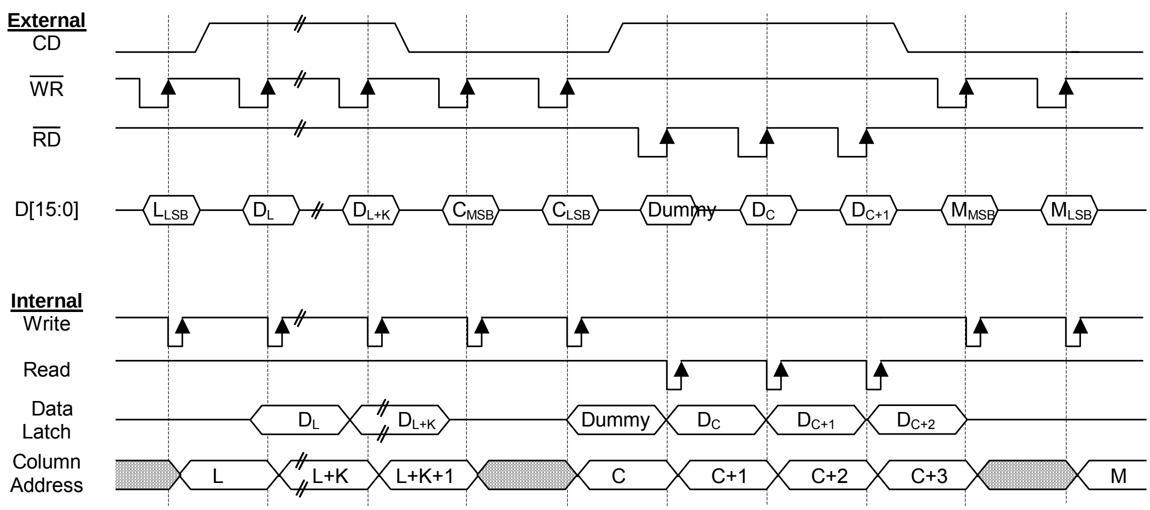


FIGURE 3.a: 16-bit Parallel Interface & Related Internal Signals

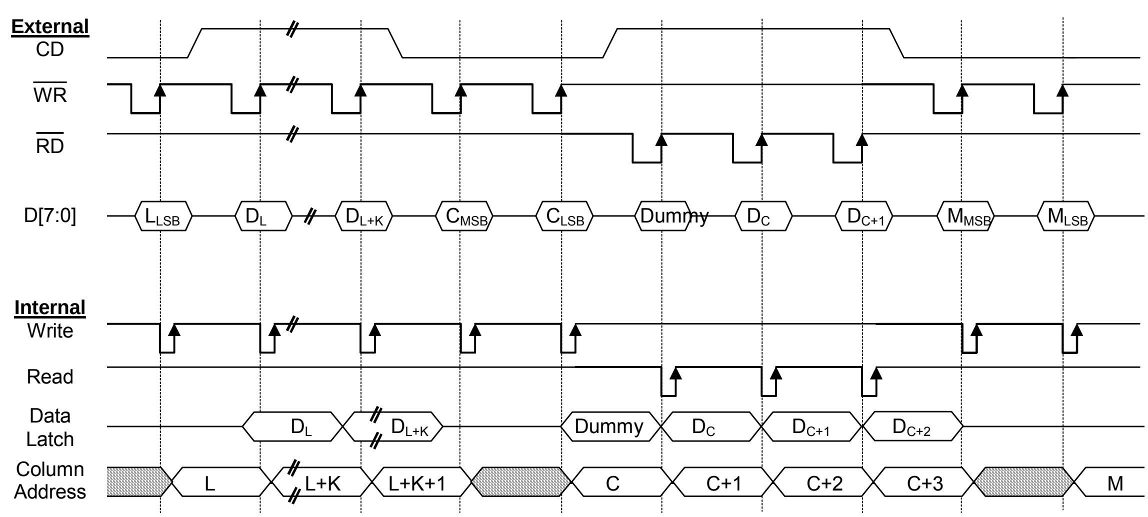


FIGURE 3.b: 8-bit Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1611s supports 3 serial modes, 4-wire SPI mode (S8), 3-wire SPI mode (S9), and 2-wire SPI mode (I^2C). Bus interface mode is determined by the wiring of the BM[1:0] and D7. See configuration table in the beginning of this section for more detail.

4-WIRE SERIAL INTERFACE (S8)

Pins CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

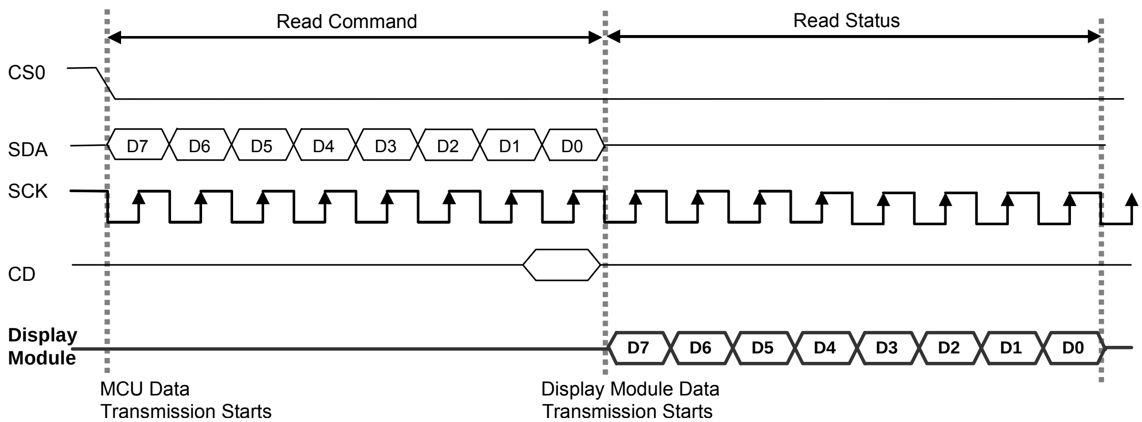


FIGURE 4.a: 4-wire Serial Interface (S8) – Read

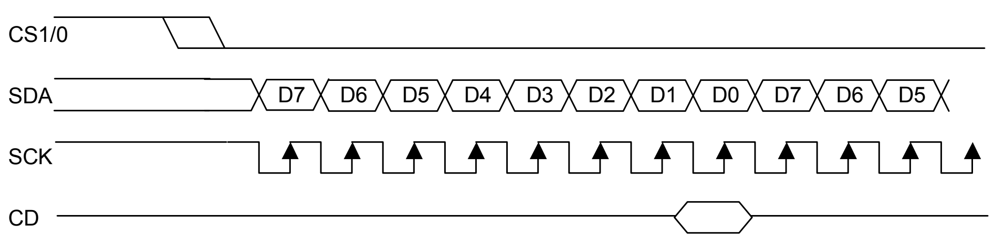


FIGURE 4.b: 4-wire Serial Interface (S8) – Write

3-WIER SERIAL INTERFACE (S9)

Pins CS[1:0] are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command or data bits are latched on rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command.

If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse. By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V_{DD} or V_{SS}. The toggle of CS0 (or CS1) for each byte of data/command is recommended but optional.

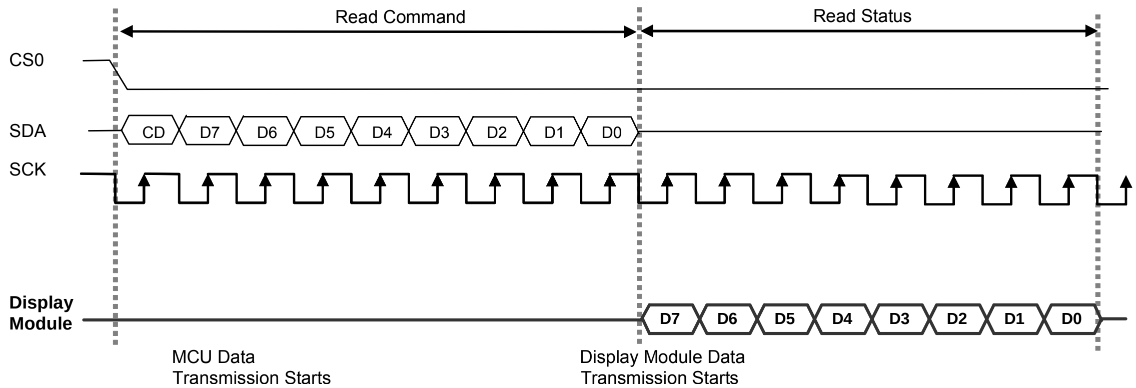


FIGURE 5.a: 3-wire Serial Interface (S9) – Read

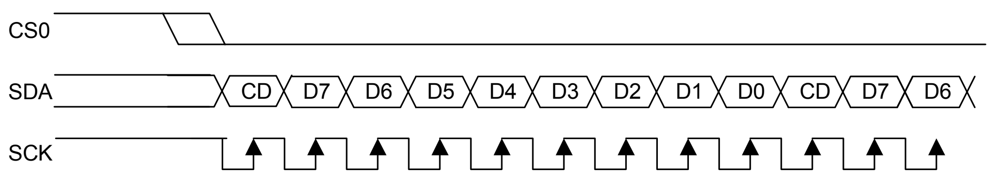


FIGURE 5.b: 3-wire Serial Interface (S9)

I^2C (2-WIRE) INTERFACE

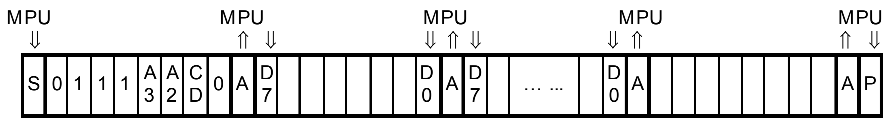
When BM[1:0] is set to “LH” and D[7:6] is set to “HH”, UC1611s is configured as an I^2C bus signaling protocol compliant slave device. Please refer to I^2C standard for details of the bus signaling protocol, and AC Characteristic section for timing parameters of UltraChip implementation.

In this mode, pins CS[1:0] become A[3:2] and are used to configure UC1611s’ device address. Proper wiring to V_{DD} or V_{SS} is required for the IC to operate properly for I^2C mode.

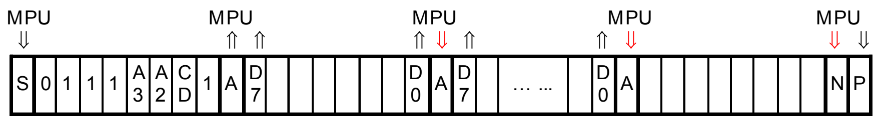
Each UC1611s I^2C interface sequence starts with a “S” (Start) from the bus master, followed by a sequence header, containing a device address, the mode of transfer (CD, 0:Control, 1:Data), and the direction of the transfer (RW, 0:Write, 1:Read).

Since both WR and CD are expressed explicitly in the header byte, the control pins WR[1:0] and CD are not used in I^2C mode and should be connected to V_{SS}.

Write Mode



Read Mode

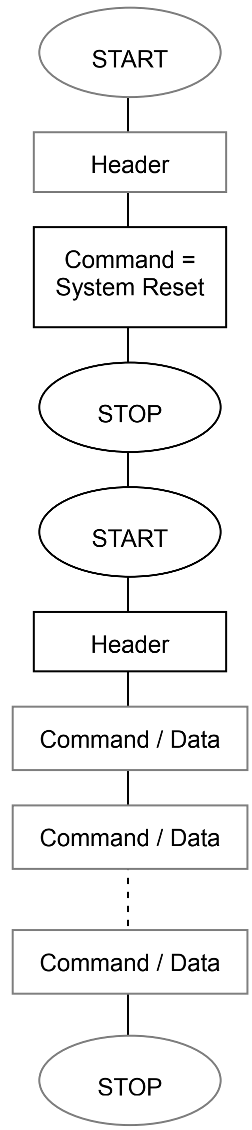


The direction (read or write) and content type (command or data) of the data bytes following each header byte are fixed for the sequence. To change the direction (R⇔W) or the content type (C⇔D), start a new sequence with a START (S) flag, followed by a new header.

After receiving the header, the UC1611s will send out a “A” (Acknowledge signal). Then, depends on the setting of the header, the transmitting device (either the bus master or UC1611s) will start placing data bits on SDA, MSB to LSB, and the sequence will repeat until a STOP signal (P, in WRITE mode), or an N (Not Acknowledged, in READ mode) is sent by the bus master.

When using I^2C serial mode, if command System Reset is to be written, the writing sequence must be finished (STOP) before succeeding data or commands start. The flow chart on the right shows a writing sequence with a "System Reset" command.

Note that, for data read (CD=1), the first byte of data transmitted will be dummy.



HOST INTERFACE REFERENCE CIRCUIT

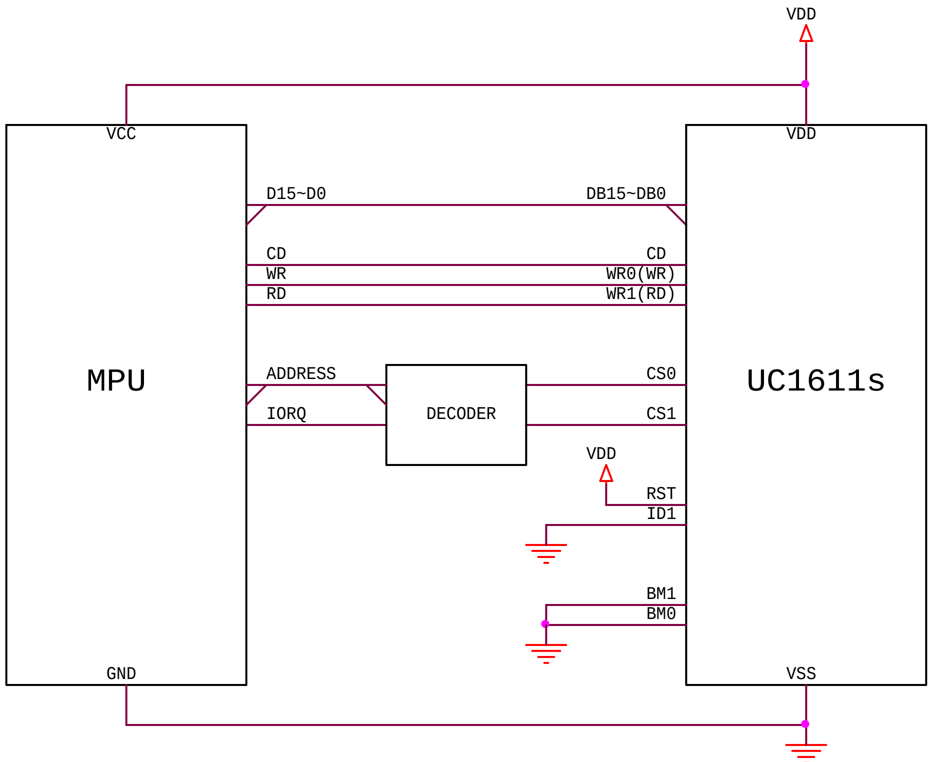


FIGURE 6: 8080/16-bit parallel mode reference circuit

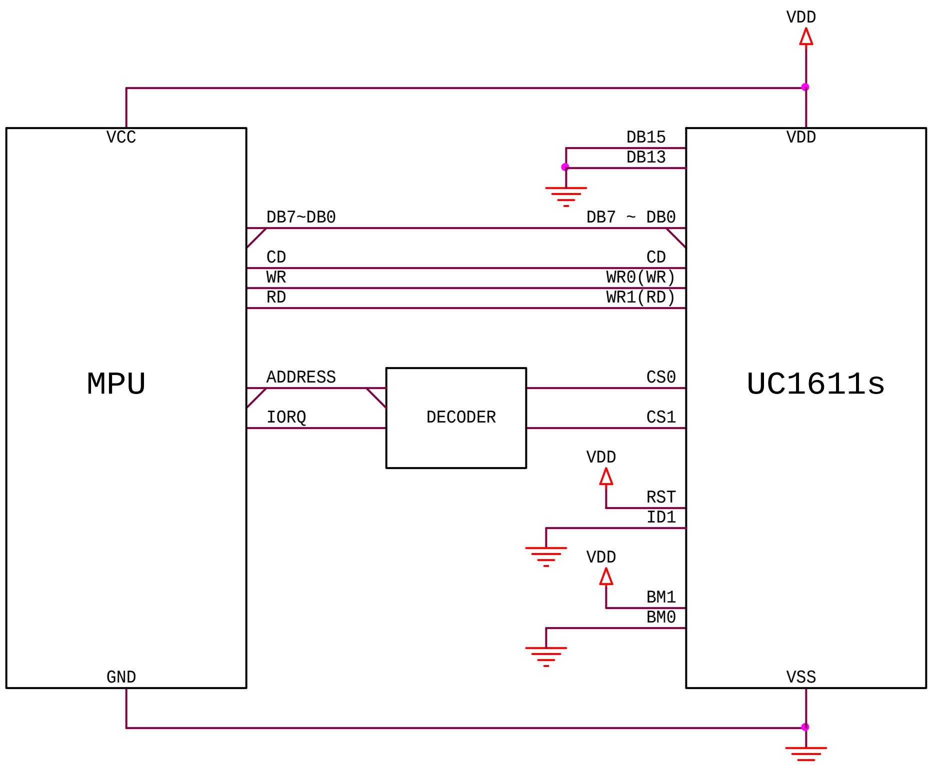


FIGURE 7: 8080/8-bit parallel mode reference circuit

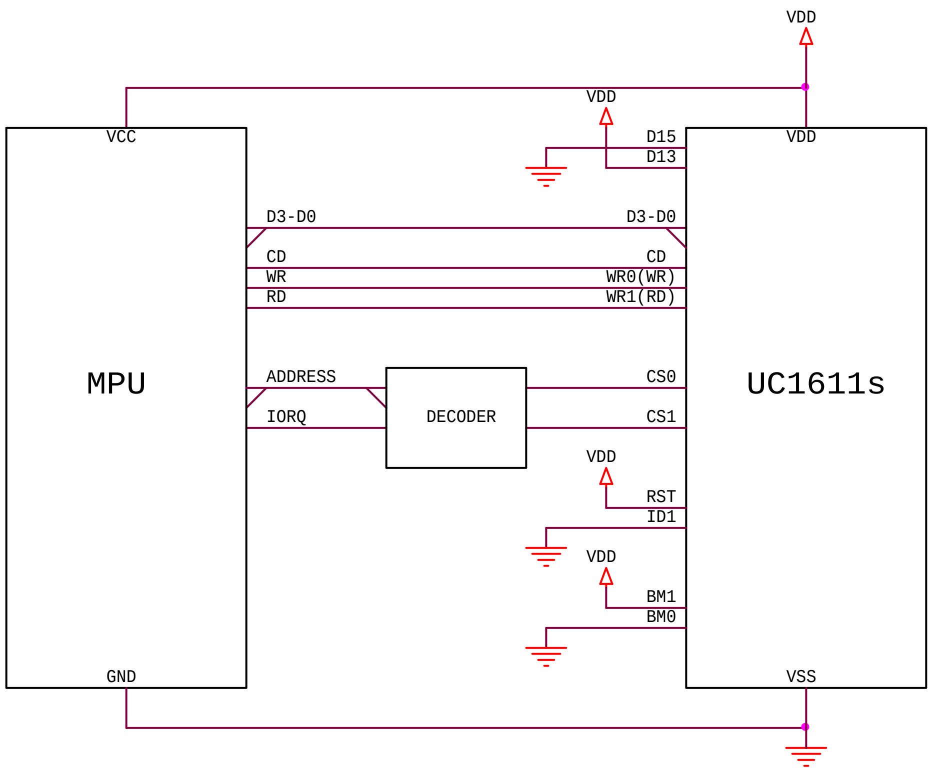


FIGURE 8: 8080/4-bit parallel mode reference circuit

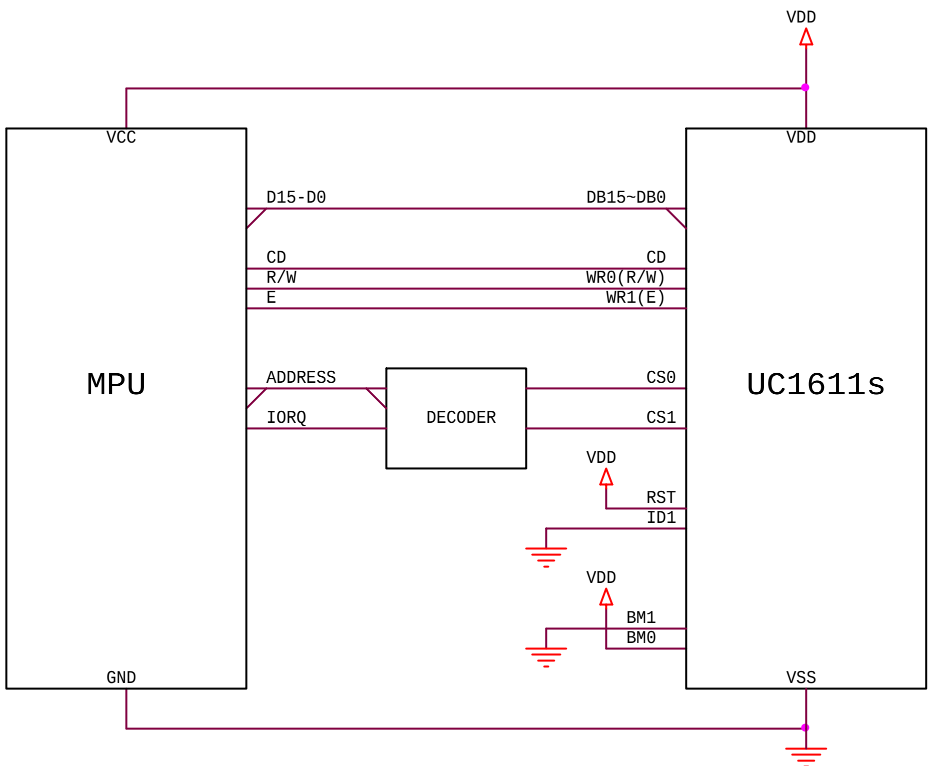


FIGURE 9: 6800/16-bit parallel mode reference circuit

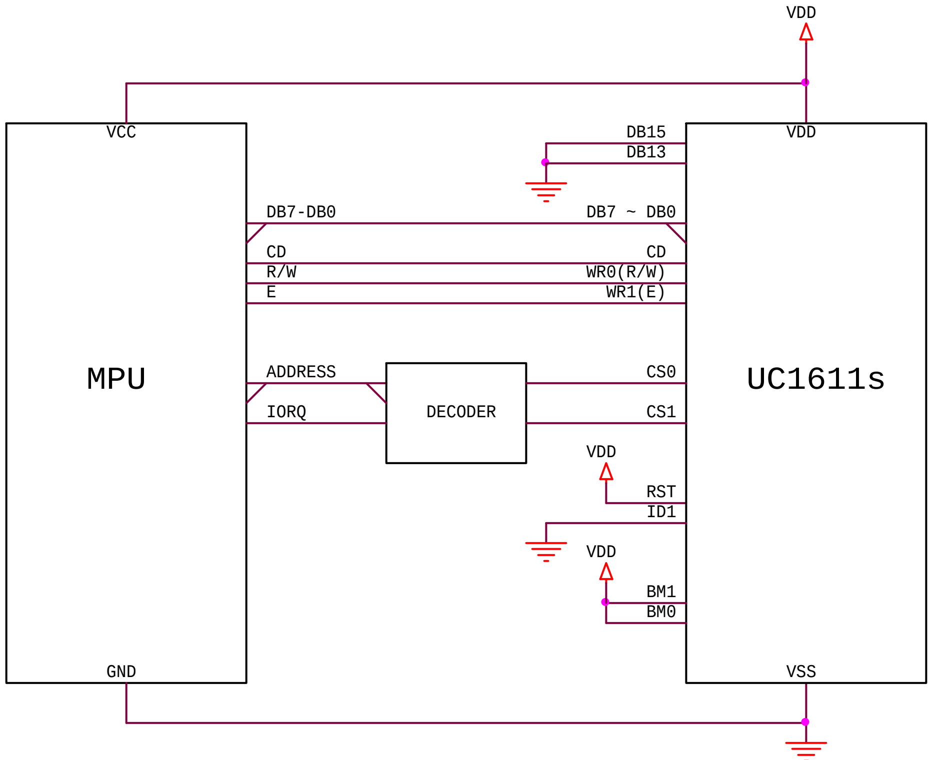


FIGURE 10: 6800/8-bit parallel mode reference circuit

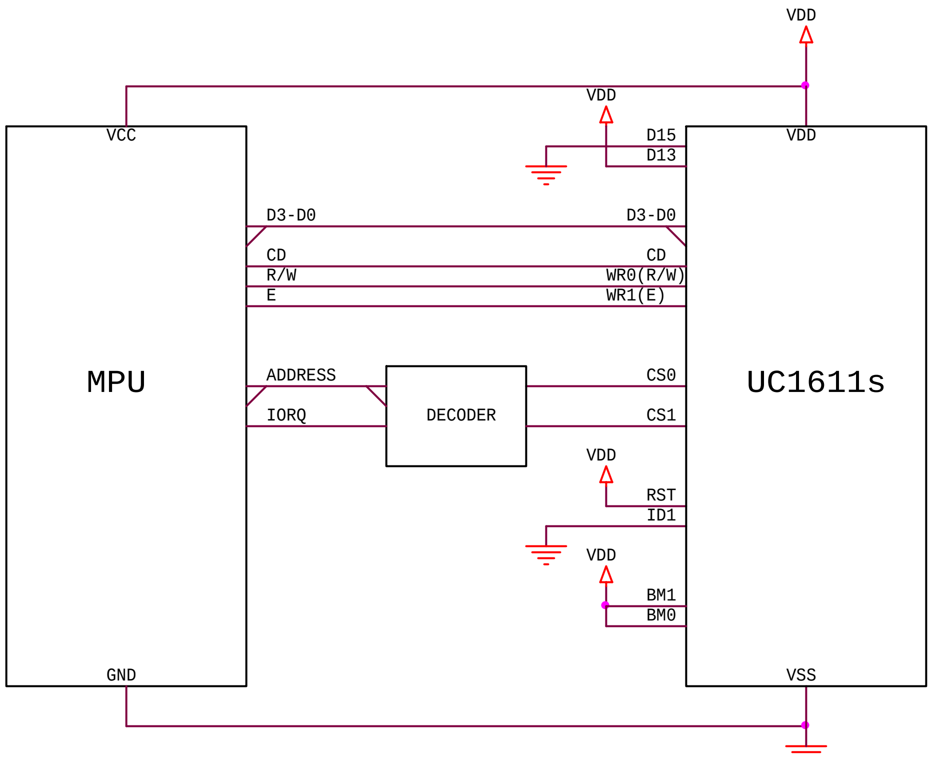


FIGURE 11: 6800/4-bit parallel mode reference circuit

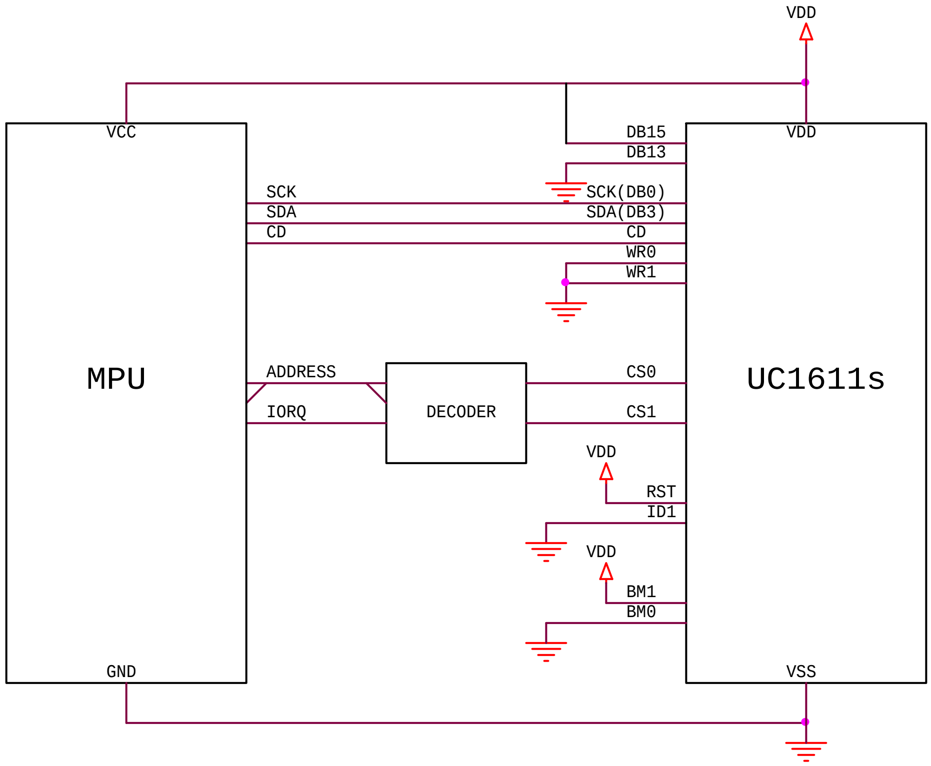


FIGURE 12: 4-Wire SPI (S8) serial mode reference circuit

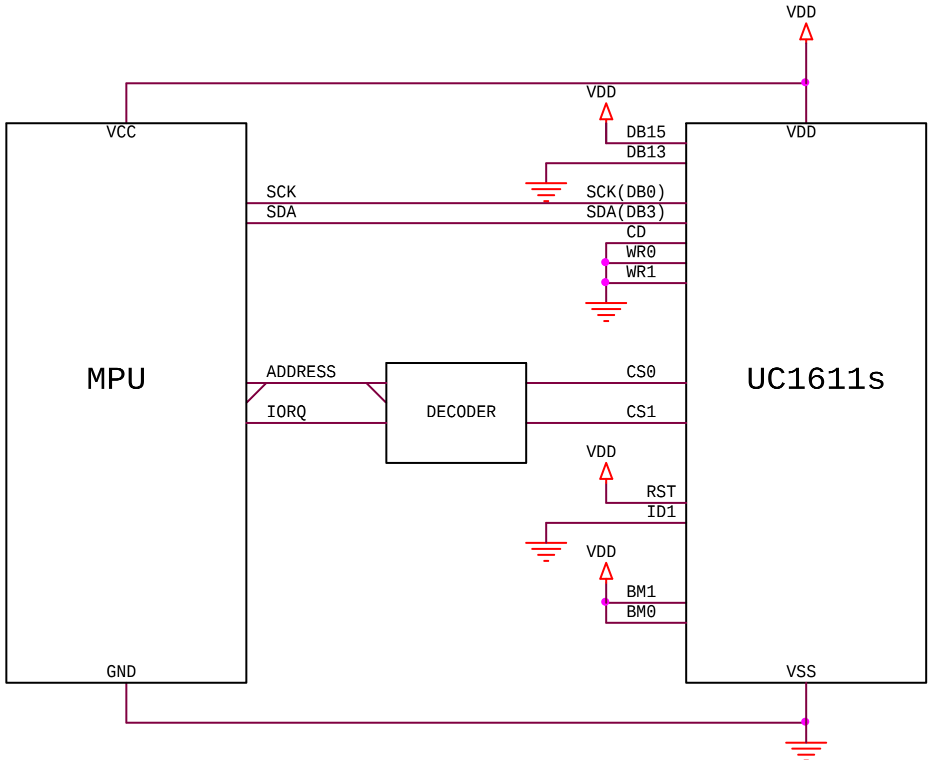


FIGURE 13: 3-Wire SPI (S9) serial mode reference circuit

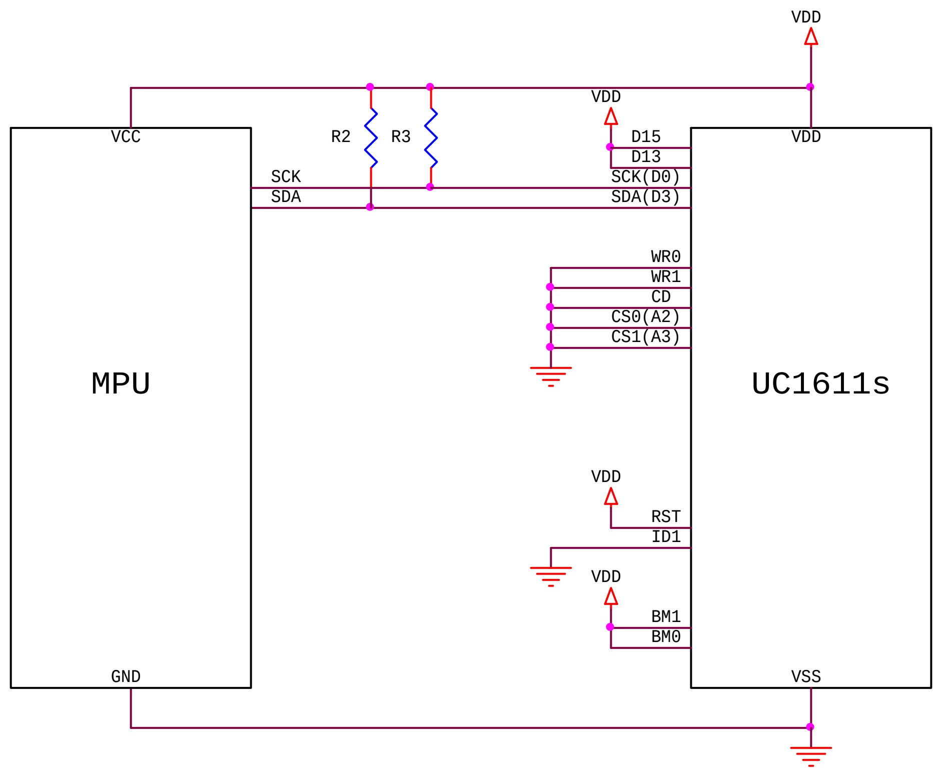


FIGURE 14: 2-Wire SPI (I^2C) serial mode reference circuit

Note:

1. RST pin is optional. When RST pin is not used, connect the pin to V_{DD}.
2. When using I^2C serial mode, CS1/0 are user configurable and affect A[3:2] of device address.
3. R1, R2: 2k ~ 10k Ω. Use lower resistor for bus speed up to 3.6MHz; while use higher resistor for lower power.

Display Data RAM

Data Organization

The display data is 4-bit per pixel and stored in a dual port SRAM. The SRAM is organized as 160x 256x4.

After setting CA and PA, the next data write cycle will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page for the relation between the COM, SEG, SRAM, and various memory control registers.

Display Data RAM Access

The Display RAM is a special purpose dual port RAM that allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

Display Data RAM Addressing

A Host Interface (HI) memory access operation starts with specifying Page Address (PA) and Column Address (CA) by issuing *Set Page Address* and *Set Column Address* commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the end of page (MC), and system programmers need to set the values of PA and CA explicitly.

If WA is ON (1), when CA reaches end of page, CA will be reset to 0 and PA will increment or decrement, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 79), PA will be wrapped around to the other end of RAM and continue.

MX Implementation

Column Mirroring (MX) is implemented by selecting either (CA) or (255–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect of the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

RAM Address Generation

The mapping of the data store in the display SRAM and the scanning electrodes can be obtained by combining the fixed COM scanning sequence and the following RAM address generation formula.

When FL=0, during the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field
Line = *SL*
Otherwise
Line = Mod (*Line* + 1, *160*)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the “loop around” effect as it effectively resets *Line* to 0 when *Line+1* reaches *160*. Effects such as page scrolling and page swapping can be emulated by changing SL dynamically.

MY Implementation

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field
Line = Mod(*SL + MUX - 1*, *160*)
where MUX is the Mux rate
Otherwise
Line = Mod(*Line - 1* , *160*)

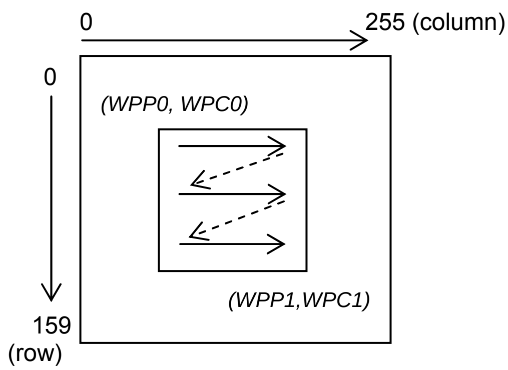
Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.

WINDOW PROGRAM

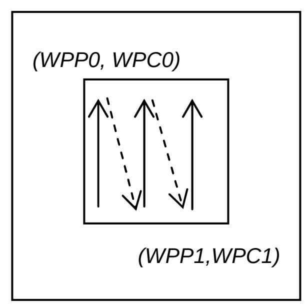
Window program is designed for data write in a specified window range of SRAM address. The procedure should start with window boundary registers setting (*WPP0*, *WPP1*, *WPC0* and *WPC1*) and then enable AC[3]. After AC[3] is set, data can be written to SRAM within the window address range which is specified by (*WPP0, WPC0*) and (*WPP1, WPC1*). AC[3] should be cleared after any modification of window boundary registers and then set again in order to initialize another window program.

The data write direction will be determined by AC[2:0] and MX settings. When AC[0]=1, the data write can be consecutive within the range of the specified window. AC[1] will control the data write in either column or row direction. AC[2] will result the data write starting either from row *WPP0* or WPP1. MX is for the initial column address either from *WPC0* to *WPC1* or from (*MC-WPC0* to *MC-WPC1*).

Example1:
AC[2:0] = 001 MX=0



Example 2:
AC[2:0] = 111 MX = 0



MSF 0	MSF 1	Line Adderss	RAM	MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=16
D3/0	D7/4	00H	Page 0	COM1	COM145	COM160	COM16
D7/4	D3/0	01H		COM2	COM146	COM159	COM15
D3/0	D7/4	02H	Page 1	COM3	COM147	COM158	COM14
D7/4	D3/0	03H		COM4	COM148	COM157	COM13
D3/0	D7/4	04H	Page 2	COM5	COM149	COM156	COM12
D7/4	D3/0	05H		COM6	COM150	COM155	COM11
D3/0	D7/4	06H	Page 3	COM7	COM151	COM154	COM10
D7/4	D3/0	07H		COM8	COM152	COM153	COM9
D3/0	D7/4	08H	Page 4	COM9	COM153	COM152	COM8
D7/4	D3/0	09H		COM10	COM154	COM151	COM7
D3/0	D7/4	0AH	Page 5	COM11	COM155	COM150	COM6
D7/4	D3/0	0BH		COM12	COM156	COM149	COM5
D3/0	D7/4	0CH	Page 6	COM13	COM157	COM148	COM4
D7/4	D3/0	0DH		COM14	COM158	COM147	COM3
D3/0	D7/4	0EH	Page 7	COM15	COM159	COM146	COM2
D7/4	D3/0	0FH		COM16	COM160	COM145	COM1
D3/0	D7/4	10H	Page 8	COM17	COM1	COM144	COM160
D7/4	D3/0	11H		COM18	COM2	COM143	COM159
D3/0	D7/4	12H	Page 9	COM19	COM3	COM142	COM158
D7/4	D3/0	13H		COM20	COM4	COM141	COM157
D3/0	D7/4	14H	Page 10	COM21	COM5	COM140	COM156
D7/4	D3/0	15H		COM22	COM6	COM139	COM155
D3/0	D7/4	16H	Page 11	COM23	COM7	COM138	COM154
D7/4	D3/0	17H		COM24	COM8	COM137	COM153
D3/0	D7/4	18H	Page 12	COM25	COM9	COM136	COM152
D7/4	D3/0	19H		COM26	COM10	COM135	COM151
D3/0	D7/4	1AH	Page 13	COM27	COM11	COM134	COM150
D7/4	D3/0	1BH		COM28	COM12	COM133	COM149
D3/0	D7/4	1CH	Page 14	COM29	COM13	COM132	COM148
D7/4	D3/0	1DH		COM30	COM14	COM131	COM147
D3/0	D7/4	1EH	Page 15	COM31	COM15	COM130	COM146
D7/4	D3/0	1FH		COM32	COM16	COM129	COM145
D3/0	D7/4	8CH	Page 70	COM141	COM125	COM20	COM36
D7/4	D3/0	8DH		COM142	COM126	COM19	COM35
D3/0	D7/4	8EH	Page 71	COM143	COM127	COM18	COM34
D7/4	D3/0	8FH		COM144	COM128	COM17	COM33
D3/0	D7/4	90H	Page 72	COM145	COM129	COM16	COM32
D7/4	D3/0	91H		COM146	COM130	COM15	COM31
D3/0	D7/4	92H	Page 73	COM147	COM131	COM14	COM30
D7/4	D3/0	93H		COM148	COM132	COM13	COM29
D3/0	D7/4	94H	Page 74	COM149	COM133	COM12	COM28
D7/4	D3/0	95H		COM150	COM134	COM11	COM27
D3/0	D7/4	96H	Page 75	COM151	COM135	COM10	COM26
D7/4	D3/0	97H		COM152	COM136	COM9	COM25
D3/0	D7/4	98H	Page 76	COM153	COM137	COM8	COM24
D7/4	D3/0	99H		COM154	COM138	COM7	COM23
D3/0	D7/4	9AH	Page 77	COM155	COM139	COM6	COM22
D7/4	D3/0	9BH		COM156	COM140	COM5	COM21
D3/0	D7/4	9CH	Page 78	COM157	COM141	COM4	COM20
D7/4	D3/0	9DH		COM158	COM142	COM3	COM19
D3/0	D7/4	9EH	Page 79	COM159	COM143	COM2	COM18
D7/4	D3/0	9FH		COM160	COM144	COM1	COM17

MX														
0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8		SEG236	SEG237	SEG238	SEG239	SEG240
1	SEG240	SEG239	SEG238	SEG237	SEG236	SEG235	SEG234	SEG233		SEG5	SEG4	SEG3	SEG2	SEG1

<u>When DC[5:3] = 0xxb :</u>

Example for memory mapping:
let MX = 0, MY = 0, SL = 0, MSF = 0, according to the data shown in the above table:

⇒ Page 0 SEG 1 : (D[7:0]) 0000 1111 b

⇒ Page 0 SEG 2 : (D[7:0]) 1111 0000 b

MSF 0	MSF 1	Line Adderss	RAM	MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=16
D0	D4	00H		COM1	COM145	COM160	COM16
D1	D5	01H		COM2	COM146	COM159	COM15
D2	D6	02H		COM3	COM147	COM158	COM14
D3	D7	03H	Page 0	COM4	COM148	COM157	COM13
D4	D0	04H		COM5	COM149	COM156	COM12
D5	D1	05H		COM6	COM150	COM155	COM11
D6	D2	06H		COM7	COM151	COM154	COM10
D7	D3	07H		COM8	COM152	COM153	COM9
D0	D4	08H		COM9	COM153	COM152	COM8
D1	D5	09H		COM10	COM154	COM151	COM7
D2	D6	0AH		COM11	COM155	COM150	COM6
D3	D7	0BH	Page 1	COM12	COM156	COM149	COM5
D4	D0	0CH		COM13	COM157	COM148	COM4
D5	D1	0DH		COM14	COM158	COM147	COM3
D6	D2	0EH		COM15	COM159	COM146	COM2
D7	D3	0FH		COM16	COM160	COM145	COM1
D0	D4	10H		COM17	COM1	COM144	COM160
D1	D5	11H		COM18	COM2	COM143	COM159
D2	D6	12H		COM19	COM3	COM142	COM158
D3	D7	13H	Page 2	COM20	COM4	COM141	COM157
D4	D0	14H		COM21	COM5	COM140	COM156
D5	D1	15H		COM22	COM6	COM139	COM155
D6	D2	16H		COM23	COM7	COM138	COM154
D7	D3	17H		COM24	COM8	COM137	COM153
D0	D4	18H		COM25	COM9	COM136	COM152
D1	D5	19H		COM26	COM10	COM135	COM151
D2	D6	1AH		COM27	COM11	COM134	COM150
D3	D7	1BH	Page 3	COM28	COM12	COM133	COM149
D4	D0	1CH		COM29	COM13	COM132	COM148
D5	D1	1DH		COM30	COM14	COM131	COM147
D6	D2	1EH		COM31	COM15	COM130	COM146
D7	D3	1FH		COM32	COM16	COM129	COM145
D0	D4	90H		COM145	COM129	COM16	COM32
D1	D5	91H		COM146	COM130	COM15	COM31
D2	D6	92H		COM147	COM131	COM14	COM30
D3	D7	93H	Page 18	COM148	COM132	COM13	COM29
D4	D0	94H		COM149	COM133	COM12	COM28
D5	D1	95H		COM150	COM134	COM11	COM27
D6	D2	96H		COM151	COM135	COM10	COM26
D7	D3	97H		COM152	COM136	COM9	COM25
D0	D4	98H		COM153	COM137	COM8	COM24
D1	D5	99H		COM154	COM138	COM7	COM23
D2	D6	9AH		COM155	COM139	COM6	COM22
D3	D7	9BH	Page 19	COM156	COM140	COM5	COM21
D4	D0	9CH		COM157	COM141	COM4	COM20
D5	D1	9DH		COM158	COM142	COM3	COM19
D6	D2	9EH		COM159	COM143	COM2	COM18
D7	D3	9FH		COM160	COM144	COM1	COM17

MX														
0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8		SEG236	SEG237	SEG238	SEG239	SEG240
1	SEG240	SEG239	SEG238	SEG237	SEG236	SEG235	SEG234	SEG233		SEG5	SEG4	SEG3	SEG2	SEG1

When DC[5:3]=100b :

Example for memory mapping:
Let MX = 0, MY = 0, SL = 0, MSF = 0, according to the data shown in the above table:

⇒ Page 0 SEG 1 : (D[7:0]) 0111 0000 b
⇒ Page 0 SEG 2 : (D[7:0]) 1011 0011 b

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1611s has two different types of Reset:
Power-ON-Reset and *System-Reset*.

Power-ON-Reset is performed right after V_{DD} is connected to power. *Power-On-Reset* will first wait for about 5~10mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

RESET STATUS

When UC1611s enters RESET sequence:

- Operation mode will be "Reset"
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1611s has 3 operating modes (OM):
Reset, Normal, Sleep.

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON-Reset, two commands will initiate OM transitions:

Set Display Enable, and *System Reset*.

When DC[2] is modified by `Set Display Enable`, OM will be updated automatically. There is no other action required to enter Sleep mode.

OM changes are synchronized with the edges of the IC's internal clock. To ensure consistent system states, wait at least 10µS after `Set Display Enable` or `System Reset` command.

Action	Mode	OM
Reset command RST_ pin pulled "L" Power-ON-Reset	Reset	00
Set Driver Enable to "0"	Sleep	10
Set Driver Enable to "1"	Normal	11

Table 5: OM changes

Both Reset mode and Sleep mode drain the charges stored in the external capacitors C_{B0}, C_{B1}, and C_L. When entering Reset mode or Sleep mode, the display drivers will be disabled.

The difference between Sleep mode and Reset mode is that, Reset mode clears all control registers and restores them to default values, while Sleep mode retains all the control registers values set by the user.

It is recommended to use Sleep Mode for Display OFF operations as the IC consumes very little energy in Sleep mode (typically under 1µA).

EXITING SLEEP MODE

UC1611s contains internal logic to check whether V_{LCD} are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset Mode, COM and SEG drivers will not be activated until UC1611s' internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

UC1611s power-up sequence is simplified by built-in "Power Ready" flags and the automatic invocation of *System-Reset* command after *Power-ON-Reset*.

System programmers are only required to wait 150 mS before the CPU starting to issue commands to UC1611s. No additional time sequences are required between enabling the charge pump, turning on the display drivers, writing to RAM or any other commands.

There's no delay needed while turning on V_{DD} and $V_{DD2/3}$, and either one can be turned on first.

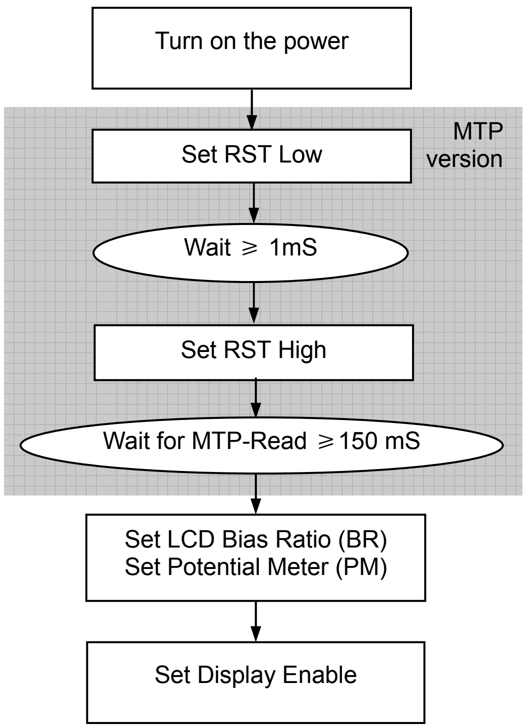


FIGURE 15: Reference Power-Up Sequence

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitor C_L from causing abnoraml residue horizontal line on display when V_{DD} is switched off, use Reset mode to enable the built-in charge draining circuit to discharge the external capacitor.

When internal V_{LCD} is not used, UC1611s will *NOT* drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD}.

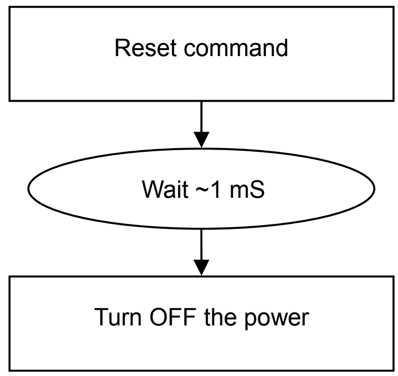


FIGURE 16: Reference Power-Down Sequence

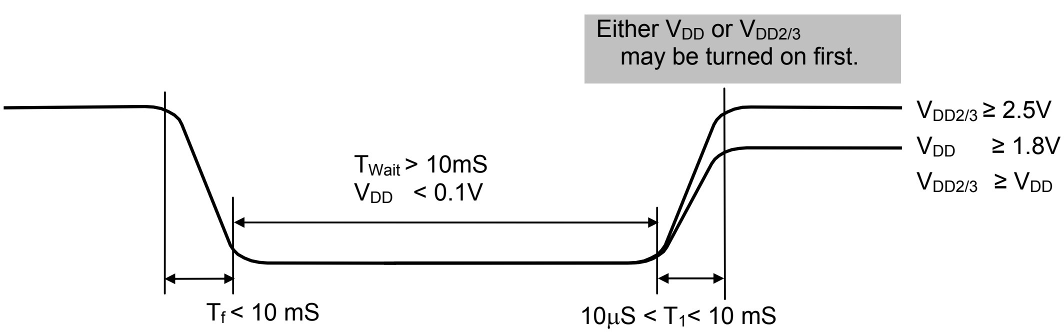


Figure 17: Delay allowance between V_{DD} and $V_{DD2/3}$

MULTI-TIME PROGRAM NV MEMORY

OVERVIEW

MTP feature is available for UC1611s such that LCM maker can record an PM offset value in non-volatile memory cells, which can then be used to adjust the effective V_{LCD} value, in order to achieve high level of consistency for LCM contrast across all shipments.

To accomplish this purpose, three operations are supported by UC1611s:
MTP-Erase, MTP-Program, MTP-Read.

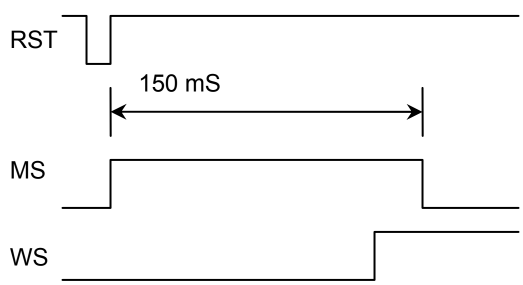
MTP-Program requires an external power source supplied to TST4 pin. MTP allows to program at least 10 times and should be performed only by the LCM makers.

MTP-Read is facilitated by the internal DC-DC converter built-in on UC1611s, no external power source is required, and it is performed automatically after hardware RESET (power-ON or pin RESET).

OPERATION FOR THE SYSTEM USERS

For the MTP version of UC1611s, the content of the NV memory will be read automatically after the power-on and hardware pin RESET. There is no user intervention or external power source required. When set up properly, the V_{LCD} will be fine tuned to achieve high level of consistency for the LCM contrast.

The MTP-READ is a relatively slow process and the time required can vary quite a bit. For a successful MTP-READ operation, the MS and WS bits in the *Read Status* commands will exhibit the following waveforms.



As illustrated above, the {MS, WS} will go through a {0,0}⇨{1,0}⇨{1,1}⇨{0,1} transition. When the {MS, WS}={0,1} state is reached, it means the LCM is ready to be turned on.

During the MTP-READ process, it is actually safe to issue commands or perform data write to the LCM. The only thing that is blocked is the LSB of the Set Display Enable command, which results in the DC[2] being effectively locked at “0” during this auto-MTP-READ process.

Although user can use *Read Status* command in a polling loop to make sure {MS,WS}={0,1} before proceeding with the Set Display Enable command, however, it may be simpler to just issue the Set Display Enable command every 0.2~2 second, repeatedly, together with other LCM optimization settings, such as BR, CEN, TC, etc.

The above “Periodical re-initializing” approach is also an effective safeguard against accidental display off events such as

- ESD strikes
- Mechanical shocks causing LCM connector to malfunction temporarily

HARDWARE VS. SOFTWARE RESET

The auto-MTP-READ is only performed for hardware RESET (power-ON and RST pin), but not for software *RESET* command. This enables the ICs to turn on display faster without the delay caused by MTP-READ.

It is recommended to use software *RESET* for normal operation control purpose and hardware RESET only during the event of power up and power down.

OPERATION FOR THE LCM MAKERS

Always ERASE the MTP NV memory cells, before starting the Write process.

MTP OPERATION FOR LCM MAKERS

1. High voltage supply and timer setting

In MTP Program operation, two different high voltages are needed. In chip design, one high voltage is generated by internal charge pump (V_{LCD}), the other high voltage must be input from TST4 by external voltage source.

V_{LCD} value is controlled by register MTP3 and MTP2. The default values of these two registers are appropriate for most applications.

External TST4 power source is required for MTP Program operation. MTP Programming speed depends on the TST4 voltage. Considering the ITO trace resistance in COG modules, it is recommended to program the MTP cells one at a time, so that the required 10V at TST4 can be maintained with proper consistency.

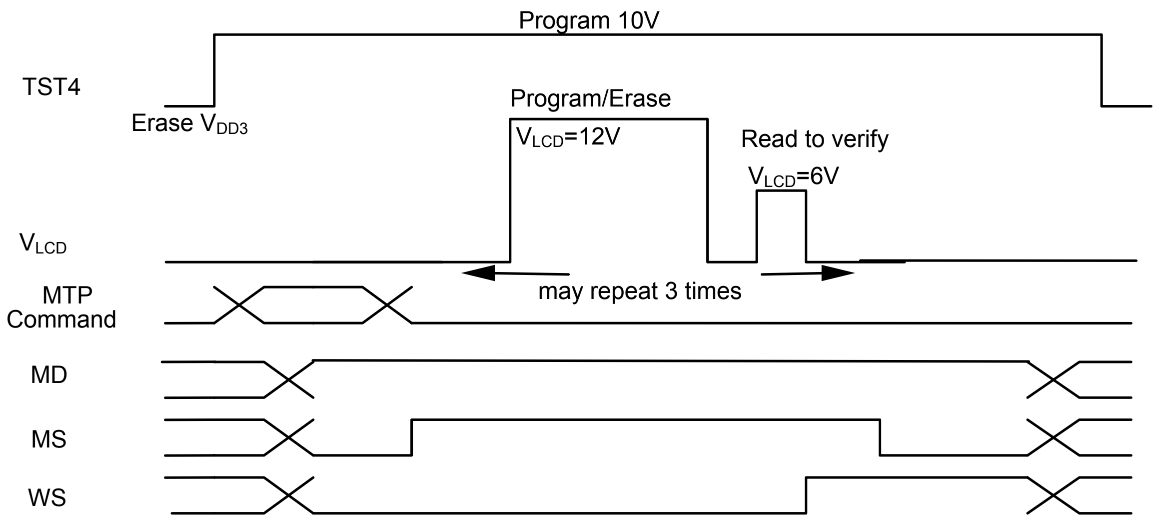
No external power source is required for MTP Erase and Read operation. For these MTP operation, TST4 should be open, or connected to V_{DD3}.

Operation	V_{LCD}	TST4 (external input)
Program	MTP3 : 15h (12V)	10V (1mA per bit)
Erase	MTP3 : 15h (12V)	Floating or V_{DD3}
Read	MTP2 : 69h (6V)	Floating or V_{DD3}

Note:
1. Do Erase before Program. Program one bit at a time.
2. When doing MTP Program or Erase, it's required to use $V_{DD2/3} \geqslant 3.0V$.

2. Read MTP status bits

With normal Get Status method (CD=0,W/R=1), MTP operation status can be monitored in the real time. There are 3 status bits (WS, MD, MS) in status register. MTP control circuit will read to verify if the operation (program, erase) success or not. If the operation succeeded, and current operation will be ended with WS=1. If it failed, last operation will be automatically retried two more times. If it fails 3 times, WS will be set to 0 and the operation is aborted. MD is MTP ID, which is either 1 for MTP IC. No transition.



MTP status bits, TST4 & V_{LCD} Waveform

MTP CELL VALUE USAGE

There are 6 MTP cell bits.

PMO[5:0] : V_{LCD} Trim
When PMO[5]=1: PM with trim = PM - PMO[4:0]
When PMO[5]=0: PM with trim = PM + PMO[4:0]

MTP COMMAND SEQUENCE SAMPLE CODES

The following tables are examples of command sequence for MTP Program and Erase operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

MTP operations (Erase, Program, Read) and Set Display ON is mutual exclusive. There is no harm done to the IC or the LCM if this is violated. However, the violating commands will be ignored.

Type Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

(1) MTP Program Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip Action	Comments
R	–	–	–	–	–	–	–	–	–	–	Set RST pin Low	Wait 1mS after RST is Low
R	–	–	–	–	–	–	–	–	–	–	Set RST pin High	
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset.	Wait ~150mS
R	0	0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[5:4]=11b
R	0	0	1	1	1	1	0	1	0	0	Set V_{MTP1} Potentiometer	Set MTP V_{LCD}
R	0	0	0	1	1	0	1	0	0	1		MTP2: 69h(6V)
R	0	0	1	1	1	1	0	1	0	1	Set V_{MTP2} Potentiometer	Set MTP V_{LCD}
R	0	0	0	0	1	0	0	1	0	1		MTP3: 25h(12V)
R	0	0	1	1	1	1	0	1	1	0	Set MTP Write Timer	Set MTP Timer
R	0	0	0	0	1	0	0	1	0	1		MTP4:25h(100mS)
R	0	0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	0	1	0	1		MTP5:05h(10mS)
R	0	0	1	0	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C	0	0	0	0	0	0	0	0	0	1	MTPM	Ex: To program PMO[5:0], set MTPM *
R	-	-	-	-	-	-	-	-	-	-		Apply TST4 voltage Program: 10V
R	0	0	1	0	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
R	0	0	-	-	0	0	1	0	1	1		Set MTPC[2:0]=011
R	0	1	-	-	-	-	-	ws	-	MS	Get Status & PM	Check MTP Status until MS=0 and WS=1
R												Remove TST4 voltage
R											V_{DD}=0V	Power OFF

* It is recommended that users program one bit at a time.

(2) MTP Erase Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Set RST pin Low	Wait 1mS after RST is Low
R	–	–	–	–	–	–	–	–	–	–	Set RST pin High	
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset.	Wait ~150mS
R	0	0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[5:4]=11b
R	0	0	1	1	1	1	0	1	0	0	Set V_{MTP1} Potentiometer	Set MTP V_{LCD}
R	0	0	0	1	1	0	1	0	0	1		MTP2: 69h(6V)
R	0	0	1	1	1	1	0	1	0	1	Set V_{MTP2} Potentiometer	Set MTP V_{LCD}
R	0	0	0	0	1	0	0	1	0	1		MTP3: 25h(12V)
R	0	0	1	1	1	1	0	1	1	0	Set MTP Write Timer	Set MTP Timer
R	0	0	0	0	1	0	0	1	0	1		MTP4:25h(100mS)
R	0	0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	0	1	0	1		MTP5:05h(10mS)
R	0	0	1	0	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C	0	0	0	1	1	1	1	1	1	1	MTPM	Ex: To erase PMO[5:0] , set MTPM
R	0	0	1	0	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
R	0	0	-	-	0	0	1	0	1	0		Set MTPC[2:0]=010
R	0	1	-	-	-	-	-	ws	-	MS	Get Status & PM	Check MTP Status
												until MS=0 WS=1
R											V_{DD}=0V	Power OFF

* It is recommended that users clear all the bits to be programmed.

SAMPLE COMMAND SEQUENCES

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

Type
- Required: These items are required
- Customized: These items are not necessary, if customer parameters are the same as default
- Advanced: We recommend new users to skip these commands and use default values.
- Optional: These commands depend on what users want to do.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)
W/R The direction of data-flow of the cycle. It can be either Write (0) or Read (1).

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Turn on V_{DD} and $V_{DD2/3}$	Wait until V_{DD} and $V_{DD2/3}$ are stable
R	–	–	–	–	–	–	–	–	–	–	Set RST pin Low	Wait 1mS after RST is Low
R	–	–	–	–	–	–	–	–	–	–	Set RST pin High	
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset.	Wait ~150mS
C	0	0	0	0	1	0	0	1	#	#	Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, etc.
C	0	0	1	1	0	0	0	0	0	0	Set LCD Mapping Control	
C	0	0	0	0	0	0	#	#	#	#		
A	0	0	1	0	1	0	0	0	#	#	Set Line Rate	Fine tune for power, flicker, contrast, and shading.
C	0	0	1	1	1	0	1	0	#	#	Set LCD Bias Ratio	LCD specific operating voltage setting
R	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set Gain and PM	
O	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	System Reset	
R	–	–	–	–	–	–	–	–	–	–	Draining capacitor	Wait ~1mS before V_{DD} OFF

DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	0	0	0	Set Display Disable	
O	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image. (Image update is optional. Data in the RAM is retained through the SLEEP state.)
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

ESD Consideration

1. UC1600 series products usually are provided in bare die format to customers. This makes the product particularly sensitive to ESD damage during handling and manufacturing process. It is therefore highly recommended that LCM makers strictly follow the "JESD 625-A Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices" when manufacturing LCM.

   In particular, the following pins in UC1611s require special "ESD Sensitivity" consideration, please refer to Table below. According to UltraChip's Mass Production experience, the following ESD tolerance conditions has been shown be very stable and produce high yield in multiple customer sites. However, special care is still required during handling and manufacturing process to avoid unnecessary yield loss due to ESD damages.

Test Mode		Machine Mode		Human Body Mode	
		V_{DD}	V_{SS}	V_{DD}	V_{SS}
LCD Driver		200V	200V	2000V	2500V
LCM Interface		300V	300V	3000V	3000V
LCM HV pin/ Test pin	TST1/2/4	300V	300V	3000V	3000V
	CB pins	300V	300V	3000V	3000V
	V_{LCDIN}	300V	300V	3000V	3000V
	V_{LCDOUT}	300V	300V	3000V	3000V
PWR / GND		-	300V	-	3000V

   * MM: Machine Mode

2. LCM design suggestions: To minimize potential ESD damages in assembly LCD modules(COG or COF) and modules test , please consider placing external components (C_{VLCD}, and C_{B0},C_{B1}) in such a way that they will not be exposed to Machine Mode ESD zap path. For example, place C_{VLCD} and C_B capacitors on the internal side after folding FPC.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134, note 1, 2 and 3.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}$-V_{DD}	Voltage difference between V_{DD} and $V_{DD2/3}$	--	2.0	V
V_{LCD}	LCD Generated voltage (-30^{O}C ~ +80^{O}C)	-0.3	+19.8	V
V_{IN}	Digital input voltage	-0.4	V_{DD} + 0.5	V
T_{OPR}	Operating temperature range	-30	+85	^{o}C
T_{STR}	Storage temperature	-55	+125	^{o}C

Note:
1. V_{DD} is based on V_{SS} = 0V
2. Stress above values listed may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		1.65	1.8~3.3	3.6	V
$V_{DD2/3}$	Supply for bias & pump		2.7	2.8~3.3	3.6	V
V_{LCD}	Charge pump output	$V_{DD2/3} \geqslant 2.4V, 25^{O}C$		17	17.5	V
V_D	LCD data voltage	$V_{DD2/3} \geqslant 2.4V, 25^{O}C$			1.69	V
V_{IL}	Input logic LOW				$0.2V_{DD}$	V
V_{IH}	Input logic HIGH		$0.8V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	μA
C_{IN}	Input capacitance			5	10	pF
C_{OUT}	Output capacitance			5	10	pF
$R_{0(SEG)}$	SEG output impedance	V_{LCD} = 17V		1.35	2.5	k Ω
$R_{0(COM)}$	COM output impedance	V_{LCD} = 17V		1.35	2.5	k Ω
f_{LINE}	Average Line rate	LC[5:4] = 10b	-10%	28	+10%	kHz

POWER CONSUMPTION

V_{DD} = 2.7 V, V_{LCD} = 17.01 V, Mux Rate = 160, C_B = 5 μF, Bias Ratio = 11, Line Rate = 10 b, Bus mode = 6800, Temperature = 25 ^{o}C, PM = 234, Panel Loading (PC[1:0]) = 11 b, C_L = 500 nF, MTP= 00 H,
All HV outputs are open circuit.

Display Pattern	Conditions	Typ. (μA)	Max. (μA)
All-OFF	Bus = idle	1656	2484
2-pixel checker	Bus = idle	2031	3046
--	Bus = idle (standby current)	--	5

AC CHARACTERISTICS

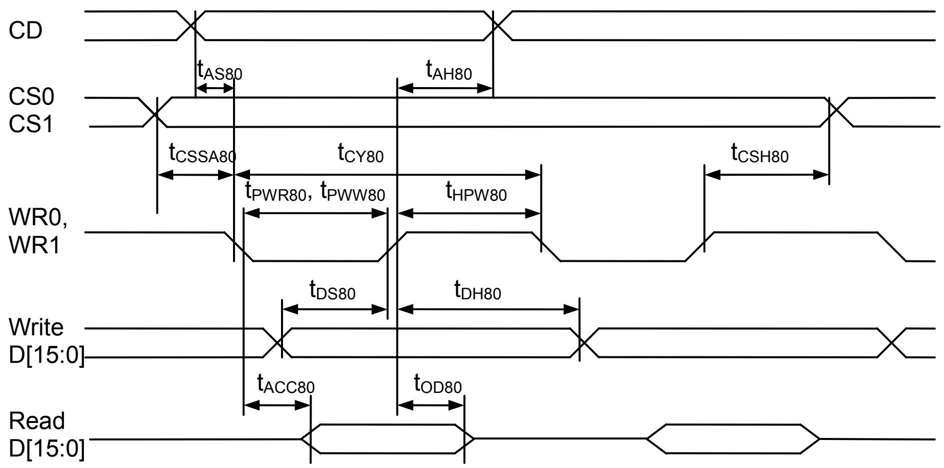


FIGURE 18: Parallel Bus Timing Characteristics (for 8080 MCU)

(2.5V $\leqslant$ V_{DD} < 3.6V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min. (nS)	Max.(nS)
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 0	–
t_{CY80}		System cycle time 16-bit bus 8-bit bus 4-bit bus	(Read / Write)	410 / 330 150 / 130 100 / 70	–
t_{PWR80} t_{PWW80}	WR1, WR0	Low Pulse width 16-bit bus 8-bit bus 4-bit bus	(Read / Write)	205 / 165 75 / 65 50 / 35	–
t_{HPW80}	WR1, WR0	High pulse width 16-bit bus 8-bit bus 4-bit bus	(Read / Write)	205 / 165 75 / 65 50 / 35	–
t_{DS80} t_{DH80}	D15~D0	Data setup time Data hold time		30 0	–
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 30	60 –
t_{SSA80} t_{CSH80}	CS1/CS0	Chip select setup time		0 0	

(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min. (nS)	Max. (nS)
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 0	–
t_{CY80}		System cycle time 16-bit bus 8-bit bus 4-bit bus	(Read / Write)	800 / 600 300 / 260 200 / 140	–
t_{PWR80} t_{PWW80}	WR1 WR0	Low Pulse width 16-bit bus 8-bit bus 4-bit bus	(Read / Write)	400 / 300 150 / 130 100 / 70	–
t_{HPW80}	WR1, WR0	High pulse width 16-bit bus 8-bit bus 4-bit bus	(Read / Write)	400 / 300 150 / 130 100 / 70	–
t_{DS80} t_{DH80}	D15~D0	Data setup time Data hold time		60 0	–
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 50	120 –
t_{SSA80} t_{CSH80}	CS1/CS0	Chip select setup time		0 0	

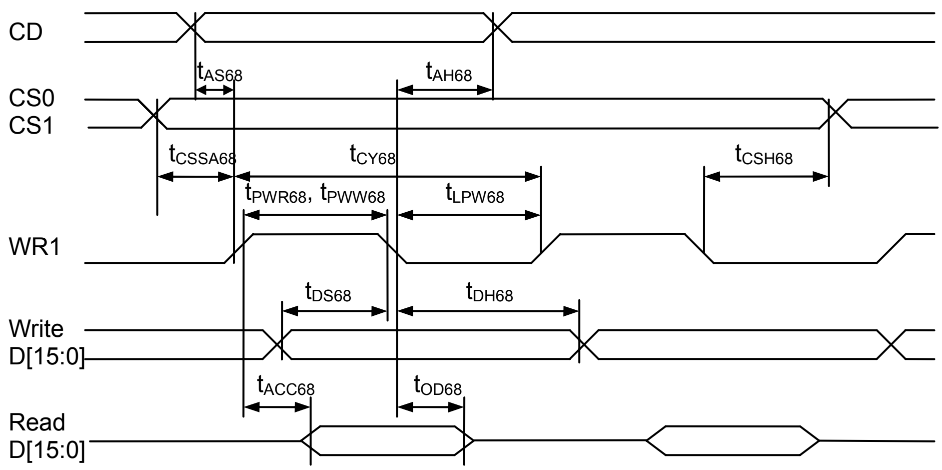


FIGURE 19: Parallel Bus Timing Characteristics (for 6800 MCU)

(2.5V ≤ V_{DD} < 3.6V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min. (nS)	Max. (nS)
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–
t_{CY68}		System cycle time 16-bit bus 8-bit bus 4-bit bus	(Read / Write)	410 / 330 150 / 130 100 / 70	–
t_{PWR68} t_{PWW68}	WR1, WR0	Low Pulse width 16-bit bus 8-bit bus 4-bit bus	(Read / Write)	205 / 165 75 / 65 50 / 35	–
t_{LPW68}	WR1, WR0	High Pulse width 16-bit bus 8-bit bus 4-bit bus	(Read / Write)	205 / 165 75 / 65 50 / 35	–
t_{DS68} t_{DH68}	D15~D0	Data setup time Data hold time		30 0	–
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 30	60 –
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time		0 0	

(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min. (nS)	Max. (nS)
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–
t_{CY68}		System cycle time 16-bit bus 8-bit bus 4-bit bus	(Read / Write)	800 / 600 300 / 260 200 / 140	–
t_{PWR68} t_{PWW68}	WR1, WR0	High Pulse width 16-bit bus 8-bit bus 4-bit bus	(Read / Write)	400 / 300 150 / 130 100 / 70	–
t_{LPW68}	WR1, WR0	Low pulse width 16-bit bus 8-bit bus 4-bit bus	(Read / Write)	400 / 300 150 / 130 100 / 70	–
t_{DS68} t_{DH68}	D15~D0	Data setup time Data hold time		60 0	–
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 50	120 –
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time		0 0	

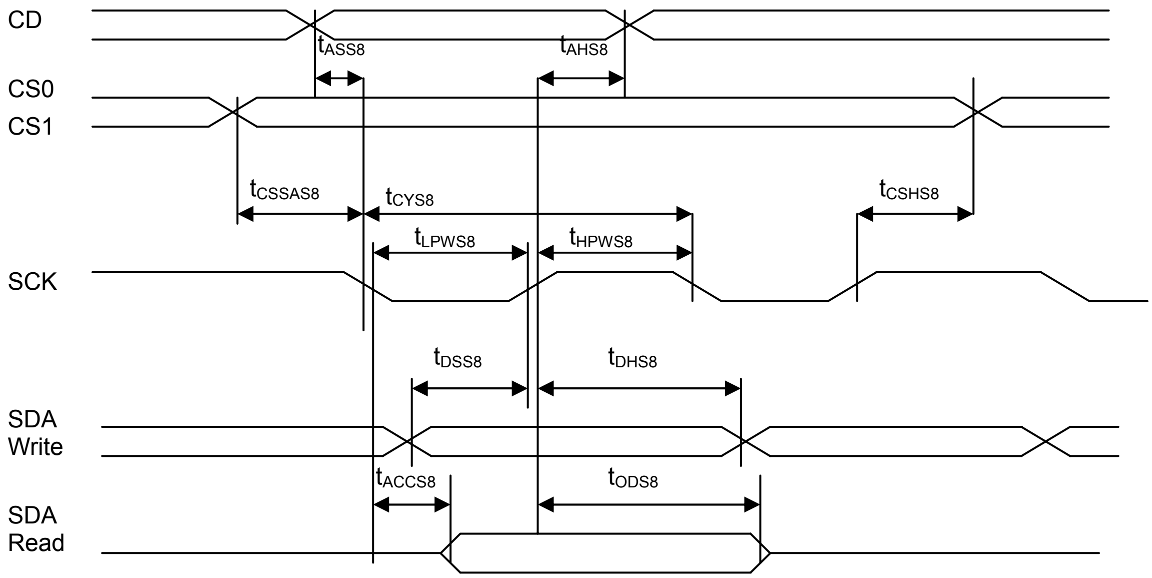


FIGURE 20: Serial Bus Timing Characteristics (for S8)

(2.5V ≤ V_{DD} < 3.6V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min. (nS)	Max. (nS)
t_{ASS8} t_{AHS8}	CD	Address setup time Address hold time		0 0	– –
t_{CYS8} t_{LPWS8} t_{HPWS8}	SCK	System cycle time Low pulse width High pulse width	(Read / Write)	120 / 36 60 / 18 60 / 18	– – –
t_{ACCS8} t_{ODS8}		Read access time Output disable time	(Read)	– 15	50 –
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time	(Write)	15 0	– –
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time	(Read / Write)	0 / 0 0 / 0	

(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min. (nS)	Max. (nS)
t_{ASS8} t_{AHS8}	CD	Address setup time Address hold time		0 0	– –
t_{CYS8} t_{LPWS8} t_{HPWS8}	SCK	System cycle time Low pulse width High pulse width	(Read / Write)	240 / 60 120 / 30 120 / 30	– – –
t_{ACCS8} t_{ODS8}		Read access time Output disable time	(Read)	– 30	90 –
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time	(Write)	30 5	–
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time	(Read / Write)	0 / 0 0 / 0	