

SSD1803A

Advance Information

100 x 34 STN LCD Segment / Common Mono Driver with Controller

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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SSD1803A | Rev 2.0 | P 1/69 | May 2011 |

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Appendix: IC Revision history of SSD1803A Specification

Version	Change Items	Effective Date
1.0	1 st Release	17-Aug-10
2.0	P.40 Added ROM selection command P.50 Added ROM selection command description	17-Jun-11

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5-dot font width

Display Line Numbers	Duty Ratio	Single-chip Operation	
		Displayable Characters	Possible Icons
1	1/9	1 line of 20 characters	80
2	1/17	2 lines of 20 characters	80
3	1/25	3 lines of 20 characters	80
4	1/33	4 line of 20 characters	80

6-dot font width

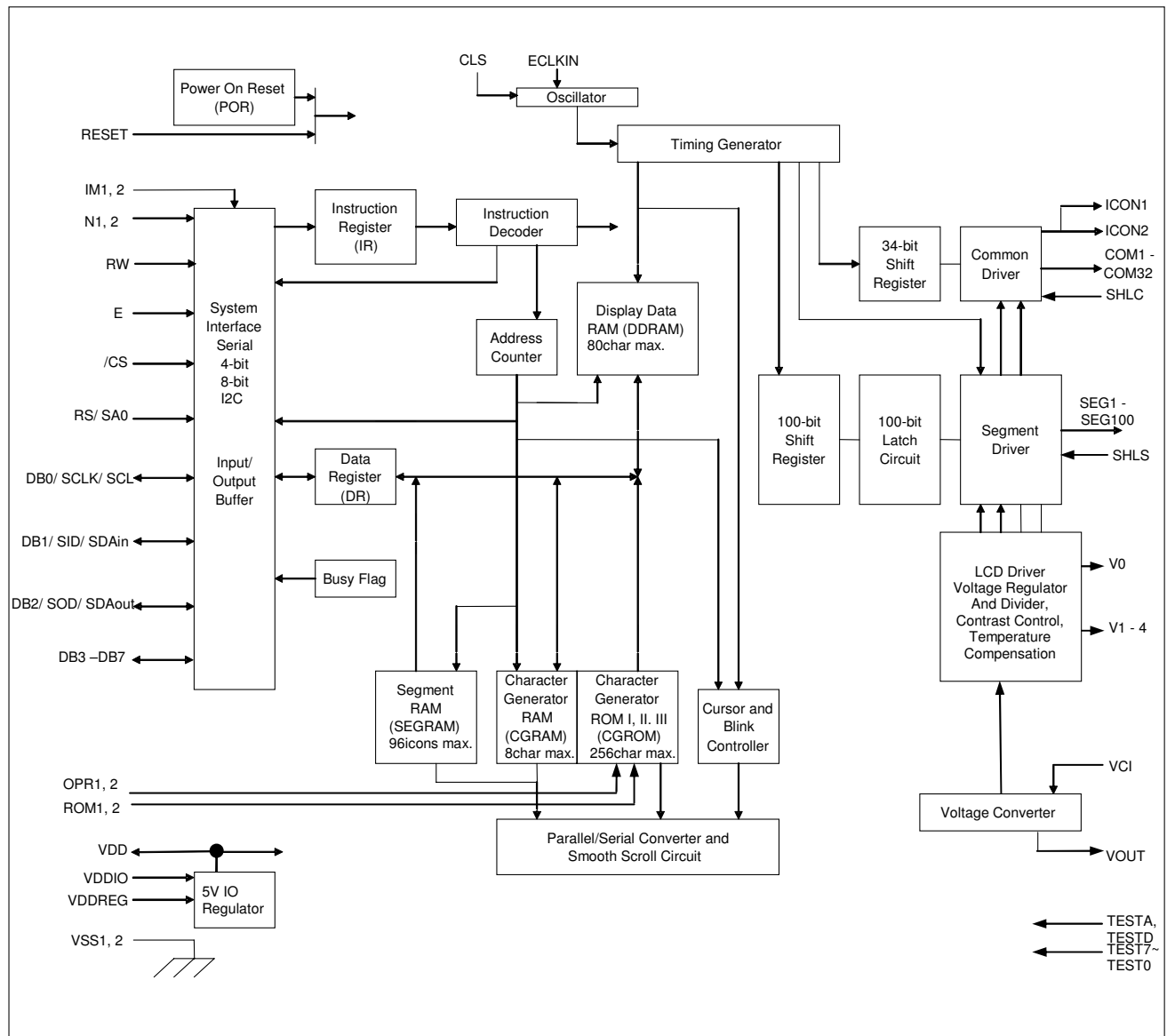
Display Line Numbers	Duty Ratio	Single-chip Operation	
		Displayable Characters	Possible Icons
1	1/9	1 line of 16 characters	96
2	1/17	2 lines of 16 characters	96
3	1/25	3 line of 16 characters	96
4	1/33	4 line of 16 characters	96

3 ORDERING INFORMATION**Table 3-1: Ordering Information**

Ordering Part Number	CGROM	Package Form	Reference	Remark
SSD1803AM1Z	A, B, C	COG	Figure 5-1 on P.10	-

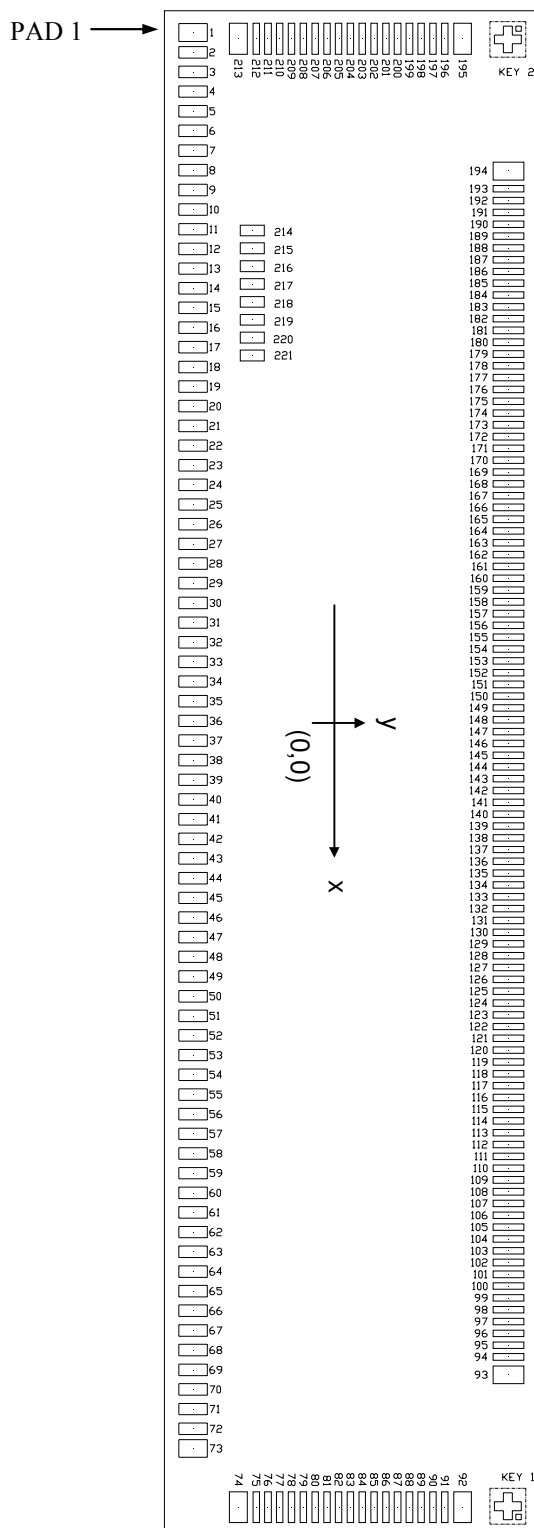
4 BLOCK DIAGRAM

Figure 4-1: SSD1803A Block Diagram



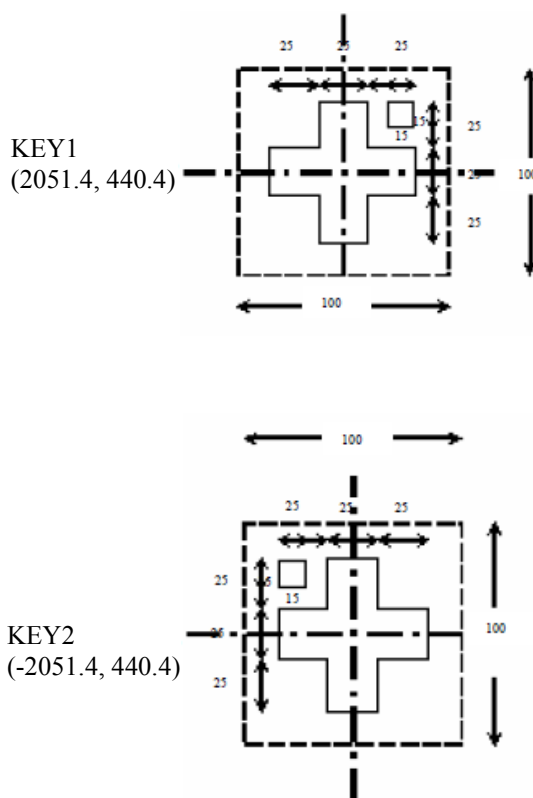
5 DIE PAD FLOOR PLAN

Figure 5-1: SSD1803A Die Pad Floor Plan



Note

- (1) Diagram showing the die face up, input on left hand side, output on right hand side.
- (2) Coordinates are referenced to center of the chip.
- (3) Coordinate units and size of all alignment marks are in μm .
- (4) All alignment keys do not contain gold bump.



Die Size (after sawing)	4264 $\pm$ 50 μm X 1042 $\pm$ 50 μm
Die Thickness	300 $\pm$ 25 μm
Typical Bump Height	12 μm
Bump Co-planarity (within die)	$\leq$ 3 μm

Note: IC material temperature expansion factor is 2.6ppm,
Customers should take into account during panel design.

Table 5-1: SSD1803A Bump Die Pad Coordinates (Bump center)

Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
1	VSS1	-2070.5	-440.5	49	VOUT	569.5	-440.5
2	V0	-2015.5	-440.5	50	VDDIO	624.5	-440.5
3	V0	-1960.5	-440.5	51	IM1	679.5	-440.5
4	V0	-1905.5	-440.5	52	IM2	734.5	-440.5
5	RESET	-1850.5	-440.5	53	VSS1	789.5	-440.5
6	ECLKIN	-1795.5	-440.5	54	CLS	844.5	-440.5
7	RS/SA0	-1740.5	-440.5	55	V4	899.5	-440.5
8	/CS	-1685.5	-440.5	56	V3	954.5	-440.5
9	RW	-1630.5	-440.5	57	V2	1009.5	-440.5
10	E	-1575.5	-440.5	58	V1	1064.5	-440.5
11	DB0/SCLK/SCL	-1520.5	-440.5	59	V0	1119.5	-440.5
12	DB1/SID/SDAin	-1465.5	-440.5	60	V0	1174.5	-440.5
13	DB2/SOD/SDAout	-1410.5	-440.5	61	V0	1229.5	-440.5
14	DB0/SCLK/SCL	-1355.5	-440.5	62	VOUT	1284.5	-440.5
15	DB3	-1300.5	-440.5	63	VOUT	1339.5	-440.5
16	DB4	-1245.5	-440.5	64	VOUT	1394.5	-440.5
17	DB5	-1190.5	-440.5	65	VOUT	1449.5	-440.5
18	DB6	-1135.5	-440.5	66	V0	1504.5	-440.5
19	DB7	-1080.5	-440.5	67	V0	1559.5	-440.5
20	VDD	-1025.5	-440.5	68	V1	1614.5	-440.5
21	VDD	-970.5	-440.5	69	V2	1669.5	-440.5
22	VSS1	-915.5	-440.5	70	V3	1724.5	-440.5
23	VSS2	-860.5	-440.5	71	V4	1779.5	-440.5
24	OPR1	-805.5	-440.5	72	RESET	1834.5	-440.5
25	OPR2	-750.5	-440.5	73	VSS1	1889.5	-440.5
26	VDDIO	-695.5	-440.5	74	Dummy	2053.4	-314
27	VDDIO	-640.5	-440.5	75	com24	2053.4	-264
28	ROM1	-585.5	-440.5	76	com23	2053.4	-231
29	ROM2	-530.5	-440.5	77	com22	2053.4	-198
30	VSS1	-475.5	-440.5	78	com21	2053.4	-165
31	SHLC	-420.5	-440.5	79	com20	2053.4	-132
32	SHLS	-365.5	-440.5	80	com19	2053.4	-99
33	VDDIO	-310.5	-440.5	81	com18	2053.4	-66
34	VDDIO	-255.5	-440.5	82	com17	2053.4	-33
35	VDDREG	-200.5	-440.5	83	com8	2053.4	0
36	VSS1	-145.5	-440.5	84	com7	2053.4	33
37	N1	-90.5	-440.5	85	com6	2053.4	66
38	N2	-35.5	-440.5	86	com5	2053.4	99
39	TESTD	19.5	-440.5	87	com4	2053.4	132
40	VDDIO	74.5	-440.5	88	com3	2053.4	165
41	VDD	129.5	-440.5	89	com2	2053.4	198
42	VDD	184.5	-440.5	90	com1	2053.4	231
43	VCI	239.5	-440.5	91	ICON1	2053.4	264
44	VCI	294.5	-440.5	92	Dummy	2053.4	314
45	TESTA	349.5	-440.5	93	Dummy	1683.5	442.4
46	VOUT	404.5	-440.5	94	seg1	1633.5	442.4
47	VOUT	459.5	-440.5	95	seg2	1600.5	442.4
48	VOUT	514.5	-440.5	96	seg3	1567.5	442.4

Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
97	seg4	1534.5	442.4	145	seg52	-49.5	442.4
98	seg5	1501.5	442.4	146	seg53	-82.5	442.4
99	seg6	1468.5	442.4	147	seg54	-115.5	442.4
100	seg7	1435.5	442.4	148	seg55	-148.5	442.4
101	seg8	1402.5	442.4	149	seg56	-181.5	442.4
102	seg9	1369.5	442.4	150	seg57	-214.5	442.4
103	seg10	1336.5	442.4	151	seg58	-247.5	442.4
104	seg11	1303.5	442.4	152	seg59	-280.5	442.4
105	seg12	1270.5	442.4	153	seg60	-313.5	442.4
106	seg13	1237.5	442.4	154	seg61	-346.5	442.4
107	seg14	1204.5	442.4	155	seg62	-379.5	442.4
108	seg15	1171.5	442.4	156	seg63	-412.5	442.4
109	seg16	1138.5	442.4	157	seg64	-445.5	442.4
110	seg17	1105.5	442.4	158	seg65	-478.5	442.4
111	seg18	1072.5	442.4	159	seg66	-511.5	442.4
112	seg19	1039.5	442.4	160	seg67	-544.5	442.4
113	seg20	1006.5	442.4	161	seg68	-577.5	442.4
114	seg21	973.5	442.4	162	seg69	-610.5	442.4
115	seg22	940.5	442.4	163	seg70	-643.5	442.4
116	seg23	907.5	442.4	164	seg71	-676.5	442.4
117	seg24	874.5	442.4	165	seg72	-709.5	442.4
118	seg25	841.5	442.4	166	seg73	-742.5	442.4
119	seg26	808.5	442.4	167	seg74	-775.5	442.4
120	seg27	775.5	442.4	168	seg75	-808.5	442.4
121	seg28	742.5	442.4	169	seg76	-841.5	442.4
122	seg29	709.5	442.4	170	seg77	-874.5	442.4
123	seg30	676.5	442.4	171	seg78	-907.5	442.4
124	seg31	643.5	442.4	172	seg79	-940.5	442.4
125	seg32	610.5	442.4	173	seg80	-973.5	442.4
126	seg33	577.5	442.4	174	seg81	-1006.5	442.4
127	seg34	544.5	442.4	175	seg82	-1039.5	442.4
128	seg35	511.5	442.4	176	seg83	-1072.5	442.4
129	seg36	478.5	442.4	177	seg84	-1105.5	442.4
130	seg37	445.5	442.4	178	seg85	-1138.5	442.4
131	seg38	412.5	442.4	179	seg86	-1171.5	442.4
132	seg39	379.5	442.4	180	seg87	-1204.5	442.4
133	seg40	346.5	442.4	181	seg88	-1237.5	442.4
134	seg41	313.5	442.4	182	seg89	-1270.5	442.4
135	seg42	280.5	442.4	183	seg90	-1303.5	442.4
136	seg43	247.5	442.4	184	seg91	-1336.5	442.4
137	seg44	214.5	442.4	185	seg92	-1369.5	442.4
138	seg45	181.5	442.4	186	seg93	-1402.5	442.4
139	seg46	148.5	442.4	187	seg94	-1435.5	442.4
140	seg47	115.5	442.4	188	seg95	-1468.5	442.4
141	seg48	82.5	442.4	189	seg96	-1501.5	442.4
142	seg49	49.5	442.4	190	seg97	-1534.5	442.4
143	seg50	16.5	442.4	191	seg98	-1567.5	442.4
144	seg51	-16.5	442.4	192	seg99	-1600.5	442.4

Pad #	Pad Name	X-pos	Y-pos
193	seg100	-1633.5	442.4
194	Dummy	-1683.5	442.4
195	Dummy	-2053.4	314
196	com9	-2053.4	264
197	com10	-2053.4	231
198	com11	-2053.4	198
199	com12	-2053.4	165
200	com13	-2053.4	132
201	com14	-2053.4	99
202	com15	-2053.4	66
203	com16	-2053.4	33
204	com25	-2053.4	0
205	com26	-2053.4	-33
206	com27	-2053.4	-66
207	com28	-2053.4	-99
208	com29	-2053.4	-132
209	com30	-2053.4	-165
210	com31	-2053.4	-198
211	com32	-2053.4	-231
212	ICON2	-2053.4	-264
213	Dummy	-2053.4	-314
214	TEST7	-1517.3	-274.7
215	TEST 6	-1467.3	-274.7
216	TEST 5	-1417.3	-274.7
217	TEST 4	-1367.3	-274.7
218	TEST 3	-1317.3	-274.7
219	TEST 2	-1267.3	-274.7
220	TEST 1	-1217.3	-274.7
221	TEST 0	-1167.3	-274.7

Bump Size

Pad #	X [um]	Y [um]	Pad pitch [um] (Min)
1	50	80	55
2-72	32	80	55
73	50	80	55
74	86	50	50
75-91	86	18	33
92	86	50	50
93	50	86	50
94-193	18	86	33
194	50	86	50
195	86	50	50
196-212	86	18	33
213	86	50	50
214-221	30	67	50

6 PIN DESCRIPTIONS

Key:

I = Input
 O =Output
 IO = Bi-directional (input/output)
 P = Power pin
 GND = System Ground

Table 6-1: Power Supply Pin Description

Pin Name	Type	Connect To	When Not in Use	Description
VCI	P	[Low Voltage I/O App.] System Supply, shorts VDD= 2.4-3.6V [5V I/O App.] shorts VDD	-	This pin is the input of the voltage converter to generate LCD drive voltage. In Low Voltage I/O application (VDDREG pulled low), it should be shorted with VDD. In 5V I/O application (VDDREG pulled high), this pin should be shorted with VDD.
VDD	P	[Low Voltage I/O App.] System Supply, shorts VCI= 2.4-3.6V [5V I/O App.] Stabilizing Capacitor	-	This pin is the power supply for logic circuit (VDD should rise within 10ms). In 3V IO application (VDDREG pulled low), this is a power input pin. In 5V IO application (VDDREG pulled high), this pin outputs 3V and should be connected with a capacitor to VSS.
VDDIO	P	[Low Voltage I/O App.] System Supply, 2.4 – VCI [5V I/O App.] System Supply, 4.5 – 5.5V	-	This pin is the power supply for bus IO buffer in both Low Voltage I/O and 5V I/O application.
VSS1	GND	Ground of Power Supply	-	System ground pin of the IC for digital part
VSS2	GND	Ground of Power Supply	-	System ground pin of the IC for analog part

Table 6-2 : LCD Driver Supply Pin Description

Pin Name	Type	Connect To	When Not in Use	Description
VOUT	O	Stabilizing Capacitor	Open	Output of the voltage converter
V0	IO	Stabilizing Capacitor	Open	Regulated voltage from voltage converter for LCD driving
V1 –V4	IO	Stabilizing Capacitors (Optional for 1-line, 2-line or low loading applications)	Open	Bias voltage levels for LCD driving

Table 6-3 : System Control Pin Description

Pin Name	Type	Connect To	When Not in Use	Description			
N2, N1	I	VDDIO or VSS	-	This pin is used to select the line display mode:			
				N2	N1	Line Display Mode	
				H	H	1 line	
				L	H	2 lines	
				H	L	3 lines	
				L	L	4 lines	
VDDREG	I	VDDIO or VSS	-	This pin is used to enable VDD regulator in 5V I/O Application:			
				VDDREG		Mode	
				H		5V I/O Application	
				L		Low Voltage I/O Application	
CLS	I	VDDIO or VSS	-	This pin is used to choose internal or external oscillator			
				CLS		Resistor	
				H		Internal oscillator is used	
				L		External oscillator is used	
ENCLKIN	I	External Frequency Source	VDDIO or VSS	When external oscillator is used (CLS = L), external clock will be input to ECLKIN. When internal oscillator is used (CLS = H), this pin should be connected to VDDIO or VSS.			
IM2, IM1	I	VDDIO or VSS	-	This pin is used to select the interface mode:			
				IM2	IM1	Interface Mode	
				H	H	4-bit/8-bit bus mode	
				L	H	serial mode	
				H	L	I2C mode	
				L	L	I2C mode	
OPR2, OPR1	I	VDDIO or VSS	-	This pin is used to select the character number of character generator: For details, please refer to the character generator selection in P23.			
				OPR2	OPR1	CGROM	CGRAM
				H	H	256	0
				L	H	248	8
				H	L	250	6
				L	L	240	8

Pin Name	Type	Connect To	When Not in Use	Description		
ROM2, ROM1	I	VDDIO or VSS	-	This pin is used to select Character ROM:		
				ROM2	ROM1	ROM
				L	L	A
				L	H	B
				H	L	C
				H	H	Invalid
SHLC	I	VDDIO or VSS	-	This pin is used to select common signal directions:		
				SHLC		Direction
				H		Com1 to Com32(Normal)
				L		Com32 to Com1 (Reverse)
SHLS	I	VDDIO or VSS	-	This pin is used to select segment signal directions:		
				SHLS		Direction
				H		Seg 1 to Seg 100 (Normal)
				L		Seg 100 to Seg 1 (Reverse)

Table 6-4 : MCU Interface Pin Description

Pin Name	Type	Connect To	When Not in Use	Description	
RW	I	MCU	VDDIO or VSS	This pin is used to select read/ write operation in bus mode:	
				RW	Operation
				H	Read operation
				L	Write operation
E	I	MCU	VDDIO or VSS	This pin is used as read/write enable signal in bus mode.	
/CS	I	MCU	VDDIO or VSS	This pin is used as chip select in bus and serial mode.	
				CS	Selection
				H	Not selected
				L	Selected
RS/ SA0	I	MCU/ VDDIO or VSS	VDDIO or VSS	This pin is used as register select in bus mode:	
				RS	Register
				H	Data register
				L	Instruction register
				This pin is to define slave address in I2C mode.	
				SA0	I2C address
				H	011 1101
L	011 1100				
DB0/ SCLK/ SCL	IO	MCU	-	This pin is used as lowest bi-direction data bit in 8-bit bus mode, no signal input is needed during 4-bit bus mode.	
				This pin is used as serial clock input pin in serial mode.	
				This pin is used as clock input pin in I2C mode.	

Pin Name	Type	Connect To	When Not in Use	Description
DB1/ SID/ SDAin	IO	MCU	-	This pin is used as second lowest bi-direction data bit in 8-bit bus mode, no signal input is needed during 4-bit bus mode. This pin is used as serial data input pin in serial mode. This pin is used as data input pin in I2C mode.
DB2/ SOD/ SDAout	IO	MCU	-	This pin is used as third lowest bi-direction data bit in 8-bit bus mode, no signal input is needed during 4-bit bus mode. This pin is used as serial data output pin in serial mode. This pin is used as data/ acknowledge response output pin in I2C mode.
DB3	IO	MCU	VDDIO or VSS	This pin is used as forth lowest bi-direction data bit in 8-bit bus mode, no signal input is needed during 4-bit bus mode. During serial mode/ I2C mode, short these pins to VDDIO or VSS.
DB4 – DB7	IO	MCU	VDDIO or VSS	When in 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order. DB7 used for busy flag output. During serial mode/ I2C mode, short these pins to VDDIO or VSS.
RESET	I	Reset Pin	-	System reset pin
TESTA, TESTD, TEST0 – TEST7	-	-	-	These pins are reserved for test purpose. Nothing should be connected to these pins, nor are they connected together.

Table 6-5 : LCD Driver Output Pin Description

Pin Name	Type	Connect To	When Not in Use	Description
SEG1 - SEG100	O	Segment Output	Open	Segment signal outputs for LCD drive
ICON1, ICON2	O	Common Output	Open	Both ICON1 and ICON2 provide same output for ICON drive
COM1 - COM32	O	Common Output	Open	Common signal outputs for LCD drive

7 FUNCTIONAL BLOCK DESCRIPTIONS

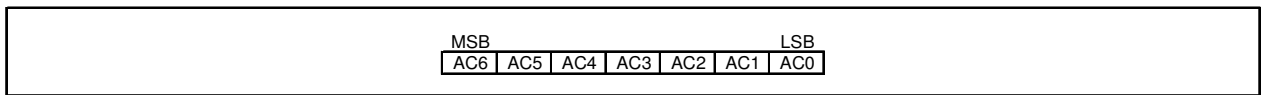
7.1 Busy Flag (BF)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation), through DB7. Before executing the next instruction, be sure that BF is not high.

7.2 Display Data Ram (DDRAM)

DDRAM stores display data of maximum 80 x 8 bits (80 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number. (Refer to Figure 7-1)

Figure 7-1: DDRAM Address

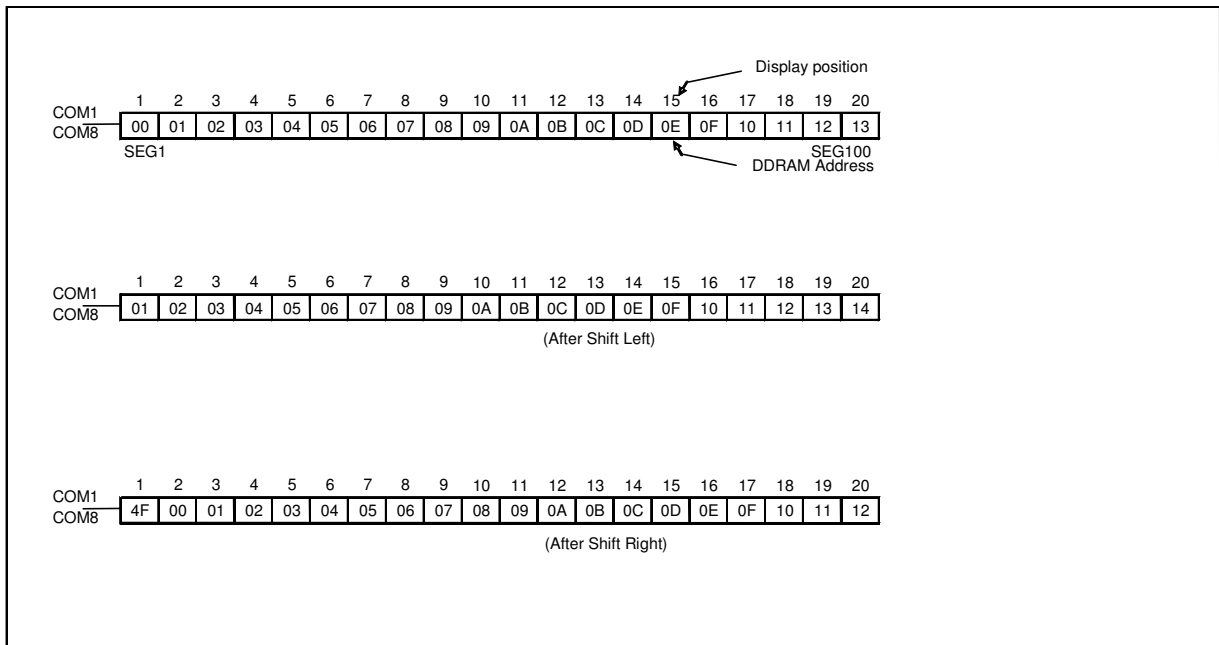


Display of 5-Dot Font Width Character

5-dot 1-line Display

In case of 1-line display with 5-dot font, the address range of DDRAM is 00H-4FH (Refer to Figure 7-2).

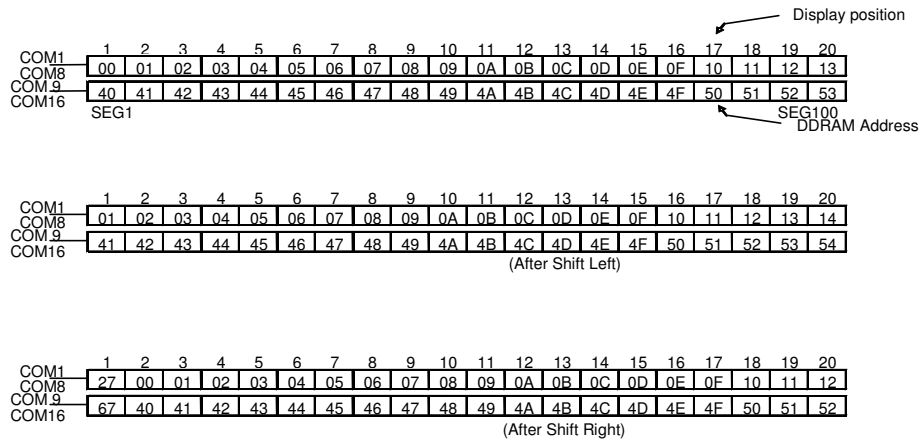
Figure 7-2: 1-line x 20ch. Display (5-dot Font Width)



5-dot 2-line Display

In case of 2-line display with 5-dot font, the address range of DDRAM is 00H-27H, 40H-67H (refer to Figure 7-3).

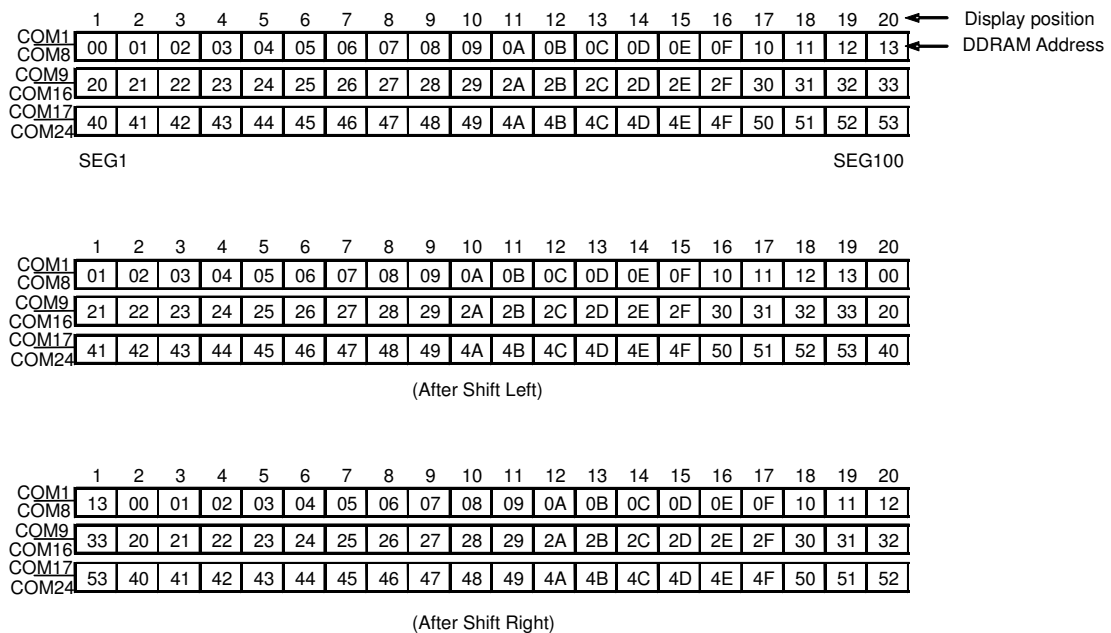
Figure 7-3: 2-line x 20ch. Display (5-dot Font Width)



5-dot 3-line Display

In case of 3-line display with 5-dot font, the address range of DDARM is 00H-13H, 20H-33H, 40H-53H (refer to Figure 7-4).

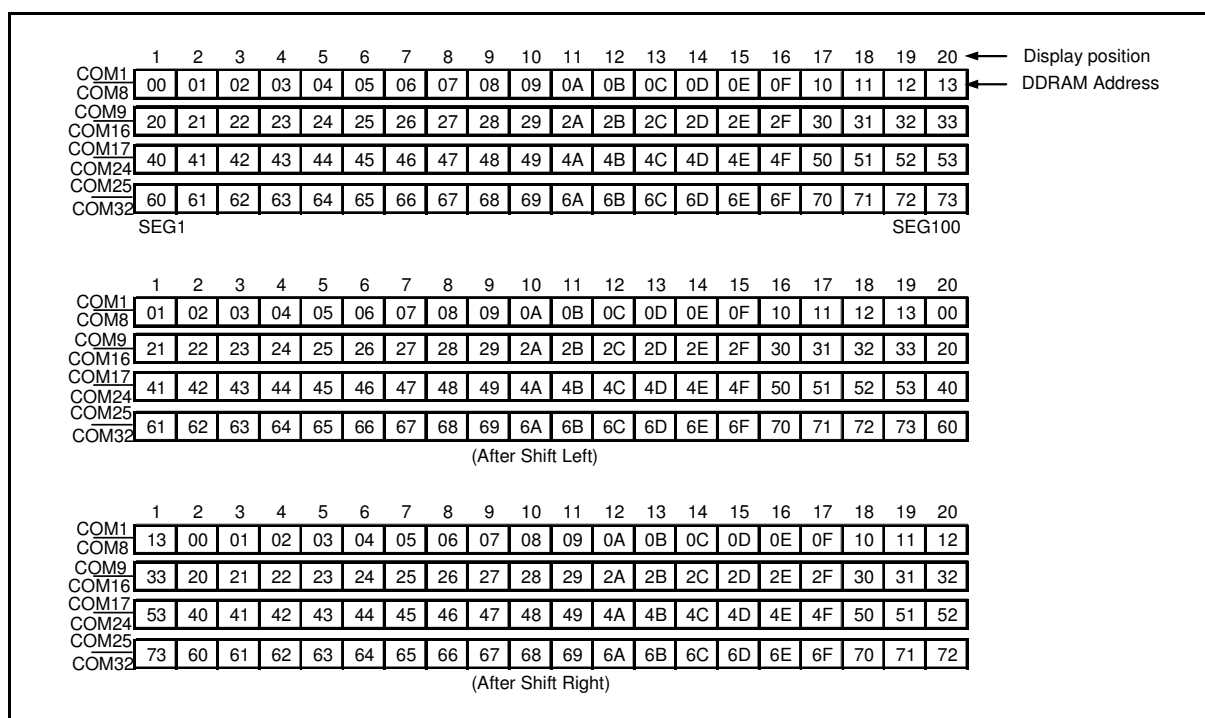
Figure 7-4: 3-line x 20ch. Display (5-dot Font Width)



5-dot 4-line Display

In case of 4-line display with 5-dot font, the address range of DDARM is 00H-13H, 20H-33H, 40H-53H, 60H-73H (refer to Figure 7-5).

Figure 7-5: 4-line x 20ch. Display (5-dot Font Width)



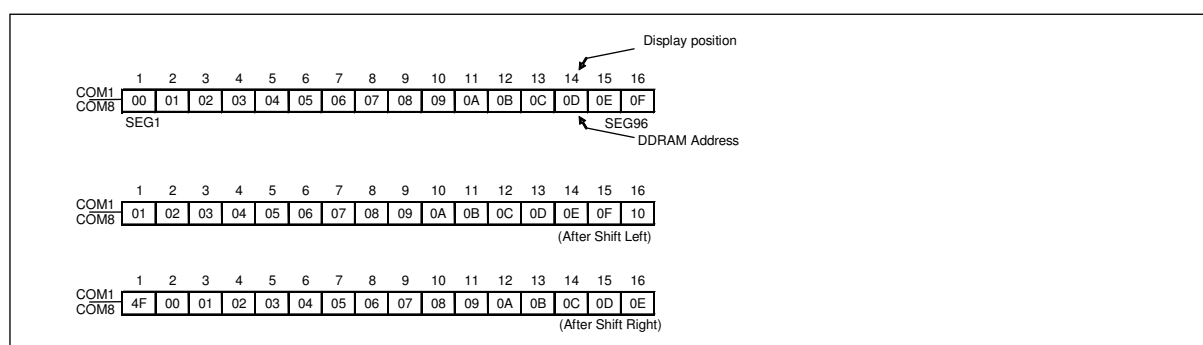
DISPLAY OF 6-DOT FONT WIDTH CHARACTER

When the device is used in 6-dot font width mode, SEG97, SEG98, SEG99 and SEG100 must be opened.

6-dot 1-line Display

In case of 1-line display with 6-dot font, the address range of DDRAM is 00H-4FH (refer to Figure 7-6).

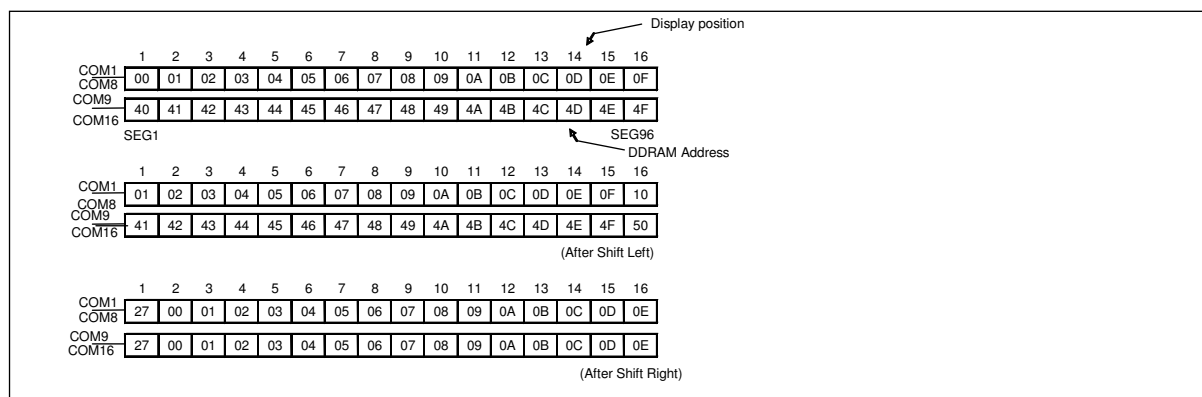
Figure 7-6: 1-line x 16ch. Display (6-dot Font Width)



6-dot 2-line Display

In case of 2-line display with 6-dot font, the address range of DDRAM is 00H-27H, 40H-67H (refer to Figure 7-7).

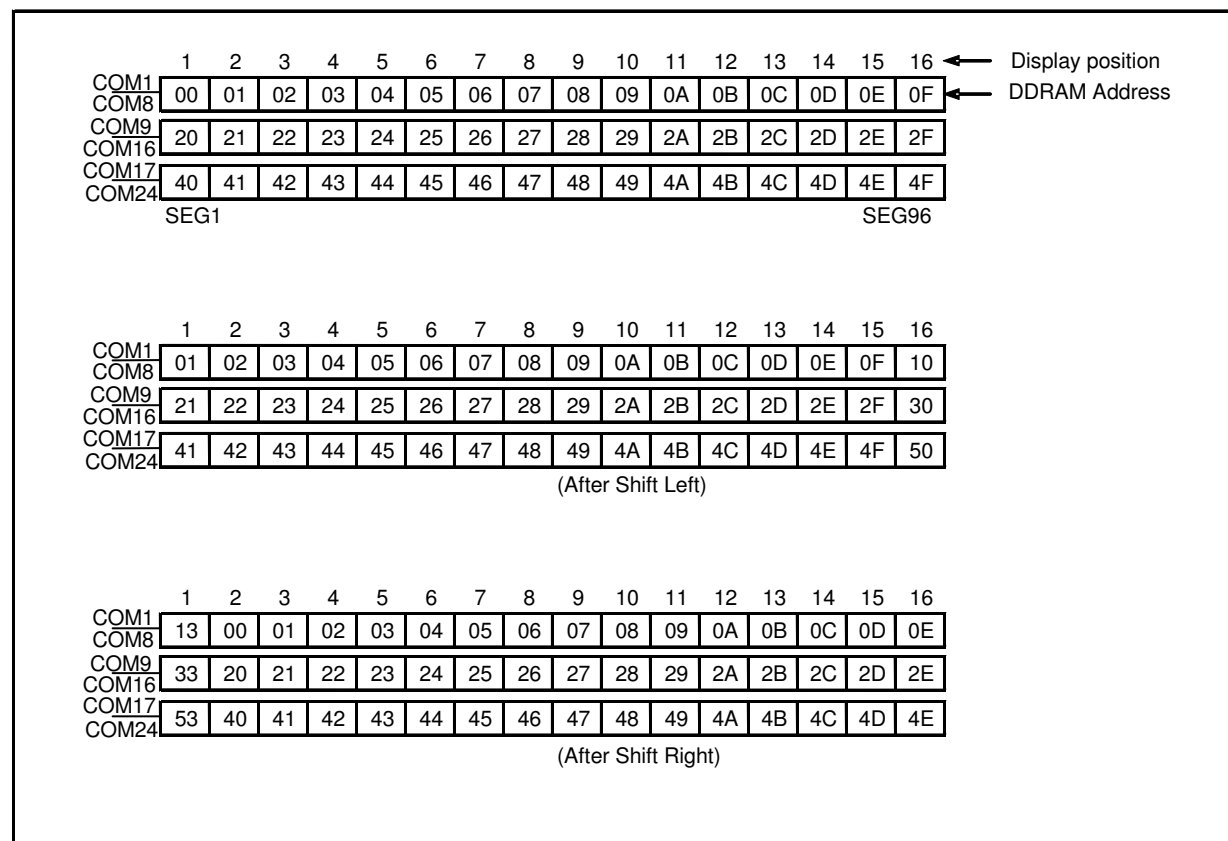
Figure 7-7: 2-line x 16ch. Display (6-dot Font Width)



6-dot 3-line Display

In case of 3-line display with 6-dot font, the address range of DDARM is 00H-13H, 20H-33H, 40H-53H (refer to Figure 7-8).

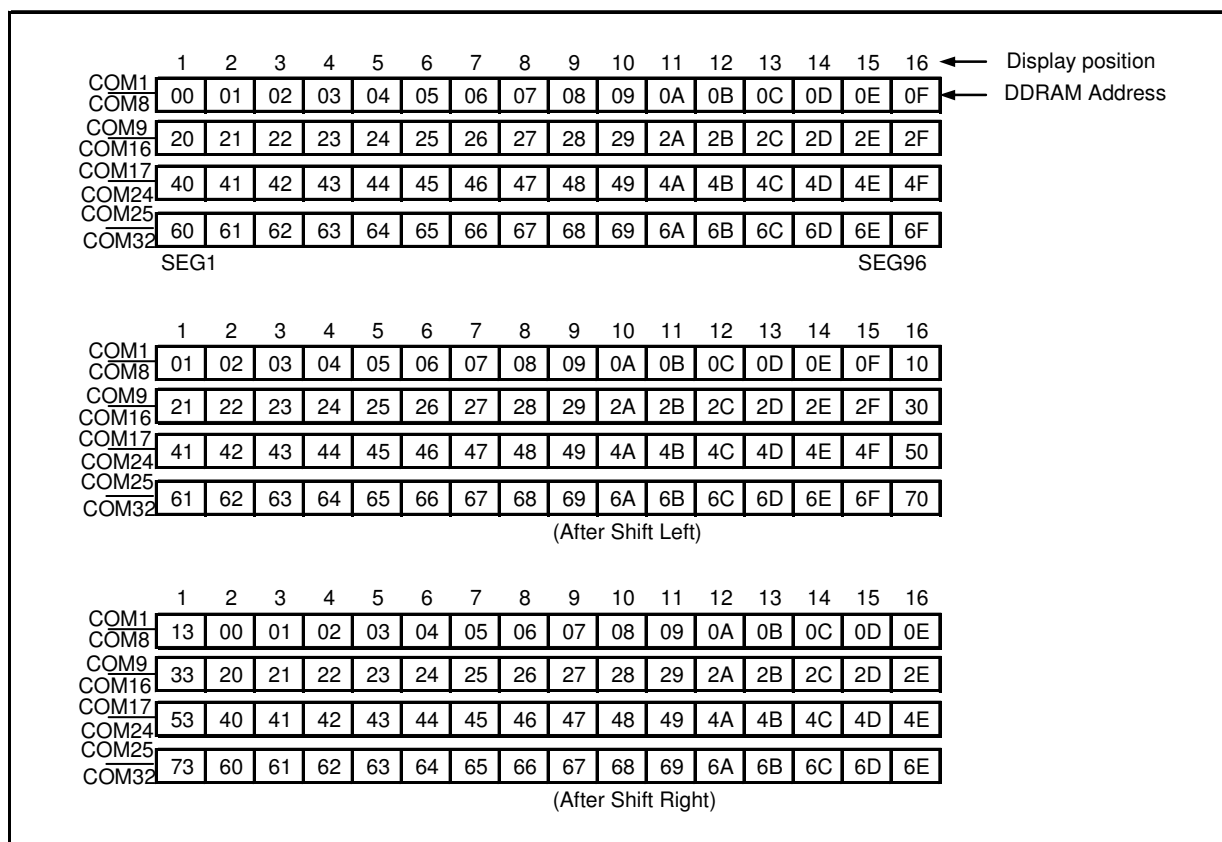
Figure 7-8 3-line x 16ch. Display (6-dot Font Width)



6-dot 4-line Display

In case of 4-line display with 6-dot font, the address range of DDARM is 00H-13H, 20H-33H, 40H-53H, 60H-73H (refer to Figure 7-9).

Figure 7-9 4-line x 16ch. Display (6-dot Font Width)



7.3 Timing Generation Circuit

Timing generation circuit generates clock signals for the internal operations.

7.4 Address Counter (AC)

Address Counter (AC) stores DDRAM/ CGRAM/ SEGRAM address, transferred from Instruction Register (IR). After writing into (reading from) DDRAM/ CGRAM/ SEGRAM, AC is automatically increased (decreased) by 1. In parallel and serial mode, when RS = "Low" and R/W = "High", AC can be read through DB0-DB6.

7.5 Cursor/Blink Control Circuit

It controls cursor/blink ON/OFF and black/white inversion at cursor position.

7.6 LCD Driver Circuit

LCD Driver circuit has 34 common and 100 segment signals for LCD driving. Data from SEGRAM/ CGRAM/ CGROM is transferred to 100-bit segment latch serially, and then it is stored to 100-bit shift latch. When each com is selected by 34-bit common register, segment data also output through segment driver from 100-bit segment latch. In case of 1-line display mode, ICON1/ICON2 and COM1-COM8 have 1/9 duty ratio; and in 4-line mode, ICON1/ICON2 and COM1-COM32 have 1/33 duty ratio.

7.7 CGROM (Character Generator ROM)

There is 3 optional CGROMs in SSD1803A in P.66-68 , which is selected by ROM1 and ROM2 pins. CGROM has 5 x 8 dots 256 Character Pattern.

7.8 CGRAM (Character Generator RAM)

CGRAM has up to 8 characters of 5 x 8 dots, selectable by OPR2 and OPR1 pins (refer to Table 7-1).

Table 7-1: CGRAM and CGROM arrangement with

(OPR2, OPR1) = (0, 0)

b7-4 \ b3-0	b3-0															
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000																
0001																

(OPR2, OPR1) = (1, 0)

b7-4 \ b3-0	b3-0															
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000																
0001																

(OPR2, OPR1) = (0, 1)

b7-4 \ b3-0	b3-0															
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000																
0001																

(OPR2, OPR1) = (1, 1)

b7-4 \ b3-0	b3-0															
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000																
0001																

By writing font data to CGRAM, user defined character can be used (refer to Table 7-2).

Table 7-2: Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

5x8 dots Character Pattern

Character Code (DDRAM Data)								CGRAM Address						CGRAM Daata								Pattern Number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	x	0	0	0	0	0	0	0	0	0	B1	B0	x	0	1	1	1	0	Pattern1
				.							0	0	1				1	0	0	0	1	
				.							0	1	0				1	0	0	0	1	
				.						.	0	1	1		.		1	1	1	1	1	
				.						.	1	0	0		.		1	0	0	0	1	
				.						.	1	0	1		.		1	0	0	0	1	
				.						.	1	1	0		.		1	0	0	0	1	
				.						.	1	1	1				0	0	0	0	0	
				.					.	.	.	.	.			.	.	.	.	.	.	
0	0	0	0	x	1	1	1	1	1	1	0	0	0	B1	B0	x	1	0	0	0	1	Pattern8
				.						.	0	0	1				1	0	0	0	1	
				.						.	0	1	0		.		1	0	0	0	1	
				.						.	0	1	1		.		1	1	1	1	1	
				.						.	1	0	0		.		1	0	0	0	1	
				.						.	1	0	1		.		1	0	0	0	1	
				.						.	1	1	0		.		1	0	0	0	1	
				.						.	1	1	1				0	0	0	0	0	

6 x 8 Dots Character Pattern

Character Code (DDRAM Data)								CGRAM Address						CGRAM Daata								Pattern Number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	x	0	0	0	0	0	0	0	0	0	B1	B0	0	0	1	1	1	0	Pattern1
				.							0	0	1			0	1	0	0	0	1	
				.						.	0	1	0			0	1	0	0	0	1	
				.						.	0	1	1	.		0	1	1	1	1	1	
				.						.	1	0	0	.		0	1	0	0	0	1	
				.						.	1	0	1	.		0	1	0	0	0	1	
				.						.	1	1	0	.		0	1	0	0	0	1	
				.						.	1	1	1			0	0	0	0	0	0	
				.					.	.	.	.	.			.	.	.	.	.	.	
0	0	0	0	x	1	1	1	1	1	1	0	0	0	B1	B0	0	1	0	0	0	1	Pattern8
				.						.	0	0	1			0	1	0	0	0	1	
				.						.	0	1	0	.		0	1	0	0	0	1	
				.						.	0	1	1	.		0	1	1	1	1	1	
				.						.	1	0	0	.		0	1	0	0	0	1	
				.						.	1	0	1	.		0	1	0	0	0	1	
				.						.	1	1	0			0	1	0	0	0	1	
				.						.	1	1	1			0	0	0	0	0	0	

- When BE (Blink Enable bit) = "High", blink is controlled by B1 and B0 bit.
In case of 5-dot font width, when B1 = "1", enabled dots of P0-P4 will blink, and when B1 = "0" and B0 = "1", enabled dots in P4 will blink, when B1 = "0" and B0 = "0", blink will not happen.
In case of 6-dot font width, when B1 = "1", enabled dots of P0-P5 will blink, and when B1 = "0" and B0 = "1", enabled dots of P5 will blink, when B1 = "0" and B0 = "0", blink will not happen.
- "X": Don't care

7.9 SEGRAM (Segment Icon RAM)

SEGRAM has segment control data and segment pattern data. During display mode, ICON1 (ICON2) makes the data of SEGRAM enable to display icons. Its higher 2-bit are blinking control data, and lower 6-bits are pattern data (refer to Table 7-3 and Figure 7-10).

Table 7-3: Relationship between SEGRAM Address and Display Pattern

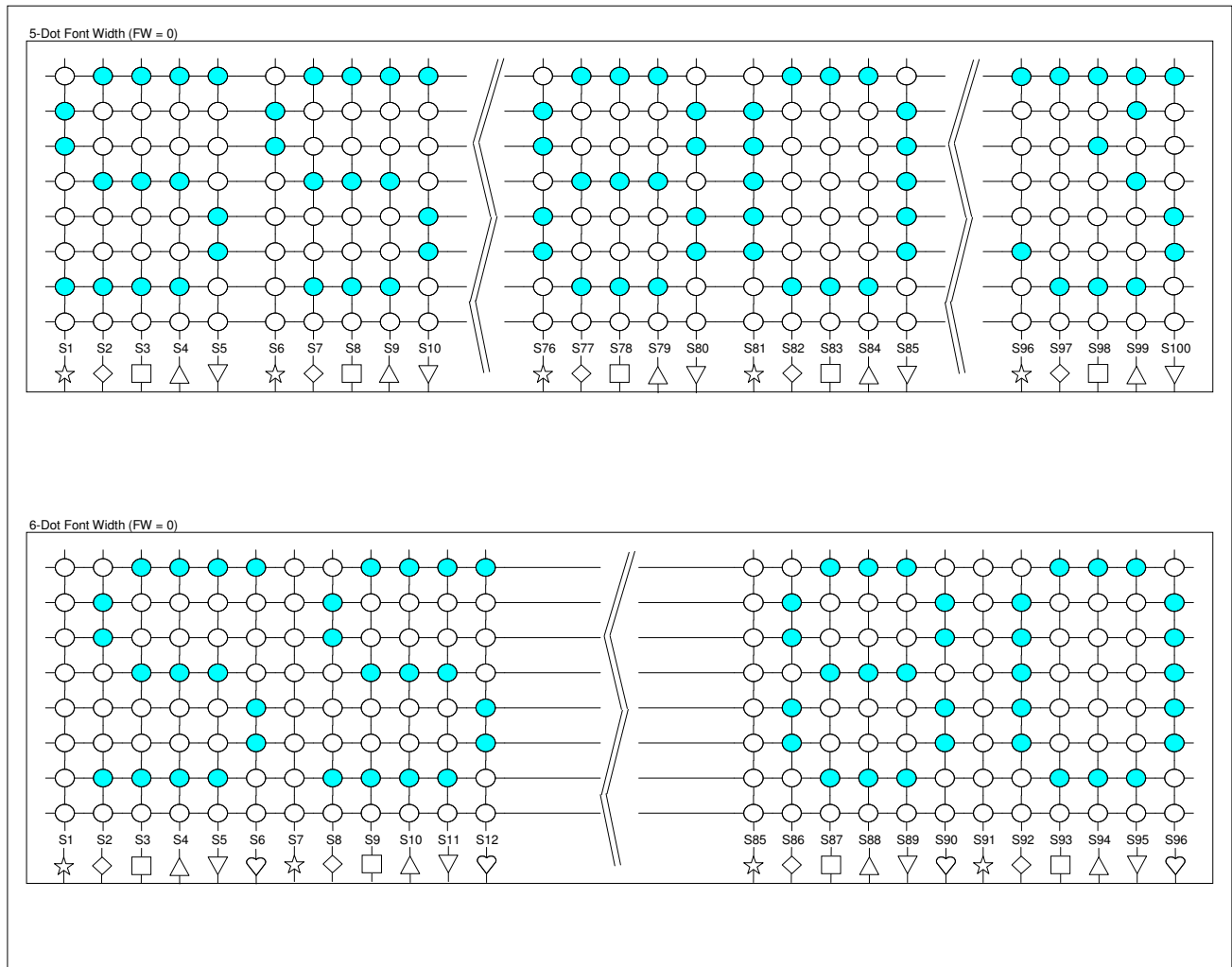
SEGRAM Address				SEGRAM Data Display Pattern															
				5-dot Font Width								6-dot Font Width							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	B1	B0	X	S1	S2	S3	S4	S5	B1	B0	S1	S2	S3	S4	S5	S6
0	0	0	1	B1	B0	X	S6	S7	S8	S9	S10	B1	B0	S7	S8	S9	S10	S11	S12
0	0	1	0	B1	B0	X	S11	S12	S13	S14	S15	B1	B0	S13	S14	S15	S16	S17	S18
0	0	1	1	B1	B0	X	S16	S17	S18	S19	S20	B1	B0	S19	S20	S21	S22	S23	S24
0	1	0	0	B1	B0	X	S21	S22	S23	S24	S25	B1	B0	S25	S26	S27	S28	S29	S30
0	1	0	1	B1	B0	X	S26	S27	S28	S29	S30	B1	B0	S31	S32	S33	S34	S35	S36
0	1	1	0	B1	B0	X	S31	S32	S33	S34	S35	B1	B0	S37	S38	S39	S40	S41	S42
0	1	1	1	B1	B0	X	S36	S37	S38	S39	S40	B1	B0	S43	S44	S45	S46	S47	S48
1	0	0	0	B1	B0	X	S41	S42	S43	S44	S45	B1	B0	S49	S50	S51	S52	S53	S54
1	0	0	1	B1	B0	X	S46	S47	S48	S49	S50	B1	B0	S55	S56	S57	S58	S59	S60
1	0	1	0	B1	B0	X	S51	S52	S53	S54	S55	B1	B0	S61	S62	S63	S64	S65	S66
1	0	1	1	B1	B0	X	S56	S57	S58	S59	S60	B1	B0	S67	S68	S69	S70	S71	S72
1	1	0	0	B1	B0	X	S61	S62	S63	S64	S65	B1	B0	S73	S74	S75	S76	S77	S78
1	1	0	1	B1	B0	X	S66	S67	S68	S69	S70	B1	B0	S79	S80	S81	S82	S83	S84
1	1	1	0	B1	B0	X	S71	S72	S73	S74	S75	B1	B0	S85	S86	S87	S88	S89	S90
1	1	1	1	B1	B0	X	S76	S77	S78	S79	S80	B1	B0	S91	S92	S93	S94	S95	S96

1. B1, B0: Blinking control bit

Control Bit	Blinking Port	
BE B1 B0	5-dot font width	6-dot font width
0 X X	No blink	No blink
1 0 0	No blink	No blink
1 0 1	D4	D5
1 1 X	D4 - D0	D5 - D0

1. S1-S80 : Icon pattern ON/OFF in 5-dot font width
S1-S96 : Icon pattern ON/OFF in 6-dot font width
2. "X": Don't care.

Figure 7-10 Relationship between SEGRAM and Segment Display



7.10 System Interface

This chip has all four kinds of interface type with MPU: I2C, serial, 4-bit bus and 8-bit bus. I2C, Serial and bus (4-bit/8-bit) is selected by IM1 and IM2 inputs, and 4-bit bus and 8-bit bus is selected by DL bit in the instruction register.

7.10.1 4-bit bus and 8-bit bus interface (IM2=H, IM1 = H)

During read or write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register (IR). The data register (DR) is used as temporary data storage place for being written into or read from DDRAM/ CGRAM/SEGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. So to speak, after MPU reads DR data, the data in the next DDRAM/ CGRAM/ SEGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/ CGRAM/ SEGRAM automatically. The Instruction register (IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data. To select register, use RS input pin in 4-bit/8-bit bus mode (IM2 = "High") or RS in serial mode (IM2 = "Low").

Table 7-4: Bus interface operations according to RS and RW bits

RS	RW	Operation
0	0	Instruction write operation (MPU writes Instruction code into IR)
0	1	Read busy flag (DB7) and address counter (DB0 - DB6)
1	0	Data write operation (MPU writes data into DR)
1	1	Data read operation (MPU reads data from DR/ Part ID)

- In case of 4-bit bus mode, data transfer is performed by two times to transfer 1 byte data.
- When interfacing data length is 4-bit, only 4 ports, from DB4 - DB7, are used as data bus.
- At first higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7) are transferred, and then lower 4-bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed by two times.
- When interfacing data length is 8-bit, transfer is performed at a time through 8 ports, from DB0 - DB7.
- Please refer to the 6800 interface timing in P.54.

7.10.2 Serial interface (IM2=L, IM1 = H)

When IM2= L and IM1=H, serial interface mode is started. At this time, all three ports, SCLK (synchronizing transfer clock), SID (serial input data), and SOD (serial output data), are used. If you want to use SSD1803A with other chips, chip select port (CS) can be used. By setting CS to "Low", SSD1803A can receive SCLK input. If CS is set to "High", SSD1803A reset the internal transfer counter.

Before transfer real data, start byte has to be transferred. It is composed of succeeding 5 "High" bits, read write control bit (R/W), register selection bit (RS) and end bit that indicates the end of start byte. Whenever succeeding 5 "High" bits are detected by SSD1803A, it makes serial transfer counter reset and ready to receive next information.

The next input data are register selection bit that determine which register will be used, and read write control bit that determine the direction of data. Then end bit is transferred, which must have "Low" value to show the end of start byte. (Refer to Figure 7-11 and Figure 7-12)

Write Operation (R/W = 0)

After start byte is transferred from MPU to SSD1803A, 8-bit data is transferred which is divided into 2 bytes, each byte has 4 bit's real data and 4 bit's partition token data. For example, if real data is "10110001" (D0 - D7), then serially transferred data becomes "1011 0000 0001 0000" where 2nd and 4th 4 bits must be "0000" for safe transfer. To transfer several bytes continuously without changing RS bit and RW bit, start byte transfer is needed only at first starting time. Namely, after first start byte is transferred, real data can be transferred succeeding.

Read Operation (R/W = 1)

After start byte is transferred to SSD1803A, MPU can receive 8-bit data through the SOD port at a time from the LSB. Wait time is needed to insert between start byte and data reading, because internal reading from RAM requires some delay. Continuous data reading is possible like serial write operation. It also needs only one start byte, only if you insert some delay between reading operations of each byte. During the reading operation, SSD1803A observes succeeding 5 "High" from MPU. If it is detected, SSD1803A restarts serial operation at once and ready to receive RS bit. So in continuous reading operation, SID port must be "Low".

Figure 7-11 Timing Diagram of Serial Data Transfer

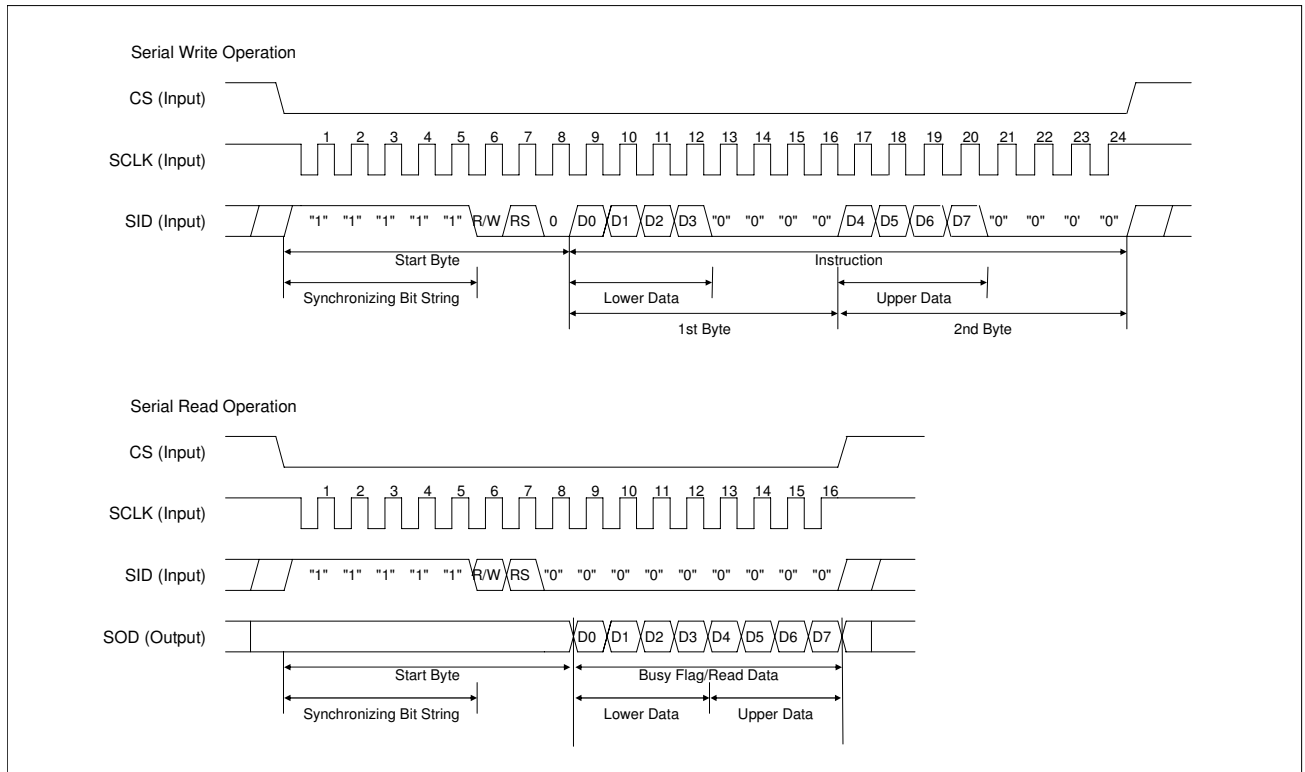
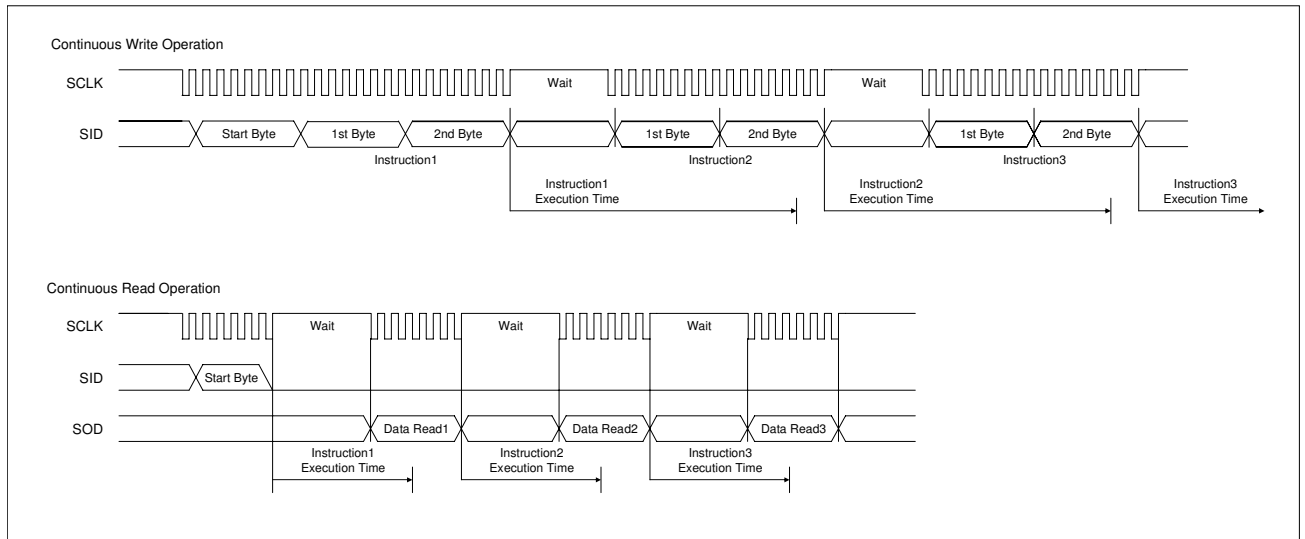


Figure 7-12 Timing Diagram of Continuous Data Transfer



7.10.3 I2C interface

SSD1803A supports I2C interface with a bit rate up to 400 kbits/s. It enables write/ read data or busy flag and supports only the mandatory slave feature showed below.

Slaver address could be set to “011 1100” or “011 1101” by SA0 pin.

The I2C interface send RAM data and executes the commands sent via the I2C Interface. It could send data in to the RAM. The I2C Interface is two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy. (Note: SDAin and SDAout are short together and forms SDA in SSD1803A)

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Figure 7-13.

Start and Stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Figure 7-14.

System Configuration

The system configuration consists of

- Transmitter: the device, which sends the data to the bus
- Master: the device, which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

Acknowledge

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I2C Interface is illustrated in Figure 7-15.

Figure 7-13: Bit transfer on the I2C-bus

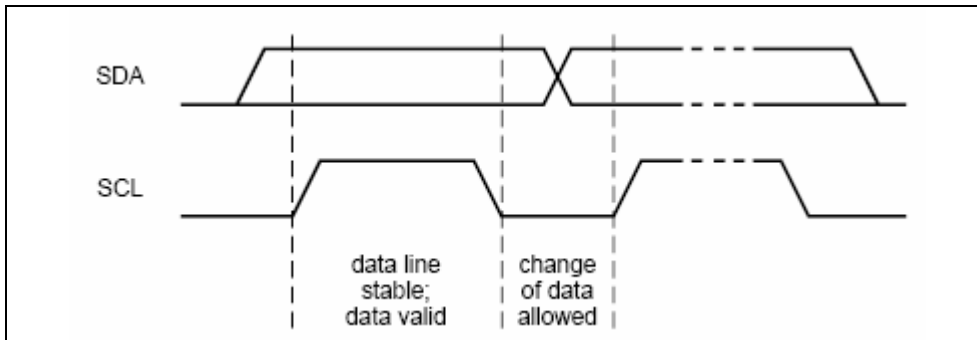


Figure 7-14: START and STOP conditions

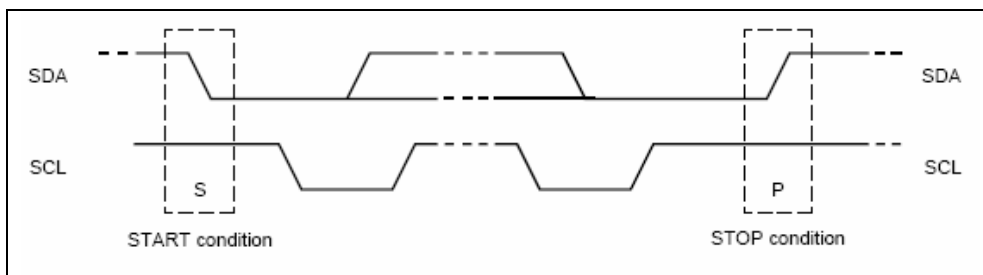
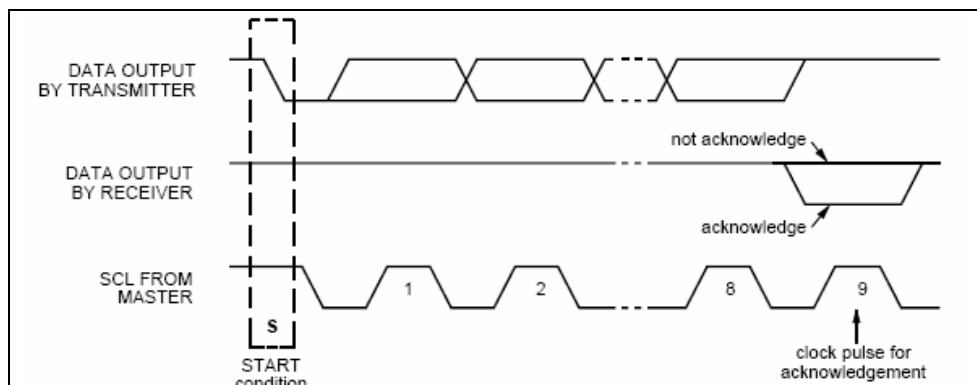


Figure 7-15: Acknowledge on the I2C bus



I2C Interface Protocol

The SSD1803A supports command, data read/ write addressed slaves on the bus.

Before any data is transmitted on the I2C Interface, the device, which should respond, is addressed first. Two 7-bit slave addresses (0111100 to 0111101) are reserved for the SSD1803A. The R/W# is assigned to 0 for Write and 1 for Read. The I2C Interface protocol is illustrated in Figure 7-16 to 7-18.

The sequence is initiated with a START condition (S) from the I2C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I2C Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.

A command word consists of control byte, which defines C0 and D/C#, plus a data byte.

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After the last control byte with a cleared Co bit, only data bytes will follow. The state of the D/C# bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the D/C# bit setting; either a series of display data bytes or command data bytes may follow. If the D/C# bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended SSD1803A device. If the D/C# bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the I2C INTERFACE-bus master issues a STOP condition (P).

Figure 7-16: I2C write mode

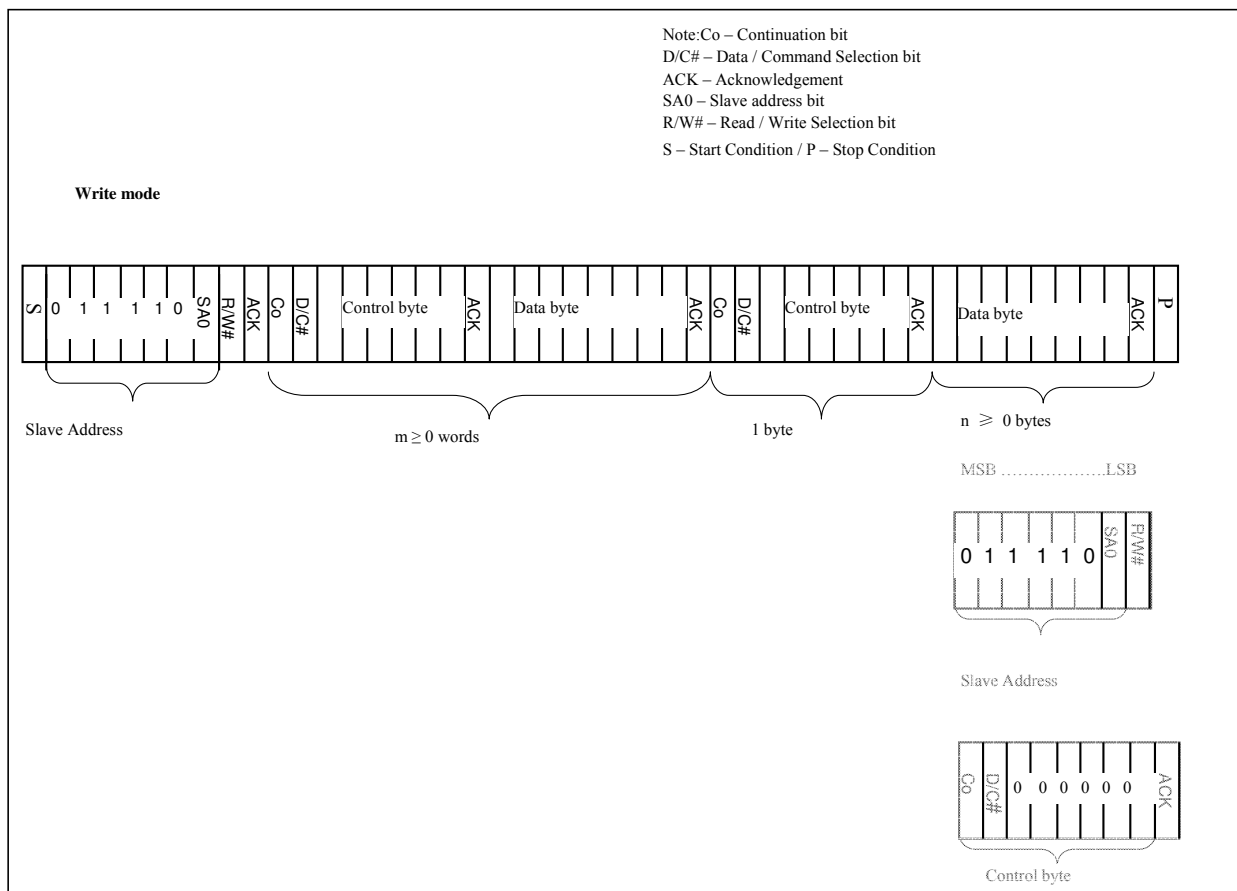
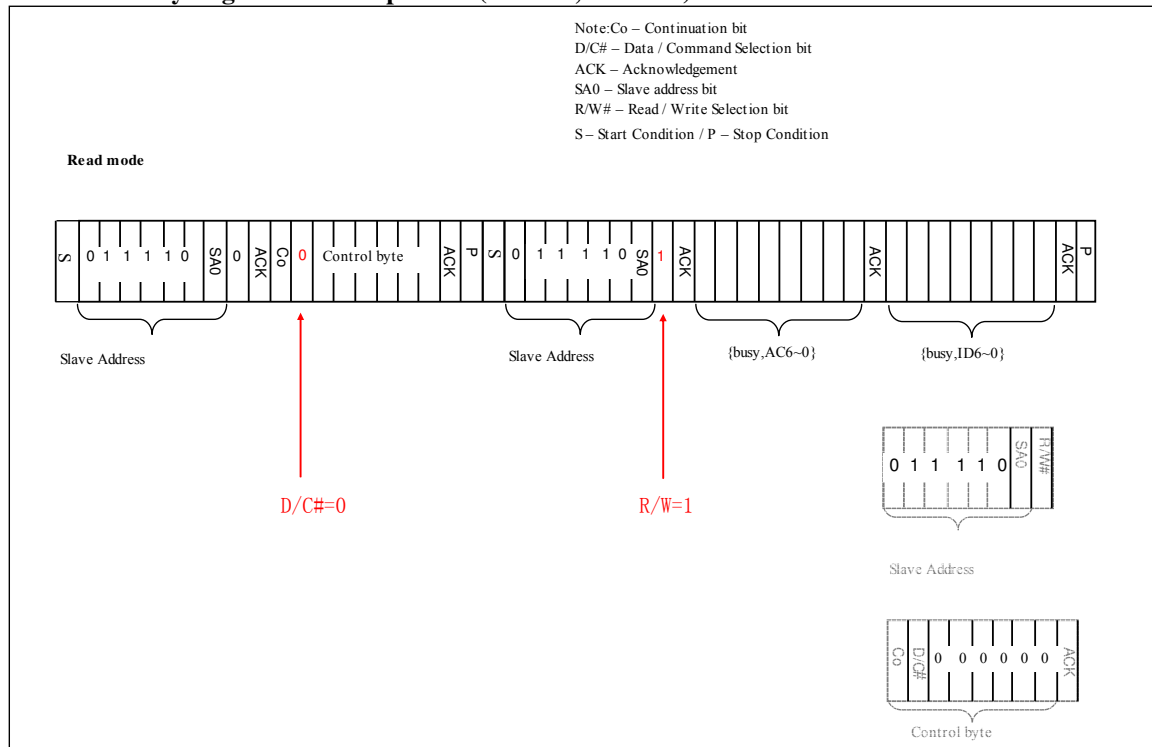


Figure 7-17: I2C read mode

Read busy flag and address/part ID (D/C#=0, R/W#=1)



Read ram (D/C#=1, R/W#=1)

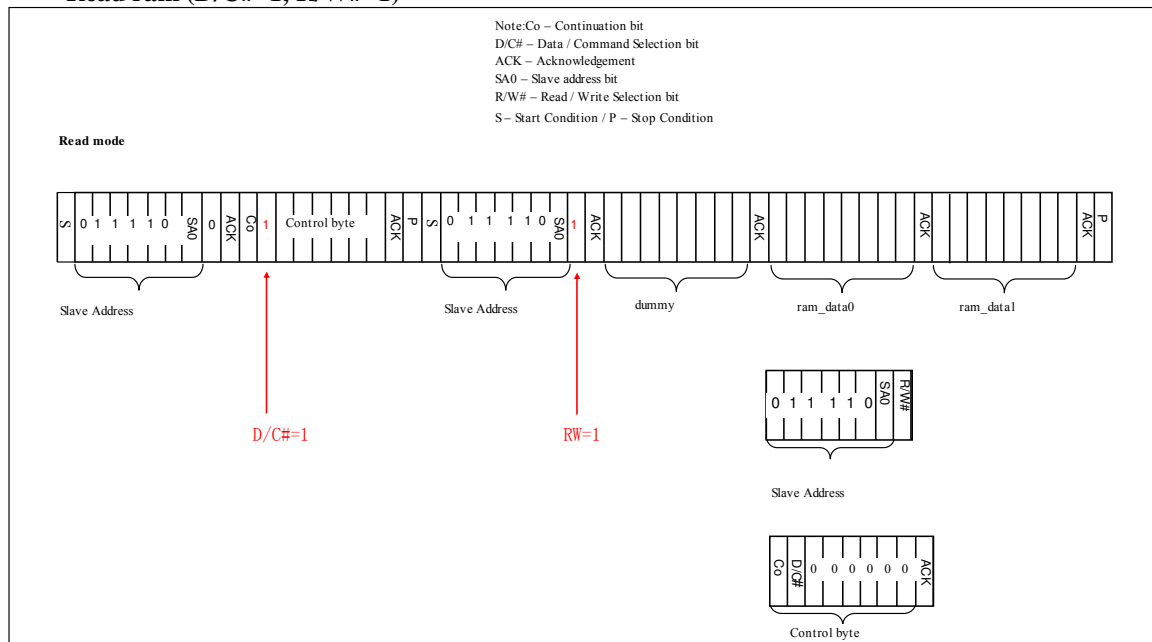
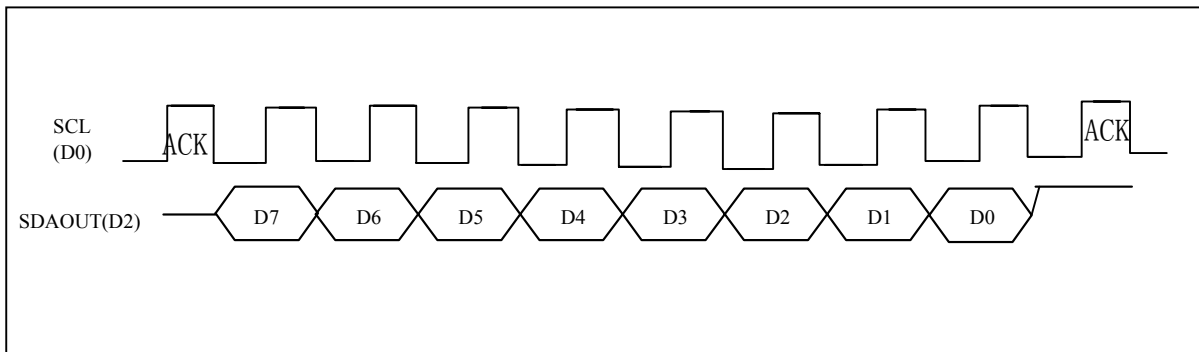


Figure 7-18: Read Timing



During read or write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register (IR). The data register (DR) is used as temporary data storage place for being written into or read from DDRAM/ CGRAM/SEGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. So to speak, after MPU reads DR data, the data in the next DDRAM/ CGRAM/ SEGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/ CGRAM/ SEGRAM automatically. The Instruction register (IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data. To select register, use D/C# I2C mode.

Table 7-5: Bus interface operations according to D/C# and R/W# inputs

D/C#	R/W#	Operation
0	0	Instruction write operation (MPU writes Instruction code into IR)
0	1	Read busy flag (DB7) and address counter (DB0 - DB6)
1	0	Data write operation (MPU writes data into DR)
1	1	Data read operation (MPU reads data from DR/ Part ID)

7.11 5V IO regulator

SSD1803A accepts two power supply range:

2.4-3.6V [**Low Voltage I/O Application**] and

4.5-5.5V [**5V I/O Application**]

5V IO Regulator is enabled to regulate 5V I/O input to 3V for power supply of internal circuit blocks.

Note: In 5V I/O Application, VOUT should not be lower than VDDIO.

Table 7-6 summarizes the input/ output connection of 5V IO regulator in normal application.

Table 7-6: 5V IO regulator pin description

Pin Name	Low Voltage I/O Application	5V I/O Application
VDDREG	Low, disable 5V IO regulator	High, enable 5V IO regulator
VCI	Short to VDD	Short to VDD
VDD	2.4 -3.6V	NC with stabilizing capacitor It outputs 3V
VDDIO	2.4 -VCI	4.5 -5.5V

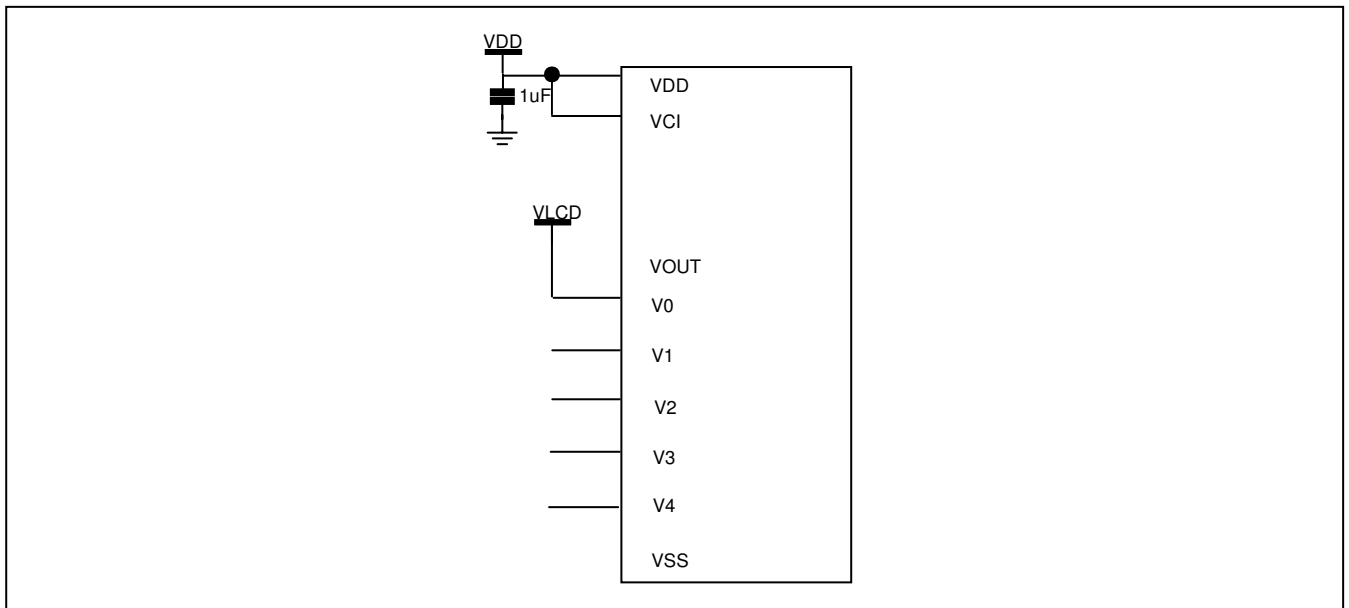
7.12 LCD Driving Voltage Generator and Regulator

This module generates the LCD voltage required for display driving output.

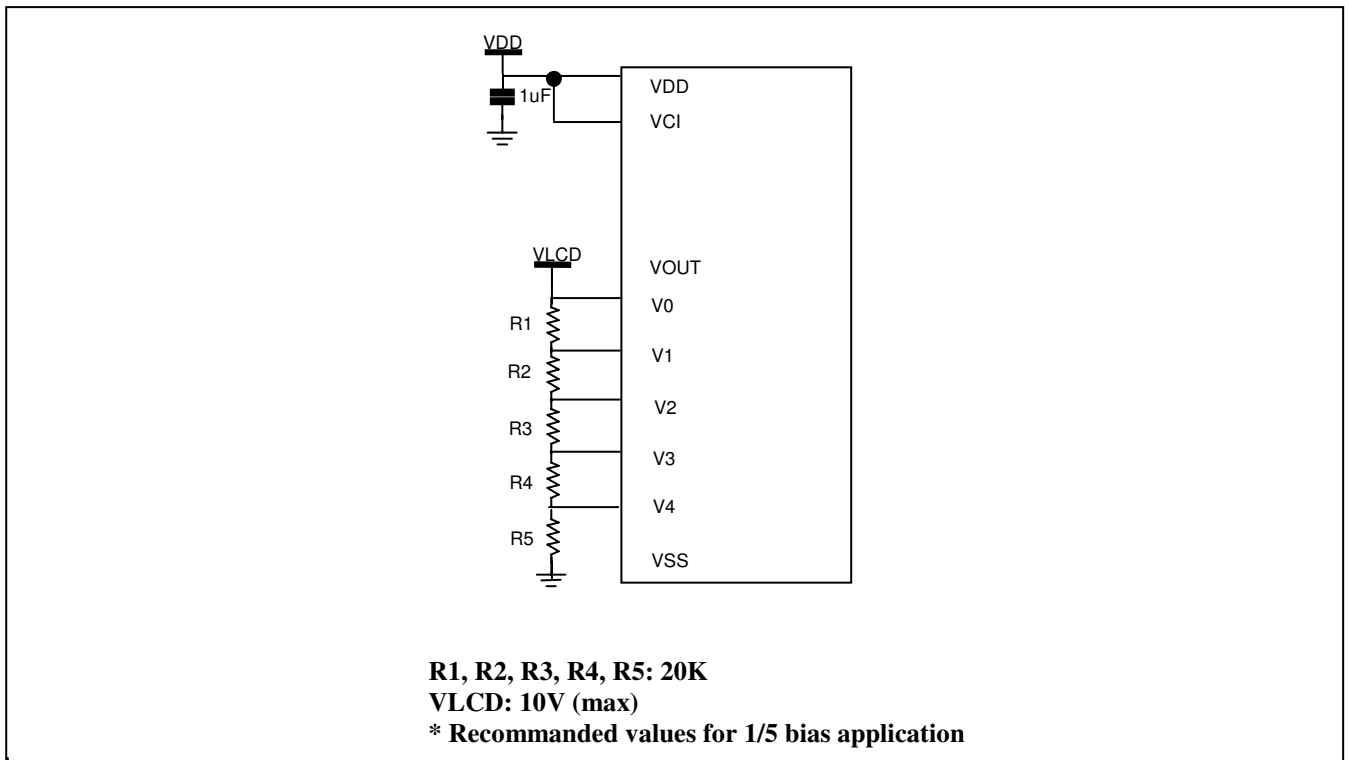
7.12.1 External VLCD mode

When on-chip booster is turned off, VLCD can be supplied externally to V0 for display driving.

**Figure 7-19: On-chip voltage converter application set up
When booster is off and voltage follower is on (Bon=0; Don=1)**



**Figure 7-20: On-chip voltage converter application set up
When both booster and voltage follower is off (Bon=0; Don=0)**



R1, R2, R3, R4, R5: 20K

VLCD: 10V (max)

*** Recommended values for 1/5 bias application**

7.12.2 Internal voltage mode

a) On-chip DC-DC voltage converter

Voltage converter is available when Bon=1. Figure 7-21 shows the circuits boosting up the electric potential between VDD – VSS toward positive side and boosted voltage is output at VOUT.

Figure 7-21: On-chip voltage converter application set up
When both booster and voltage follower is on (Bon=1; Don=1)

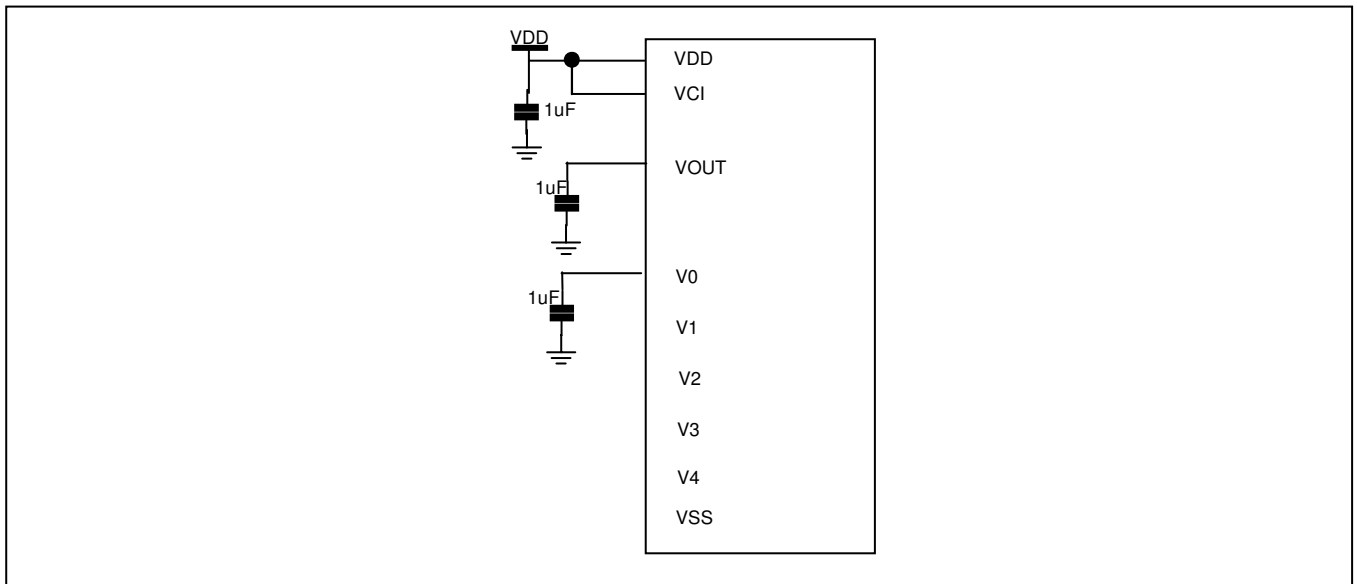
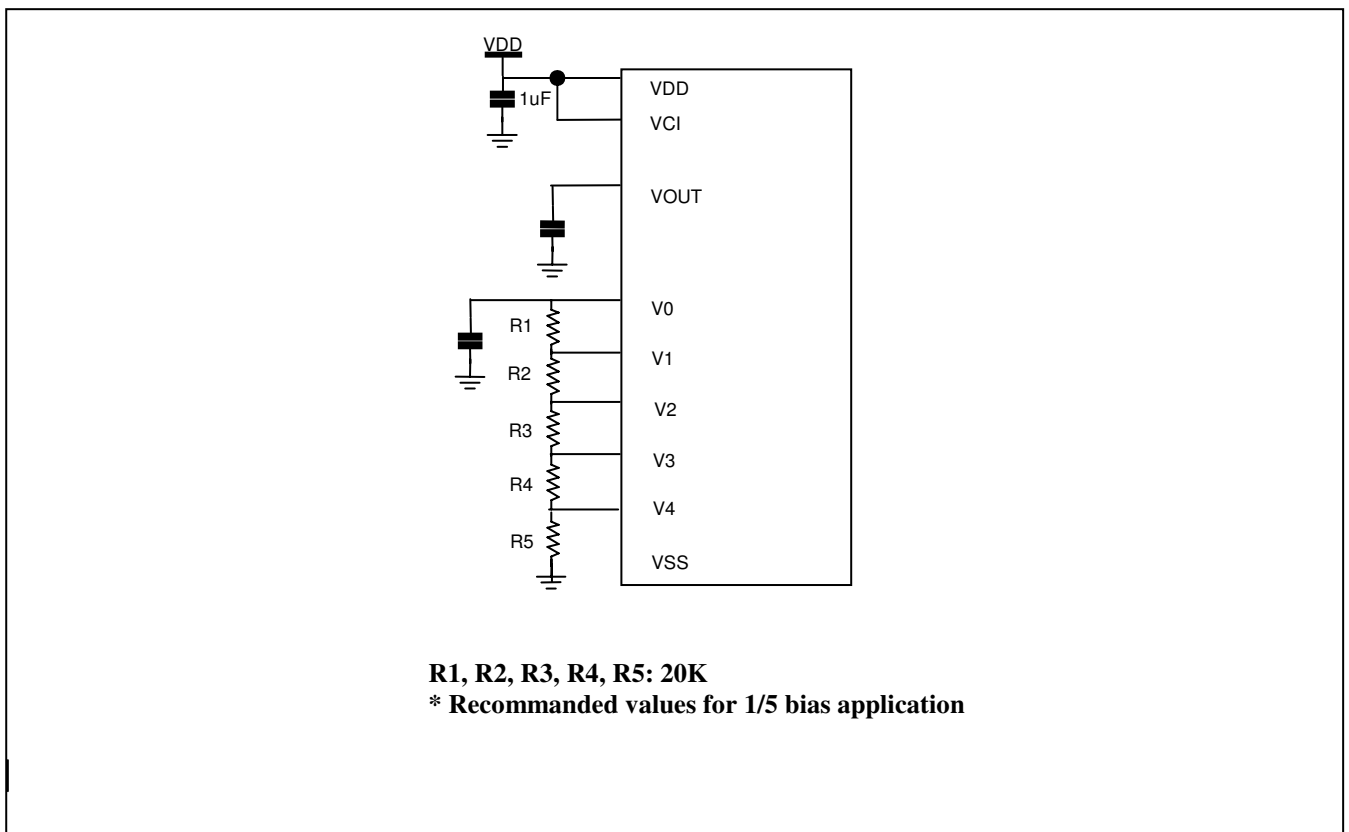


Figure 7-22: On-chip voltage converter application set up
When both booster is on and voltage follower is off (Bon=1; Don=0)

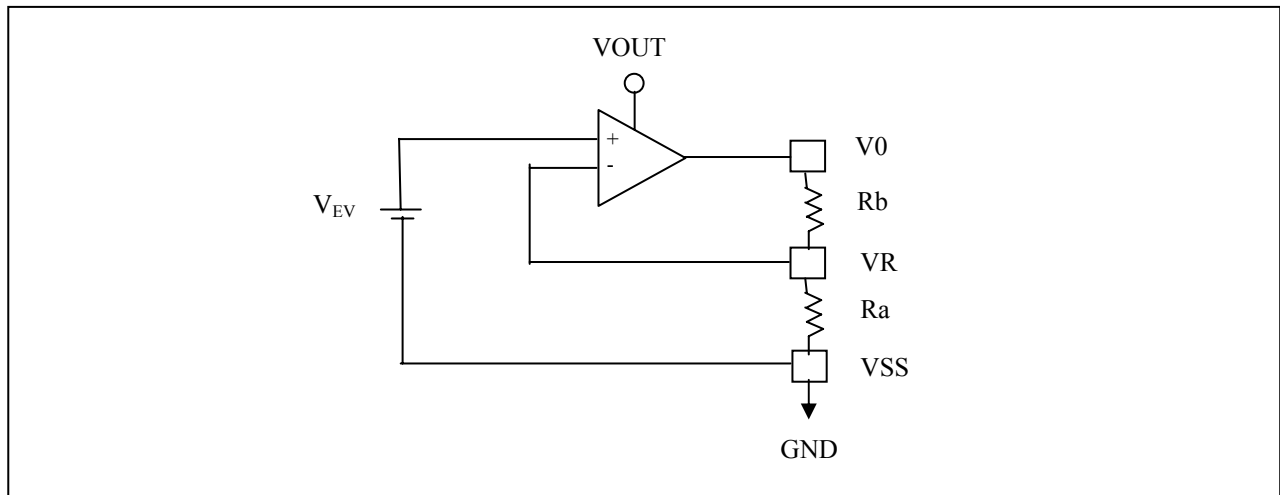


b) Voltage regulator circuits (Gain) and Contrast Control

There is a voltage regulator circuit to determine liquid crystal operating voltage, V_0 , by adjusting resistors, R_a and R_b , within the range of $|V_4| < |V_0|$. The circuit which is turned on with voltage converter consists of an operational-amplifier circuit and a feedback gain control.

V_{OUT} is the operating voltage for the op-amp, it is required to supply internally or externally. It consists of a feedback gain control for LCD driving contrast curves, eight settings can be selected through software command (Internal resistor ratio $R_{ab2} \sim 0$).

Figure 7-23: Voltage regulator circuit



Also, software command (C1-5) is used to adjust the 64 contrast voltage levels at each voltage regulator feedback gain. The equation of calculating the LCD driving voltage is given as:

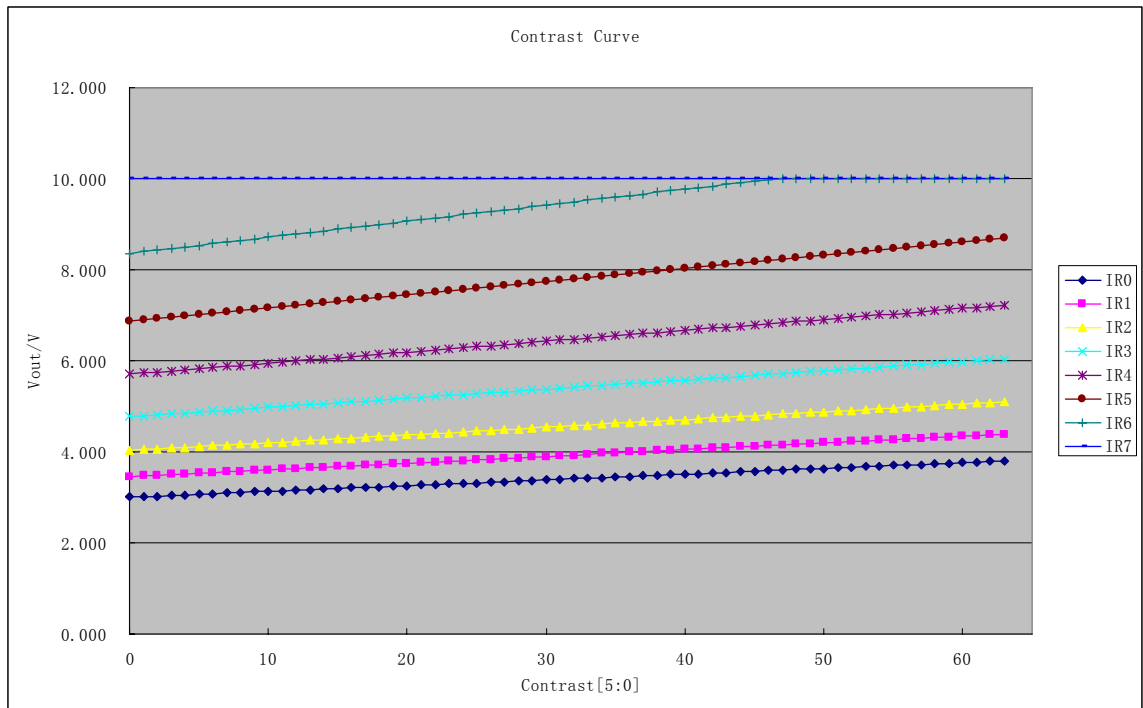
$$V_0 = \left(1 + \frac{R_b}{R_a}\right) \times V_{EV} [V] \text{ -----(Equation 1)}$$

$$V_{EV} = \left[1 - \frac{(63 - \alpha)}{300}\right] \times V_{REF} [V] \text{ --(Equation 2)}$$

, where $V_{REF} = 2$ and $\alpha = \text{contrast setting}_{(d)}$

Please refer to Figure 7-24 for the contrast curve with 8 sets of internal resistor network gain.

Figure 7-24: Contrast curve



c) Bias Divider

If the Don command is enabled, this circuit block will divide the voltage regulator circuit output (V0) to give the LCD driving levels. External stabilizing capacitors for the divider are optional to reduce the external hardware and pin counts.

d) Bias Ratio Selection circuitry

The software control circuit of 1/4 to 1/7 bias ratio in order to match the characteristic of LCD panel.

e) Self adjust temperature compensation circuitry

Provide 4 different compensation grade selections to satisfy the various liquid crystal temperature grades (-0.05%, -0.10%, -0.15%, -0.20%). The grading can be selected by software control. Defaulted temperature coefficient (TC) value is $-0.05\%/^{\circ}\text{C}$.

7.13 Oscillator Circuit

This module is an On-Chip low power temperature compensation oscillator circuitry. The oscillator generates the clock for the DC-DC voltage converter and the Display Timing Generator. User may choose to use internal oscillator clock or supply external clock by CLS pin.

8 Command Table

Table 8-1: Instruction Set

Instruction	IS	RE	Instruction Code										Description
			RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Clear display	X	X	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC.
Return home	X	0	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.
Power down mode	X	1	0	0	0	0	0	0	0	0	1	PD	Set power down mode bit. PD = "1": power down mode set, PD = "0": power down mode disable (POR)
Entry mode set	X	0	0	0	0	0	0	0	0	1	I/D	S	Assign cursor/ blink moving direction with DDRAM address I/D = "1": cursor/ blink moves to right and DDRAM address is increased by 1 (POR) I/D = "0": cursor/ blink moves to left and DDRAM address is decreased by 1 Assign display shift with DDRAM address S = "1": make display shift of the enabled lines by the DS4 to DS1 bits in the shift enable instruction. Left/ right direction depends on I/D bit selection. S = "0": display shift disable (POR)
	X	1	0	0	0	0	0	0	0	1	BDC	BDS	Segment bi-direction function. BDS = "0": Seg100 -> Seg1, BDS = "1": Seg1 -> Seg100. Segment bi-direction function. BDC = "0": Com32 -> Com1 BDC = "1": Com1 -> Com32
Display On/Off control	X	0	0	0	0	0	0	0	1	D	C	B	Set display/cursor/blink on/off D = "1": display on, D = "0": display off (POR), C = "1": cursor on, C = "0": cursor off (POR), B = "1": blink on, B = "0": blink off (POR).
Extended function set	X	1	0	0	0	0	0	0	1	FW	B/W	NW	Assign font width, black/white inverting of cursor, and 4-line display mode control bit. FW = "1": 6-dot font width, FW = "0": 5-dot font width (POR), B/W = "1": black/white inverting of cursor enable, B/W = "0": black/white inverting of cursor disable (POR) NW = "1": 3-line or 4-line display mode, NW = "0": 1-line or 2-line display mode
Cursor or display shift	0	0	0	0	0	0	0	1	S/C	R/L	x	x	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data. S/C = "1": display shift, S/C = "0": cursor shift, R/L = "1": shift to right, R/L = "0": shift to left.

*POR stands for Power On Reset Values.

Instruction	IS	RE	Instruction Code										Description
			RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Double height(4-line)/ Bias/ Display-dot shift	0	1	0	0	0	0	0	1	UD2	UD1	BS1	DH'	UD2~1: Assign different doubt height format (POR=11) BS1:BS0 = "00": 1/5 bias (POR) BS1:BS0 = "01": 1/4 bias BS1:BS0 = "10": 1/7 bias BS1:BS0 = "11": 1/6 bias DH' = "1": display shift enable DH' = "0": dot scroll enable (POR)
Internal OSC frequency	1	0	0	0	0	0	0	1	BS0	F2	F1	F0	F2~0: adjust internal OSC frequency for FE frequency (POR: 011)
Shift enable	1	1	0	0	0	0	0	1	DS4	DS3	DS2	DS1	(when DH' = "1") POR DS4~1=1111 Determine the line for display shift. DS1 = "1/0": 1st line display shift enable/disable DS2 = "1/0": 2nd line display shift enable/disable DS3 = "1/0": 3rd line display shift enable/disable DS4 = "1/0": 4th line display shift enable/disable.
Scroll enable	1	1	0	0	0	0	0	1	HS4	HS3	HS2	HS1	(when DH' = "0") POR HS4~1=1111 Determine the line for horizontal smooth scroll. HS1 = "1/0": 1st line dot scroll enable/disable HS2 = "1/0": 2nd line dot scroll enable/disable HS3 = "1/0": 3rd line dot scroll enable/disable HS4 = "1/0": 4th line dot scroll enable/disable.
Function set	X	0	0	0	0	0	1	DL	N	DH	RE (0)	IS	Set interface data length DL = "1": 8-bit (POR), DL = "0": 4-bit Numbers of display line when NW = "0", N = "1": 2-line (NW=0)/ 4-line(NW=1), N = "0": 1-line (NW=0)/ 3-line(NW=1) Extension register, RE("0") Shift/scroll enable DH = "1/0": Double height font control for 2-line mode enable/disable (POR=0) Extension register, IS
	X	1	0	0	0	0	1	DL	N	BE	RE (1)	REV	Set DL, N, RE("1") CGRAM/SEGRAM blink enable BE = "1/0": CGRAM/SEGRAM blink enable/disable (POR=0) Reverse bit REV = "1": reverse display, REV = "0": normal display (POR).
set CGRAM address	0	0	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter. (POR=00 0000)
set SEGRAM address	1	0	0	0	0	1	0	0	AC3	AC2	AC1	AC0	Set SEGRAM address in address counter. (POR=0000)
Power/ Icon control/ Contrast set	1	0	0	0	0	1	0	1	Ion	Bon	C5	C4	Ion = "1/0": ICON (SEGRAM) display on/off (POR=0) Bon = "1/0": set booster and regulator circuit on/off (POR=0) C5, C4: Contrast set for internal follower mode (POR=10)

Instruction	IS	RE	Instruction Code										Description
			RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Follower Control	1	0	0	0	0	1	1	0	Don	Rab2	Rab1	Rab0	Don: Set divider circuit on/ off (POR=0) Rab2~0: Select Amplifier internal resistor ratio (POR=010)
Contrast Set	1	0	0	0	0	1	1	1	C3	C2	C1	C0	C3~0: Contrast set for internal follower mode (POR=0000)
set DDRAM address	X	0	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter. (POR=000 0000)
set scroll quantity	X	1	0	0	1	X	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Set the quantity of horizontal dot scroll. (POR=00 0000)
Read busy flag and address/ part ID	X	X	0	1	BF	AC6 / ID6	AC5 / ID5	AC4 / ID4	AC3 / ID3	AC2 / ID2	AC1 / ID1	AC0 / ID0	Can be known whether during internal operation or not by reading BF. The contents of address counter or the part ID can also be read. When it is read the first time, the address counter can be read. When it is read the second time, the part ID can be read. BF = "1": busy state BF = "0": ready state
write data	X	X	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM / CGRAM / SEGRAM).
read data	X	X	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM / CGRAM / SEGRAM).

Table 8-2: Extended Instruction Set

Instruction	IS	RE	Instruction Code										Description
			RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Temperature Coefficient Control	X	1	0	0	0	1	1	1	0	1	1	0	Set Temperature Coefficient TC2~0: 000: Reserved 001: Reserved 010: -0.05%/° C (POR) 011: Reserved 100: -0.10%/° C 101: Reserved 110: -0.15%/° C 111: -0.20%/° C
Temperature Coefficient Control Settings	X	X	1	0	0	0	0	0	0	TC2	TC1	TC0	

Instruction	IS	RE	Instruction Code										Description
			RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
ROM Selection	X	1	0	0	0	1	1	1	0	0	1	0	Writing data into ROM selection register enables the selection of ROMA, B or C.
ROM Selection Settings	X	X	1	0	0	0	0	0	ROM2	ROM1	0	0	ROM2~1: 00: ROMA 01: ROMB 10: ROMC 11: Invalid

9 COMMAND DESCRIPTIONS

9.1 Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

9.2 Return Home (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM do not change.

9.3 Power Down Mode set (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	PD

Power down mode enable bit set instruction. When PD = "High", it makes SSD1803A suppress current consumption except the current needed for data storage by executing next three functions.

- Make the output value of all the COM/SEG ports VSS
- Disable voltage converter to remove the current through the divide resistor of power supply.
You can use this instruction as power sleep mode.
- When PD = "Low", power down mode becomes disabled.

9.4 Entry Mode Set

RE = 0

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.

I/D: Increment/decrement of DDRAM address (cursor or blink)

When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.

When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.

- CGRAM/SEGRAM operates the same as DDRAM, when read from or write to CGRAM/SEGRAM.

When S = "High", after DDRAM write, the display of enabled line by DS1 - DS4 bits in the shift enable instruction is shifted to the right (I/D = "0") or to the left (I/D = "1"). But it will seem as if the cursor does not move. When S = "Low", or DDRAM read, or CGRAM/SEGRAM read/write operation, shift of display like this function is not performed.

RE = 1

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	BDC	BDS

Set the data shift direction of segment in the application set.

BDC: Data shift direction of common

When BDC = "Low", common data shift direction is set to reverse from COM32 to COM1.

When BDC = "High", common data shift direction is set to normal order from COM1 to COM32.

BDS: Data shift direction of segment

When BDS = "Low", segment data shift direction is set to reverse from SEG100 to SEG1.

When BDS = "High", segment data shift direction is set to normal order from SEG1 to SEG100.

By using this instruction, you can raise the efficiency of application board area.

- The BID setting instruction is recommended to be set at the same time level of function set instruction.

9.5 Display ON/OFF Control (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF control bit

When D = "High", entire display is turned on.

When D = "Low", display is turned off, but display data is remained in DDRAM.

C: Cursor ON/OFF control bit

When C = "High", cursor is turned on.

When C = "Low", cursor is disappeared in current display, but I/D register remains its data.

B: Cursor Blink ON/OFF control bit

When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position. If fosc has 540kHz frequency, blinking has 370 ms interval.

When B = "Low", blink is off.

9.6 Extended Function Set (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	FW	B/W	NW

FW: Font Width control

When FW = "High", display character font width is assigned to 6-dot and execution time becomes 6/5 times than that of 5-dot font width.

The user font, specified in CGRAM, is displayed into 6-dot font width, bit-5 to bit-0, including the leftmost space bit of CGRAM. (refer to Figure 9-1)

When FW = "Low", 5-dot font width is set.

B/W: Black/White Inversion enable bit

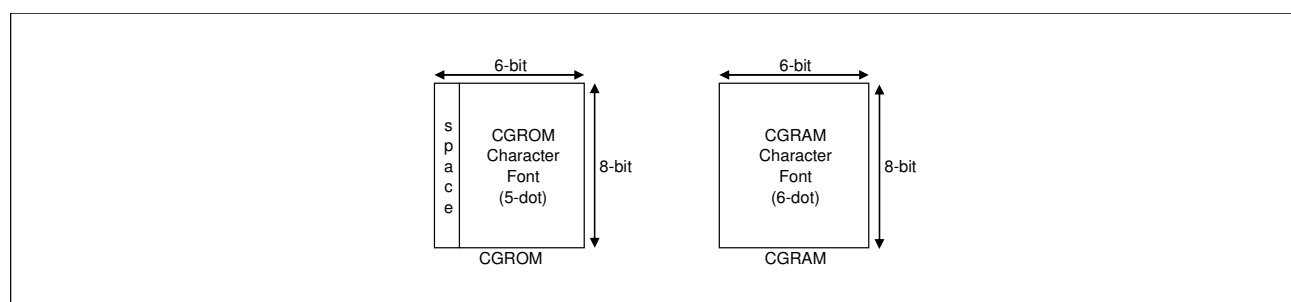
When B/W = "High", black/white inversion at the cursor position is set. In this case C/B bit of display ON/OFF control instruction becomes don't care condition. If fosc has frequency of 540kHz, inversion has 370 ms intervals.

NW: 4 Line mode enable bit

When NW = "High", 3 or 4 line display mode is set. In this case N bit of function set instruction becomes don't care condition.

When NW = "Low", 1 or 2 line display mode is set. In this case N bit of function set instruction becomes don't care condition.

Figure 9-1: 6-dot Font Width CGROM/CGRAM



9.7 Cursor or Display Shift / Bias Ratio Select (IS = 0, RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	X	X

Shift right/left cursor position or display, without writing or reading of display data, this instruction is use to corrector search display data (refer to Table 9-1). During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. When 4-line mode, cursor moves to the next line, only after every 20th digit of the current line. Note that display shift is performed simultaneously in all the line enabled by DS1-DS4 in the shift enable instruction. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

Table 9-1: Shift patterns According to S/C and R/L Bits

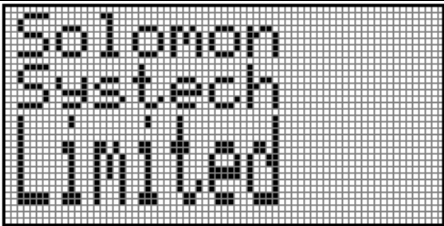
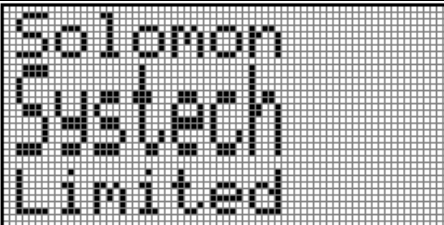
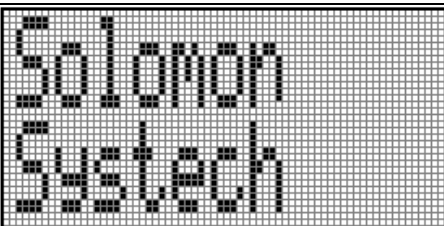
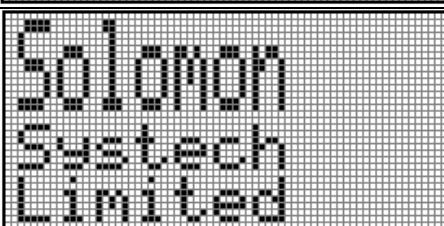
S/C	R/L	Operation
0	0	Shift cursor to the left, address counter is decreased by 1.
0	1	Shift cursor to the right, address counter is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display.
1	1	Shift all the display to the right, cursor moves according to the display.

9.8 Double height(4-line)/ Bias/ Display-dot shift (IS = 0, RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	UD2	UD1	BS1	DH'

UD2, UD1: Assign different double height features, it is applicable to different line display mode when DH=1. Note that UD1=0 and UD2=0 are forbidden in 2-line display mode. UD1=0 is forbidden in 3-line display mode.

Table 9-2: Double Height Display According to UD2 and UD1 Bits (when DH=1)

UD2	UD1	Character Displays
0	0	
0	1	
1	0	
1	1	

BS1, BS0 (included in Internal divider/ OSC frequency register) define the internal divider bias:

Table 9-3: Bias divider According to BS1 and BS0 Bits

BS1	BS0	Bias
0	0	1/5 bias (POR)
0	1	1/4 bias
1	0	1/7 bias
1	1	1/6 bias

DH': Display shift enable selection bit.

When DH' = "High", display shift per line becomes enable.

When DH' = "Low", smooth dot scroll becomes enable.

9.9 Internal divider / OSC frequency (IS = 1, RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	BS0	F2	F1	F0

BS0 works with BS1, which is defined in Table 9-3

F2 : 0 : defines internal oscillator frequency

Table 9-4: Oscillator Frequency According to F2:0 bits

F2	F1	F0	Oscillator Frequency (kHz)
1	1	1	680
1	1	0	640
1	0	1	620
1	0	0	580
0	1	1	540(POR)
0	1	0	500
0	0	1	460
0	0	0	420

9.10 Shift/Scroll Enable (IS = 1, RE = 1)

DH' = 0

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	HS4	HS3	HS2	HS1

HS: Horizontal scroll per line enable

This instruction makes valid dot shift by a display line unit. HS1, HS2, HS3 and HS4 indicate each line to be dot scrolled, and each scroll is performed individually in each line.

If you want to scroll the line in 1-line display mode, set HS1 to “High”.

If the 2nd line scroll is needed in 2-line mode, set HS2 to “High”. (refer to Table 9-5)

DH' = 1

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	DS4	DS3	DS2	DS1

DS: Display shift per line enable this instruction selects shifting line to be shifted according to each line mode in display shift right/left instruction. DS1, DS2, DS3 and DS4 indicate each line to be shifted, and each shift is performed individually in each line.

If you set DS1 and DS2 to “High” (enable) in 2 line mode, 1st line and 2nd line are shifted. If all the DS bits (DS1 to DS4) are set to “Low” (disable), no display is shifted.

Table 9-5: Relationship between DS and COM signal

Enable Bit	Enabled Common Signals During Shift	Description
HS1/DS1	COM1 – COM8	The part of display line that corresponds to enabled common signal can be shifted.
HS2/DS2	COM9 – COM16	
HS3/DS3	COM17 – COM24	
HS4/DS4	COM25 – COM32	

9.11 Function Set

RE = 0

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	DH	RE(0)	IS

DL: Interface data length control bit

When DL = “High”, it means 8-bit bus mode with MPU.

When DL = “Low”, it means 4-bit bus mode with MPU.

So to speak, DL is a signal to select 8-bit or 4-bit bus mode.

When 4-bit bus mode, it needs to transfer 4-bit data by two times.

N: Display line number control bit

It is variable only when NW bit of extended function set instruction is low.

When N = “Low”, 1-line display mode (for NW=0), or 3-line display mode (for NW=1).

When N = “High”, 2-line display mode is set (for NW=0), or 4-line display mode (for NW=1).

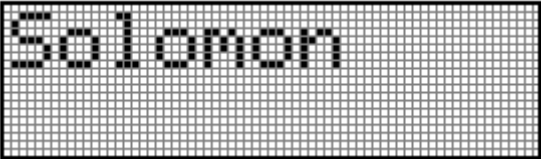
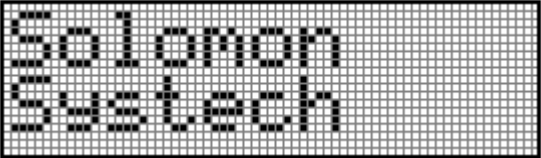
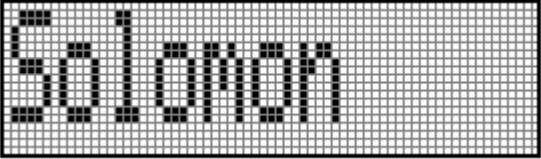
When NW = “High”, N bit is invalid, it means 4-line mode independent of N bit.

RE: Extended function registers enable bit

At this instruction, RE must be “Low”.

DH: When DH= “High”, UD2=1 and UD1=1 Double height font type control bit for 2 line mode:

Table 9-6: Double Height display when DH=1, UD2=1 and UD1=1

NW	N	DH	Character Displays		
			Display lines	Character font	
0	0	0	1	5 x 8	
0	0	1	1	Forbidden	
0	1	0	2	5 x 8	
0	1	1	2	5 x 16	

When DH= “Low”, Double height font type control is disabled.

IS: Special registers enable bit

At this moment, IS must be “Low”.

RE = 1

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	BE	RE(1)	REV

DL: Interface data length control bit

When DL = “High”, it means 8-bit bus mode with MPU.

When DL = “Low”, it means 4-bit bus mode with MPU.

So to speak, DL is a signal to select 8-bit or 4-bit bus mode.

When 4-bit bus mode, it needs to transfer 4-bit data by two times.

- N: Display line number control bit
It is variable only when NW bit of extended function set instruction is low.
When N = “Low”, 1-line display mode (for NW=0), or 3-line display mode (for NW=1).
When N = “High”, 2-line display mode is set (for NW=0), or 4-line display mode (for NW=1).
When NW = “High”, N bit is invalid, it means 4-line mode independent of N bit.
- BE: CGRAM/SEGRAM data blink enable bit
If BE is “High”, It makes user font of CGRAM and segment of SEGRAM blink. The quantity of blink is assigned the highest 2 bit of CGRAM/SEGRAM.
- RE: Extended function registers enable bit
When RE = “High”, power down mode registers, extended function set registers, SEGRAM address set registers, BDC/ BDS bits, HS/DS bits of shift/scroll enable instruction and BE/ REV bits of function set register can be accessed.
- REV: Reverse enable bit
When REV = “High”, all the display data are reversed. Namely, all the white dots become black and black dots become white.
When REV = “Low”, the display mode set normal display.

9.12 Set CGRAM Address (IS = 0, RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC. This instruction makes CGRAM data available from MPU.

9.13 Set SEGRAM Address (IS = 1, RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	AC3	AC2	AC1	AC0

Set SEGRAM address to AC. This instruction makes SEGRAM data available from MPU.

9.14 Power/ Icon Control/ Contrast Set (IS = 1, RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	Ion	Bon	C5	C4

- Ion: Set ICON display on/off
When Ion = “High”, ICON display on.
When Ion = “Low”, ICON display off.
- Bon: Switch DCDC converter and regulator circuit
When Bon = “High”, DCDC converter and regulator circuit is turn on.
When Bon = “Low”, DCDC converter and regulator circuit is turn off.
- C5,C4 : Contrast set(high byte)
C5,C4,C3,C2,C1,C0 can more precisely adjust the input reference voltage of V0 generator. The details please refer to LCD driving voltage generator of block descriptions.

9.15 Follower Control (IS = 1, RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	Don	Rab2	Rab1	Rab0

Don: Switch divider circuit

When Don = “High”, internal divider circuit is turn on.

When Don = “Low”, internal divider circuit is turn off.

Rab2,Rab1,Rab0 : V0 generator internal resistor ratio

Rab2,Rab1,Rab0 can adjust the amplified ratio of V0 generator. The details please refer to LCD driving voltage generator of block descriptions.

Table 9-7: Internal Resistor Ratio for LCD Driving Voltage

	Rab2	Rab1	Rab0	1+Rb/Ra
IR7	1	1	1	6.5
IR6	1	1	0	5.3
IR5	1	0	1	4.4
IR4	1	0	0	3.6
IR3	0	1	1	3.0
IR2	0	1	0	2.6
IR1	0	0	1	2.2
IR0	0	0	0	1.9

9.16 Contrast Set (IS = 1, RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	C3	C2	C1	C0

C3,C2,C1,C0:Contrast set(low byte)

C5,C4,C3,C2,C1,C0 can more precisely adjust the input reference voltage of V0 generator. The details please refer to LCD driving voltage generator of block descriptions.

9.17 Set DDRAM Address (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC. This instruction makes DDRAM data available from MPU.

When 1-line display mode (N = 0, NW = 0), DDRAM address is from “00H” to “4FH”.

In 2-line display mode (N = 1, NW = 0), DDRAM address in the 1st line is from “00H” – “27H”, and DDRAM address in the 2nd line is from “40H” – “67H”.

In 3-line display mode (N=0, NW = 1), DDRAM address is from “00H” – “13H” in the 1st line, from “20H” to “33H” in the 2nd line and from “40H” – “53H” in the 3rd line.

In 4-line display mode (N=1, NW = 1), DDRAM address is from “00H” – “13H” in the 1st line, from “20H” to “33H” in the 2nd line, from “40H” – “53H” in the 3rd line and from “60H” – “73H” in the 4th line.

9.18 Set Scroll Quantity (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	X	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0

As set SQ5 to SQ0, horizontal scroll quantity can be controlled in dot units (Refer to Table 9-8). In this case SSD1803A can show hidden areas of DDRAM by executing smooth scroll from 1 to 48 dots.

Table 9-8: Scroll Quantity According to HDS Bits

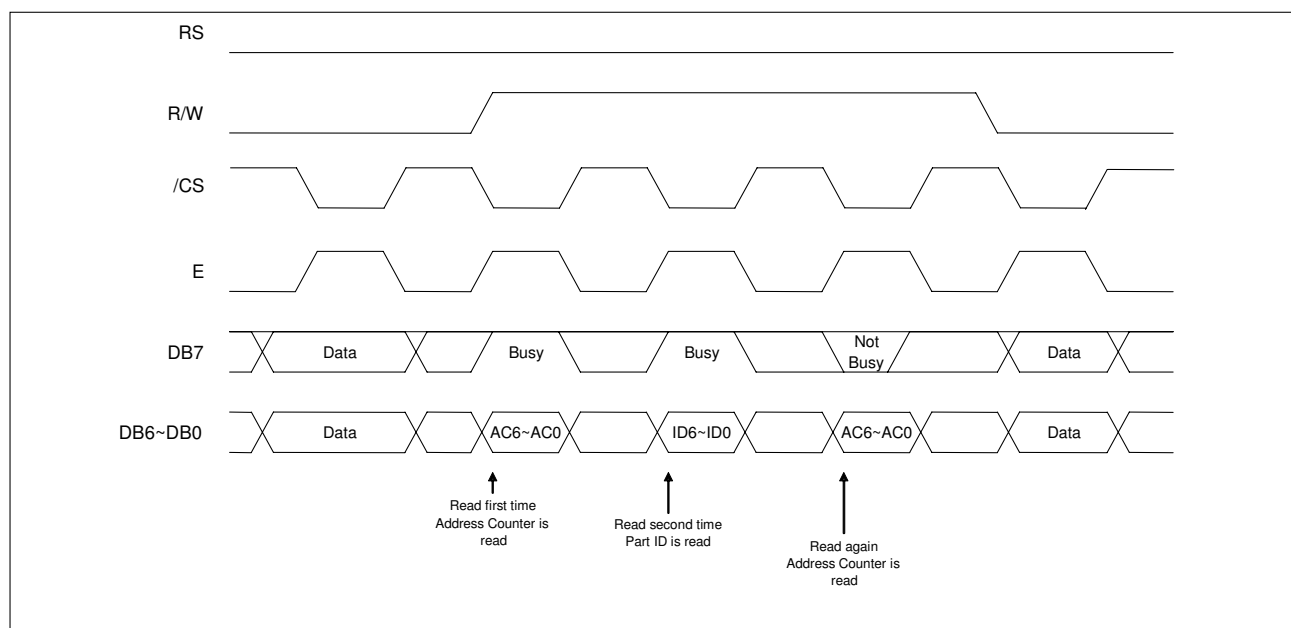
SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Function
0	0	0	0	0	0	No shift
0	0	0	0	0	1	Shift left by 1-dot
0	0	0	0	1	0	Shift left by 2-dot
0	0	0	0	1	1	Shift left by 3-dot
:	:	:	:	:	:	:
1	0	1	1	1	1	Shift left by 47-dot
1	1	X	X	X	X	Shift left by 48-dot

9.19 Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6/ID6	AC5/ID5	AC4/ID4	AC3/ID3	AC2/ID2	AC1/ID1	AC0/ID0

This instruction shows whether SSD1803A is in internal operation or not. If the resultant BF is High, it means the internal operation is in progress and you have to wait until BF to be Low, and then the next instruction can be performed. In this instruction you can read also the value of address counter or the part ID. When the first time the instruction is run, you can read the address counter. When the instruction is run the second time, you can read the part ID (refer to Figure 9-2).

Figure 9-2: Read Busy Flag & Address/Part ID (6800 – parallel interface)



Part Number	Part ID
SSD1803AM1V	0011010

9.20 Write Data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM/SEGRAM. The selection of RAM from DDRAM, CGRAM, or SEGRAM, is set by the previous address set instruction: DDRAM address set, CGRAM address set, SEGRAM address set. RAM set instruction can also determine the AC direction to RAM. After write operation, the address is automatically increased/ decreased by 1, according to the entry mode.

9.21 Read Data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM/SEGRAM. The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data. In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction: it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM/SEGRAM read operation, display shift may not be executed correctly. In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

In order to match the operating frequency of the GDDRAM with that of the MCU, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read.

9.22 Extended Instruction Set

Extended instruction set includes a register selection and writing a data into the register. By writing temperature coefficient register, user can select one out of four TC settings. Similarly, by writing ROM selection register, user can select using ROMA, ROMB or ROMC by software settings.

10 MAXIMUM RATINGS

Table 10-1 Maximum Ratings (Voltage Referenced to VSS)

Symbol	Parameter	Value	Unit
V _{DDIO}	Power Supply Voltage	-0.3 to 6.0	V
V _{DD}		-0.3 to 6.0	
V _{CI}		-0.3 to 6.0	
V _{LCD}		-0.3 to 15.0	V
V _{IN}	Input Voltage	-0.3 to V _{DD} + 0.3	V
T _A	Operating Temperature	-40 to 85	°C
T _{STG}	Storage Temperature	-55 to 125	°C

Voltage greater than above may damage to the circuit ($V_0 \geq V_1 \geq V_4 \geq V_3 \geq V_4 \geq V_{SS}$)

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DDIO}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

11 DC CHARACTERISTICS

Conditions (Unless Otherwise Specified):

Voltage referenced to V_{SS}

V_{DD} = 2.4 to 3.6V

T_A = -40 to 85°C

Table 11-1: DC Characteristics

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V _{DDIO}	Operating Voltage	Low Voltage I/O Application		2.4	3	V _{CI}	V
		5V I/O Application		4.5	5	5.5	V
V _{DD}	Operating Voltage	Low Voltage I/O Application		2.4	3	3.6	V
		5V I/O Application (V _{DD} as output)		-	-	-	V
V _{CI}	Operating Voltage	-		V _{DD}	V _{DD}	V _{DD}	V
I _{DD}	Supply Current	Internal oscillation (V _{DD} = 3.0V, f _{OSC} = 540kHz)		-	0.3	0.55	mA
V _{IH}	Input Voltage	-		0.8V _{DDIO}	-	V _{DDIO}	V
V _{IL}		-		-	-	0.2V _{DDIO}	
V _{OH1}	Output Voltage 1 (DB0-DB7)	I _{OH} = -0.1mA		0.8V _{DDIO}	-	-	V
V _{OL1}		I _{OL} = 0.1mA		-	-	0.2V _{DDIO}	V
V _{OH2}	Output Voltage 2 (except DB0-DB7)	I _O = -40μA		0.8V _{DDIO}	-	-	V
V _{OL2}		I _O = 40μA		-	-	0.2V _{DDIO}	V
V _{dCOM}	Voltage Drop	I _O = ± 0.1mA		-	-	1	V
V _{dSEG}				-	-	1	
I _{LKG}	Input Leakage Current	V _{IN} = 0V – V _{DD}		-1	-	1	μA
I _{IL}	Low Input Current	V _{IN} = 0V, V _{DD} = 3V (pull up)		-10	-50	-120	
f _{OSC}	Internal Clock	V _{DD} = 3.0V		480	540	600	kHz
f _{ECLKIN}	External Clock	-		250	540	820	kHz
duty				45	50	55	%
tr, tf				-	-	0.2	μs
V _{out}	Voltage Converter Output	T _a =25°C, C=1μF, f _{osc} =540kHz	V _{CI} =2.4V, I _{out} =0.15mA	6.4	7.1	-	V
			V _{CI} =3.0V, I _{out} =0.20mA	7.5	8.1	-	
			V _{CI} =3.6V, I _{out} =0.25mA	9.6	10.5	-	
V _{LCD}	LCD Driving Voltage	V ₀ – V _{SS}		3.0	-	10.0	V
TC2	Temperature Coefficient Compensation Flat Temperature Coefficient (POR)	V _{DD} = 3.0V T _A = -40 to 85°C		-0.04	-0.05	-0.06	%/°C
TC4	Temperature Coefficient 4			-0.09	-0.10	-0.11	%/°C
TC6	Temperature Coefficient 6			-0.14	-0.15	-0.16	%/°C
TC7	Temperature Coefficient 7			-0.19	-0.20	-0.21	%/°C

$$TC(\%) = \frac{V_{ref} \text{ at } 50^{\circ}\text{C} - V_{ref} \text{ at } 0^{\circ}\text{C}}{50^{\circ}\text{C} - 0^{\circ}\text{C}} \times \frac{1}{V_{ref} \text{ at } 25^{\circ}\text{C}} \times 100\%$$

12 AC CHARACTERISTICS

Conditions (Unless Otherwise Specified):

Voltage referenced to V_{SS}

$V_{DD} = 2.4$ to $3.6V$

$T_A = -40$ to $85^{\circ}C$

Table 12-1: Oscillator Frequency

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$F_{OSC}^{(1)}$	Oscillator frequency	$V_{DD} = 2.4$ to $3.6V$ $T_A = -40$ to $85^{\circ}C$	480	540	600	kHz

Table 12-2: Frame Frequency in Different Line Mode

Display Mode	Duty Cycle	Line Period (clocks)		Frame Frequency (Hz)	
		5-dot	6- dot	5-dot	6- dot
1-line display mode	1/9	370	440	81	68
2-line display mode	1/17	200	240	79	66
3-line display mode	1/25	130	160	83	68
4-line display mode	1/33	100	120	82	68

Note

⁽¹⁾ F_{OSC} stands for the frequency value of the internal oscillator.

12.1 CPU Interface Timing

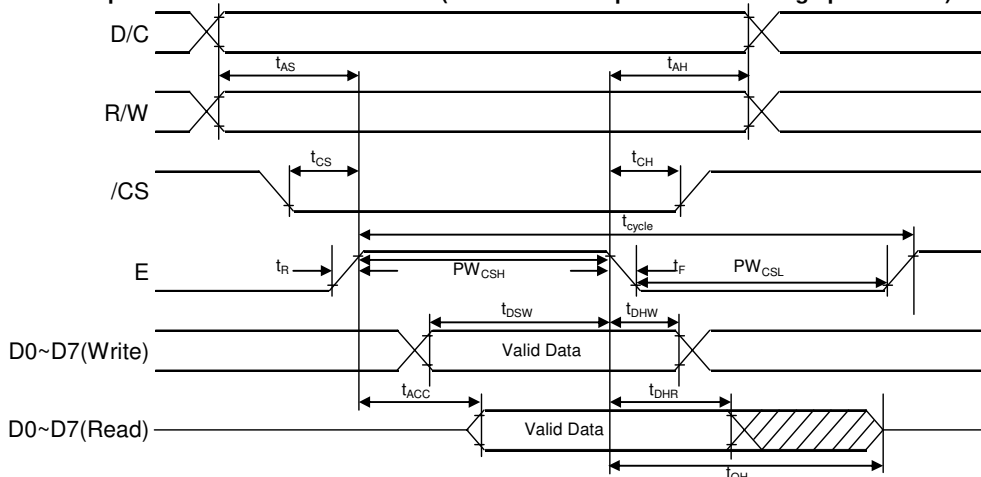
12.1.1 Parallel 6800-series Interface Timing

Table 12-3: Parallel Timing Characteristics (TA = -40 to 85° C, VDDIO = 2.4-3.6/ 4.5-5.5V, VSS =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t _{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t _{AS}	Address Setup Time	13	-	-	ns
t _{AH}	Address Hold Time	17	-	-	ns
t _{CS}	Chip Select Time	0	-	-	ns
t _{CH}	Chip Select Hold Time	0	-	-	ns
t _{DSW}	Write Data Setup Time	35	-	-	ns
t _{DHW}	Write Data Hold Time	13	-	-	ns
t _{DHR}	Read Data Hold Time	13	-	-	ns
t _{OH}	Output Disable Time	10	-	90	ns
t _{ACC}	Access Time (RAM)	-	-	125	ns
	Access Time (command)	-	-	125	ns
PW _{CSL}	Chip Select Low Pulse Width (read RAM)	250	-	-	ns
	Chip Select Low Pulse Width (read Command)	250	-	-	ns
	Chip Select Low Pulse Width (write)	50	-	-	ns
PW _{CSH}	Chip Select High Pulse Width (read)	155	-	-	ns
	Chip Select High Pulse Width (write)	55	-	-	ns
t _R	Rise Time	-	-	15	ns
t _F	Fall Time	-	-	15	ns

Note: All timings are based on 20% to 80% of V_{DDIO}-V_{SS}

6800-series parallel interface characteristics (Form 1: /CS low pulse width > E high pulse width)



6800-series parallel interface characteristics (Form 2: /CS low pulse width < E high pulse width)

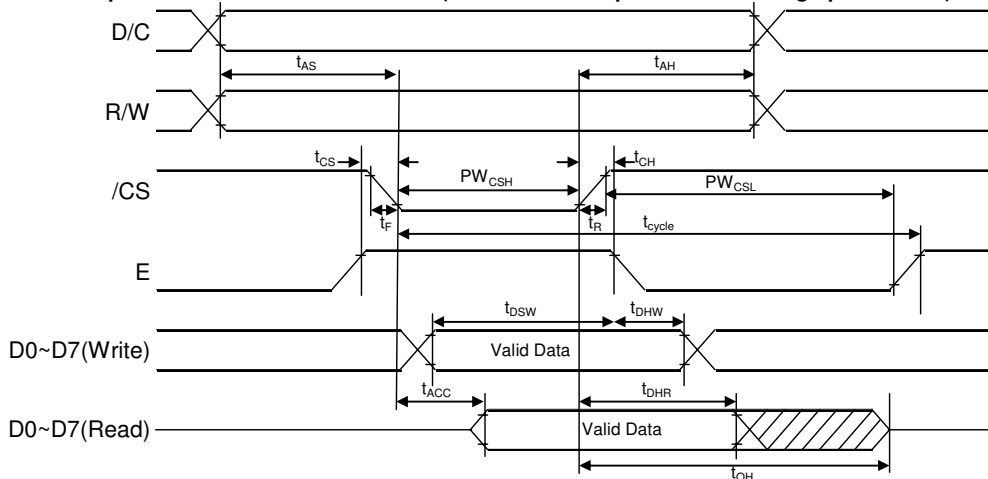


Figure 12-1 : Parallel 6800-series Interface Timing Characteristics (IM2 = H, IM1 = H)

Table 12-4 : Serial Timing Characteristics (TA = -40 to 85 ° C, VDDIO = 2.4-3.6/ 4.5-5.5V, VSS =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_c	Serial clock cycle time	1	-	20	us
t_r, t_f	Serial clock rise/fall time	-	-	50	ns
t_w	Serial clock width (high, low)	400	-	-	ns
t_{su1}	Chip select setup time	60	-	-	ns
t_{h1}	Chip select hold time	20	-	-	ns
t_{su2}	Serial input data setup time	200	-	-	ns
t_{h2}	Serial input data hold time	200	-	-	ns
t_D	Serial output data delay time	-	-	360	ns
t_{DH}	Serial output data hold time	5	-	-	ns

Note: All timings are based on 20% to 80% of $V_{DDIO}-V_{SS}$

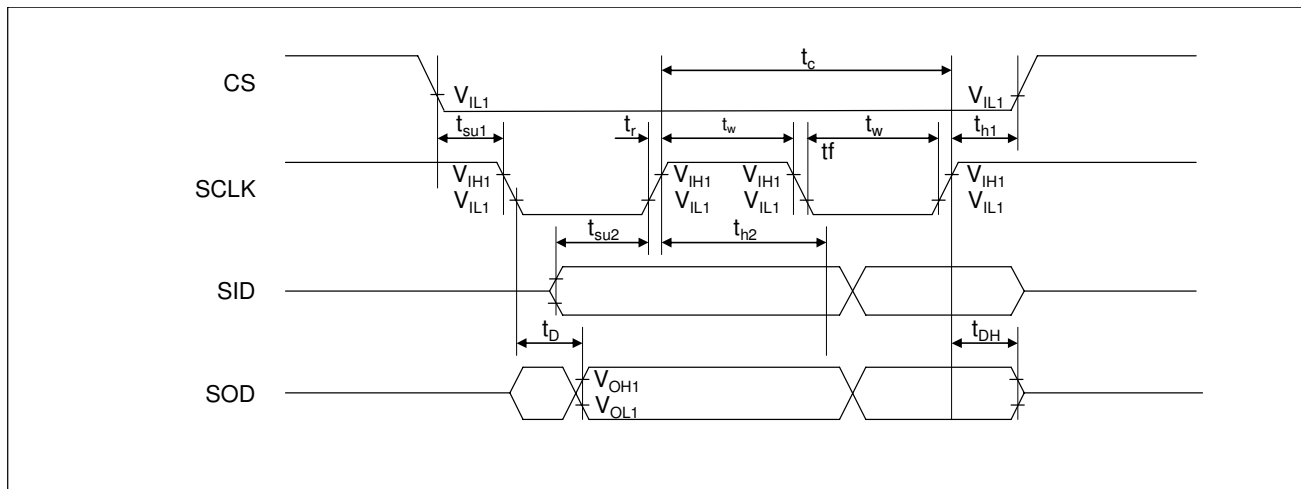


Figure 12-2 : Serial Timing Characteristics (IM2 = L, IM1 = H)

Table 12-5 : I2C Timing Characteristics (TA = -40 to 85° C, VDDIO = 2.4-3.6/ 4.5-5.5V, VSS =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t _{cycle}	Clock Cycle Time	2.5	-	-	us
t _{HSTART}	Start condition Hold Time	0.6	-	-	us
t _{HD}	Data Hold Time (for “SDA _{OUT} ” pin)	0	-	-	ns
	Data Hold Time (for “SDA _{IN} ” pin)	300	-	-	ns
t _{SD}	Data Setup Time	100	-	-	ns
t _{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t _{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t _R	Rise Time for data and clock pin	-	-	300	ns
t _F	Fall Time for data and clock pin	-	-	300	ns
t _{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

Note: All timings are based on 20% to 80% of V_{DDIO}-V_{SS}

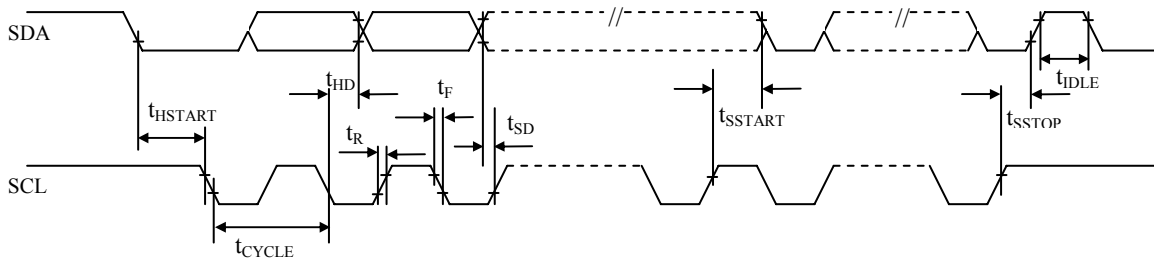
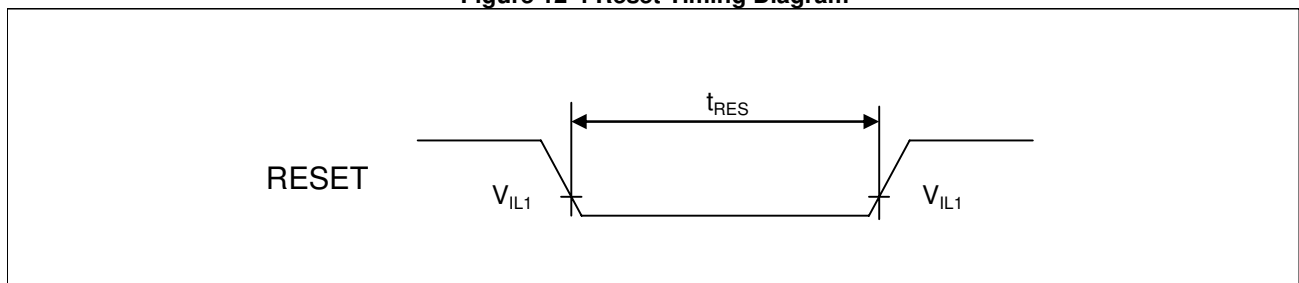


Figure 12-3 : I2C Timing Characteristics (IM2 = L, IM1 = H)

Table 12-6: Reset Timing (TA = -40 to 85° C, VDD = 2.4-3.6, VSS =0V)

Item	Symbol	Min	Typ	Max	Unit
Reset Low level (refer to figure 12-4)	t _{RES}	20	-	-	us

Figure 12-4 Reset Timing Diagram



13 APPLICATION EXAMPLES

13.1 Application Example I (I2C interface, 3-line display, 3V VDDIO mode)

Figure 13-1: Block Diagram of Application Example I

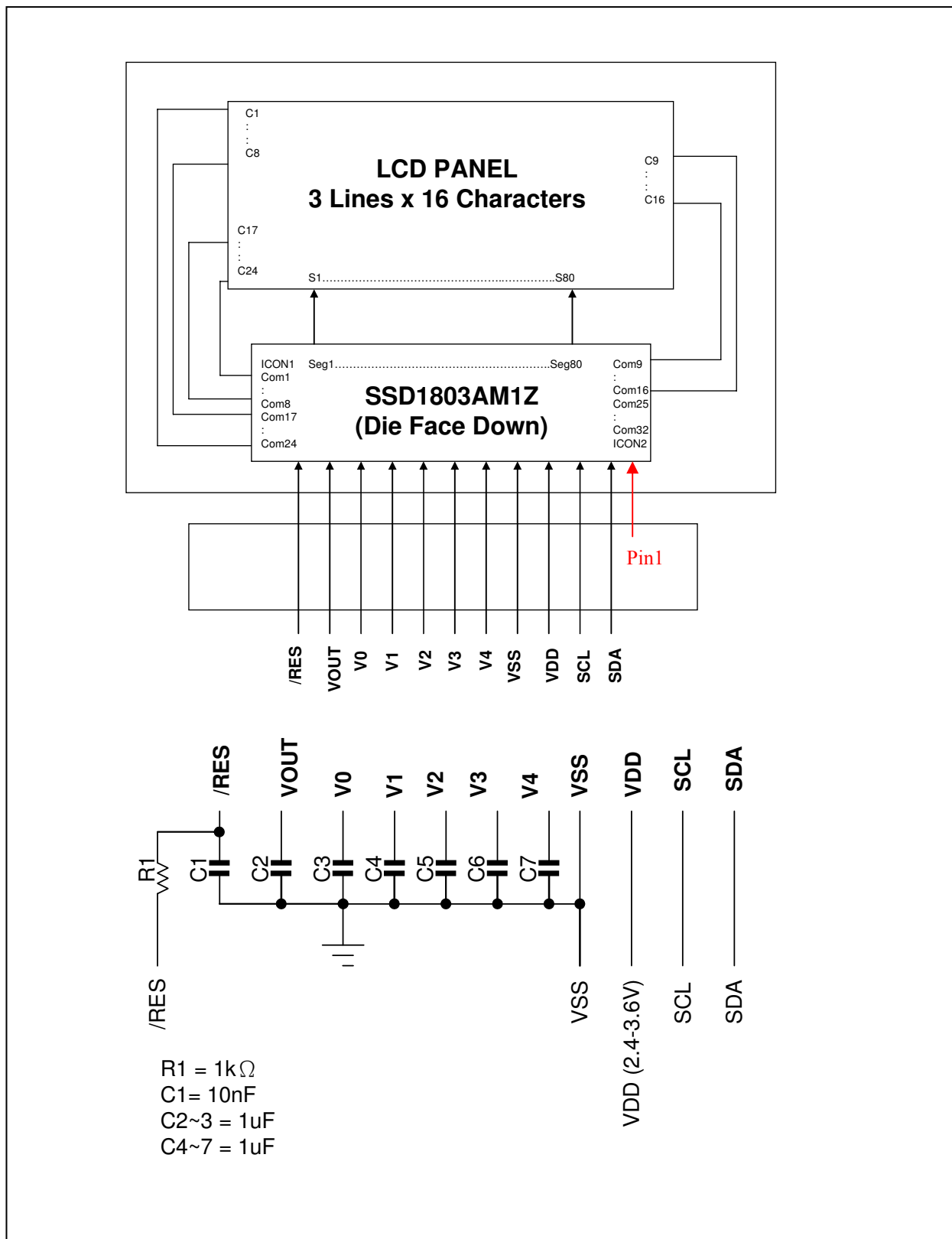
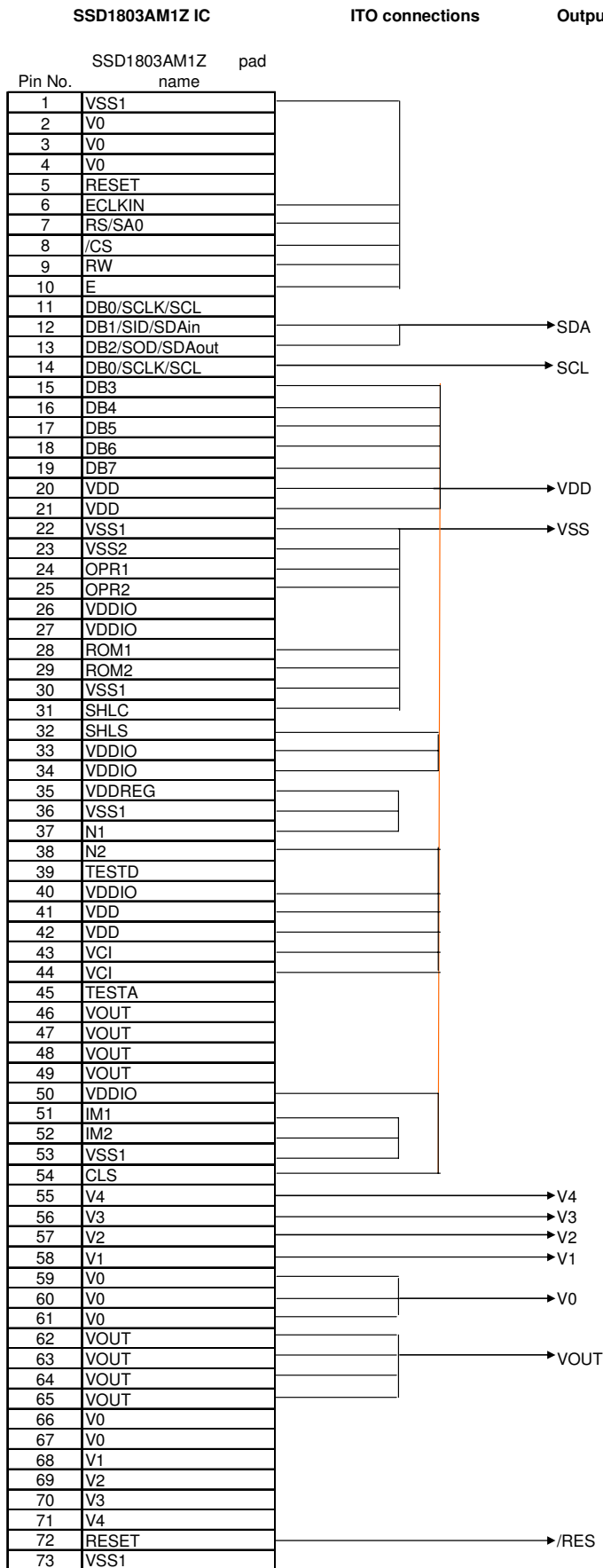


Figure 13-2: Pin Connections of Application Example I



13.2 Application Example II (4-line display, 5V IO mode)

Figure 13-3: Block Diagram of Application Example II

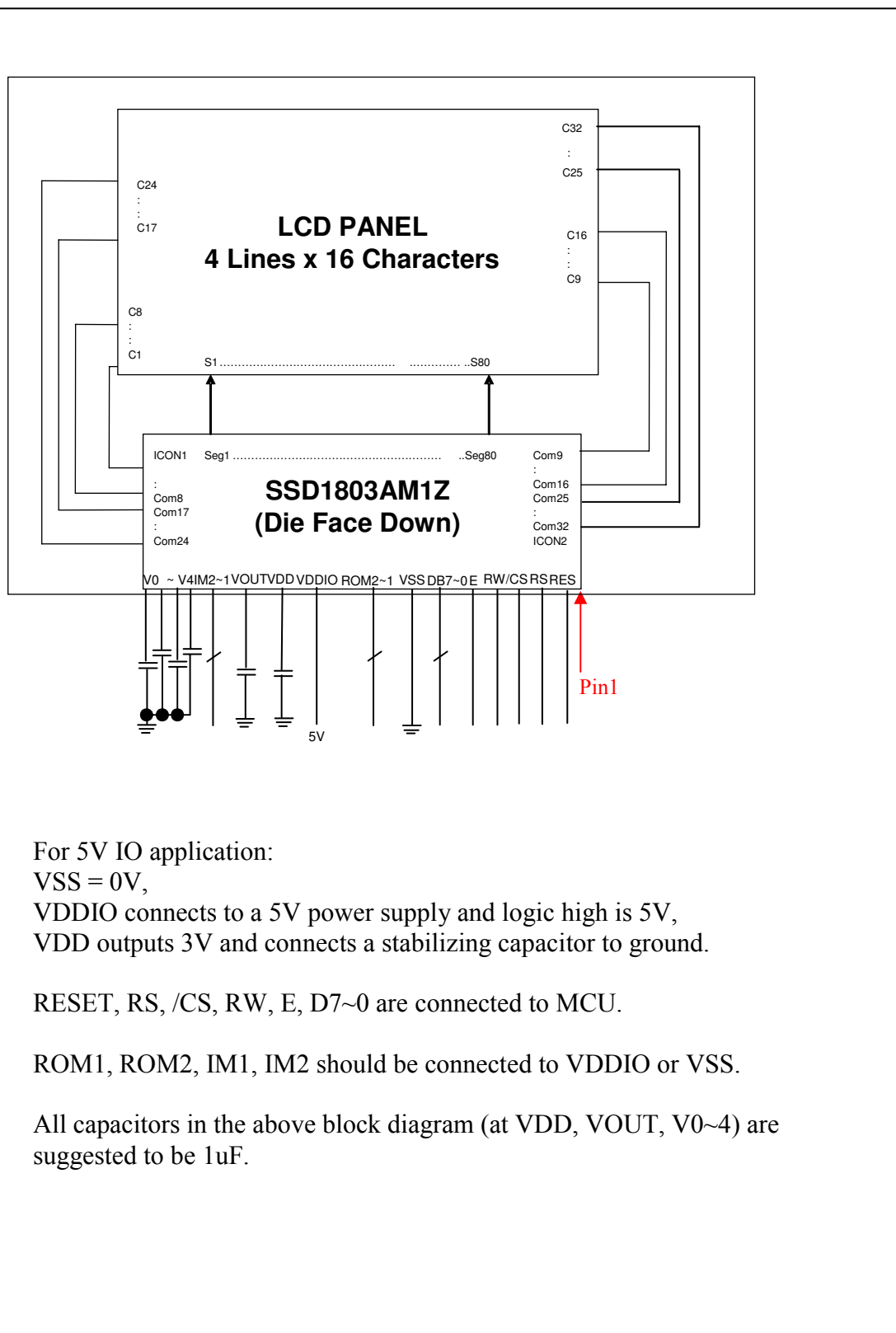
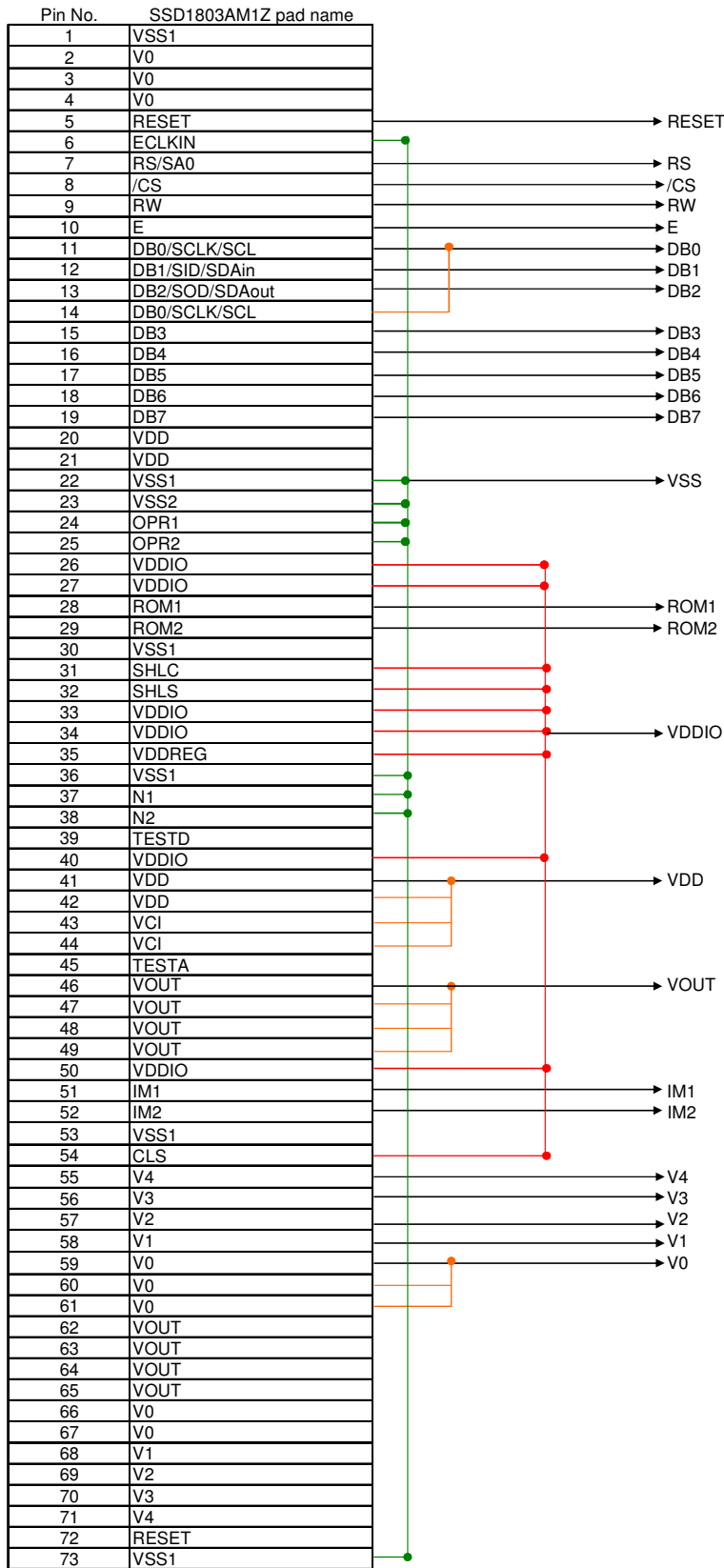


Figure 13-4: Pin Connections of Application Example II

SSD1803AM1Z IC

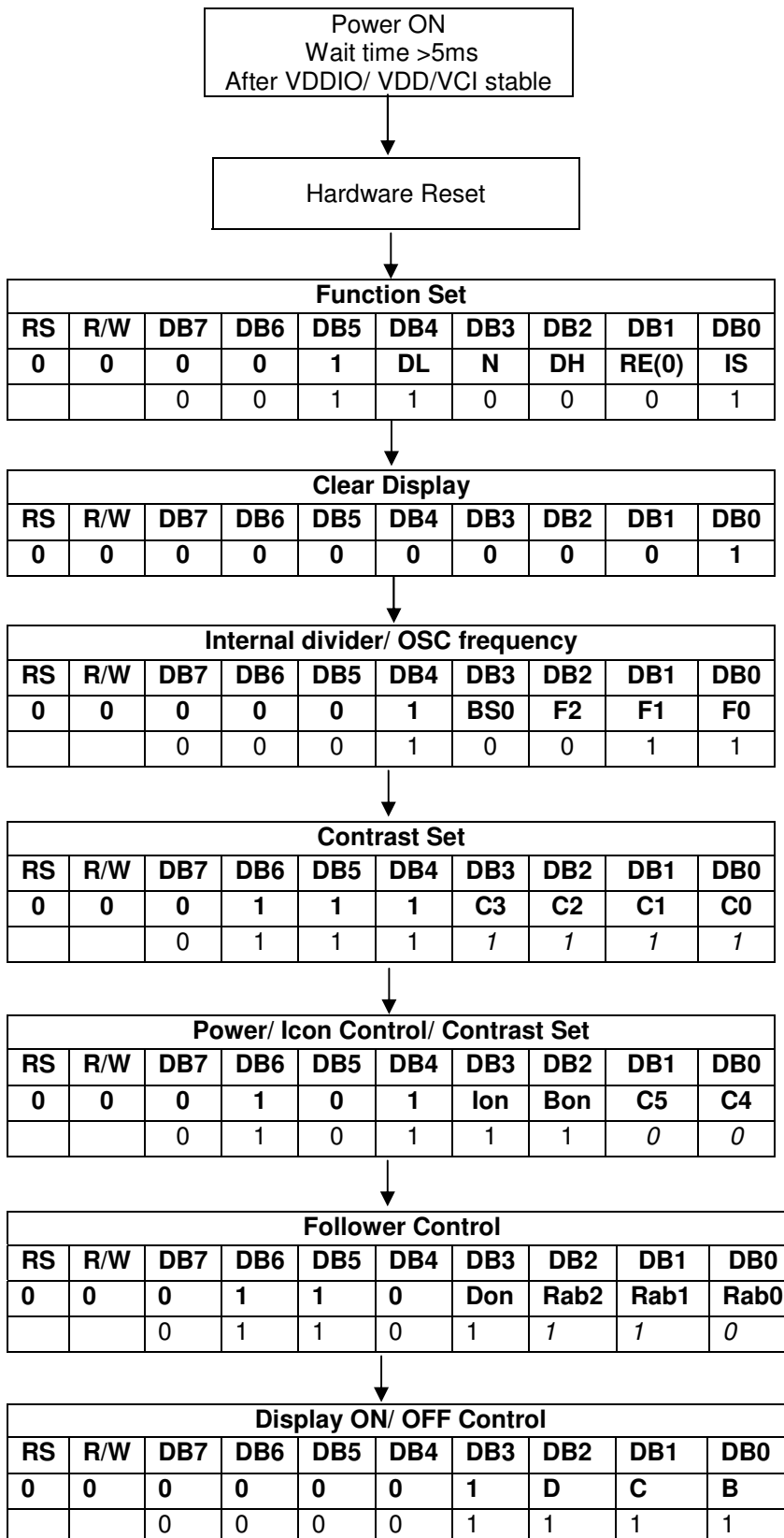
ITO connections

Output pins



13.3 Initialization

Figure 13-5: Initialization Code Example



*C5~0 and Rab2~0 setting depends on actual panel loadings and application

13.4 Power On/Off Sequence & Vout Timing

Note: To prevent potential damage to the device, all capacitors must be discharged to below 0.5V before the driver is removed from, or before the driver is attached to those components.

Figure 13-6: Power On Sequence

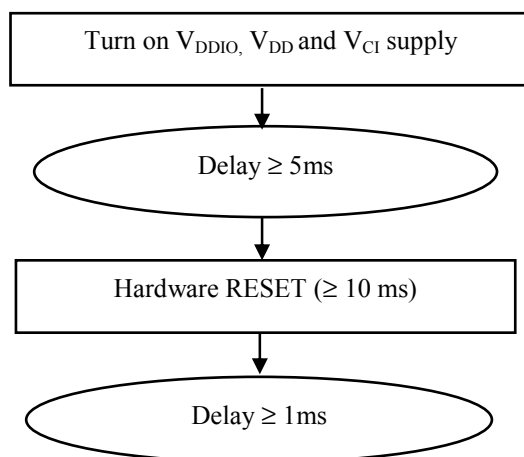
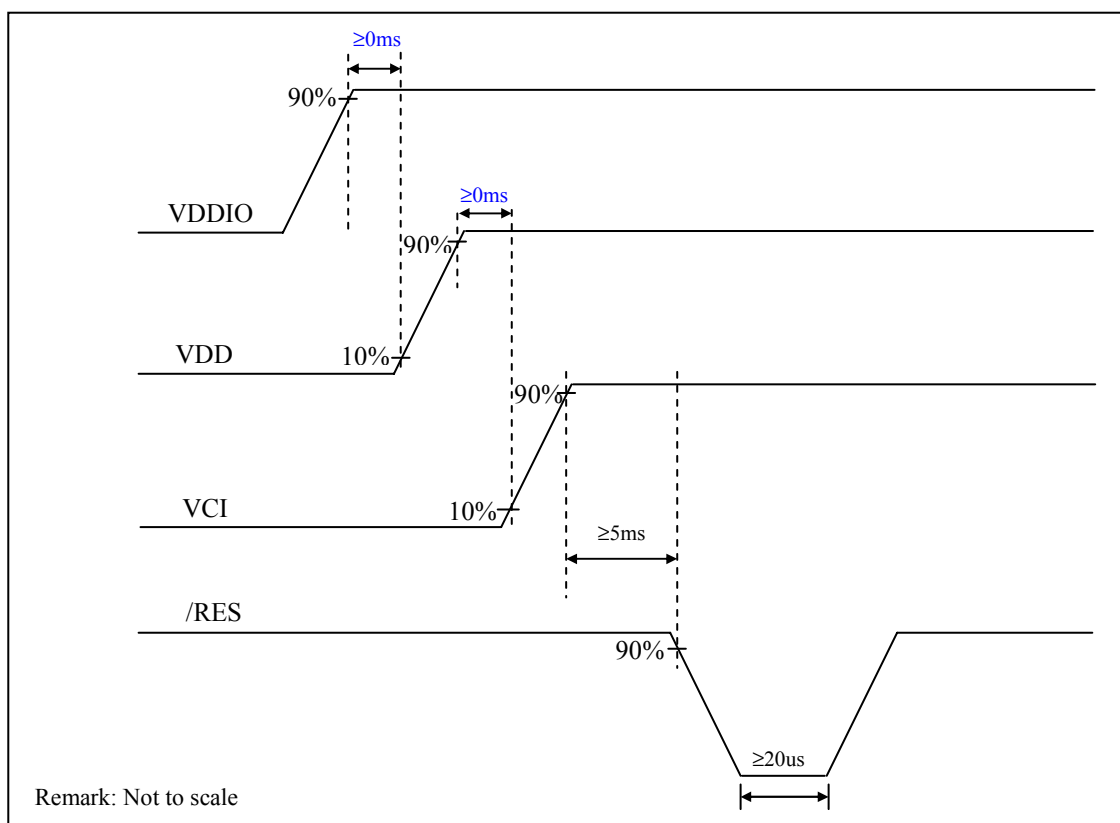


Figure 13-7: Power Up Sequence (if VDDIO, VDD and VCI not shorted together)

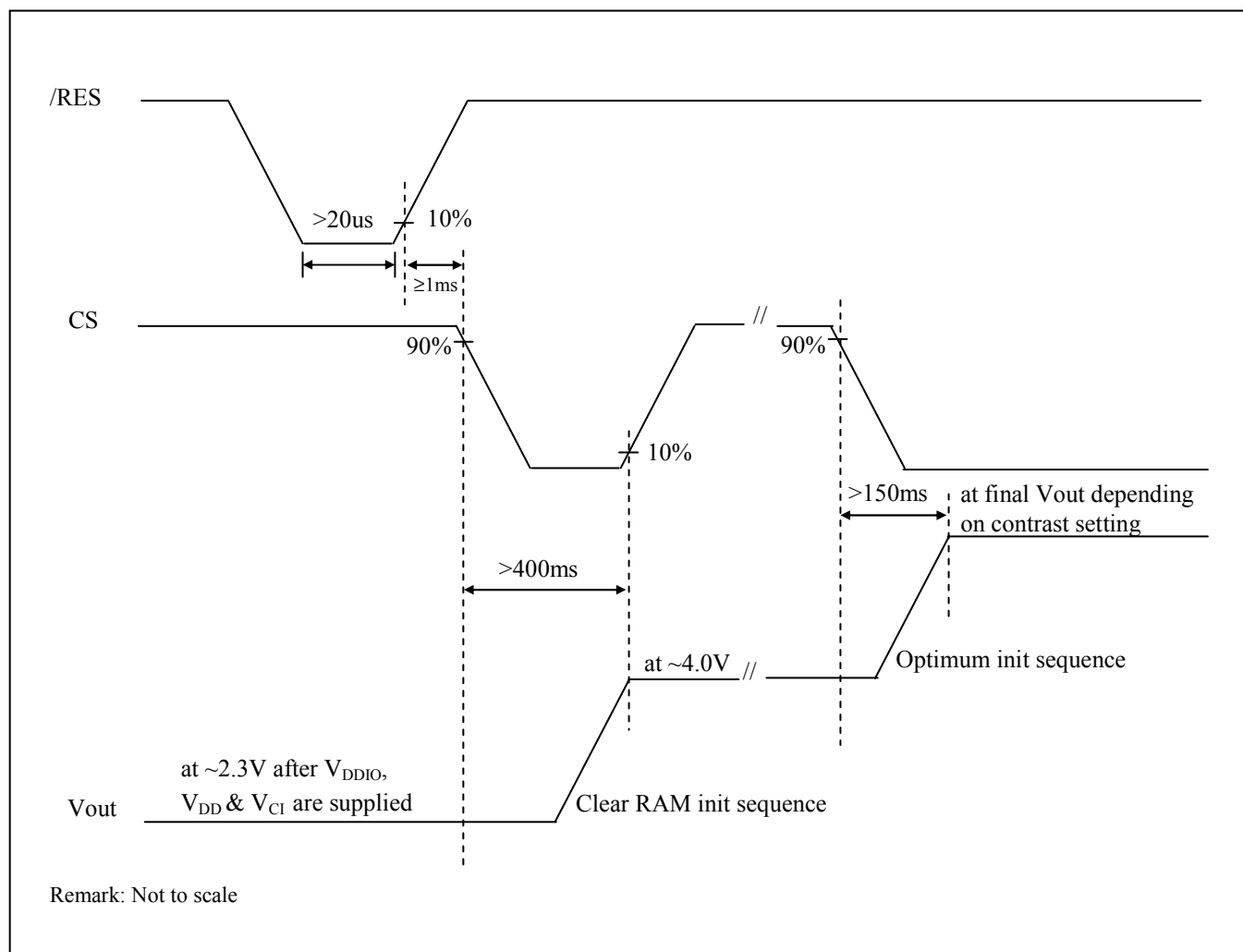


Recommended enter power save mode (sleep mode) Sequence:

1. Display off (Set DB2 = 0 in Display On/Off control)
2. Enter sleep mode (Set DB1 = 1 in Power down mode)

Recommended leave power save Sequence:

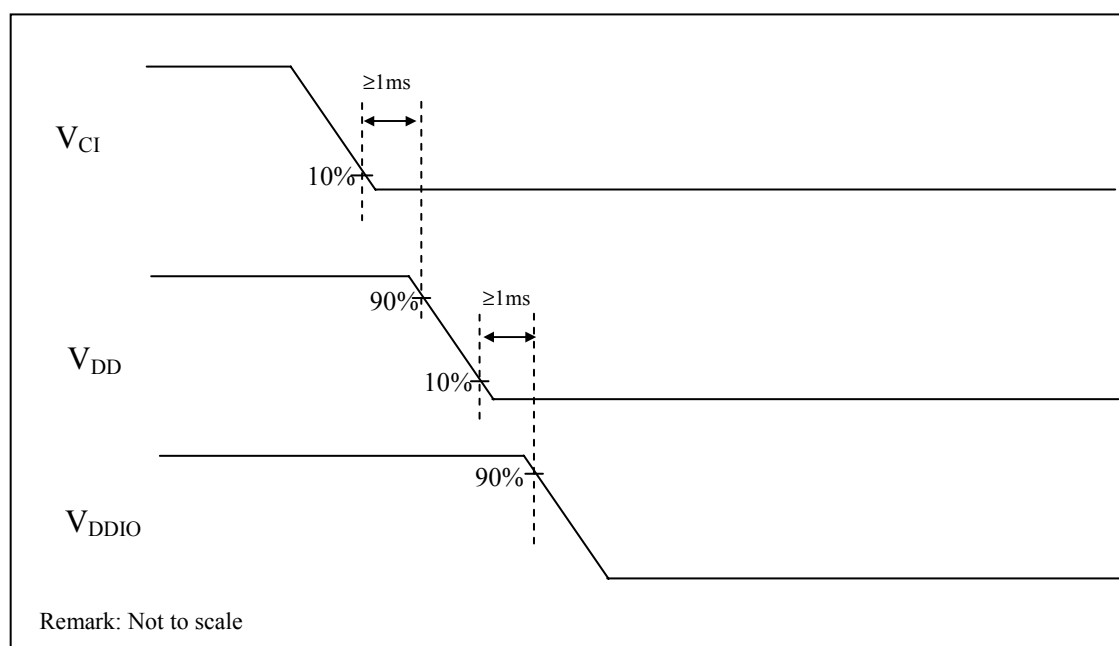
1. Leave sleep mode (Set DB1 = 0 in Power down mode)
2. Display On (Set DB2 = 1 in Display On/Off control)

Figure 13-8: Vout Timing Diagram

Recommended Power Off Sequence:

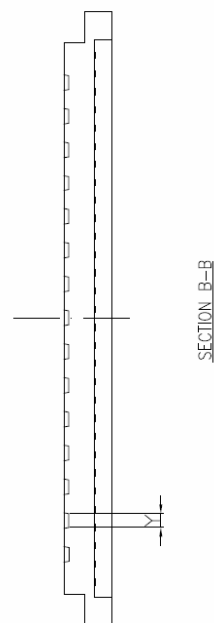
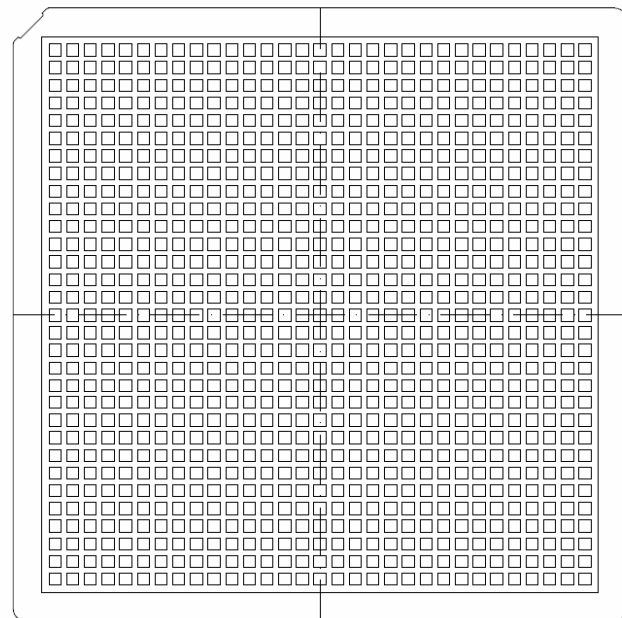
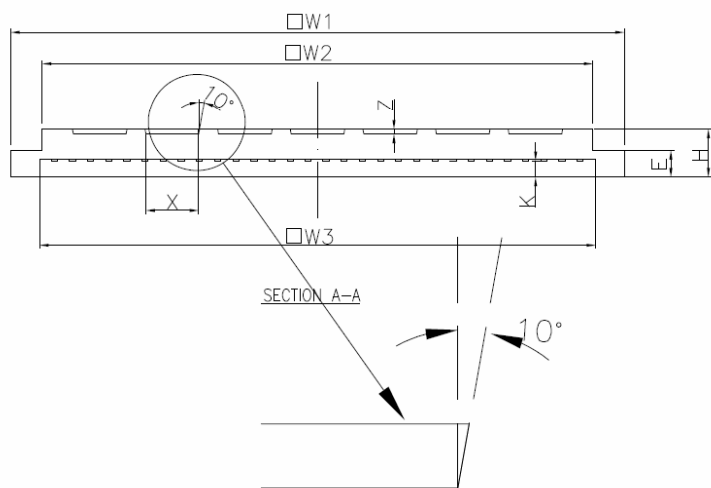
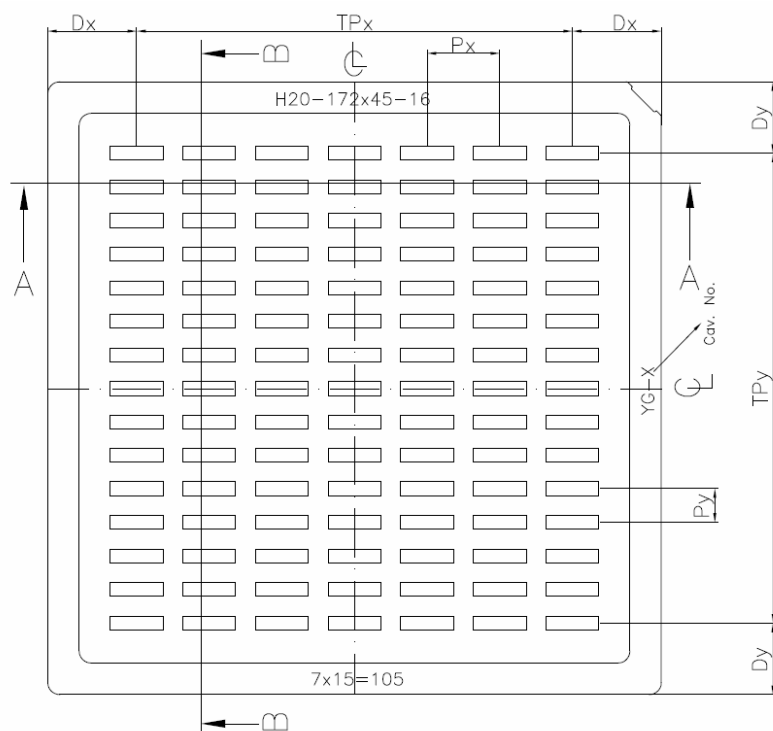
1. Drop the contrast & gain (Set DB2~0 = 0 in Power/ Icon control/ Contrast Set)
(Set DB2~0 = 0 in Follower Control)
(Set DB3~0 = 0 in Contrast Set)
2. Delay $\geq 25\text{ms}$
3. Display off (Set DB2 = 0 in Display On/Off control)
4. Delay $\geq 1\text{ms}$
5. Enter sleep mode (Set DB1 = 1 in Power down mode)
6. Delay $\geq 1\text{ms}$
7. Power off V_{DDIO} , V_{DD} and V_{CI} supplies
($V_{\text{CI}} \rightarrow V_{\text{DD}} \rightarrow V_{\text{DDIO}}$ if they are not shorted together)

Figure 13-9: Power Down Sequence (if VDDIO, VDD and VCI not shorted together)



14 PACKAGE INFORMATION

14.1 DIE TRAY DIMENSIONS



Spec	mm	(mil)
W1	50.70±0.05	(1996)
W2	45.50±0.10	(1791)
W3	45.95±0.10	(1809)
H	3.95±0.10	(156)
E	2.20±0.05	(87)
K	1.45±0.10	(57)
Dx	7.35±0.05	(289)
TPx	36.00±0.10	(1417)
Dy	5.89±0.05	(232)
TPy	38.92±0.10	(1532)
Px	6.00±0.05	(236)
Py	2.78±0.05	(109)
X	4.36±0.05	(172)
Y	1.14±0.05	(45)
Z	0.40±0.05	(16)
N	105(pocket number)	

15 SSD1803AM1 CGROM CHARACTER CODE

15.1 ROM A

b7-4	b3-0																
		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000																	
0001		✶	✷	✸	✹	✺	✻	✼	✽	✾	✿	⬆	⬇	⬈	⬉	⬊	■
0010			!	"	#	\$	%	&	'	(	)	*	+	,	-	.	/
0011		0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
0100		I	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
0101		P	Q	R	S	T	U	V	W	X	Y	Z	A	B	C	D	E
0110		z	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
0111		P	Q	R	S	T	U	V	W	X	Y	Z	A	B	C	D	E
1000		0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
1001		⌋	⌌	⌍	⌎	⌏	⌐	⌑	⌒	⌓	⌔	⌕	⌖	⌗	⌘	⌙	⌚
1010		Ⓐ	Ⓑ	Ⓒ	Ⓓ	Ⓔ	Ⓕ	Ⓖ	Ⓗ	Ⓘ	Ⓚ	Ⓛ	Ⓜ	Ⓝ	Ⓞ	Ⓟ	Ⓠ
1011		Ⓡ	Ⓢ	Ⓣ	Ⓤ	Ⓡ	Ⓢ	Ⓣ	Ⓤ	Ⓡ	Ⓢ	Ⓣ	Ⓤ	Ⓡ	Ⓢ	Ⓣ	Ⓤ
1100		Γ	Δ	⌒	⌓	⌔	⌕	⌖	⌗	⌘	⌙	⌚	⌛	⌜	⌝	⌞	⌟
1101		■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
1110		⌋	⌌	⌍	⌎	⌏	⌐	⌑	⌒	⌓	⌔	⌕	⌖	⌗	⌘	⌙	⌚
1111		Ⓐ	Ⓑ	Ⓒ	Ⓓ	Ⓔ	Ⓕ	Ⓖ	Ⓗ	Ⓘ	Ⓚ	Ⓛ	Ⓜ	Ⓝ	Ⓞ	Ⓟ	Ⓠ

15.2 ROM B

b7-4	b3-0															
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000																
0001	Ⓜ	Ⓝ	Ⓟ	Ⓡ	Ⓢ	Ⓣ	Ⓤ	Ⓡ	Ⓣ	Ⓥ	Ⓦ	Ⓧ				
0010		!	"	#	\$	%	&	'	(	)	*	+	,	-	.	/
0011	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
0100	ⓐ	ⓑ	ⓒ	ⓓ	ⓔ	ⓕ	ⓖ	ⓗ	ⓘ	ⓙ	ⓚ	ⓛ	ⓜ	ⓝ	ⓞ	ⓟ
0101	ⓑ	ⓓ	ⓔ	ⓕ	ⓖ	ⓗ	ⓘ	ⓙ	ⓚ	ⓛ	ⓜ	ⓝ	ⓞ	ⓟ	ⓠ	ⓡ
0110	'	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
0111	p	q	r	s	t	u	v	w	x	y	z	[	\	]	~	ⓧ
1000	Ⓐ	Ⓑ	Ⓒ	Ⓓ	Ⓔ	Ⓕ	Ⓖ	Ⓗ	Ⓘ	Ⓚ	Ⓛ	Ⓜ	Ⓢ	Ⓣ	Ⓤ	Ⓡ
1001	ⓐ	ⓑ	ⓒ	ⓓ	ⓔ	ⓕ	ⓖ	ⓗ	ⓘ	ⓙ	ⓚ	ⓛ	ⓜ	ⓝ	ⓞ	ⓟ
1010	Ⓐ	Ⓑ	Ⓒ	Ⓓ	Ⓔ	Ⓕ	Ⓖ	Ⓗ	Ⓘ	Ⓚ	Ⓛ	Ⓜ	Ⓢ	Ⓣ	Ⓤ	Ⓡ
1011	Ⓐ	Ⓑ	Ⓒ	Ⓓ	Ⓔ	Ⓕ	Ⓖ	Ⓗ	Ⓘ	Ⓚ	Ⓛ	Ⓜ	Ⓢ	Ⓣ	Ⓤ	Ⓡ
1100	Ⓐ	Ⓑ	Ⓒ	Ⓓ	Ⓔ	Ⓕ	Ⓖ	Ⓗ	Ⓘ	Ⓚ	Ⓛ	Ⓜ	Ⓢ	Ⓣ	Ⓤ	Ⓡ
1101	Ⓐ	Ⓑ	Ⓒ	Ⓓ	Ⓔ	Ⓕ	Ⓖ	Ⓗ	Ⓘ	Ⓚ	Ⓛ	Ⓜ	Ⓢ	Ⓣ	Ⓤ	Ⓡ
1110	Ⓐ	Ⓑ	Ⓒ	Ⓓ	Ⓔ	Ⓕ	Ⓖ	Ⓗ	Ⓘ	Ⓚ	Ⓛ	Ⓜ	Ⓢ	Ⓣ	Ⓤ	Ⓡ
1111	Ⓐ	Ⓑ	Ⓒ	Ⓓ	Ⓔ	Ⓕ	Ⓖ	Ⓗ	Ⓘ	Ⓚ	Ⓛ	Ⓜ	Ⓢ	Ⓣ	Ⓤ	Ⓡ

15.3 ROM C

b7-4	b3-0															
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0001	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
0010	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41
0011	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57
0100	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73
0101	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89
0110	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105
0111	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121
1000	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137
1001	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153
1010	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169
1011	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185
1100	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201
1101	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217
1110	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233
1111	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249

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