

## **SN55450B - SN55454B, SN75451B - SN75454B**

### *Dual Peripheral Drivers*

Series 55450B/75451B dual peripheral drivers are a family of versatile devices designed for use in systems that employ TTL logic. This family is functionally interchangeable with and replaces the 75450 family and the 75450A family of devices. The speed of 55450B/75451B family is equal to that of the 75450 family, and the parts have been designed to ensure freedom from latch-up. Diode clamped inputs simplify circuit design.

Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

---

### **Rochester Electronics Manufactured Components**

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

### **Quality Overview**

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

---

*The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

8961724 TEXAS INSTR (LIN/INTFC)

91D 75850 D

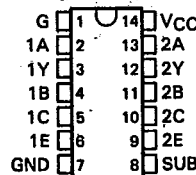
**SN55450B THRU SN55454B  
SN75451B THRU SN75454B  
DUAL PERIPHERAL DRIVERS**

D2217, DECEMBER 1976—REVISED SEPTEMBER 1986

**PERIPHERAL DRIVERS FOR  
HIGH-CURRENT SWITCHING  
AT VERY HIGH SPEEDS**

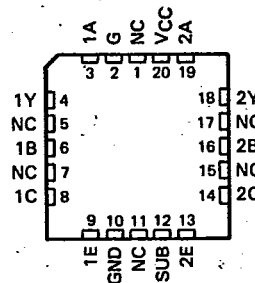
- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 20 V (After Conducting 300 mA)
- High-Speed Switching
- Circuit Flexibility for Varied Applications
- TTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- New Plastic DIP (P) with Copper Lead Frame Provides Cooler Operation and Improved Reliability
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

SN55450B . . . J PACKAGE  
(TOP VIEW)



T-52-17

SN55450B . . . FK PACKAGE  
(TOP VIEW)



**SUMMARY OF SERIES 55450B/75451B**

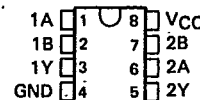
DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
SN55450B	AND <sup>†</sup>	FK,J
SN55451B	AND	FK,JG
SN55452B	NAND	FK,JG
SN55453B	OR	FK,JG
SN55454B	NOR	FK,JG
SN75451B	AND	D,P
SN75452B	NAND	D,P
SN75453B	OR	D,P
SN75454B	NOR	D,P

<sup>†</sup>With output transistor base connected externally to output of gate.

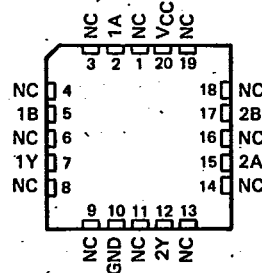
**description**

Series 55450B/75451B dual peripheral drivers are a family of versatile devices designed for use in systems that employ TTL logic. This family is functionally interchangeable with and replaces the 75450 family and the 75450A family devices manufactured previously. The speed of the 55450B/75451B family is equal to that of the 75450 family, and the parts have been designed to ensure freedom from latch-up. Diode-clamped inputs simplify circuit design.

SN55451B, SN55452B,  
SN55453B, SN55454B . . . JG PACKAGE  
SN75451B, SN75452B,  
SN75453B, SN75454B . . . D OR P PACKAGE  
(TOP VIEW)



SN55451B, SN55452B,  
SN55453B, SN55454B . . . FK PACKAGE  
(TOP VIEW)



NC—No internal connection

Peripheral Drivers/Actuators

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



Copyright © 1981, Texas Instruments Incorporated

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

8961724 TEXAS INSTR (LIN/INTFC)

91D 75851 D

**SN55450B THRU SN55454B  
SN75451B THRU SN75454B  
DUAL PERIPHERAL DRIVERS**

T-52-17

**description (cont'd)**

Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN55450B is a unique general-purpose device, featuring two standard Series 54 TTL gates and two uncommitted, high-current, high-voltage n-p-n transistors. The device offers the system designer the flexibility of tailoring the circuit to the application.

The SN55451B/SN75451B, SN55452B/SN75452B, SN55453B/SN75453B, and SN55454B/SN75454B are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic), with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

Series 55450B drivers are characterized for operation over the full military range of -55°C to 125°C. Series 75451B drivers are characterized for operation from 0°C to 70°C.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

	SN55450B	SN55451B SN55452B SN55453B SN55454B	SN75451B SN75452B SN75453B SN75454B	UNIT
Supply voltage, V <sub>CC</sub> (see Note 1)	7	7	7	V
Input voltage	5.5	5.5	5.5	V
Interemitter voltage (see Note 2)	5.5	5.5	5.5	V
V <sub>CC</sub> -to-substrate voltage	35			V
Collector-to-substrate voltage	35			V
Collector-base voltage	35			V
Collector-emitter voltage (see Note 3)	30			V
Emitter-base voltage	5			V
Off-state output voltage		30	30	V
Continuous collector or output current (see Note 4)	400	400	400	mA
Peak collector or output current (t <sub>w</sub> ≤ 10 ms, duty cycle ≤ 50%, (see Note 4)	500	500	500	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	D package		725	mW
	FK package	1375		
	J package	1375		
	JG package		1050	
	P package		1200	
Operating free-air temperature range	-55 to 125	-55 to 125	0 to 70	°C
Storage temperature range	-65 to 150	-65 to 150	-65 to 150	°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or JG package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	°C

- NOTES: 1. Voltage values are with respect to the network ground terminal unless otherwise specified.  
 2. This is the voltage between two emitters of a multiple-emitter transistor.  
 3. This value applies when the base-emitter resistance (R<sub>BE</sub>) is equal to or less than 500 Ω.  
 4. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.  
 5. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table.

Peripheral Drivers/Actuators

8961724 TEXAS INSTR (LIN/INTFC)

91D 75852 D

**SN55450B THRU SN55454B  
SN75451B THRU SN75454B  
DUAL PERIPHERAL DRIVERS**

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T <sub>A</sub>
D	725 mW	5.8 mW/°C	25°C
FK	1375 mW	11.0 mW/°C	25°C
J	1375 mW	11.0 mW/°C	25°C
JG	1050 mW	8.4 mW/°C	25°C
P	1200 mW	9.6 mW/°C	25°C

T-52-17

recommended operating conditions (see Note 6)

	SERIES 55450B			SERIES 75451B			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V <sub>CC</sub>	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V <sub>IH</sub>	2.2			2			V
Low-level input voltage, V <sub>IL</sub>	0.8			0.8			V
Operating free-air temperature, T <sub>A</sub>	-55			125			0 70 °C

NOTE 6: For the SN55450B only, the substrate (pin 8) must always be at the most negative device voltage for proper operation.



Peripheral Drivers/Actuators

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

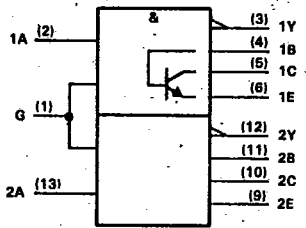
8961724 TEXAS INSTR (LIN/INTFC)

91D 75853 D

**SN55450B  
DUAL PERIPHERAL POSITIVE-AND DRIVER**

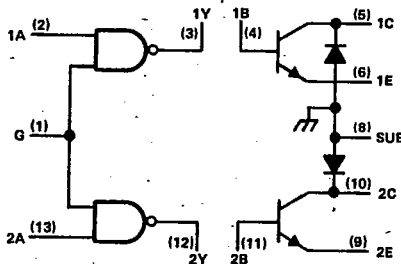
T-52-17

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



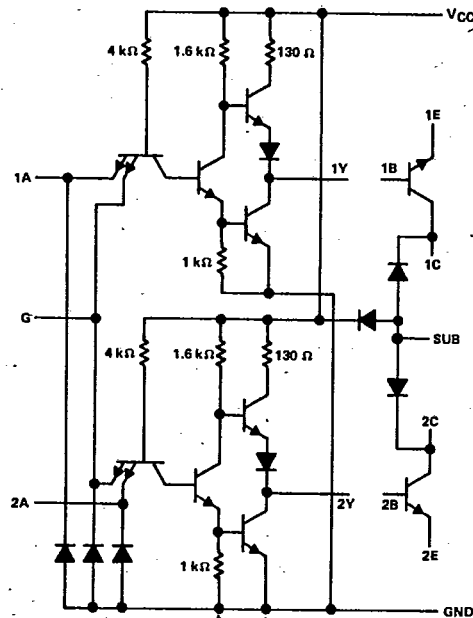
positive logic:

$Y = \overline{A}G \text{ or } \overline{A} + \overline{G}$  (gate only)

$C = AG \text{ or } \overline{A} + \overline{G}$  (gate and transistor)

Pin numbers shown are for the J package.

schematic



Resistor values shown are nominal.

Peripheral Drivers/Actuators

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TTL gates

PARAMETER	TEST CONDITIONS‡	SN55450B			UNIT
		MIN	TYP‡	MAX	
V <sub>IK</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA		-1.2	-1.5	V
V <sub>OH</sub> High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -400 μA	2.4	3.3		V
V <sub>OL</sub> Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = MIN, I <sub>OL</sub> = 16 mA		0.25	0.5	V
I <sub>I</sub> Input current at maximum input voltage	input A			1	mA
	input G	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V		2	
I <sub>IH</sub> High-level input current	input A			40	μA
	input G	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V		80	
I <sub>IL</sub> Low-level input current	input A			-1.8	mA
	input G	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		-3.2	
I <sub>OS</sub> Short-circuit output current†	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0	-18	-35	-55	mA
I <sub>CCH</sub> Supply current, outputs high	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0		2.8	4	mA
I <sub>CCL</sub> Supply current, outputs low	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5 V		7	11	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

† Not more than one output should be shorted at a time.

8961724 TEXAS INSTR (LIN/INTFC)

91D 75854 D

**SN55450B  
DUAL PERIPHERAL POSITIVE-AND DRIVER**

T-52-17

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

**output transistors**

PARAMETER	TEST CONDITIONS†	SN55450B			UNIT
		MIN	TYP‡	MAX	
V <sub>(BR)CBO</sub> Collector-base breakdown voltage	I <sub>C</sub> = 100 µA, I <sub>E</sub> = 0	35			V
V <sub>(BR)CER</sub> Collector-emitter breakdown voltage	I <sub>C</sub> = 100 µA, R <sub>BE</sub> = 500 Ω	30			V
V <sub>(BR)EBO</sub> Emitter-base breakdown voltage	I <sub>E</sub> = 100 µA, I <sub>C</sub> = 0	5			V
h <sub>FE</sub> Static forward current transfer ratio	V <sub>CE</sub> = 3 V, T <sub>A</sub> = 25°C See Note 7	I <sub>C</sub> = 100 mA	25		
		I <sub>C</sub> = 300 mA	30		
	V <sub>CE</sub> = 3 V, T <sub>A</sub> = MIN, See Note 7	I <sub>C</sub> = 100 mA	10		
		I <sub>C</sub> = 300 mA	15		
V <sub>BE</sub> Base-emitter voltage	I <sub>B</sub> = 10 mA, I <sub>C</sub> = 100 mA, See Note 7	0.85	1.2		V
	I <sub>B</sub> = 30 mA, I <sub>C</sub> = 300 mA, See Note 7	1	1.4		
V <sub>CE(sat)</sub> Collector-emitter saturation voltage	I <sub>B</sub> = 10 mA, I <sub>C</sub> = 100 mA, See Note 7	0.25	0.5		V
	I <sub>B</sub> = 30 mA, I <sub>C</sub> = 300 mA, See Note 7	0.45	0.8		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

NOTE 7: These parameters must be measured using pulse techniques. t<sub>w</sub> = 300 µs, duty cycle ≤ 2%.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

**TTL gates**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> Propagation delay time, low-to-high-level output	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 400 Ω, See Figure 1	12			ns
t <sub>PHL</sub> Propagation delay time, high-to-low-level output		8			ns

**output transistors**

PARAMETER	TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
t <sub>d</sub> Delay time	I <sub>C</sub> = 200 mA, I <sub>B(1)</sub> = 20 mA, I <sub>B(2)</sub> = -40 mA, V <sub>BE(off)</sub> = -1 V, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 50 Ω, See Figure 2	8			ns
t <sub>r</sub> Rise time		12			ns
t <sub>s</sub> Storage time		7			ns
t <sub>f</sub> Fall time		6			ns

‡ Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

**gate and transistors combined**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t <sub>PLH</sub> Propagation delay time, low-to-high-level output	I <sub>C</sub> ≈ 200 mA, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 50 Ω, See Figure 3	20			30	ns
t <sub>PHL</sub> Propagation delay time, high-to-low-level output		20			30	ns
t <sub>TLH</sub> Transition time, low-to-high-level output		7			12	ns
t <sub>THL</sub> Transition time, high-to-low-level output		9			15	ns
V <sub>OH</sub> High-level output voltage after switching	V <sub>S</sub> = 20 V, I <sub>C</sub> ≈ 300 mA, R <sub>BE</sub> = 500 Ω, See Figure 4	V <sub>S</sub> -6.5			mV	

5

Peripheral Drivers/Actuators



POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

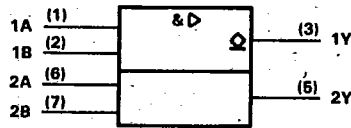
8961724 TEXAS INSTR (LIN/INTFC)

91D 75855 D

**SN55451B, SN75451B  
DUAL PERIPHERAL POSITIVE-AND DRIVERS**

T-52-17

logic symbol†



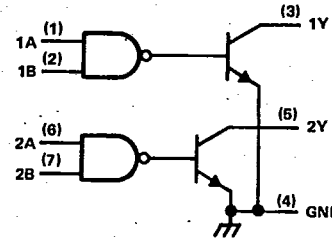
†This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.

FUNCTION TABLE  
(EACH DRIVER)

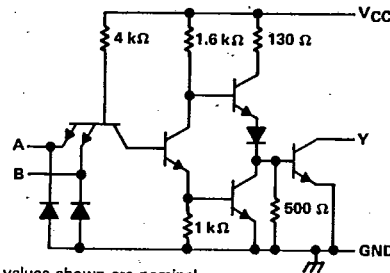
A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

positive logic:  
 $Y = AB \text{ or } \overline{A+B}$

logic diagram (positive logic)



schematic (each driver)



Pin numbers shown are for D, JG, and P packages.

Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN55451B		SN75451B		UNIT
		MIN	TYP <sup>‡</sup> MAX	MIN	TYP <sup>‡</sup> MAX	
V <sub>IK</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA	-1.2	-1.5	-1.2	-1.5	V
I <sub>OH</sub> High-level output current	V <sub>CC</sub> = MIN, V <sub>IH</sub> = MIN, V <sub>OH</sub> = 30 V	300		100		μA
V <sub>OL</sub> Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 100 mA	0.25	0.5	0.25	0.4	V
	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 300 mA	0.5	0.8	0.5	0.7	
I <sub>I</sub> Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V	1		1		mA
I <sub>IH</sub> High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V	40		40		μA
I <sub>IL</sub> Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V	-1	-1.6	-1	-1.6	mA
I <sub>CCH</sub> Supply current, outputs high	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5 V	7	11	7	11	mA
I <sub>CCL</sub> Supply current, outputs low	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0	62	65	62	65	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> Propagation delay time, low-to-high-level output	I <sub>O</sub> ≈ 200 mA, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 50 Ω, See Figure 3	18		25	ns
t <sub>PHL</sub> Propagation delay time, high-to-low-level output		18		25	
t <sub>TLH</sub> Transition time, low-to-high-level output		5		8	ns
t <sub>THL</sub> Transition time, high-to-low-level output		7		12	
V <sub>OH</sub> High-level output voltage after switching	V <sub>S</sub> = 20 V, See Figure 4	V <sub>S</sub> - 6.5			mV

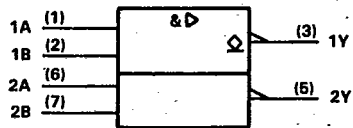
8961724 TEXAS INSTR (LIN/INTFC)

91D 75856 D

**SN55452B, SN75452B  
DUAL PERIPHERAL POSITIVE-NAND DRIVERS**

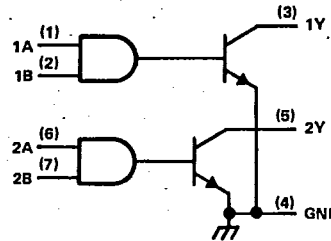
T-52-17

logic symbol†



†This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

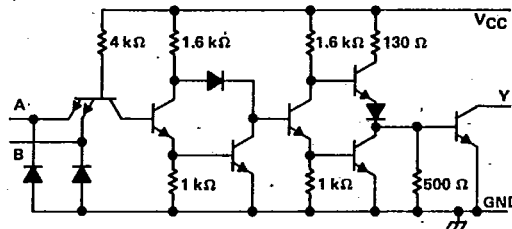


FUNCTION TABLE  
(EACH DRIVER)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

positive logic:  
 $Y = \overline{AB}$  or  $\overline{A+B}$

schematic (each driver)



Pin numbers shown are for D, JG, and P packages.

Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN55452B		SN75452B		UNIT
		MIN	TYP‡	MAX	MIN	
V <sub>IK</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA	-1.2	-1.5	-1.2	-1.5	V
I <sub>OH</sub> High-level output current	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, V <sub>OH</sub> = 30 V		300		100	μA
V <sub>OL</sub> Low-level output voltage	V <sub>CC</sub> = MIN, I <sub>OL</sub> = 100 mA, V <sub>IH</sub> = MIN	0.25	0.5	0.25	0.4	V
	V <sub>CC</sub> = MIN, I <sub>OL</sub> = 300 mA, V <sub>IH</sub> = MIN	0.5	0.8	0.5	0.7	
I <sub>I</sub> Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V		1		1	mA
I <sub>IH</sub> High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V		40		40	μA
I <sub>IL</sub> Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V	-1.1	-1.6	-1.1	-1.6	mA
I <sub>CC</sub> H Supply current, outputs high	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0	11	14	11	14	mA
I <sub>CC</sub> L Supply current, outputs low	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5 V	56	71	56	71	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t <sub>PLH</sub> Propagation delay time, low-to-high-level output	I <sub>O</sub> ≈ 200 mA, C <sub>L</sub> = 16 pF, R <sub>L</sub> = 60 Ω, See Figure 3		26	35	ns	
t <sub>PHL</sub> Propagation delay time, high-to-low-level output			24	35	ns	
t <sub>TLH</sub> Transition time, low-to-high-level output				5	8	ns
t <sub>THL</sub> Transition time, high-to-low-level output				7	12	ns
V <sub>OH</sub> High-level output voltage after switching	V <sub>S</sub> = 20 V, I <sub>O</sub> ≈ 300 mA, See Figure 4		V <sub>S</sub> - 6.5		mV	

TEXAS  
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

5-87

Peripheral Drivers/Actuators



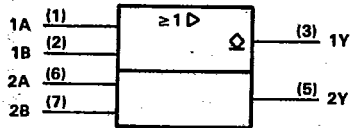
8961724 TEXAS INSTR (LIN/INTFC)

91D 75857 D

**SN55453B, SN75453B  
DUAL PERIPHERAL POSITIVE-OR DRIVERS**

T-5a-17

logic symbol†



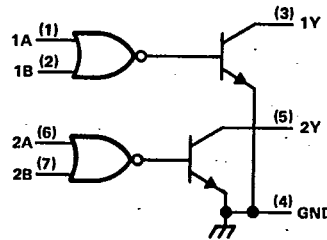
†This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.

FUNCTION TABLE  
(EACH DRIVER)

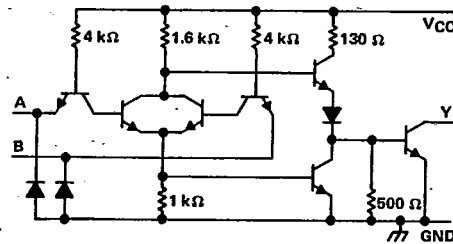
A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

positive logic:  
 $Y = A + B$  or  $\overline{AB}$

logic diagram (positive logic)



schematic (each driver)



Pin numbers shown are for D, JG, and P packages.

Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	SN55453B		SN75453B		UNIT
		MIN	TYP <sup>§</sup> MAX	MIN	TYP <sup>§</sup> MAX	
V <sub>IK</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA	-1.2	-1.5	-1.2	-1.5	V
I <sub>OH</sub> High-level output current	V <sub>CC</sub> = MIN, V <sub>IH</sub> = MIN, V <sub>OH</sub> = 30 V	300		100		μA
V <sub>OL</sub> Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 100 mA	0.25	0.5	0.25	0.4	V
	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 300 mA	0.5	0.8	0.5	0.7	
	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V	1		1		
I <sub>I</sub> Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V	1		1		mA
I <sub>IH</sub> High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V	40		40		μA
I <sub>IL</sub> Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V	-1	-1.6	-1	-1.6	mA
I <sub>CCH</sub> Supply current, outputs high	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5 V	8	11	8	11	mA
I <sub>CCL</sub> Supply current, outputs low	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0	54	68	54	68	mA

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> Propagation delay time, low-to-high-level output	I <sub>O</sub> ≈ 200 mA, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 50 Ω, See Figure 3	18 25			ns
t <sub>PHL</sub> Propagation delay time, high-to-low-level output		16 25			ns
t <sub>TLH</sub> Transition time, low-to-high-level output		6 8			ns
t <sub>THL</sub> Transition time, high-to-low-level output		7 12			ns
V <sub>OH</sub> High-level output voltage after switching	V <sub>S</sub> = 20 V, See Figure 4	V <sub>S</sub> -6.5			mV

Peripheral Drivers/Actuators

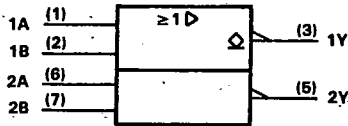
8961724 TEXAS INSTR (LIN/INTFC)

91D 75858 D

**SN55454B, SN75454B  
DUAL PERIPHERAL POSITIVE-NOR DRIVERS**

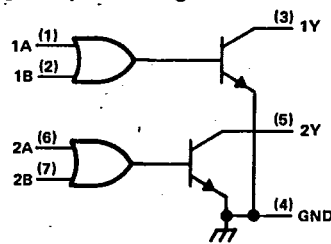
T-52-17

logic symbol†



†This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

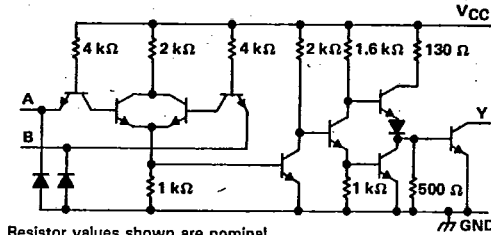


**FUNCTION TABLE  
(EACH DRIVER)**

A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

positive logic:  
 $Y = \overline{A+B}$  or  $\overline{AB}$

schematic (each driver)



Pin numbers shown are for D, JG, and P packages.

Resistor values shown are nominal.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	SN55454B		SN75454B		UNIT
		MIN	TYP‡	MAX	MIN	
V <sub>IK</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA	-1.2	-1.5	-1.2	-1.5	V
I <sub>OH</sub> High-level output current	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, V <sub>OH</sub> = 30 V	300		100		μA
V <sub>OL</sub> Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = MIN, I <sub>OL</sub> = 100 mA	0.25	0.5	0.25	0.4	V
	V <sub>CC</sub> = MIN, V <sub>IH</sub> = MIN, I <sub>OL</sub> = 300 mA	0.5	0.8	0.5	0.7	
I <sub>I</sub> Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V	1		1		mA
I <sub>IH</sub> High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V	40		40		μA
I <sub>IL</sub> Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V	-1	-1.6	-1	-1.6	mA
I <sub>CCH</sub> Supply current, outputs high	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0	13	17	13	17	mA
I <sub>CCL</sub> Supply current, outputs low	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5 V	61	79	61	79	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> Propagation delay time, low-to-high-level output	I <sub>O</sub> ≈ 200 mA, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 50 Ω, See Figure 3	27	35		ns
t <sub>PHL</sub> Propagation delay time, high-to-low-level output		24	35		ns
t <sub>TLH</sub> Transition time, low-to-high-level output		5	8		ns
t <sub>THL</sub> Transition time, high-to-low-level output		7	12		ns
V <sub>OH</sub> High-level output voltage after switching	V <sub>S</sub> = 20 V, See Figure 4, I <sub>O</sub> ≈ 300 mA	V <sub>S</sub> - 6.5			mV

Peripheral Drivers/Actuators

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75286

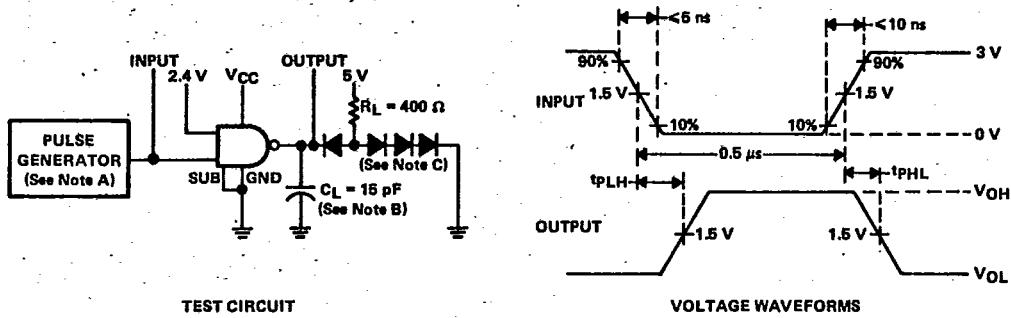
8961724 TEXAS INSTR (LIN/INTFC)

91D 75859 D

**SN55450B  
DUAL PERIPHERAL DRIVER**

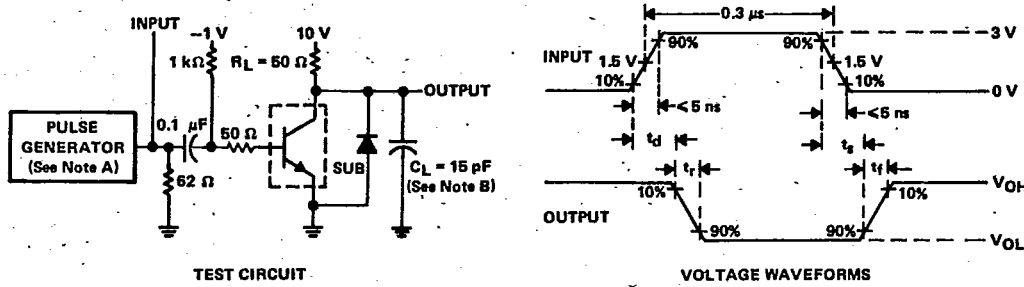
T-52-17

**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A. The pulse generator has the following characteristics:  $\text{PRR} \leq 1\text{ MHz}$ ,  $Z_{\text{out}} = 50\ \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.  
 C. All diodes are 1N3064.

**FIGURE 1. PROPAGATION DELAY TIMES, EACH GATE (SN55450B ONLY)**



- NOTES: A. The pulse generator has the following characteristics: duty cycle  $\leq 1\%$ ,  $Z_{\text{out}} = 50\ \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

**FIGURE 2. SWITCHING TIMES, EACH TRANSISTOR (SN55450B ONLY)**

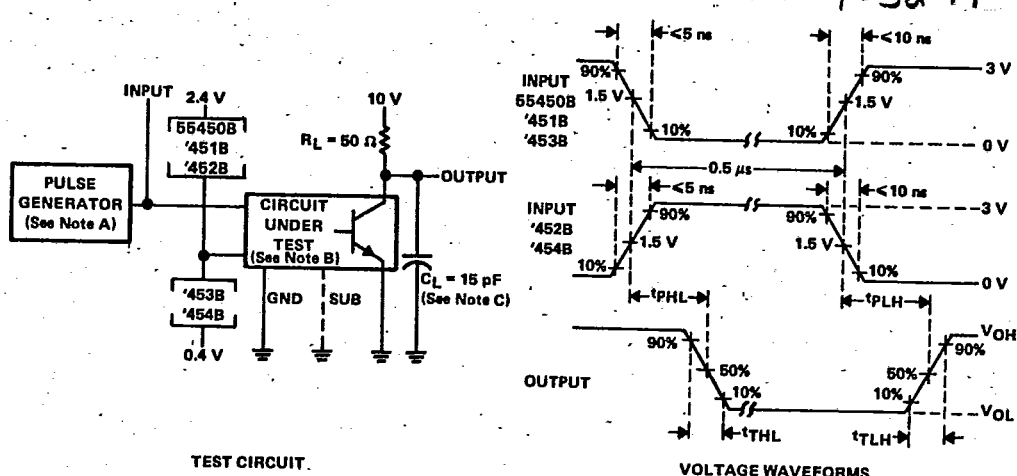
Peripheral Drivers/Actuators

8961724 TEXAS INSTR (LIN/INTFC)

91D 75860 D

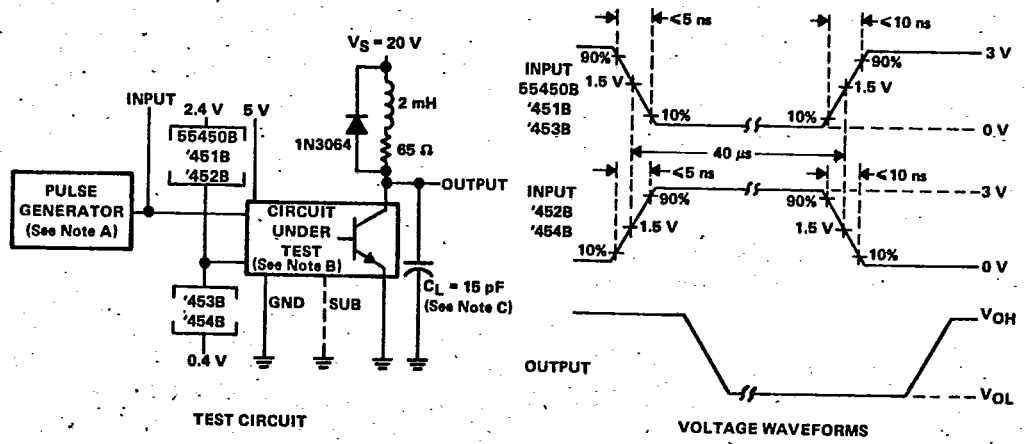
**SN55450B THRU SN55454B  
SN75451B THRU SN75454B  
DUAL PERIPHERAL DRIVERS**

**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A. The pulse generator has the following characteristics: PRR  $\le 1$  MHz,  $Z_{out} = 50 \Omega$ .  
 B. When testing SN55450B, connect output Y to transistor base and ground the substrate terminal.  
 C.  $C_L$  includes probe and jig capacitance.

**FIGURE 3. SWITCHING TIMES OF COMPLETE DRIVERS**



- NOTES: A. The pulse generator has the following characteristics: PRR  $\le 12.5$  kHz,  $Z_{out} = 50 \Omega$ .  
 B. When testing SN55450B, connect output Y to transistor base with a 500- $\Omega$  resistor from there to ground, and ground the substrate terminal.  
 C.  $C_L$  includes probe and jig capacitance.

**FIGURE 4. LATCH-UP TEST OF COMPLETE DRIVERS**

Peripheral Drivers/Actuators

8961724 TEXAS INSTR (LIN/INTFC)

91D 75861 D

SN55450B THRU SN55454B  
SN75451B THRU SN75454B  
DUAL PERIPHERAL DRIVERS

T-52-17

TYPICAL CHARACTERISTICS

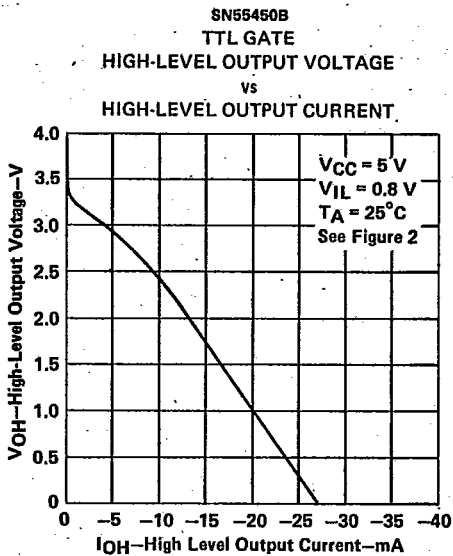


FIGURE 5

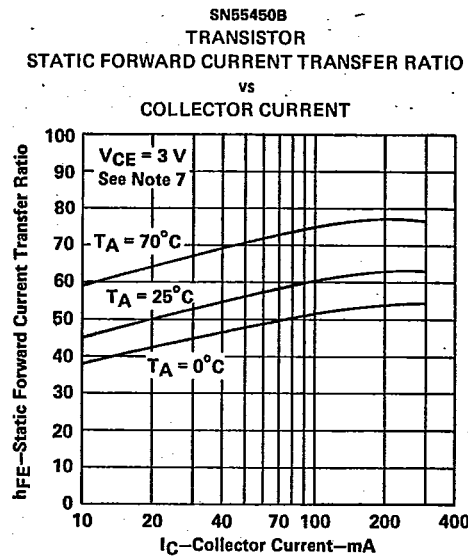


FIGURE 6

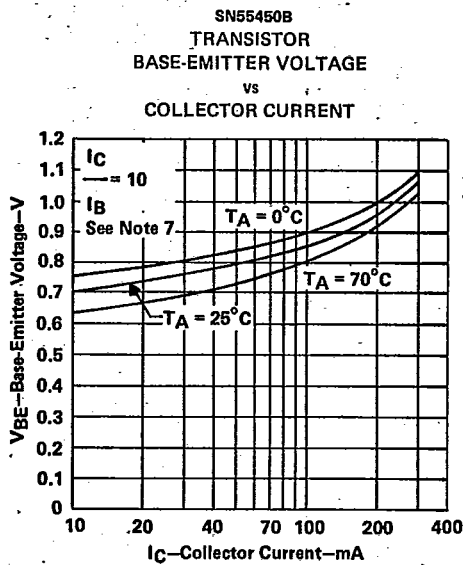


FIGURE 7

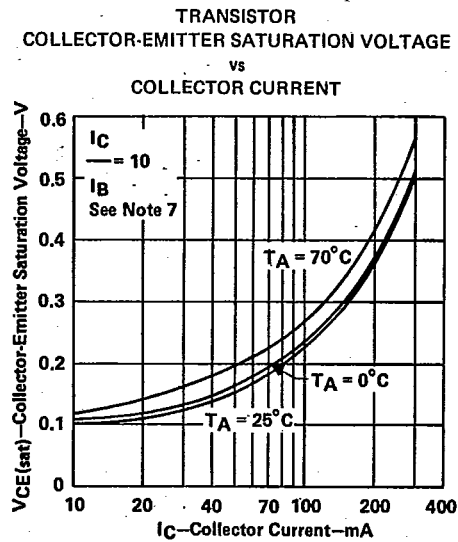


FIGURE 8

NOTE 7: These parameters must be measured using pulse techniques,  $t_w = .300 \mu s$ , duty cycle  $\leq 2\%$ .

5  
Peripheral Drivers/Actuators