

## **SN5496, SN7496, SN54LS96, SN74LS96**

### ***5-Bit Shift Registers***

These shift registers consist of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is inactive (low). Clearing is independent of the level of the clock input. The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting like clearing is independent of the level of the clock input.

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### **Rochester Electronics Manufactured Components**

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

### **Quality Overview**

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

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*The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

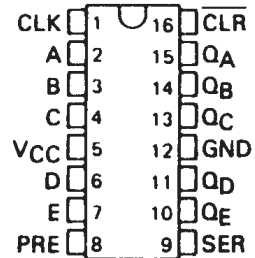
# SN5496, SN54LS96, SN7496, SN74LS96 5-BIT SHIFT REGISTERS

SDLS946 - MARCH 1974 - REVISED MARCH 1988

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

SN5496, SN54LS96 . . . J OR W PACKAGE  
SN7496 . . . N PACKAGE  
SN74LS96 . . . D OR N PACKAGE  
(TOP VIEW)

TYPE	TYPICAL	
	PROPAGATION DELAY TIME	POWER DISSIPATION
'96	25 ns	240 mW
'LS96	25 ns	60 mW



## description

These shift registers consist of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is inactive (low). Clearing is independent of the level of the clock input.

The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting like clearing is independent of the level of the clock input.

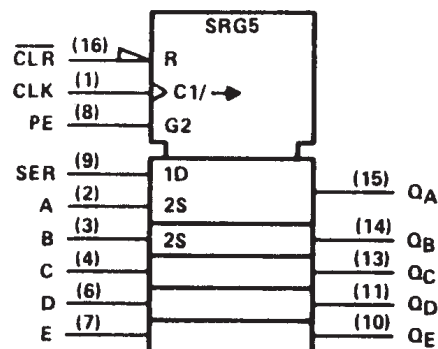
Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be set up at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.

FUNCTION TABLE

CLEAR	PRESET					CLOCK	SERIAL	OUTPUTS				
	ENABLE	A	B	C	D			E	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>
L	L	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>
H	H	H	L	H	L	H	X	H	Q <sub>B0</sub>	H	Q <sub>D0</sub>	H
H	L	X	X	X	X	L	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>
H	L	X	X	X	X	↑	H	H	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>
H	L	X	X	X	X	↑	L	L	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>

H = high level (steady state), L = low level (steady state)  
X = irrelevant (any input, including transition)  
↑ = transition from low to high level  
Q<sub>A0</sub>, Q<sub>B0</sub>, etc. = the level of Q<sub>A</sub>, Q<sub>B</sub>, etc. respectively before the indicated steady-state input conditions were established.  
Q<sub>An</sub>, Q<sub>Bn</sub>, etc. = the level of Q<sub>A</sub>, Q<sub>B</sub>, etc. respectively before the most recent ↑ transition of the clock.

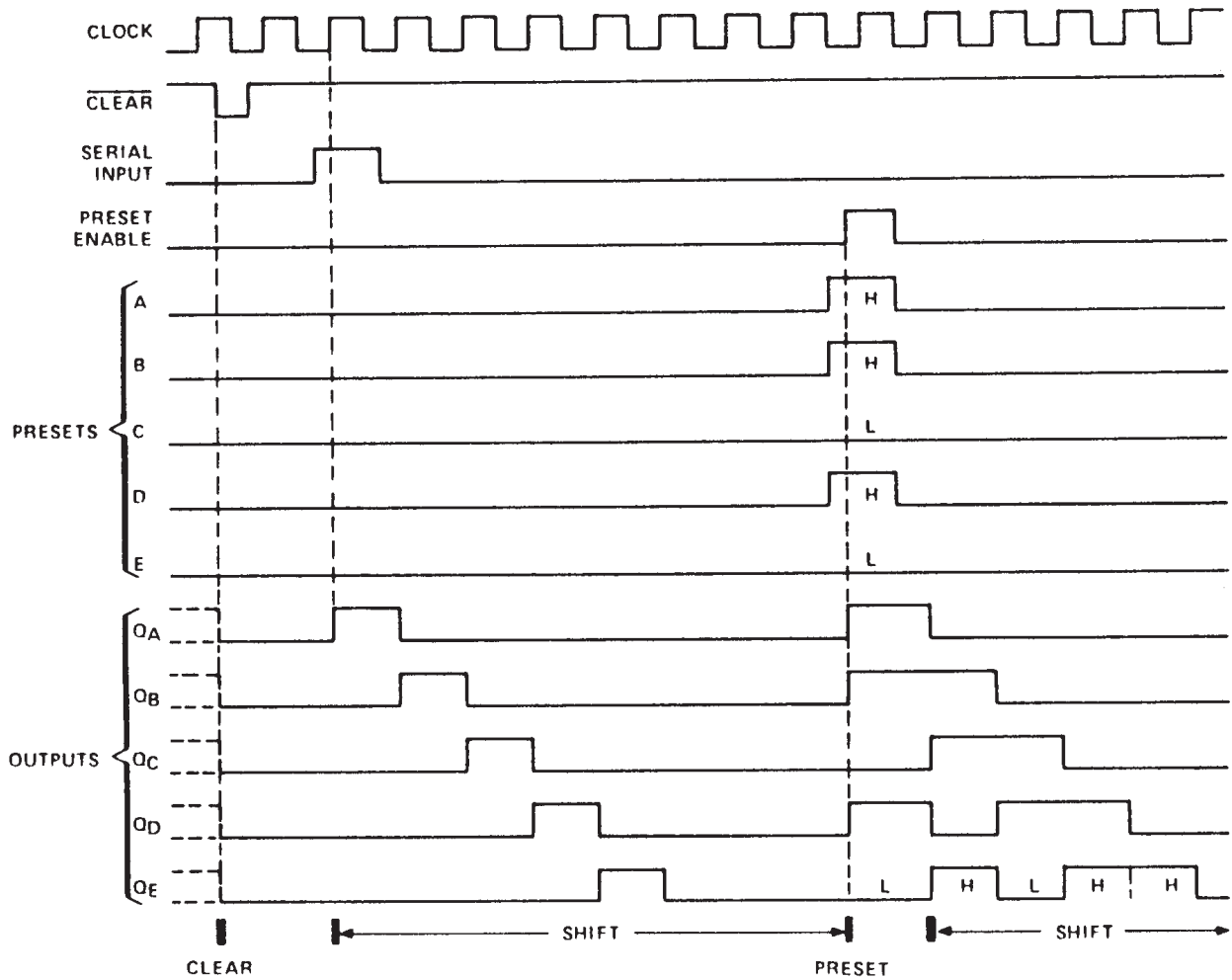
logic symbol<sup>1</sup>



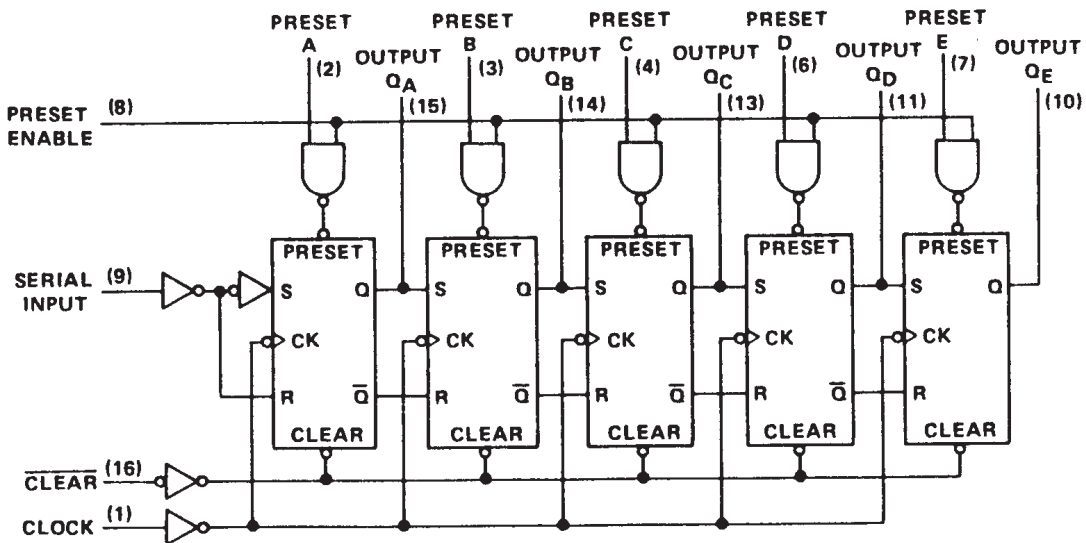
<sup>1</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**SN5496, SN54LS96,  
SN7496, SN74LS96  
5-BIT SHIFT REGISTERS**

typical clear, shift, preset, and shift sequences

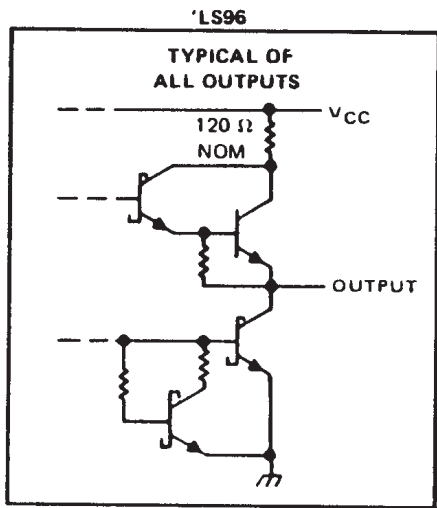
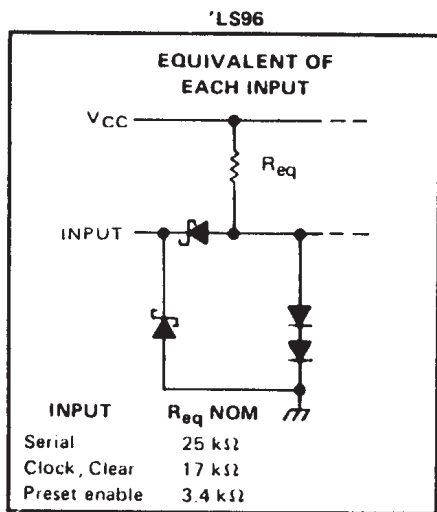
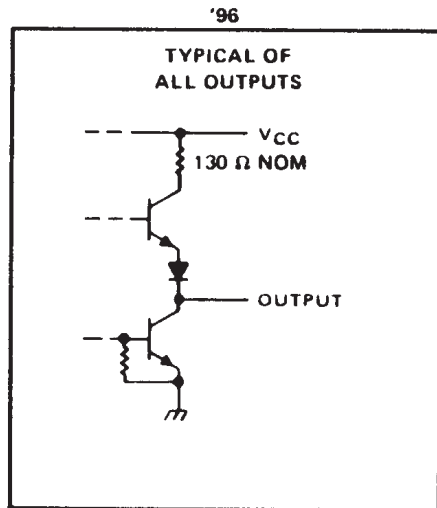
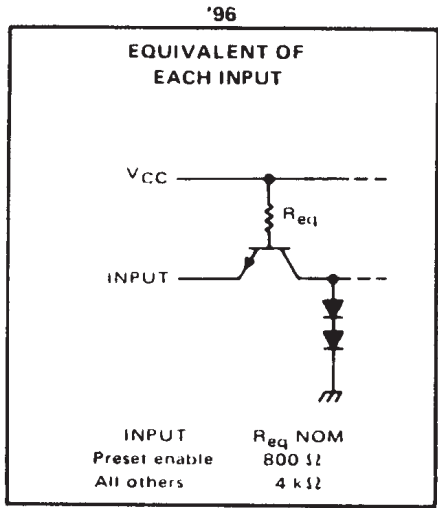


logic diagram (positive logic)



**SN5496, SN54LS96,  
SN7496, SN74LS96  
5-BIT SHIFT REGISTERS**

**schematics of inputs and outputs**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage (see Note 2): '96	5.5 V
'LS96	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

- NOTES: 1. Voltage values are with respect to network ground terminal.  
2. Input voltage must be zero or positive with respect to network ground terminal.

# SN5496, SN7496 5-BIT REGISTERS

## recommended operating conditions

	SN5496			SN7496			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-400			-400	$\mu$ A
Low-level output current, $I_{OL}$			16			16	mA
Clock frequency, $f_{clock}$	0		10	0		10	MHz
Width of clock input pulse, $t_w(\text{clock})$	35			35			ns
Width of preset and clear input pulse, $t_w$	30			30			ns
Serial input setup time, $t_{SU}$ (see Figure 1)	30			30			ns
Serial input hold time, $t_h$ (see Figure 1)	0			0			ns
Operating free-air temperature, $T_A$	-55		125	0		70	$^{\circ}$ C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5496			SN7496			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IH}$	High-level input voltage		2			2			V
$V_{IL}$	Low-level input voltage				0.8			0.8	V
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -400 \mu\text{A}$	2.4	3.4		2.4	3.4		V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
$I_{IH}$	High-level input current	any input except preset enable			40			40	$\mu$ A
		preset enable			200			200	
$I_{IL}$	Low-level input current	any input except preset enable			-1.6			-1.6	mA
		preset enable			-8			-8	
$I_{OS}$	Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		-57	-18		-57	mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 3}$		48	68		48	79	mA

† For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ .

§ Not more than one output should be shorted at a time.

NOTE 3:  $I_{CC}$  is measured with the clear input grounded and all other inputs and outputs open.

## switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output from clock		25	40	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output from clock		25	40	ns
$t_{PLH}$	Propagation delay time, low-to-high-level output from preset or preset enable		28	35	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output from clear			55	ns

$C_L = 15 \text{ pF}, R_L = 400 \Omega, \text{ See Figure 1}$

# SN54LS96, SN74LS96 5-BIT SHIFT REGISTERS

## recommended operating conditions

	SN54LS96			SN74LS96			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-400			-400	$\mu$ A
Low-level output current, $I_{OL}$			4			8	mA
Clock frequency, $f_{clock}$	0		25	0		25	MHz
Width of clock input pulse, $t_{W(clock)}$	20			20			ns
Width of preset and clear input pulse, $t_W$	30			30			ns
Serial input setup time, $t_{setup}$ (see Figure 1)	30			30			ns
Serial input hold time, $t_{hold}$ (see Figure 1)	0			0			ns
Operating free-air temperature, $T_A$	-55		125	0		70	$^{\circ}$ C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS96			SN74LS96			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IH}$	High-level input voltage		2			2			V
$V_{IL}$	Low-level input voltage				0.7			0.8	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN.}$ , $I_I = -18 \text{ mA}$			-1.5			-1.5	V
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN.}$ , $V_{IH} = 2 \text{ V.}$ $V_{IL} = V_{IL \text{ max.}}$ , $I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN.}$ , $V_{IH} = 2 \text{ V.}$ $V_{IL} = V_{IL \text{ max.}}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	0.25	0.4		V
			$I_{OL} = 8 \text{ mA}$			0.35	0.5		
$I_I$	Input current at maximum input voltage	Preset enable	$V_{CC} = \text{MAX.}$ , $V_I = 7 \text{ V}$						mA
		All others							
$I_{IH}$	High-level input current	Preset enable	$V_{CC} = \text{MAX.}$ , $V_I = 2.7 \text{ V}$						$\mu$ A
		All others							
$I_{IL}$	Low-level input current	Preset enable	$V_{CC} = \text{MAX.}$ , $V_I = 0.4 \text{ V}$						mA
		All others							
$I_{OS}$	Short-circuit output current§	$V_{CC} = \text{MAX.}$	-20		-100	-20		-100	mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX.}$ , See Note 3	12	20		12	20		mA

† For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25 \text{ }^{\circ}\text{C}$ .

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

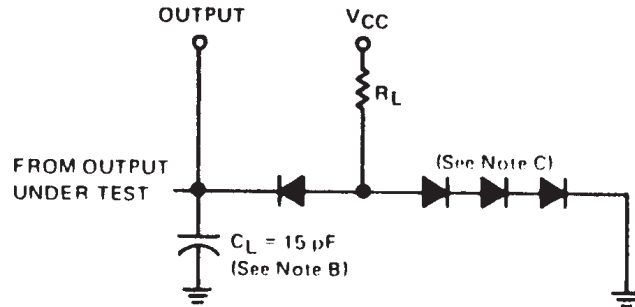
NOTE 3:  $I_{CC}$  is measured with the clear input grounded and all other inputs and outputs open.

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

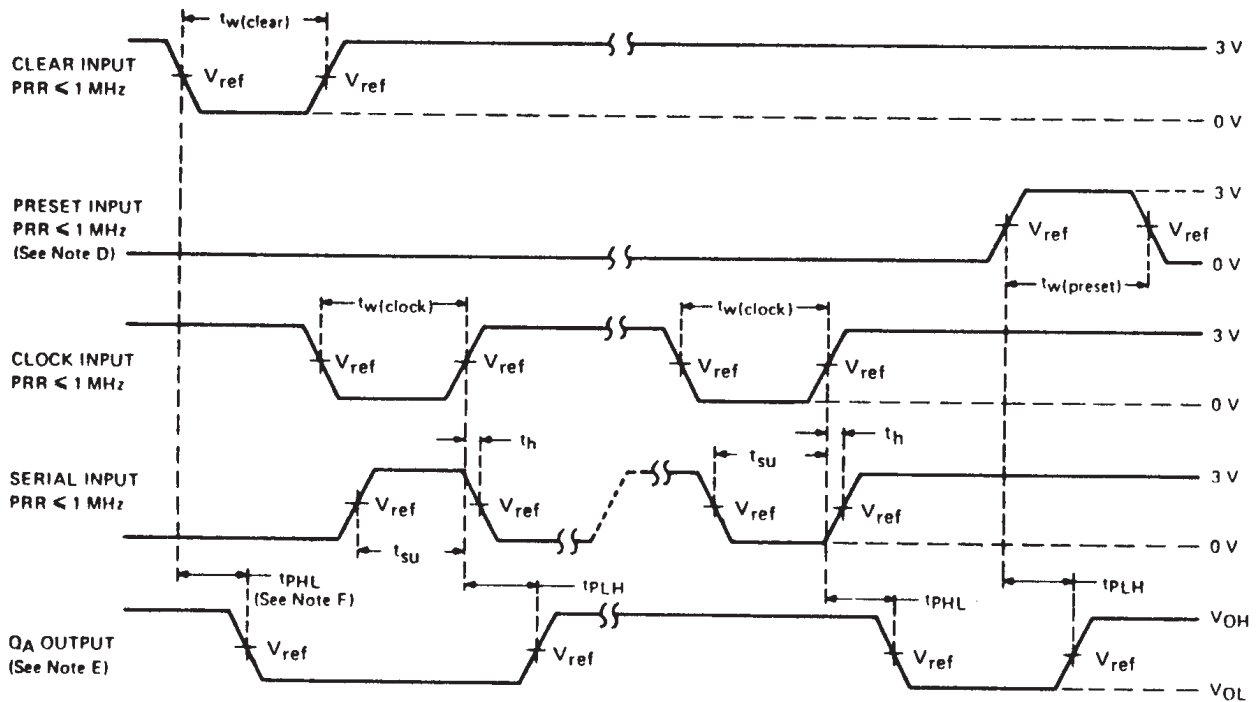
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low-to-high-level output from clock	$C_L = 15 \text{ pF}$ , $R_L = 2 \text{ k}\Omega$ , See Figure 1		25	40	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output from clock			25	40	ns
$t_{PLH}$ Propagation delay time, low-to-high-level output from preset or preset enable			28	35	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output from clear				55	ns

**SN5496, SN54LS96,  
SN7496, SN74LS96  
5-BIT SHIFT REGISTERS**

**PARAMETER MEASUREMENT INFORMATION**



**LOAD CIRCUIT**



**VOLTAGE WAVEFORMS**

- NOTES: A. Input pulses are supplied by pulse generators having the following characteristics: duty cycle  $\leq 50\%$ ,  $Z_{out} \approx 50 \Omega$ ; for '96,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns, and for 'LS96  $t_r = 15$  ns,  $t_f = 6$  ns.  
 B.  $C_L$  includes probe and jig capacitance.  
 C. All diodes are 1N3064 or equivalent.  
 D. Preset may be tested by applying a high-level voltage to the individual preset inputs and pulsing the preset enable or by applying a high-level voltage to the preset enable and pulsing the individual preset inputs.  
 E.  $Q_A$  output is illustrated. Relationship of serial input to other Q outputs is illustrated in the typical shift sequence.  
 F. Outputs are set to the high level prior to the measurement of  $t_{PHL}$  from the clear input.  
 G. For '96,  $V_{ref} = 1.5$  V; for 'LS96  $V_{ref} = 1.3$  V.

**FIGURE 1—SWITCHING TIMES**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN5496J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	Samples Not Available
SN7496N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	Samples Not Available
SN74LS96D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	Samples Not Available
SN74LS96DR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	Samples Not Available
SN74LS96J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	Samples Not Available
SN74LS96N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	Samples Not Available
SN74LS96N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	Samples Not Available
SNJ5496J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	Samples Not Available
SNJ5496W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI	Samples Not Available

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF SN5496, SN7496 :**

- Catalog: [SN7496](#)
- Military: [SN5496](#)

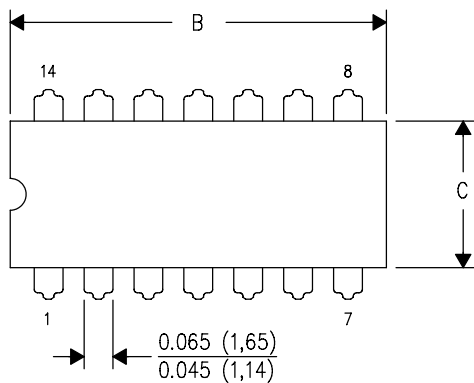
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

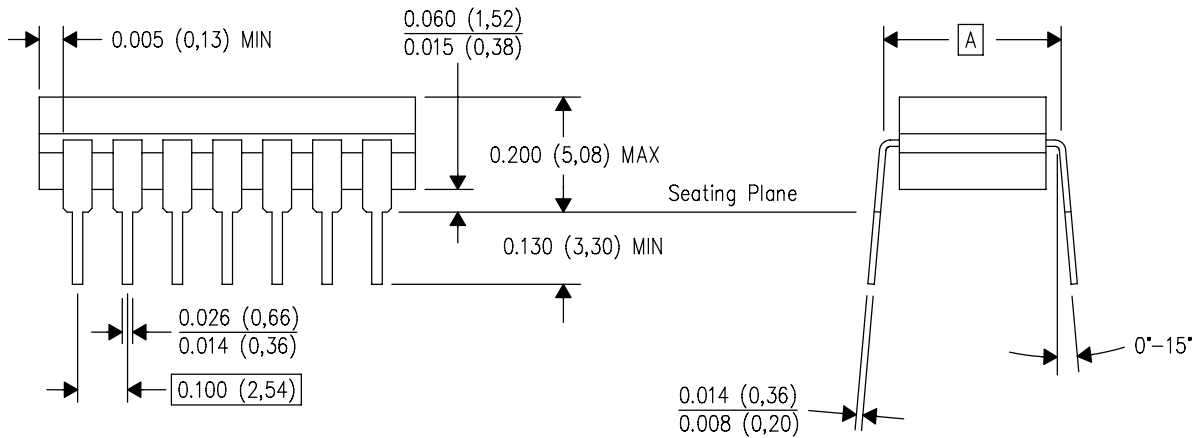
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

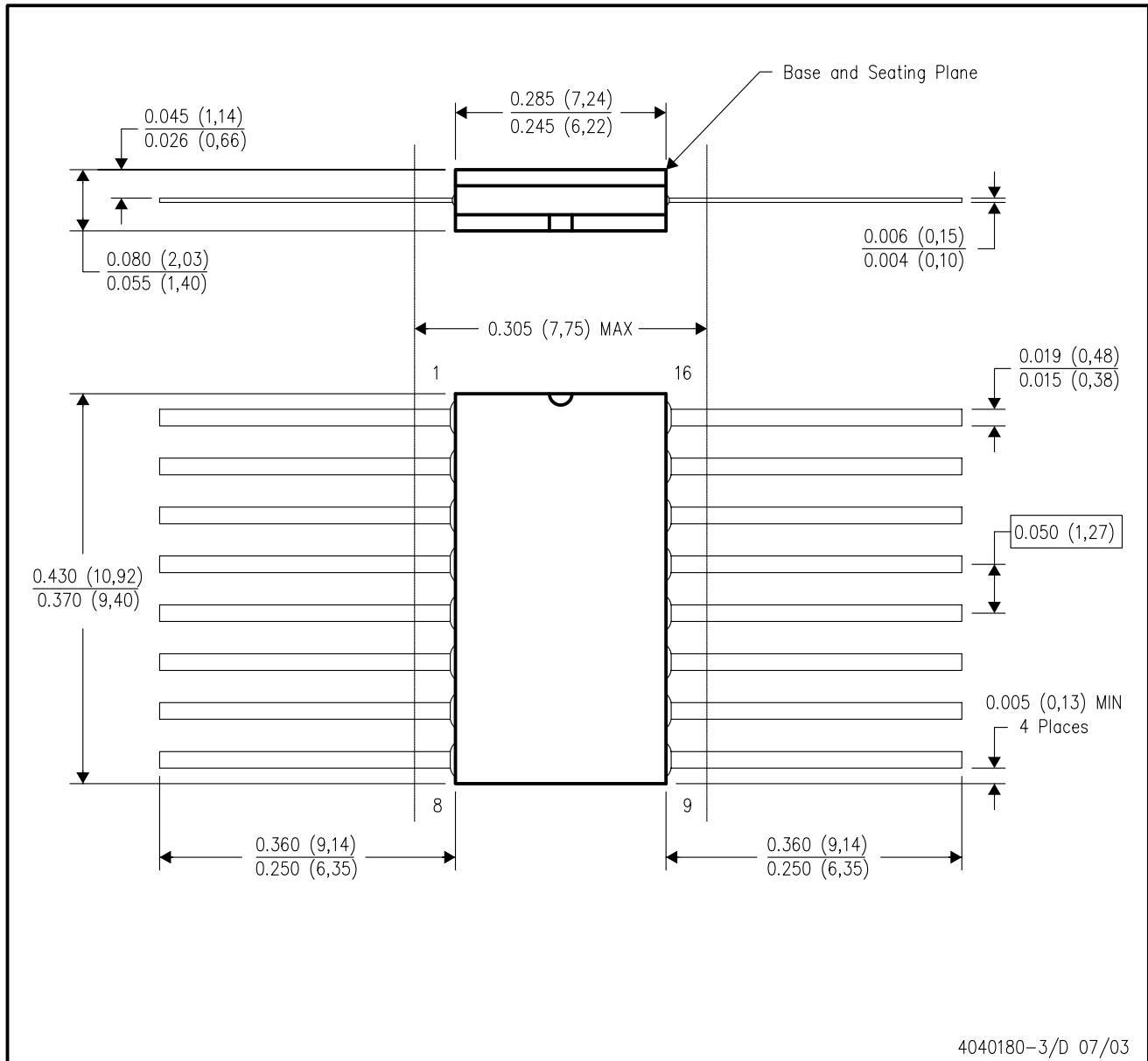


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

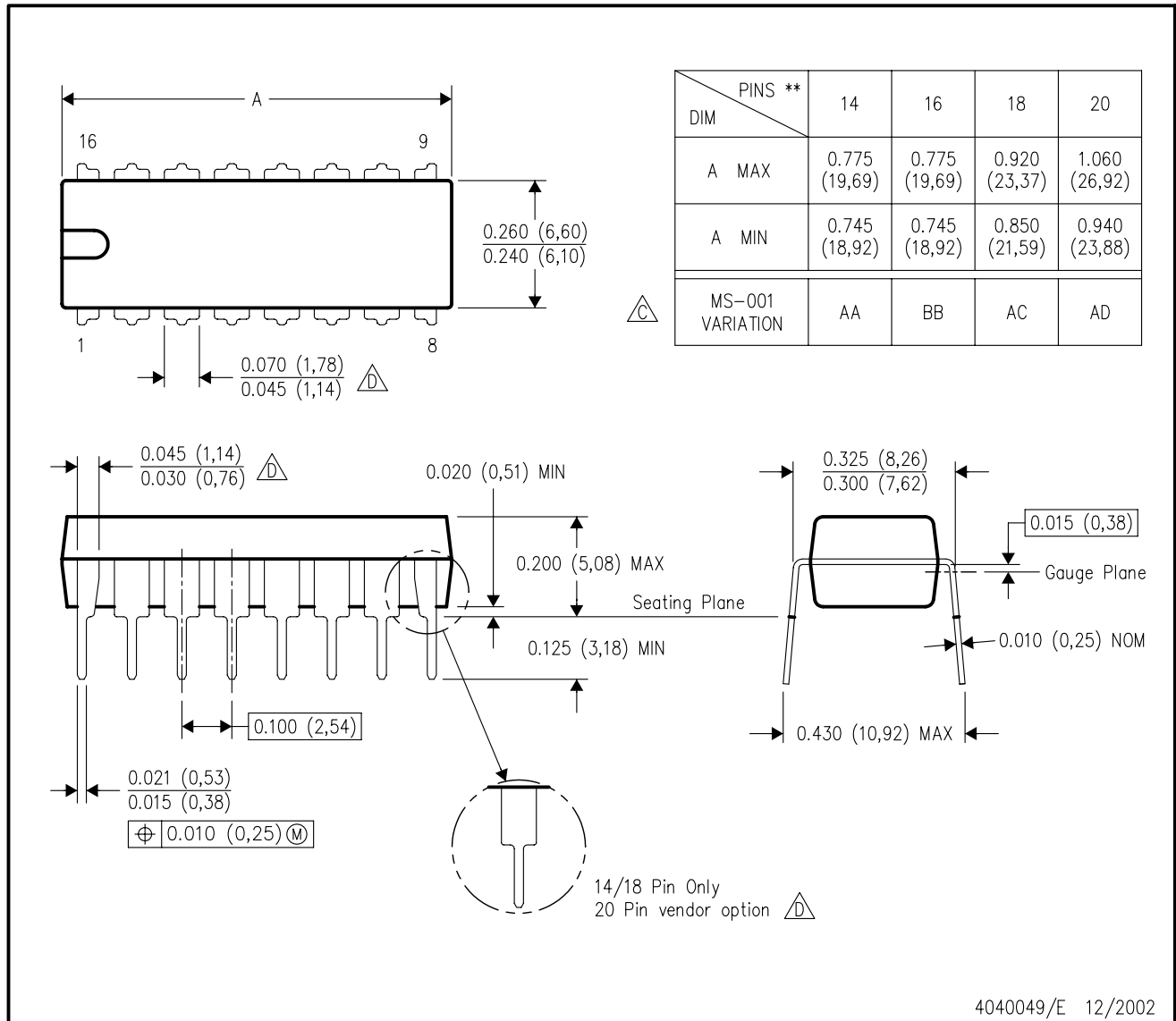


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

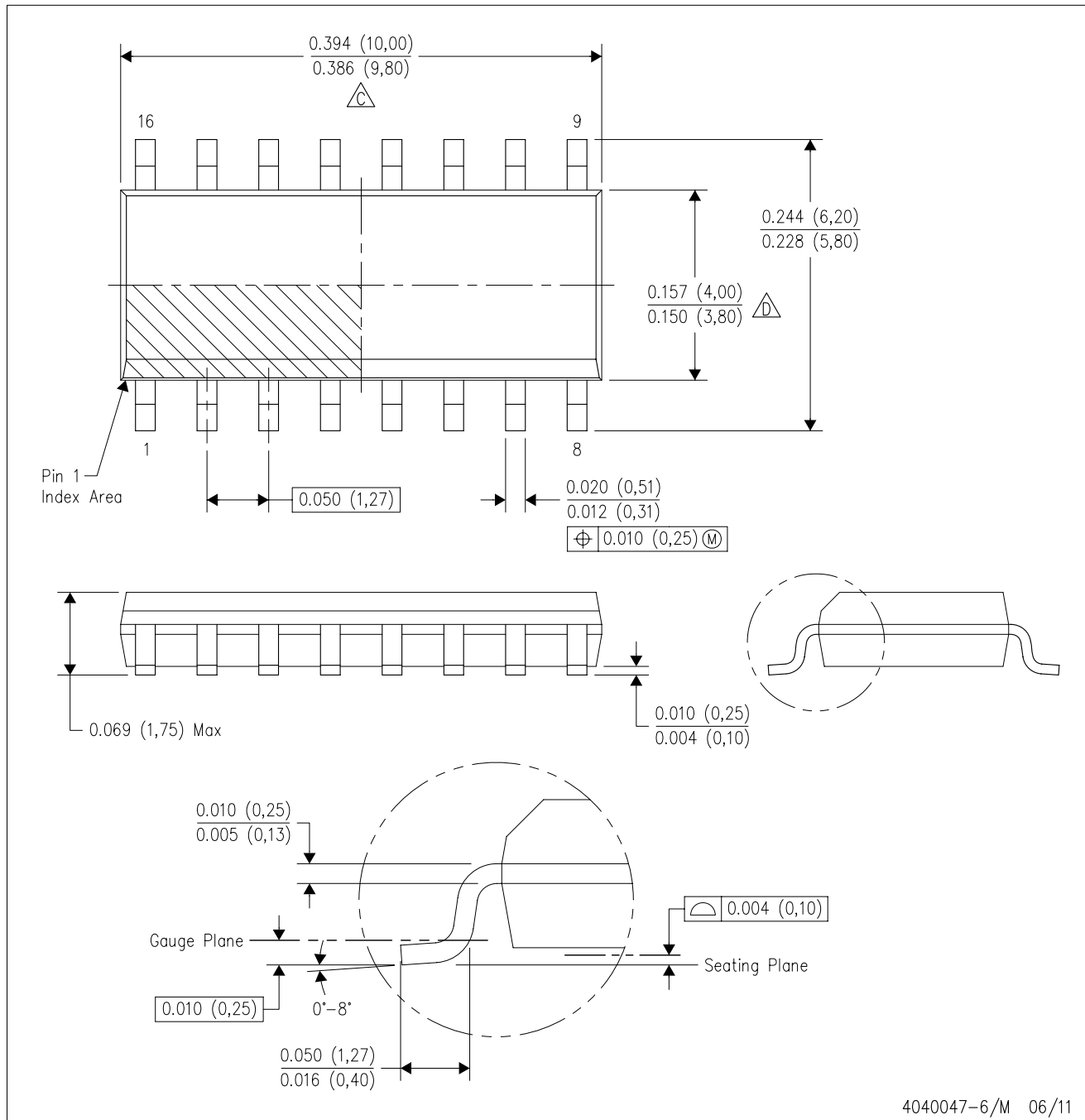


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.



4040049/E 12/2002

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

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