

# SN5474, SN54H74, SN54L74, SN54LS74A, SN54S74 SN7474, SN74H74, SN74LS74A, SN74S74

Dual D-Type Positive-Edge-Triggered Flip-Flops with Preset and Clear

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

# Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

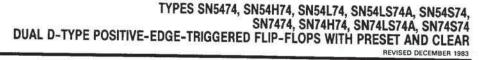
Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

# **Quality Overview**

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.



. Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

Dependable Texas Instruments Quality and Reliability

#### description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

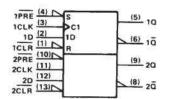
The SN54' family is characterized for operation over the full military temperature range of - 55°C to 125°C. The SN74' family is characterized for operation from 0 °C to 70 °C.

FUNCTION T	ABLE
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	INPUT	INPUTS			UTS
PRE	CLR	CLK	D	a	ā
L	н	х	х	н	L
н	L	×	x	L	н
L	L	×	×	нt	H
н	н	1	н	н	L
н	н	1	L	L	н
н	н	L	x	00	ã

<sup>†</sup> The output levels in this configuration are not guaranteed to meet the minimum levels in  $V_{OH}$  if the lows at preset and clear are near  $V_{1L}$  maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

#### logic symbol



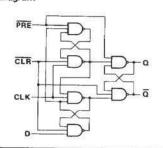
Pin numbers shown on logic notation are for D, J or N packages.

SN5474, SN54H74, SN54L74 ... J PACKAGE SN54LS74A, SN54S74 ... J OR W PACKAGE SN7474, SN74H74 ... J OR N PACKAGE SN74LS74A, SN74S74 ... D. J OR N PACKAGE (TOP VIEW) 1CLR D1 U14DVCC 13 2CLR 12 2D 1D02 1CLKD3 1PRE 4 11D2CLK 10 2PRE 1005 1006 9 20 8 20 GND 7 SN5474, SN54H74 ... W PACKAGE (TOP VIEW) 1CLKQ1 U 14 1 PRE 13010 12010 1002 1CLR C3 VccQ 11 GND 2CLR 5 10 20 2D 6 9 20 2CLK 7 8 2PRE SN54LS74A, SN54S74 ... FK PACKAGE SN74LS74A, SN74S74 ... FN PACKAGE (TOP VIEW) NC 1 20 19 1CLK 18 2D NCD 5 17 NC 1PRE 6 16 2CLK NCD7 1018 14 2PRE

NC - No internal connection

10 GNE 20 NC 20

logic diagram



PRODUCTION DATA

PRODUCTION DATA This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warrenty. Production processing does not necessarily include testing of all parameters.

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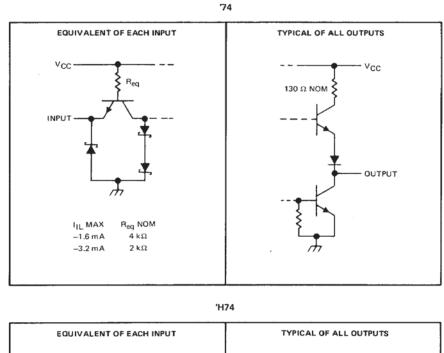


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*ITL DEVICES* 

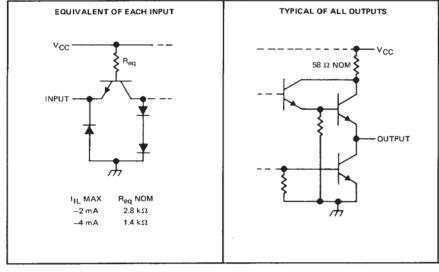
### TYPES SN5474, SN54H74, SN7474, SN74H74 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

schematics of inputs and outputs



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**TTL DEVICES** 

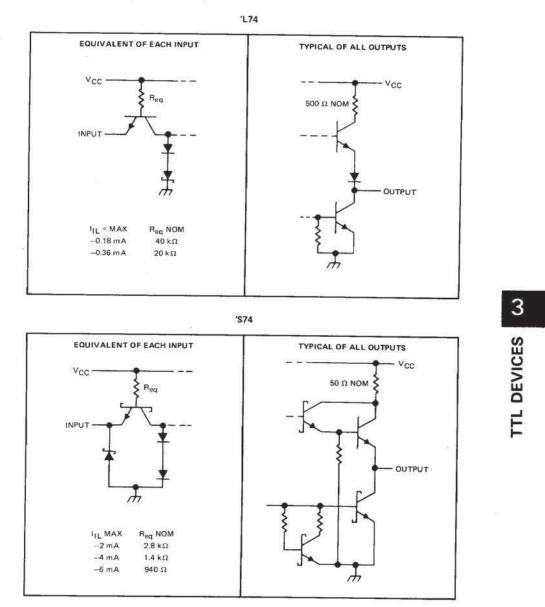




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## TYPES SN54L74, SN54S74, SN74S74 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR



schematics of inputs and outputs (continued)



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### TYPES SN5474, SN54H74, SN54L74, SN54LS74A, SN54S74, SN7474, SN74H74, SN74LS74A, SN74S74 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

schematic 'LS74A Vcc §16 kΩ 120 Ω ξ9kΩ **ξ16 k**Ω 39kΩ ş 120Ω V 5 ō ko r. 1 k!0 \$1.7 kΩ 1.7 kn 2 3.3 kn 2 3.3 kn CLR PRE  $\forall$  $\forall$ 16 kΩ \$ **ξ**16 kΩ 3 1 **ξ18 k**Ω V Г **TTL DEVICES** 36 kΩ CLK V \$31 kΩ D - GND the

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Input voltage: '74, 'H74, 'L74, 'S74	5.5 V
Operating free-air temperature range:	SN54'
	SN74' 0°C to 70°C
Storage temperature range	

NOTE 1: Voltage values are with respect to network ground terminal.



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## **TYPES \$N5474, SN7474** DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended	operating conditions
	-per uning contantions

			-	SN5474		SN7474			
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage			- 224		2		S	V
VIL	Low-level input voltage				0.8		102	0.8	V
IOH	High-level output current				- 0.4		21116-3-24	- 0.4	mA
IOL	Low-level output current				16			16	mA
		CLK high	30		1	30	10000		
tw	Pulse duration	CLK low	37	38-0.82		37			ns
		PRE or CLR low	30	ano -	and the second	30			0008
tsu	Input setup time before CLK t		20			20	17.22		ns
th	Input hold time-data after CLK 1		5			5			ns
TA	Operating free-air temperature		- 55		125	0		70	°c

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER		EST CONDITION	uet		SN5474			SN7474		
		TEST CONDITIONS.		MIN	TYP#	MAX	MIN	TYP <sup>‡</sup>	MAX	UNIT	
VIK		V <sub>CC</sub> = MIN,	lţ = - 12 mA				- 1.5			- 1.5	V
VOH		V <sub>CC</sub> = MIN, I <sub>OH</sub> = - 0.4 mA	V <sub>IH</sub> = 2 V,	V <sub>IL</sub> = 0.8 V,	2.4	3.4		2.4	3.4		v
VOL		V <sub>CC</sub> = MIN, I <sub>OL</sub> = 16 mA	V <sub>IH</sub> = 2 V,	V <sub>IL</sub> ≈ 0.8 V,		0.2	0.4		0.2	0.4	v
lj –		V <sub>CC</sub> = MAX,	VI = 5.5 V				1			1	mA
	D			116			40			40	
ЧH	CLR	CLR VCC = MAX,	V1 = 2.4 V				120	1		120	mA
	All Other	VCC-WAA,	V] - 2.4 V				80			80	1
	D						- 1.6	1		- 1.6	
13	PRE*	V <sub>CC</sub> = MAX,	V1 = 0.4 V				- 1.6			- 1.6	1 37
ΊL	L CLR*		V] = 0.4 V		- 3.2		- 3.2			- 3.2	mA
	CLK						- 3.2			- 3.2	
los§		V <sub>CC</sub> = MAX			- 20		- 57	- 18		- 57	mA
lcc		V <sub>CC</sub> = MAX,	See Note 2		-	8.5	15		8.5	15	mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
<sup>‡</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C,
\* Clear is tested with preset high and preset is tested with clear high.
<sup>§</sup> Not more than one output should be shorted at a time.
NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and Q outputs high in turn. At the time of measurement, the clock input is arounded. grounded.

#### switching charateristics, VCC = 5 V, TA = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	түр	мах	UNIT
f <sub>max</sub>				15	25	1	MHz
TPLH	PRE or CLR	Qorā				25	ns
TPHL	THE OF CEN	2012	R <sub>L</sub> = 400 Ω, C <sub>L</sub> = 15 pF			40	ns
TPLH	CLK	CLK Q or ā			14	25	ns
TPHL	CER Q OF Q				20	40	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.



### TYPES SN54H74, SN74H74 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

## recommended operating conditions

			SN54H74			SN74H74			
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage				-	2			V
VIL	Low-level input voltage			-	0.8	-		0.8	v
IOH	High-level output current				- 1	-	*	- 1	mA
IOL	Low-level output current				20			20	mA
		CLK high	15	-	11-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1	15	0		
tw	Pulse duration	CLK low	13.5		dimensi-	13.5			ns
		CLR or PRE low	25			25			
tsu	Setup time-before CLK t	High-level data	10			10	10		
su	Low-level data		15			15			ns
th	Hold time - data after CLK f		5			5	_		ns
TA	Operating free-air temperature		- 55		125	D		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

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PA	RAMETER	т	EST CONDITIC	taur		SN54H7	4									
9.3000.90092453.000.00		TEST CONDITIONS.			MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	UNIT					
VIK		VCC = MIN,	II = - 8 mA				- 1.5			- 1.5	V					
∨он	Sec. 1	V <sub>CC</sub> = MIN, I <sub>OH</sub> = - 1 mA	2016-614 (C 1101-8100-810)	V <sub>IL</sub> = 0.8 V,	2.4	3.4		2.4	3.4		v					
VOL		V <sub>CC</sub> = MIN, I <sub>OL</sub> = 20 mA	V <sub>IH</sub> = 2 V,	V <sub>IL</sub> = 0.8 V,		0.2	0.4		0.2	0.4	v					
4		V <sub>CC</sub> = MAX,	V <sub>I</sub> = 5.5 V				1			1	mA					
	D	1					50			50	1200.3					
	CLR	V <sub>CC</sub> = MAX, V <sub>1</sub> = 2.4 V		150		and the second sec			μA							
	PRE or CLK		<ul> <li>description</li> </ul>							pro-						
	D						-2			- 2						
	CLR*						-4	-	-	-4						
IL	PRE*	V <sub>CC</sub> = MAX,	$V_{1} = 0.4 V$	$v_1 = 0.4 V$	$v_1 = 0.4 V$	$v_1 = 0.4 V$	$v_1 = 0.4 V$	$v_1 = 0.4 V$	2	1 100		- 2			-2	mA
	CLK			<i>.</i> *			- 4			-4						
OS §		V <sub>CC</sub> = MAX			- 40		- 100	- 40		- 100	mA					
cc		VCC = MAX.	See Note 2			15	21		15	25	mA					

T For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. T All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^{\circ} C$ . S Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. \* Clear is tested with preset high and preset is tested with clear high. NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and Q outputs high in turn. At the time of measurement, the clock input is arounded

#### switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = $25^{\circ}$ C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	түр	мах	UNIT
fmax				35	43		MHz
<b>TPLH</b>	PRE or CLR				11.5	20	ns
1PHL	PREOFCLR	uoru	RL = 280 Ω, CL = 25 pF			30	ns
<sup>t</sup> PLH	CLK	Q or Q			8.5	15	ns
TPHL	CEN	4014			13	20	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.



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# TYPE SN54L74 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

#### recommended operating conditions

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	V
VIH	High-level input voltage		2			V
VIL	Low-level input voltage				0.7	v
IOH	High-level output current			231	- 0.1	mA
IOL	Low-level output current				2	mA
tw	Pulse duration	CLK high or low	200		100	
w	T dise duration	CLR or PRE low	100			ns
t <sub>su</sub>	Setup time before CLK f	in the second	50			ns
th	Hold time data after CLK †		15			ns
TA	Operating free-air temperature		- 55	21 1 2 2	125	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P	ARAMETER	1975	TE	ST CONDITIONS <sup>†</sup>		MIN T	PI MAX	UNIT
VOH		V <sub>CC</sub> = MIN,	VIH = 2 V,	VIL = 0.7 V,	OH = 0.1 mA	2.4	3.3	V
VOL		V <sub>CC</sub> = MIN,	VIH = 2 V,	V <sub>1L</sub> = 0.7 V,	IOL = 2 mA		.15 0.3	V
1111	D						0.1	1
\$ <sub>1</sub>	CLR	VCC = MAX,	V1 = 5.5 V				0.3	mA
	PRE or CLK							1
	D			198			0.2	10-02-1
Чн	CLR	VCC = MAX.	V <sub>1</sub> = 2.4 V			μA		
	PRE or CLK					1	30	per
50 C	D or PRE	0.00	223 (1772)	8			- 0.18	-
μL	CLR or CLK	V <sub>CC</sub> = MAX,	V1 = 0.3 V				- 0.36	μA
los		V <sub>CC</sub> = MAX				-3	- 15	mA
lcc		V <sub>CC</sub> = MAX,	See Note 2				0.8 1.5	mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. <sup>‡</sup> All typical values are at  $V_{CC}$  = 5 V,  $T_A$  = 25°C. NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and  $\overline{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

## switching characteristics, $V_{CC} = 5 V$ , $T_A = 25^{\circ}C$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST COND	MIN	түр	мах	UNIT	
fmax					2.5	3		MHz
<b>tPLH</b>	PRE or CLR	QorQ				50	75	ns
	PRE or CLR (CLK high)           PRE or CLR (CLK low)           PRE or CLR (CLK low)	ā or Q		80	80	150		
TPHL			$R_L = 4 k\Omega$ ,	$C_L = 50 pF$		80	150	ns
<sup>T</sup> PLH		QorQ			15 65		100	ns
TPHL Clock	U or Q			15	65	150	ns	

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NOTE 3: See General Information Section for load circuits and voltage waveforms.



TTL DEVICES



#### TYPES SN54LS74A, SN74LS74A DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

#### recommended operating conditions

			SN54LS74A			SN74LS74A			12001022
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage		2			2		2	V
VIL	Low-level input voltage				0.7		1000	0.8	V
юн	High-level output current				-0.4			-0.4	mA
OL	Low-level output current			Č.	4			8	mA
fclock	Clock frequency		0		25	0	-	25	MHz
	Pulse duration	CLK high	25			25			
tw	Fuise duration	PRE or CLR low	25		-	25	10	11	ns
tsu	Setup time-before CLK t	High-level data	20	- 1900C		20		24440440	
su	Low-level data		20			20			ns
th	Hold time-data after CLK 1		5	1111		5		1023	ns
TA	Operating free-air temperature	2000	- 55		125	0	1-01	70	°c

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P	ARAMETER	TEC	T CONDITIONS		S	N54LS7	4A	S	N74LS7	4A	
	ANAMETEN	TEST CONDITIONS'			MIN	TYP <sup>‡</sup>	MAX	MIN	TYP\$	MAX	UNIT
VIK		V <sub>CC</sub> = MIN,	lj = - 18 mA		T		- 1.5			- 1.5	V
v <sub>он</sub>		V <sub>CC</sub> = MIN, I <sub>OH</sub> = - 0.4 mA	V <sub>IH</sub> = 2 V,	VIL - MAX,	2.5	3.4		2.7	3.4		v
VOL		V <sub>CC</sub> = MIN, I <sub>OL</sub> = 4 mA	VIL = MAX,	V <sub>IH</sub> = 2 V,		0.25	0.4		0.25	0.4	
		V <sub>CC</sub> = MIN, I <sub>OL</sub> = 8 mA	V <sub>IL</sub> = MAX,	IL = MAX, VIH = 2 V,					0.35	0.5	v
h	D or CLK	VCC = MAX,	= MAX, VI = 7 V		1	07.55	0.1	1.21		0.1	1.000
"	CLR or PRE	VCC - MAA,	v1 - 3 v				0.2		0.2	0.2	mA
Inc	D or CLK	Vcc = MAX,	V 2 7 V		1	9765	20	-		20	
чн	CLR or PRE	VCC - MAA,	V1 - 2.7 V		40		40	40			μA
IIL D or CLK		Ver a MAX	N - 0 4 M			- 0.4		-0.4			Content of the
		V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			- 0.8		- 0.8			mA	
loss		V <sub>CC</sub> = MAX,	See Note 4		- 20		- 100	20		- 100	mA
lcc		V <sub>CC</sub> = MAX,	See Note 2			4	8		4	8	mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommanded operating conditions. <sup>‡</sup> All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^{\circ}C$ . § Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. NOTE 2: With all outputs open,  $I_{CC}$  is measured with the Q and Q outputs high in turn. At the time of measurement, the clock input is arounded

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and Q datasets high a state of the state of the

#### switching characteristics, $V_{CC} = 5 V$ , $T_A = 25^{\circ}C$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	түр	мах	UNIT
f <sub>max</sub>					25	33		MHz
TPLH	CLR, PRE or CLK	QorQ	$R_L = 2 k\Omega$ ,	CL = 15 pF		13	25	MHz
TPHL	ULN, PHE OF ULK	QOFQ				25	40	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.



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**TTL DEVICES** 

# **TYPES SN54S74, SN74S74** DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

#### recommended operating conditions

_			SN54S74			SN74S74				
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	V	
VIH	High-level input voltage		2			2			V	
VIL	Low-level input voltage			-	0.8			0.8	V	
ОН	High-level output current				- 1			- 1	mA	
OL	Low-level output current				20			20	mA	
01		CLK high	6			6				
tw	Pulse duration	CLK low	7.3			7.3	1025		ns	
		CLR or PRE low	7		015015	7				
	S Sections	High-level data	3	201 C		3			ns	
tsu	Setup time, before CLK f Low-level data		3		7.8	3	-		1.5	
<sup>t</sup> h	Input hold time - data after CLK †		2			2	-		ns	
TA	Operating free-air temperature		- 55		125	0	0.55	70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

0.000					SN54S74		SN74S74			
PARAMETER		TEST CONDITIONS <sup>†</sup>		MIN	TYP <sup>‡</sup> MA	X MIN	түр‡	MAX	UNIT	
VIK		V <sub>CC</sub> = MIN,	II = - 18 mA,		- 1	.2		- 1.2	V	
Voн		V <sub>CC</sub> = MIN, I <sub>OH</sub> = -1 mA	V <sub>IH</sub> = 2 V, V <sub>IL</sub> =	0.8 V, 2.5	3.4	2.7	3.4		v	
VOL		V <sub>CC</sub> = MIN, I <sub>OL</sub> = 20 mA	V <sub>IH</sub> = 2 V, V <sub>IL</sub> =	0.8 V.	0	.5		0.5	v	
4		VCC = MAX,	V <sub>1</sub> = 5.5 V			1		1	mA	
	D					50		50	mA	
чн	CLR	Vcc = MAX,	V <sub>CC</sub> = MAX, V <sub>1</sub> = 2.7 V		1	50				
111	PRE or CLK	- CC			100					
	D				- 2		2 - 2			
	CLR*		101 23232		- 6 - 4 - 4		- 4			
ηL	PRE*	V <sub>CC</sub> = MAX,	VI = 0.5 V	0						
	CLK									
los§	102.0	Vcc = MAX		- 40	- 1	00 - 40	)	- 100	mA	
ICC		VCC = MAX,	See Note 2		15	25	15	25	mA	

<sup>1</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
 <sup>1</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.
 <sup>2</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
 <sup>3</sup> Clear is tested with preset high and preset is tested with clear high.
 NOTE 2: All outputs open, I<sub>CC</sub> is measured with the Q and Q outputs high in turn. At the time of measurement, the clock input is grounded.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25 $^{\circ}$ C (see note 3)

PARAMETER	TER FROM TO TEST CONDITIONS		MIN	TYP	мах	UNIT	
fmax	16.2			75	110		MHz
IPLH	PRE or CLR	QorQ			4	6	ns
	PRE or CLR (CLK high)			r . r	9	13.5	ns
TPHL	PRE or CLR (CLK low)	Q or Q	$R_{L} = 280 \Omega$ , $C_{L} = 1$	5 pF	5	8	115
					6	9	ns
	CLK	QorQ			6	9	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.



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