

SN5473, SN54H73, SN54L73, SN54LS73A SN7473, SN74H73, SN74LS73A

Dual J-K Flip-Flops with Clear

The '73, 'H73, and 'L73 contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '73, 'H73, and 'L73 are positive pulse-triggered flip-flops. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS73A contain two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the \bar{Q} output high.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

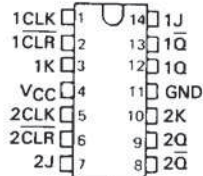
The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

TYPES SN5473, SN54H73, SN54L73, SN54LS73A,
SN7473, SN74H73, SN74LS73A
DUAL J-K FLIP-FLOPS WITH CLEAR

REVISED DECEMBER 1983

- Package Options Include Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN5473, SN54H73, SN54LS73A ... J OR W PACKAGE
SN54L73 ... J PACKAGE
SN7473, SN74H73 ... J OR N PACKAGE
SN74LS73A ... D, J OR N PACKAGE
(TOP VIEW)



description

The '73, 'H73, and 'L73 contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '73, 'H73, and 'L73 are positive pulse-triggered flip-flops. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS73A contain two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the \bar{Q} output high.

The SN5473, SN54H73, SN54L73, and the SN54LS73A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7473, SN74H73, and the SN74LS73A are characterized for operation from 0°C to 70°C .

'73, 'H73, 'L73
FUNCTION TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	\downarrow	L	L	Q_0	\bar{Q}_0
H	\downarrow	H	L	H	L
H	\downarrow	L	H	L	H
H	\downarrow	H	H	TOGGLE	

'LS73A
FUNCTION TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	\downarrow	L	L	Q_0	\bar{Q}_0
H	\downarrow	H	L	H	L
H	\downarrow	L	H	L	H
H	\downarrow	H	H	TOGGLE	
H	H	X	X	Q_0	Q_0

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CONTACT THE FACTORY

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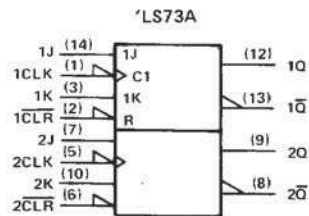
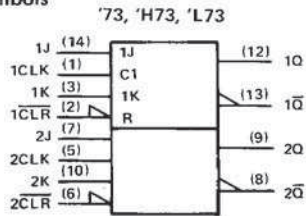
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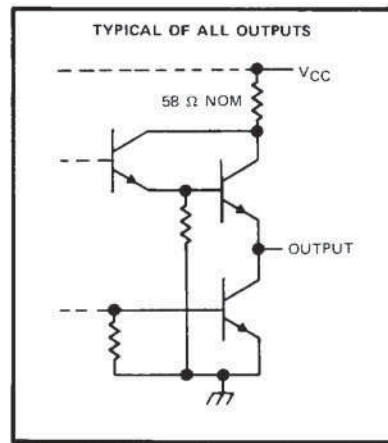
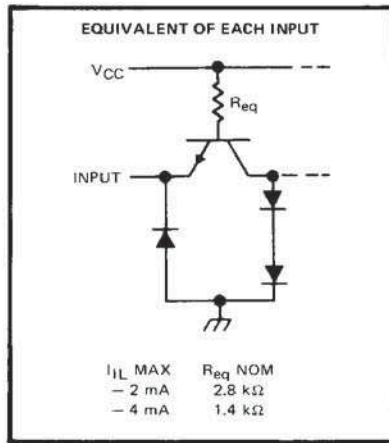
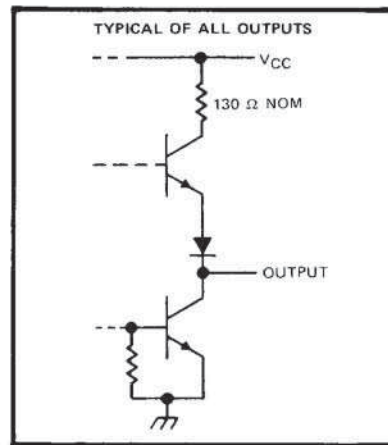
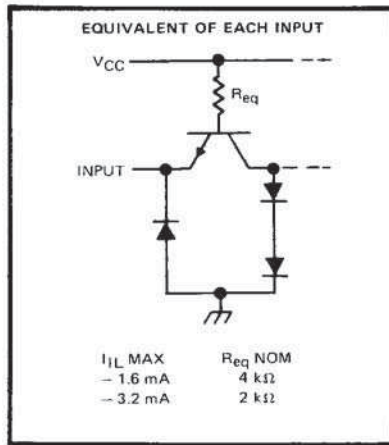
TYPES SN5473, SN54H73, SN54L73, SN54LS73A,
SN7473, SN74H73, SN74LS73A
DUAL J-K FLIP-FLOPS WITH CLEAR

logic symbols



Pin numbers shown on logic notation are for D, J or N packages.

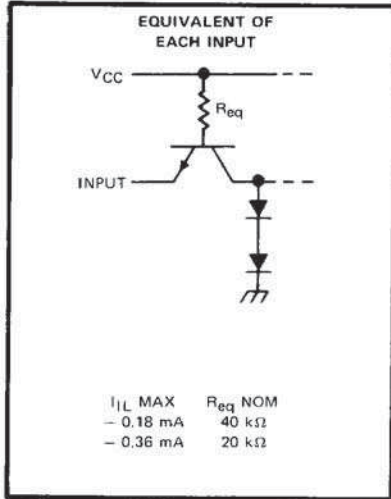
schematics of inputs and outputs



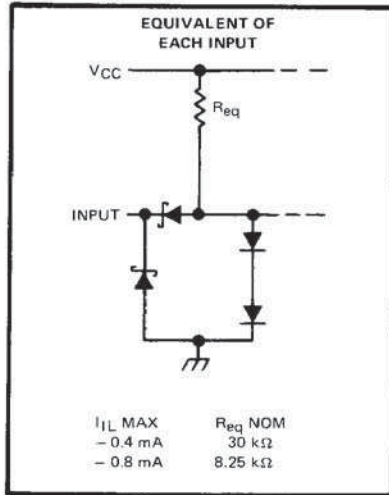
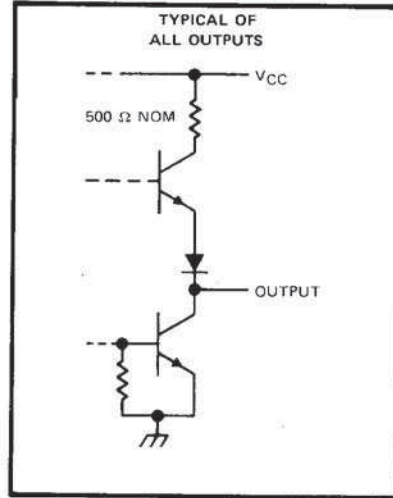
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TYPES SN54L73, SN54LS73A, SN74LS73A
DUAL J-K FLIP-FLOPS WITH CLEAR

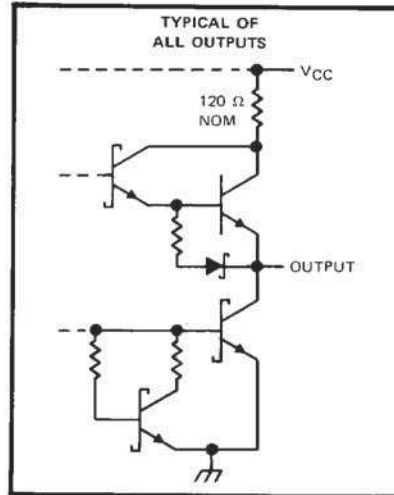
schematics of inputs and outputs (continued)



'L73



'LS73A

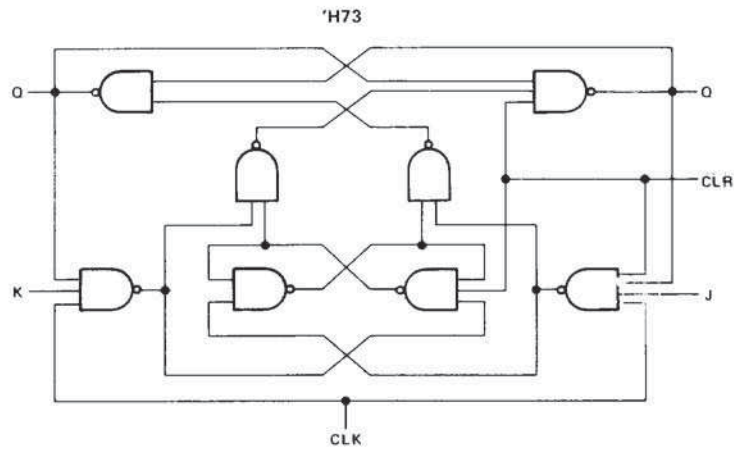
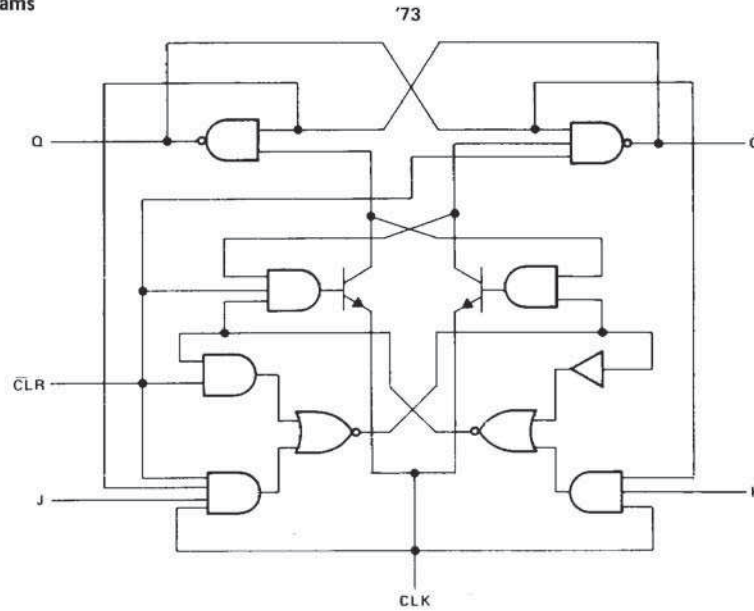


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TYPES SN5473, SN54H73, SN7473, SN74H73
 DUAL J-K FLIP-FLOPS WITH CLEAR

logic diagrams

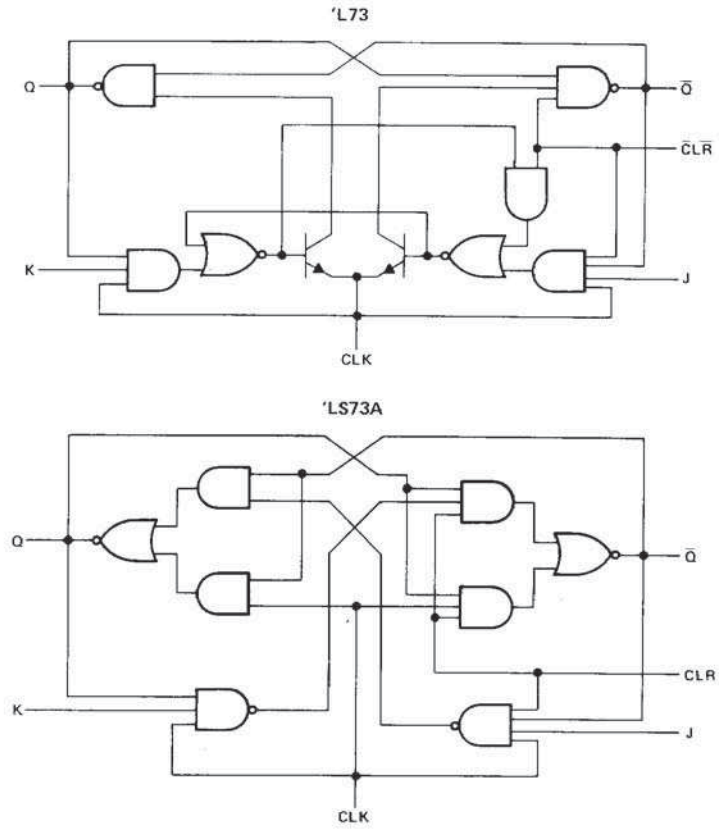


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TTL DEVICES

TYPES SN5473, SN54H73, SN54L73, SN54LS73A,
SN7473, SN74H73, SN74LS73A
DUAL J-K FLIP-FLOPS WITH CLEAR

logic diagrams (continued)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '73, 'H73, 'L73	5.5 V
'LS73A	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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TYPES SN5473, SN7473
DUAL J-K FLIP-FLOPS WITH CLEAR

recommended operating conditions

	SN5473			SN7473			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			-0.4			-0.4	mA
I _{OL} Low-level output current			16			16	mA
t _w Pulse duration	CLK high	20		20			ns
	CLK low	47		47			
	CLR low	25		25			
t _{su} Input setup time before CLK †	0			0			ns
t _h Input hold time data after CLK †	0			0			ns
T _A Operating free-air temperature	-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5473		SN7473		UNIT		
		MIN	TYP‡	MAX	MIN		TYP‡	MAX
V _{IK}	V _{CC} = MIN, I _I = -12 mA			-1.5		-1.5	V	
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -0.4 mA	2.4	3.4		2.4	3.4	V	
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1		1	mA	
I _{IH}	J or K		40			40	µA	
	CLR or CLK	V _{CC} = MAX, V _I = 2.4 V		80		80		
I _{IL}	J or K		-1.6			-1.6	mA	
	CLR	V _{CC} = MAX, V _I = 0.4 V		-3.2		-3.2		
	CLK			-3.2		-3.2		
I _{OS} §	V _{CC} = MAX	-20		-57		-18	-57	mA
I _{CC}	V _{CC} = MAX, See Note 2		10	20		10	20	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and Q outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}				15	20		MHz
t _{PLH}	CLR	Q	R _L = 400 Ω, C _L = 15 pF		16	25	ns
t _{PHL}		Q			25	40	ns
t _{PLH}	CLK	Q or Q̄			16	25	ns
t _{PHL}		Q or Q̄			25	40	ns

¶ f_{max} = maximum clock frequency; t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output.

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54H73, SN74H73
DUAL J-K FLIP-FLOPS WITH CLEAR

recommended operating conditions

		SN54H73			SN74H73			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage	0.8			0.8			V
I _{OH}	High-level output current	-0.5			-0.5			mA
I _{OL}	Low-level output current	20			20			mA
t _w	Pulse duration	CLK high	12		12		ns	
		CLK low	28		28			
		CLR low	16		16			
t _{su}	Input setup time before CLK↑	High-level data	0		0		ns	
		Low-level data	0		0			
t _h	Input hold time, data after CLK↓	0			0			ns
T _A	Operating free-air temperature	-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54H73			SN74H73			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -8 mA	-1.5			-1.5			V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -0.5 mA	2.4	3.4		2.4	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA	0.2 0.4		0.2 0.4				V
I _I	V _{CC} = MAX, V _I = 5.5 V	1			1			mA
I _{IH}	J, K, or CLK	50			50			μA
	CLR	100			100			
I _{IL}	J, K, or CLK	-2			-2			mA
	CLR	-4			-4			
I _{OS} §	V _{CC} = MAX	-40	-100		-40	-100		mA
I _{CC}	V _{CC} = MAX, See Note 2	16	25		16	25		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			R _L = 280 Ω, C _L = 25 pF	25	30		MHz
t _{PLH}	CLR	\bar{Q}		6	13		ns
t _{PHL}		Q		12	24		ns
t _{PLH}	CLK	Q or \bar{Q}		14	21		ns
t _{PHL}				22	27		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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**TYPE SN54L73
DUAL J-K FLIP-FLOPS WITH CLEAR**

recommended operating conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			V
V _{IL}	Low-level input voltage			0.6	V
				0.7	
I _{OH}	High-level output current			-0.1	mA
I _{OL}	Low-level output current			2	mA
t _w	Pulse duration			200	ns
				100	
t _{su}	Setup time before CLK ↑			0	ns
t _h	Hold time-data after CLK ↓			0	ns
T _A	Operating free-air temperature	-55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP ‡	MAX	UNIT
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.1 mA	2.4	3.3			V	
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OL} = 2 mA		0.15	0.3		V	
I _I	J or K	V _{CC} = MAX, V _I = 5.5 V			0.1		mA	
	CLR or CLK				0.2			
I _{IH}	J or K	V _{CC} = MAX, V _I = 2.4 V			10		μA	
	CLR				20			
	CLK				-200			
I _{IL}	J or K	V _{CC} = MAX, V _I = 0.3 V			-0.18		mA	
	CLR or CLK				-0.36			
I _{OS}		V _{CC} = MAX	-3		-15		mA	
I _{CC}		V _{CC} = MAX, See Note 2	0.76	1.44			mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f _{max}					2.5	3		MHz
t _{PLH}	CLR	Q or \bar{Q}	R _L = 4 kΩ, C _L = 50 pF		35	75		ns
t _{PHL}	CLR (CLK high)	\bar{Q} or Q		60	150			ns
	CLR (CLK low)				200			
t _{PLH}	CLK	Q or \bar{Q}		10	35	75		ns
t _{PHL}				10	60	150		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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TTL DEVICES

TYPES SN54LS73A, SN74LS73A
DUAL J-K FLIP-FLOPS WITH CLEAR

recommended operating conditions

		SN54LS73A			SN74LS73A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage				0.8			V
I _{OH}	High-level output current				-0.4			mA
I _{OL}	Low-level output current				4			mA
f _{clock}	Clock frequency	0	30		0	30		MHz
t _w	Pulse duration	CLK high		20		20		ns
		CLR low		25		20		
t _{su}	Set up time-before CLK ↓	data high or low		20		20		ns
		CLR inactive		20		20		
t _h	Hold time-data after CLK ↓	0		0		0		ns
T _A	Operating free-air temperature	-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS73A			SN74LS73A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA	-1.5			-1.5			V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.4 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 4 mA	0.25 0.4			0.25 0.4			V
	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 8 mA				0.35 0.5			
I _I	J or K	0.1			0.1			mA
	CLR	0.3			0.3			
	CLK	0.4			0.4			
I _{IH}	J or K	20			20			μA
	CLR	60			60			
	CLK	80			80			
I _{IL}	J or K	-0.4			-0.4			mA
	CLR or CLK	-0.8			-0.8			
I _{OS} §	V _{CC} = MAX, See Note 4	-20	-100		-20	-100		mA
I _{CC}	V _{CC} = MAX, See Note 2	4 6			4 6			mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{max}				30	45		MHz
t _{PLH}	CLR or CLK	Q or Q̄	R _L = 2 kΩ, C _L = 15 pF	15		20	ns
t _{PHL}				15		20	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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TTL DEVICES