DM54LS196, DM74LS196, DM54LS197, DM74LS197

Presettable Decade and Binary Counters

These high-speed counters consists of four d-c coupled, master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter (196) or a divide-by-two and a divide-by-eight counter (197). These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which, when taken low, sets all outputs low regardless of the state of the clocks.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

National Semiconductor

DM54LS196/DM74LS196, DM54LS197/DM74LS197 Presettable Decade and Binary Counters

General Description

These high-speed counters consist of four d-c coupled, master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter (196) or a divide-by-two and a divide-by-eight counter (197). These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which, when taken low, sets all outputs low regardless of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

TYPICAL COUNT CONFIGURATIONS LS196

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

1. When used as a BCD decade counter, the clock-2 input must be externally connected to the Q_A output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary truth table.
3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

LS197

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore the counter may be operated in two independent modes:

1. When used as a high-speed 4-bit ripple-through counter, output Q_A must be externally connected to the clock-2 input. The input count pulses are applied to the clock-1 input. Simultaneous divisions by 2, 4, 8, and 16 are performed at the Q_A, Q_B, Q_C, and Q_D outputs as shown in the truth table.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock-2 input. Simultaneous frequency divisions by 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple-through counter.

Features

- Performs BCD, bi-quinary, or binary counting
- Fully programmable
- Fully independent clear input
- Output Q_A maintains full fan-out capability in addition to driving clock-2 input
- Typical count frequency
  Clock 1 40 MHz
  Clock 2 20 MHz
- Typical power dissipation 80 mW

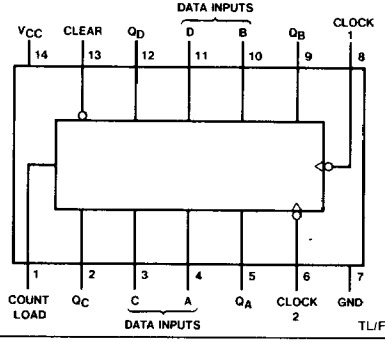
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram (Dual-In-Line Package)

54LS196 (J) **74LS196 (N)**
54LS197 (J) **74LS197 (N)**



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Note: Low input to clear sets Q_A, Q_B, Q_C and Q_D low.

Recommended Operating Conditions

Symbol	Parameter		DM54LS196			DM74LS196			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		30	0		30	MHz
	Clock Frequency (Note 3)		0		20	0		20	MHz
t_W	Pulse Width	Clock 1	20			20			ns
		Clock 2	30			30			
		Clear	15			15			
		Load	20			20			
t_{SU}	Setup Time (Note 1)	Data High	8↑			8↑			ns
		Data Low	12↑			12↑			
t_H	Hold Time (Note 1)	Data High	0↑			0↑			ns
		Data Low	6↑			6↑			
t_{EN}	Count Enable Time (Note 4)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: $C_L = 15$ pF and $R_L = 2$ kΩ.

Note 3: $C_L = 50$ pF and $R_L = 2$ kΩ.

Note 4: Count-enable time is the interval immediately preceding the negative-going edge of the clock pulse during which the COUNT/LOAD and CLEAR inputs must both be high to ensure counting.

'LS196 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min (Note 4)	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V	Clock 1			0.2	mA
			Clock 2			0.4	
			Clear			0.2	
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Clock 1			40	μA
			Clock 2			80	
			Clear			40	
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clock 1			−2.4	mA
			Clock 2			−2.8	
			Clear			−0.8	
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			16	27	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Note 4: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the CLOCK 2 input. This permits driving the CLOCK 2 input while maintaining full fan-out capability.

'LS196 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	Clock 1 to Q_A	30	40		20	30		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 1 to Q_A		8	15		11	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 1 to Q_A		13	20		20	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_B		10	24		19	29	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_B		22	33		28	42	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_C		22	57		45	68	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_C		22	62		48	72	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_D		12	18		15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_D		12	45		36	54	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Any Q		11	30		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Any Q		29	44		35	53	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Any Q		27	41		30	45	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Any Q		30	45		36	54	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		29	51		40	60	ns

Recommended Operating Conditions

Symbol	Parameter		DM54LS197			DM74LS197			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		30	0		30	MHz
	Clock Frequency (Note 3)		0		20	0		20	MHz
t_W	Pulse Width	Clock 1	20			20			ns
		Clock 2	30			30			
		Clear	15			15			
		Load	20			20			
t_{SU}	Setup Time (Note 1)	Data High	8↑			8↑			ns
		Data Low	12↑			12↑			
t_H	Hold Time (Note 1)	Data High	0↑			0↑			ns
		Data Low	6↑			6↑			
t_{EN}	Count Enable Time (Note 4)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: $C_L = 15$ pF and $R_L = 2$ kΩ.

Note 3: $C_L = 50$ pF and $R_L = 2$ kΩ.

Note 4: Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which the COUNT/LOAD and CLEAR inputs must both be high to ensure counting.

'LS197 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min (Note 4)	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V	Clock 1			0.2	mA
			Clock 2			0.2	
			Clear			0.2	
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Clock 1			40	μA
			Clock 2			40	
			Clear			40	
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clock 1			−2.4	mA
			Clock 2			−1.3	
			Clear			−0.8	
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			16	27	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Note 4: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the CLOCK 2 input. This permits driving the CLOCK 2 input while maintaining full fan-out capability.

'LS197 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	Clock 1 to Q_A	30	40		20	30		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 1 to Q_A		8	15		11	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 1 to Q_A		14	21		20	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_B		12	19		15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_B		15	35		29	44	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_C		22	51		40	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_C		25	63		50	75	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_D		30	78		65	98	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_D		35	95		71	106	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Any Q		15	27		21	32	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Any Q		29	44		35	53	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Any Q		20	39		29	45	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Any Q		30	45		36	54	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		29	51		40	60	ns

Function Tables

LS196
Decade (BCD)
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

LS196
(See Note B)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

LS197
(See Note A)

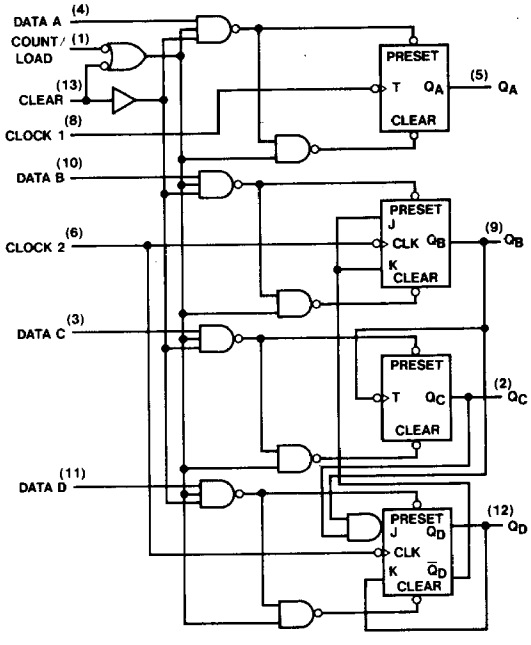
Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = High Level, L = Low Level

Note A: Output Q_A connected to clock-2 input.
Note B: Output Q_D connected to clock-1 input.

Logic Diagrams

LS196



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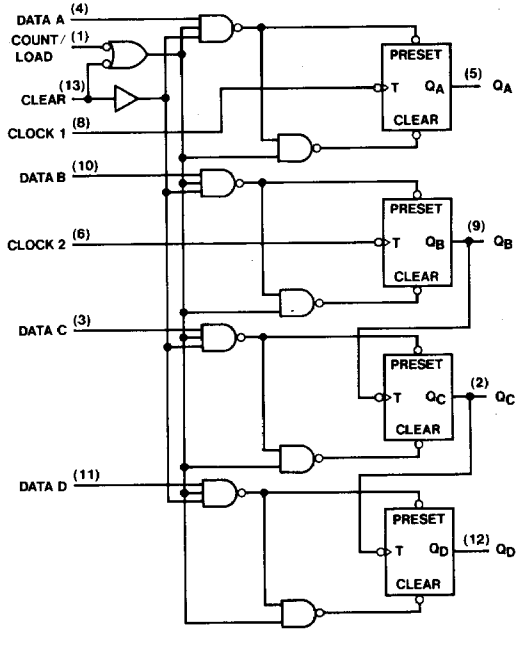

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