# DG181-DG191

## *High-Speed Drivers with JFET Switch*

The DG181 thru DG191 series of analog gates consist of 2 or 4 N-channel junction-type field-effect transistors (JFET) designed to function as electronic switches. Level-shifting drivers enable low-level inputs (0.8V to 2V) to control the ON-OFF state of each switch. The driver is designed to provide a turn-off speed which is faster than turn-on speed, so that break-before-make action is achieved when switching from one channel to another. In the ON state, each switch conducts current equally well in both directions. In the OFF condition, the switches will block voltages up to 20V peak-to-peak. Switch-OFF input-output isolation 50dB at 10MHz, due to the low output impedance of the FET-gate driving circuit.

### Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

### Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

*The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

HARRIS Semiconductor

# DG181 thru DG191

April 1999

OBSOLETE PRODUCT
POSSIBLE SUBSTITUTE PRODUCT
DG184, DG185: HI-5049, HI-5045
DG190: DG403, HI-5051, IH5151
DG191: HI-5043, HI-0390, IH5043

## High-Speed Drivers with JFET Switch

### Features

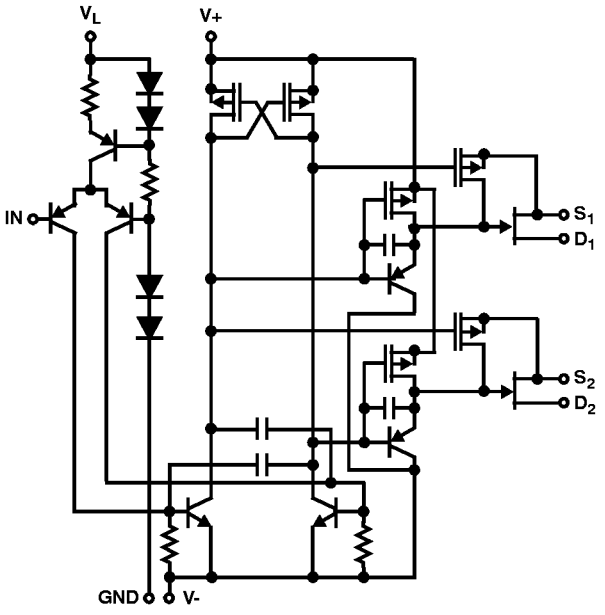
- **Constant ON ... signals to ±10V (DG182, DG185, DG18... ), to ±7.5V (All Devices)**
- **±15V Power Supplies**
- **<2nA Leakage from Signal Channel in Both ON and OFF States**
- **TTL, DTL, RTL Direct Drive Compatibility**
- **$t_{ON}$, $t_{OFF}$ <150ns, Break-Before-Make Action**
- **Cross-Talk and Open Switch Isolation >50dB at 10MHz (75Ω Load)**

### Description

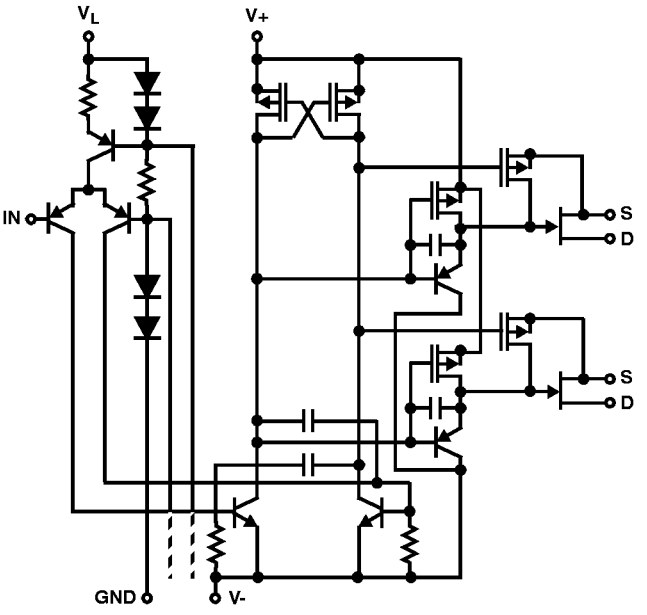
The DG181 thru DG191 series of analog gates consist of 2 or 4 N-channel junction-type field-effect transistors (JFET) designed to function as electronic switches. Level-shifting drivers enable low-level inputs (0.8V to 2V) to control the ON-OFF state of each switch. The driver is designed to provide a turn-off speed which is faster than turn-on speed, so that break-before-make action is achieved when switching from one channel to another. In the ON state, each switch conducts current equally well in both directions. In the OFF condition, the switches will block voltages up to 20V peak-to-peak. Switch-OFF input-output isolation 50dB at 10MHz, due to the low output impedance of the FET-gate driving circuit.

### Functional Diagrams (Typical Channel)

**DG186, DG187, DG188 - ONE AND TWO CHANNEL SPDT AND SPST CIRCUIT CONFIGURATION**




**DG183, DG184, DG185 - TWO CHANNEL DPST CIRCUIT CONFIGURATION**






File Number **3114.4**

## Part Number Information

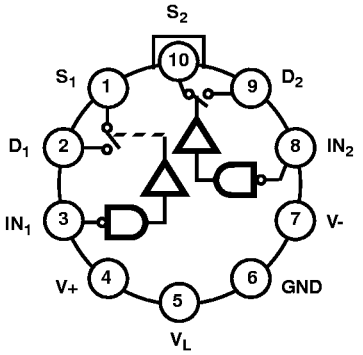
| PART NUMBER | TYPE | $R_{DS(ON)}$ (MAX) | PACKAGE |
|---|---|---|---|
| DG181AA | Dual SPST | 30Ω | 10 Lead CAN |
| DG181AA/883B | Dual SPST | 30Ω | 10 Lead CAN |
| DG181AP | Dual SPST | 30Ω | 14 Lead SBDIP |
| DG181AP/883B | Dual SPST | 30Ω | 14 Lead SBDIP |
| DG181BA | Dual SPST | 30Ω | 10 Lead CAN |
| DG181BP | Dual SPST | 30Ω | 14 Lead SBDIP |
| DG182AA | Dual SPST | 75Ω | 10 Lead CAN |
| DG182AA/883B | Dual SPST | 75Ω | 10 Lead CAN |
| DG182AP | Dual SPST | 75Ω | 14 Lead SBDIP |
| DG182AP/883B | Dual SPST | 75Ω | 14 Lead SBDIP |
| DG182BA | Dual SPST | 75Ω | 10 Lead CAN |
| DG182BP | Dual SPST | 75Ω | 14 Lead SBDIP |
| DG184AP | Dual DPST | 30Ω | 16 Lead SBDIP |
| DG184AP/883B | Dual DPST | 30Ω | 16 Lead SBDIP |
| DG184BP | Dual DPST | 30Ω | 16 Lead SBDIP |
| DG185AP | Dual DPST | 75Ω | 16 Lead SBDIP |
| DG185AP/883B | Dual DPST | 75Ω | 16 Lead SBDIP |
| DG185BP | Dual DPST | 75Ω | 16 Lead SBDIP |

## Part Number Information (Continued)

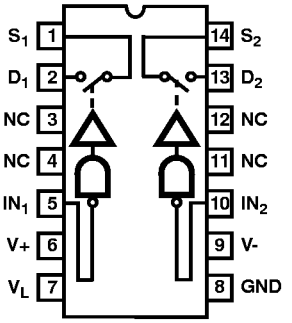
| PART NUMBER | TYPE | $R_{DS(ON)}$ (MAX) | PACKAGE |
|---|---|---|---|
| DG187AA | SPDT | 30Ω | 10 Lead CAN |
| DG187AA/883B | SPDT | 30Ω | 10 Lead CAN |
| DG187AP | SPDT | 30Ω | 14 Lead SBDIP |
| DG187AP/883B | SPDT | 30Ω | 14 Lead SBDIP |
| DG187BA | SPDT | 30Ω | 10 Lead CAN |
| DG187BP | SPDT | 30Ω | 14 Lead SBDIP |
| DG188AA | SPDT | 75Ω | 10 Lead CAN |
| DG188AA/883B | SPDT | 75Ω | 10 Lead CAN |
| DG188AP | SPDT | 75Ω | 14 Lead SBDIP |
| DG188AP/883B | SPDT | 75Ω | 14 Lead SBDIP |
| DG188BA | SPDT | 75Ω | 10 Lead CAN |
| DG188BP | SPDT | 75Ω | 14 Lead SBDIP |
| DG190AP | Dual SPDT | 30Ω | 16 Lead SBDIP |
| DG190AP/883B | Dual SPDT | 30Ω | 16 Lead SBDIP |
| DG190BP | Dual SPDT | 30Ω | 16 Lead SBDIP |
| DG191AP | Dual SPDT | 75Ω | 16 Lead SBDIP |
| DG191AP/883B | Dual SPDT | 75Ω | 16 Lead SBDIP |
| DG191BP | Dual SPDT | 75Ω | 16 Lead SBDIP |

## *Pinouts and Switching State Diagrams*

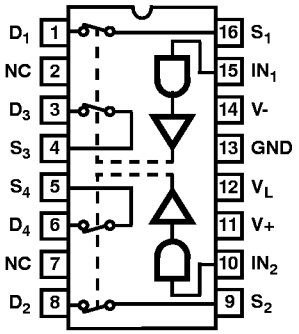
**DUAL SPST - DG181, DG182**
**(TO-100 METAL CAN)**
TOP VIEW



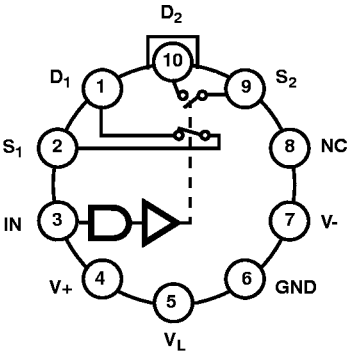

**DUAL SPST - DG181, DG182**
**(CDIP)**
TOP VIEW



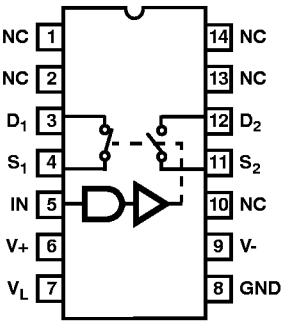

**DUAL DPST - DG184, DG185**
**(CDIP)**
TOP VIEW



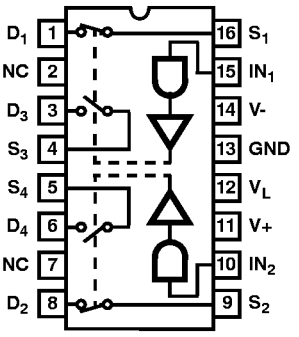

**SPDT - DG187, DG188**
**(TO-100 METAL CAN)**
TOP VIEW




**SPDT - DG187, DG188**
**(CDIP)**
TOP VIEW




**DUAL SPDT - DG190, DG191**
**(CDIP)**
TOP VIEW



## Absolute Maximum Ratings

V+ - V- . . . . . 36V
V+ - $V_D$ . . . . . 33V
$V_D$ - V- . . . . . 33V
$V_D$ - $V_S$ . . . . . ±22V
$V_L$ - V- . . . . . 36V
$V_L$ - $V_{IN}$, $V_L$ - GND, $V_{IN}$ - GND . . . . . 8V
GND - V- . . . . . 27V
GND - $V_{IN}$ . . . . . 20V
Current (S or D) (Note 3) . . . . . 200mA
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10s) . . . . . +300°C

## Thermal Information

Operating Temperature . . . . . -55°C to +125°C
Maximum Power Dissipation †
TO Metal Can Packages . . . . . 450mW
Derate 6mW/°C above +75°C
Ceramic DIP Packages . . . . . 825mW
Derate 11mW/°C above +75°C
† Device mounted with all leads welded or soldered to PC board.

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## Electrical Specifications

V+ = +15V, V- = -15V, $V_L$ = 5V, Unless Otherwise Specified

| PARAMETER | DEVICE NUMBER | (NOTE 1) TEST CONDITIONS | A SERIES | | | B SERIES | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | -55°C | +25°C | +125°C | -20°C | +25°C | +85°C | |
| SWITCH | | | | | | | | | |
| $I_{S(OFF)}$ | DG181, DG182, DG184, DG185, DG187, DG188, DG190, DG191 | $V_S$ = 10V, $V_D$ = -10V, V+ = 10V, V- = -20V, $V_{IN}$ = "OFF" | - | ±1 | 100 | - | ±5 | 100 | nA |
| | DG181, DG184, DG187, DG190 | $V_S$ = 7.5V, $V_D$ = -7.5V, $V_{IN}$ = "OFF" | - | ±1 | 100 | - | ±5 | 100 | nA |
| | DG182, DG185, DG188, DG191 | $V_S$ = 10V, $V_D$ = -10V, $V_{IN}$ = "OFF" | - | ±1 | 100 | - | ±5 | 100 | nA |
| $I_{D(OFF)}$ | DG181, DG182, DG184, DG185, DG187, DG188, DG190, DG191 | $V_S$ = 10V, $V_D$ = -10V, V+ = 10V, V- = -20V, $V_{IN}$ = "OFF" | - | ±1 | 100 | - | ±5 | 100 | nA |
| | DG181, DG184, DG187, DG190 | $V_S$ = 7.5V, $V_D$ = -7.5V, $V_{IN}$ = "OFF" | - | ±1 | 100 | - | ±5 | 100 | nA |
| | DG182, DG185, DG188, DG191 | $V_S$ = 10V, $V_D$ = -10V, $V_{IN}$ = "OFF" | - | ±1 | 100 | - | ±5 | 100 | nA |
| $I_{D(ON)}$ + $I_{S(ON)}$ | DG181, DG184, DG187, DG190 | $V_D$ = $V_S$ = -7.5V, $V_{IN}$ = "ON" | - | ±2 | -200 | - | -10 | -200 | nA |
| | DG182, DG185, DG188, DG191 | $V_D$ = $V_S$ = -10V, $V_{IN}$ = "ON" | - | ±2 | -200 | - | -10 | -200 | nA |
| INPUT | | | | | | | | | |
| $I_{INL}$ | All | $V_{IN}$ = 0V | -250 | -250 | -250 | -250 | -250 | -250 | µA |
| $I_{INH}$ | All | $V_{IN}$ = 5V | - | 10 | 20 | - | 10 | 20 | µA |
| DYNAMIC | | | | | | | | | |
| $t_{ON}$ | 30Ω Switches | See Switching Time Test Circuit | - | 150 | - | - | 180 | - | ns |
| | 75Ω Switches | | - | 250 | - | - | 300 | - | ns |
| $t_{OFF}$ | 30Ω and 75Ω Switches | | - | 130 | - | - | 150 | - | ns |
| $C_{S(OFF)}$ | DG181, DG182, DG184, DG185, DG187, DG188, DG190, DG191 | $V_S$ = -5V, $I_D$ = 0, f = 1MHz | 9 Typical | | | | | | pF |
| | | $V_D$ = +5V, $I_S$ = 0, f = 1MHz | 6 Typical | | | | | | pF |
| $C_{D(ON)}$ + $C_{S(ON)}$ | | $V_D$ = $V_S$ = 0, f = 1MHz | 14 Typical | | | | | | pF |
| OFF Isolation | | $R_L$ = 75Ω, $C_L$ = 3pF | Typically >50dB at 10MHz | | | | | | - |

**Electrical Specifications** V+ = +15V, V- = -15V, $V_L$ = 5V, Unless Otherwise Specified **(Continued)**

| PARAMETER | DEVICE NUMBER | (NOTE 1) TEST CONDITIONS | A SERIES | | | B SERIES | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | -55°C | +25°C | +125°C | -20°C | +25°C | +85°C | |
| SUPPLY | | | | | | | | | |
| I+ | DG181, DG182, DG190, DG191 | $V_{IN}$ = 5V | - | 1.5 | - | - | 1.5 | - | mA |
| | DG184, DG185 | | - | 0.1 | - | - | 0.1 | - | mA |
| | DG187, DG188 | | - | 0.8 | - | - | 0.8 | - | mA |
| I- | DG181, DG182, DG190, DG191 | | - | -5.0 | - | - | -5.0 | - | mA |
| | DG184, DG185 | | - | -4.0 | - | - | -4.0 | - | mA |
| | DG187, DG188 | | - | -3.0 | - | - | -3.0 | - | mA |
| $I_L$ | DG181, DG182, DG184, DG185, DG190, DG191 | | - | 4.5 | - | - | 4.5 | - | mA |
| | DG187, DG188 | | - | 3.2 | - | - | 3.2 | - | mA |
| $I_{GND}$ | All | | - | -2.0 | - | - | -2.0 | - | mA |
| I+ | DG181, DG182, DG190, DG191 | $V_{IN}$ = 0V | - | 1.5 | - | - | 1.5 | - | mA |
| | DG184, DG185 | | - | 3.0 | - | - | 3.0 | - | mA |
| | DG187, DG188 | | - | 0.8 | - | - | 0.8 | - | mA |
| I- | DG181, DG182, DG190, DG191 | | - | -5.0 | - | - | -5.0 | - | mA |
| | DG184, DG185 | | - | -5.5 | - | - | -5.5 | - | mA |
| | DG187, DG188 | | - | -3.0 | - | - | -3.0 | - | mA |
| $I_L$ | DG181, DG182, DG184, DG185, DG190, DG191 | | - | 4.5 | - | - | 4.5 | - | mA |
| | DG187, DG188 | | - | 3.2 | - | - | 3.2 | - | mA |
| $I_{GND}$ | All | | - | -2.0 | - | - | -2.0 | - | mA |

NOTE:

1. See Switching State Diagrams for $V_{IN}$ "ON" and $V_{IN}$ "OFF" Test Conditions.

**Electrical Specifications** Maximum Resistances ($R_{DS(ON)}$ MAX)

| DEVICE NUMBER | TEST CONDITIONS (NOTE 1) V+ = 15V, V- = -15V, $V_L$ = 5V | | MILITARY TEMPERATURE | | | INDUSTRIAL TEMPERATURE | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | -55°C | +25°C | +125°C | -20°C | +25°C | +85°C | |
| DG181 | $V_D$ = -7.5V | $I_S$ = -10mA, $V_{IN}$ = "ON" | 30 | 30 | 60 | 50 | 50 | 75 | Ω |
| DG182 | $V_D$ = -10V | | 75 | 75 | 100 | 100 | 100 | 150 | Ω |
| DG184 | $V_D$ = -7.5V | | 30 | 30 | 60 | 50 | 50 | 75 | Ω |
| DG185 | $V_D$ = -10V | | 75 | 75 | 150 | 100 | 100 | 150 | Ω |
| DG187 | $V_D$ = -7.5V | | 30 | 30 | 60 | 50 | 50 | 75 | Ω |
| DG188 | $V_D$ = -10V | | 75 | 75 | 150 | 100 | 100 | 150 | Ω |
| DG190 | $V_D$ = -7.5V | | 30 | 30 | 60 | 50 | 50 | 75 | Ω |
| DG191 | $V_D$ = -10V | | 75 | 75 | 150 | 100 | 100 | 150 | Ω |

NOTES:

1. See Switching State Diagrams for $V_{IN}$ "ON" and $V_{IN}$ "OFF" Test Conditions.
2. Normally the minimum signal handling capability of the DG181 thru DG191 family is 20V peak to peak for the 75Ω switches and 15V peak-to-peak for the 30Ω (refer $I_D$ and $I_S$ tests above).
3. For other Analog Signals, the following guidelines can be used: proper switch turn-off requires that V- ≤ $V_{ANALOG}$(peak) - $V_P$ where $V_P$ = 7.5V for the 80Ω switches and $V_P$ = 5.0V for 75Ω switches e.g., - 10V minimum (-peak) analog signal and a 75Ω switch ($V_P$ = 5V), requires that V- ≤ -10V -5V = -15V.

### DUAL SPST - DG181/182

| TEST CONDITIONS | |
|---|---|
| $V_{IN}$ "ON" = 0.8V | All Channels |
| $V_{IN}$ "OFF" = 2.0V | All Channels |

NOTE:

1. Switch states are for logic "1" input = 2.0V.

### DUAL DPST - DG184/185

| TEST CONDITIONS | |
|---|---|
| $V_{IN}$ "ON" = 2.0V | All Channels |
| $V_{IN}$ "OFF" = 0.8V | All Channels |

NOTE:

1. Switch states are for logic "1" input = 2.0V.

### SPDT - DG187/188

| TEST CONDITIONS | |
|---|---|
| $V_{IN}$ "ON" = 2.0V | Channel 1 |
| $V_{IN}$ "ON" = 0.8V | Channel 2 |
| $V_{IN}$ "OFF" = 2.0V | Channel 2 |
| $V_{IN}$ "OFF" = 0.8V | Channel 1 |

NOTE:

1. Switch states are for logic "1" input = 2.0V.

### SPDT - DG190/191

| TEST CONDITIONS | |
|---|---|
| $V_{IN}$ "ON" = 2.0V | Channel 1 and 2 |
| $V_{IN}$ "ON" = 0.8V | Channel 3 and 4 |
| $V_{IN}$ "OFF" = 2.0V | Channel 3 and 4 |
| $V_{IN}$ "OFF" = 0.8V | Channel 1 and 2 |

NOTE:

1. Switch states are for logic "1" input = 2.0V.

## *Switching Time Test Circuits*

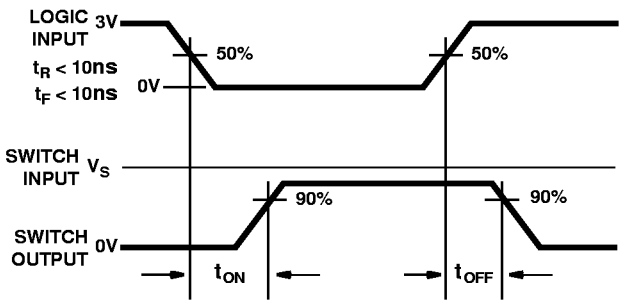



**FIGURE 1. SWITCHING TIME TEST WAVEFORMS** (Note 1)

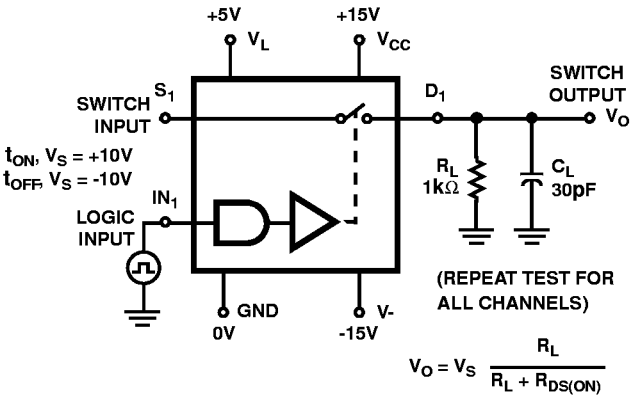
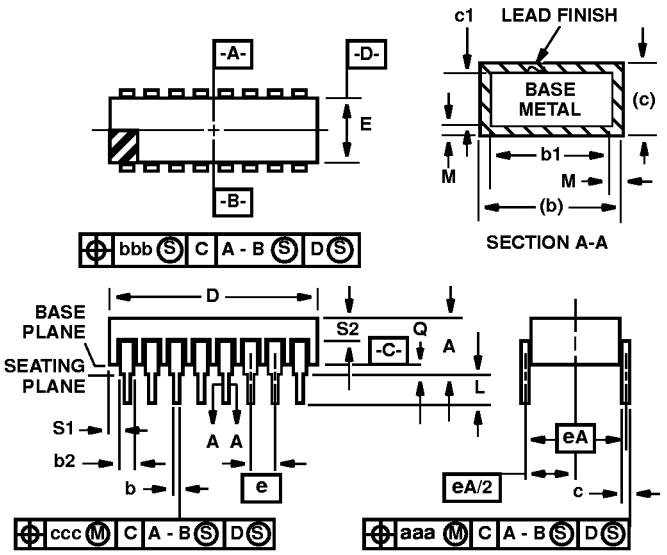



**FIGURE 2. SWITCHING TIME TEST CIRCUIT** (Note 2)

NOTES:

1. Switch output waveform shown for $V_S$ = constant with logic input waveform as shown.
2. $V_S$ may be + or - as per switching time test circuit. $V_O$ is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

## Ceramic Dual-In-Line Metal Seal Packages (SBDIP)




**D14.3** MIL-STD-1835 CDIP2-T14 (D-1, CONFIGURATION C)
14 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.200 | - | 5.08 | - |
| b | 0.014 | 0.026 | 0.36 | 0.66 | 2 |
| b1 | 0.014 | 0.023 | 0.36 | 0.58 | 3 |
| b2 | 0.045 | 0.065 | 1.14 | 1.65 | - |
| b3 | 0.023 | 0.045 | 0.58 | 1.14 | 4 |
| c | 0.008 | 0.018 | 0.20 | 0.46 | 2 |
| c1 | 0.008 | 0.015 | 0.20 | 0.38 | 3 |
| D | - | 0.785 | - | 19.94 | - |
| E | 0.220 | 0.310 | 5.59 | 7.87 | - |
| e | 0.100 BSC | | 2.54 BSC | | - |
| eA | 0.300 BSC | | 7.62 BSC | | - |
| eA/2 | 0.150 BSC | | 3.81 BSC | | - |
| L | 0.125 | 0.200 | 3.18 | 5.08 | - |
| Q | 0.015 | 0.060 | 0.38 | 1.52 | 5 |
| S1 | 0.005 | - | 0.13 | - | 6 |
| S2 | 0.005 | - | 0.13 | - | 7 |
| $\alpha$ | $90^o$ | $105^o$ | $90^o$ | $105^o$ | - |
| aaa | - | 0.015 | - | 0.38 | - |
| bbb | - | 0.030 | - | 0.76 | - |
| ccc | - | 0.010 | - | 0.25 | - |
| M | - | 0.0015 | - | 0.038 | 2 |
| N | 14 | | 14 | | 8 |

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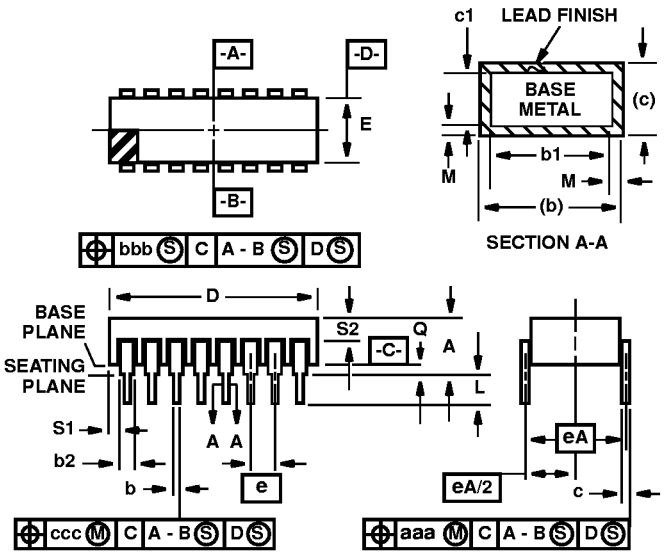
NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

## Ceramic Dual-In-Line Metal Seal Packages (SBDIP)




**D16.3** MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.200 | - | 5.08 | - |
| b | 0.014 | 0.026 | 0.36 | 0.66 | 2 |
| b1 | 0.014 | 0.023 | 0.36 | 0.58 | 3 |
| b2 | 0.045 | 0.065 | 1.14 | 1.65 | - |
| b3 | 0.023 | 0.045 | 0.58 | 1.14 | 4 |
| c | 0.008 | 0.018 | 0.20 | 0.46 | 2 |
| c1 | 0.008 | 0.015 | 0.20 | 0.38 | 3 |
| D | - | 0.840 | - | 21.34 | - |
| E | 0.220 | 0.310 | 5.59 | 7.87 | - |
| e | 0.100 BSC | | 2.54 BSC | | - |
| eA | 0.300 BSC | | 7.62 BSC | | - |
| eA/2 | 0.150 BSC | | 3.81 BSC | | - |
| L | 0.125 | 0.200 | 3.18 | 5.08 | - |
| Q | 0.015 | 0.060 | 0.38 | 1.52 | 5 |
| S1 | 0.005 | - | 0.13 | - | 6 |
| S2 | 0.005 | - | 0.13 | - | 7 |
| $\alpha$ | $90^o$ | $105^o$ | $90^o$ | $105^o$ | - |
| aaa | - | 0.015 | - | 0.38 | - |
| bbb | - | 0.030 | - | 0.76 | - |
| ccc | - | 0.010 | - | 0.25 | - |
| M | - | 0.0015 | - | 0.038 | 2 |
| N | 16 | | 16 | | 8 |

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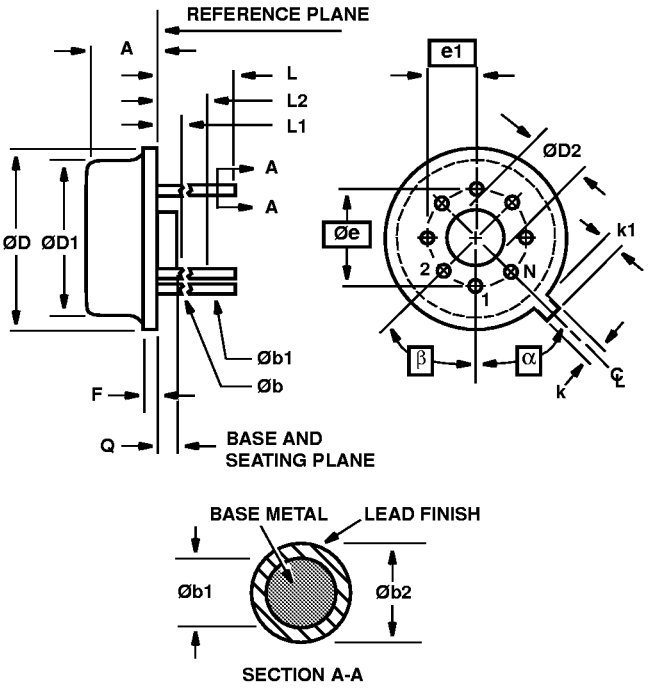
NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

## Metal Can Packages (Can)




**T10.B** MIL-STD-1835 MACY1-X10 (A2)
10 LEAD METAL CAN PACKAGE

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.165 | 0.185 | 4.19 | 4.70 | - |
| Øb | 0.016 | 0.019 | 0.41 | 0.48 | 1 |
| Øb1 | 0.016 | 0.021 | 0.41 | 0.53 | 1 |
| Øb2 | 0.016 | 0.024 | 0.41 | 0.61 | - |
| ØD | 0.335 | 0.375 | 8.51 | 9.52 | - |
| ØD1 | 0.305 | 0.335 | 7.75 | 8.51 | - |
| ØD2 | 0.110 | 0.160 | 2.79 | 4.06 | - |
| e | 0.230 BSC | | 5.84 BSC | | - |
| e1 | 0.115 BSC | | 2.92 BSC | | - |
| F | - | 0.040 | - | 1.02 | - |
| k | 0.027 | 0.034 | 0.69 | 0.86 | - |
| k1 | 0.027 | 0.045 | 0.69 | 1.14 | 2 |
| L | 0.500 | 0.750 | 12.70 | 19.05 | 1 |
| L1 | - | 0.050 | - | 1.27 | 1 |
| L2 | 0.250 | - | 6.35 | - | 1 |
| Q | 0.010 | 0.045 | 0.25 | 1.14 | - |
| α | $36^{o}$ BSC | | $36^{o}$ BSC | | 3 |
| β | $36^{o}$ BSC | | $36^{o}$ BSC | | 3 |
| N | 10 | | 10 | | 4 |

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NOTES:

1. (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N -1 places) from α, looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
6. Controlling dimension: INCH.