AM8212

Eight-Bit Input/Output Port

All of the principal peripheral and input/output functions of a Microcomputer System can be implemented with the AM8212. The AM8212 input/output port consists of an 8-latch with 3-state output buffers along with control and device selection logic, which can be used to implement latches, gated buffers or multiplexers.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Am8212

Eight-Bit Input/Output Port

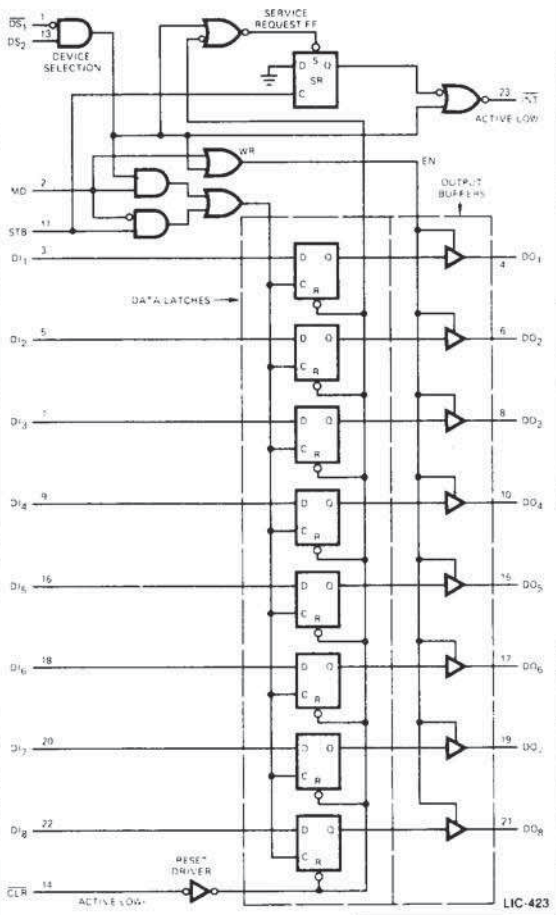
Distinctive Characteristics

- Fully parallel, 8-bit data register and buffer replacing latches, multiplexers and buffers needed in microprocessor systems.
- 4.0V output high voltage for direct interface to MOS microprocessors, such as the Am9080A family.
- Input load current 250μA max.
- Reduces system package count
- Available for operation over both commercial and military temperature ranges.
- Service request flip-flop for interrupt generation
- Three-state outputs sink 15mA
- Asynchronous register clear with clock over-ride

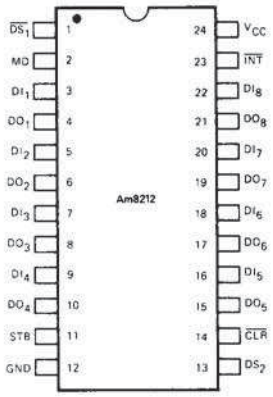
FUNCTIONAL DESCRIPTION

All of the principal peripheral and input/output functions of a Microcomputer System can be implemented with the Am8212. The Am8212 input/output port consists of an 8-latch with 3-state output buffers along with control and device selection logic, which can be used to implement latches, gated buffers or multiplexers.

LOGIC DIAGRAM



CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

PIN DEFINITION

$DI_1 - DI_8$	DATA IN
$DO_1 - DO_8$	DATA OUT
$\overline{DS_1} - DS_2$	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	–55°C to +125°C	AM8212DM
Hermetic DIP	0°C to +70°C	D8212
Molded DIP	0°C to +70°C	P8212
Dice	0°C to +70°C	AM8212XC

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FUNCTIONAL DESCRIPTION (Cont'd)

Data Latch

The 8 flip-flops that make up the data latch are of a "D" type design. The output (Q) of the flip-flop will follow the data input (D) while the clock input (C) is high. Latching will occur when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$). (Note: Clock (C) Overrides Reset ($\overline{CLR}$)).

Output Buffer

The outputs of the data latch (Q) are connected to 3-state, non-inverting output buffers. These buffers have a common control line (EN); this control line either enables the buffer to transmit the data from the outputs of the data latch (Q) or disables the buffer, forcing the output into a high impedance state. (3-state). This high-impedance state allows the Am8212 to be connected directly onto the microprocessor bi-directional data bus.

Control Logic

The Am8212 has control inputs $\overline{DS_1}$, DS_2, MD and STB. These inputs are used to control device selection, data latching, output buffer state and service request flip-flop.

$\overline{DS_1}$, DS_2 (Device Select)

These 2 inputs are used for device selection. When $\overline{DS_1}$ is low and DS_2 is high ($\overline{DS_1} \cdot DS_2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

MD (Mode)

This input is used to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is high (output mode) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS_1} \cdot DS_2$).

When MD is low (input mode) the output buffer state is determined by the device selection logic ($\overline{DS_1} \cdot DS_2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

This input is used as the clock (C) to the data latch for the input mode MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop is negative edge triggered.

Service Request Flip-Flop

The SR flip-flop is used to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output of the (SR) flip-flop (Q) is connected to an inverting input of a "NOR" gate. The other input to the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS_1} \cdot DS_2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.

TRUTH TABLE

STB	MD	$\overline{DS_1} - DS_2$	Data Out Equals
0	0	0	Three-State
1	0	0	Three-State
0	1	0	Data Latch
1	1	0	Data Latch
0	0	1	Data Latch
1	0	1	Data In
0	1	1	Data In
1	1	1	Data In

CLR	$\overline{DS_1} - DS_2$	STB	SR*	$\overline{INT}$
0	0	0	1	1
0	1	0	1	0
1	1	↘	0	0
1	1	0	1	0
1	0	0	1	1
1	1	↘	1	0

$\overline{CLR}$ – Resets Data Latch
– Sets SR Flip-Flop (no effect on Output Buffer)
* Internal SR Flip-Flop

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage	−0.5V to +7.0V
Output Voltage	−0.5V to +7.0V
Input Voltages	−1.0V to +5.5V
Output Current (Each Output)	125mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

P8212, D8212 (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$
Am8212DM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$

DC CHARACTERISTICS

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
I_F	Input Load Current ACK, DS_2, CR, $DI_1 - DI_8$ Inputs	$V_F = 0.45V$				−0.25	mA
I_F	Input Load Current MD Input	$V_F = 0.45V$				−0.75	mA
I_F	Input Load Current DS_1 Input	$V_F = 0.45V$				−1.0	mA
I_R	Input Leakage Current ACK, DS, CR, $DI_1 - DI_8$ Inputs	$V_R = 5.25V$				10	μA
I_R	Input Leakage Current MO Input	$V_R = 5.25V$				30	μA
I_R	Input Leakage Current DS_1 Input	$V_R = 5.25V$				40	μA
V_C	Input Forward Voltage Clamp	$I_C = -5.0mA$	COM'L			−1.0	Volts
			MIL			−1.2	
V_{IL}	Input LOW Voltage		COM'L			0.85	Volts
			MIL			0.80	
V_{IH}	Input HIGH Voltage			2.0			Volts
V_{OL}	Output LOW Voltage	$I_{OL} = 15mA$				0.45	Volts
V_{OH}	Output HIGH Voltage	$I_{OH} = -1.0mA$	COM'L	3.65	4.0		Volts
			MIL	3.3	4.0		
		$I_{OH} = -0.5mA$	MIL	3.4	4.0		
I_{SC}	Short Circuit Output Current	$V_O = 0V$		−15		−75	mA
$\|I_O\|$	Output Leakage Current High Impedance	$V_O = 0.45V/5.25V$				20	μA
I_{CC}	Power Supply Current	Note 2			90	130	mA

AC CHARACTERISTICS (Note 3)

Parameters	Description	Min.	Typ. (Note 1)	Max.	Units
t_{pw}	Pulse Width	30	8		ns
t_{pd}	Data to Output Delay		12	30	ns
t_{we}	Write Enable to Output Delay		18	40	ns
t_{set}	Data Set-up Time	15			ns
t_h	Data Hold Time	20			ns
t_r	Reset to Output Delay		18	40	ns
t_s	Set to Output Delay		15	30	ns
t_e	Output Enable/Disable Time		14	45	ns
t_c	Clear to Output Delay		25	55	ns

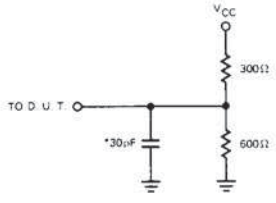
CAPACITANCE (Note 4)

F = 1.0MHz, $V_{BIAS} = 2.5V$, $V_{CC} = +5.0V$, $T_A = 25°C$

Parameters	Description	Typ.	Max.	Units
C_{IN}	DS_1 MD Input Capacitance	9.0	12	pF
C_{IN}	DS_2, CK, ACK, $DI_1 - DI_8$ Input Capacitance	5.0	9.0	pF
C_{OUT}	$DO_1 - DO_8$ Output Capacitance	8.0	12	pF

Notes: 1. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
2. CLR = STB = HIGH; $DS_1 = DS_2$ = MD = LOW; all data inputs are gound, all data outputs are open.
3. Conditions of Test: a) Input pulse amplitude = 2.5V
b) Input rise and fall times 5.0ns
c) Between 1.0V and 2.0V measurements made at 1.5V with 15mA and 30pF Test Load.
4. This parameter is sampled and not 100% tested.

TEST LOAD (15mA and 30pF)



*Including Jig and Probe Capacitance.

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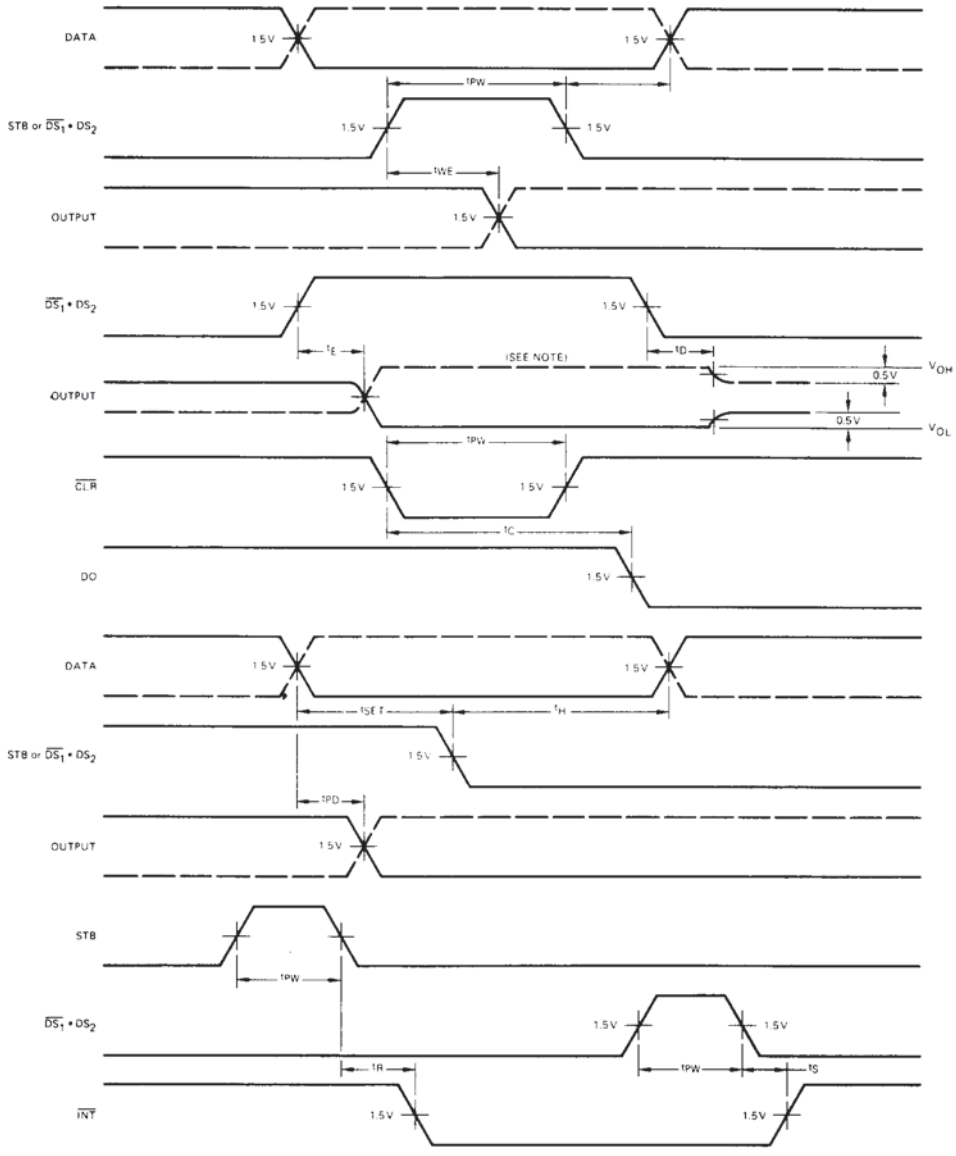
TIMING DIAGRAM



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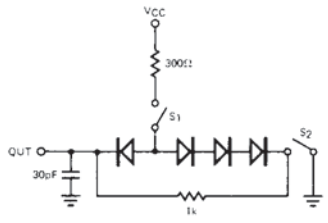
Note: Alternative Test Load.



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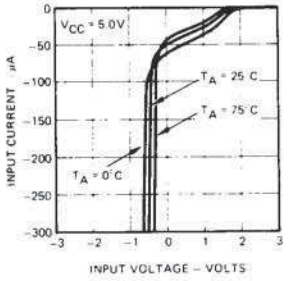
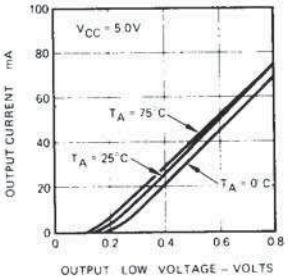
TYPICAL CHARACTERISTICS

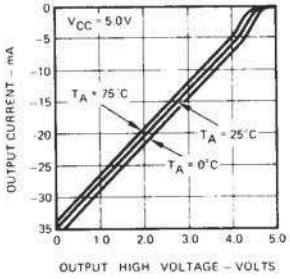
Input Current Versus Input Voltage



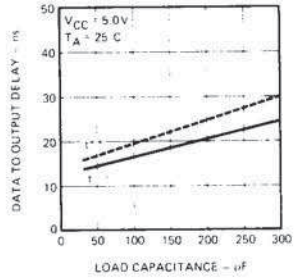
Output Current Versus Output LOW Voltage



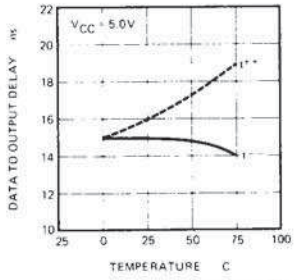
Output Current Versus Output HIGH Voltage



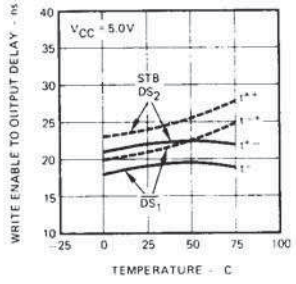
Data to Output Delay Versus Load Capacitance



Data to Output Delay Versus Temperature



Write Enable to Output Delay Versus Temperature



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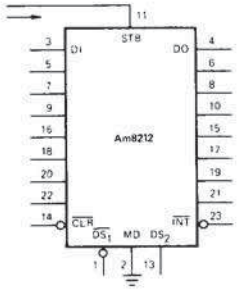
LOGIC SYMBOLS

INPUT DEVICE

Detailed



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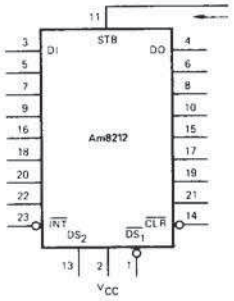
OUTPUT DEVICE



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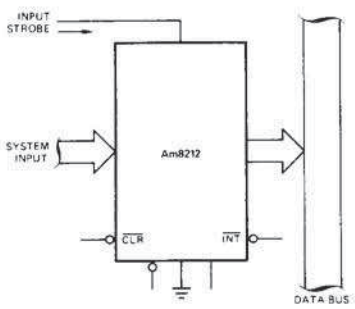
Symbolic



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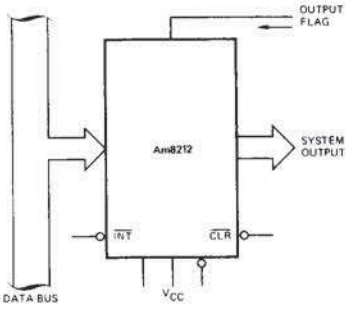

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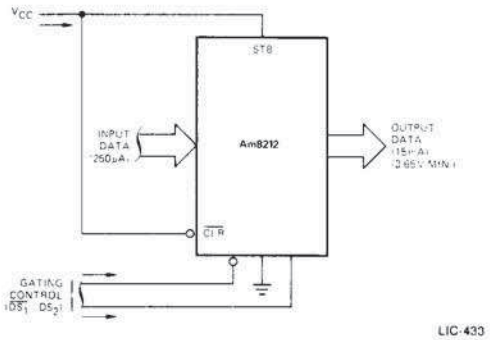
TYPICAL APPLICATIONS OF THE Am8212

GATED BUFFER (3-STATE)

By tying the mode signal low and the strobe input high, the data latch is acting as a straight through gate. The output buffers are then enabled from the device selection logic $\overline{DS_1}$ and DS_2.

When the device selection logic is false, the outputs are 3-state.

When the device selection logic is true, the input data from the system is directly transferred to the output.



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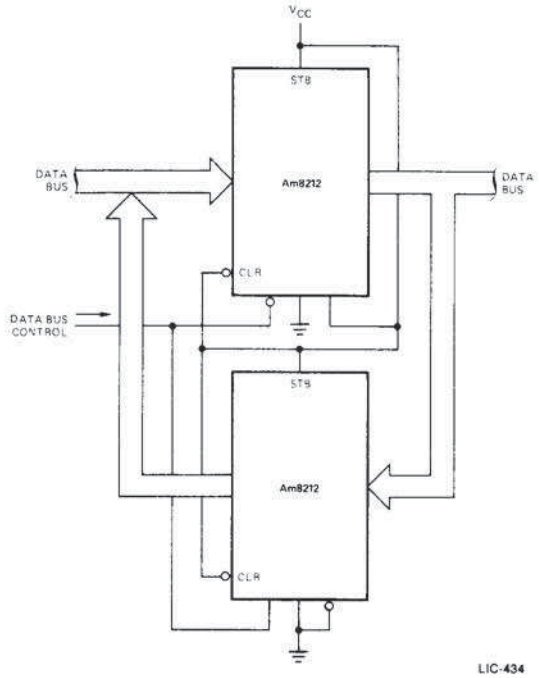
Bi-Directional Bus Driver

Two Am8212s wired back to back can be used as a symmetrical drive, bi-directional bus driver. The devices are controlled by the data bus input control which is connected to $\overline{DS_1}$ on the first Am8212 and to DS_2 on the second. While one device is active, and acting as a straight through buffer the other is in its 3-state mode.



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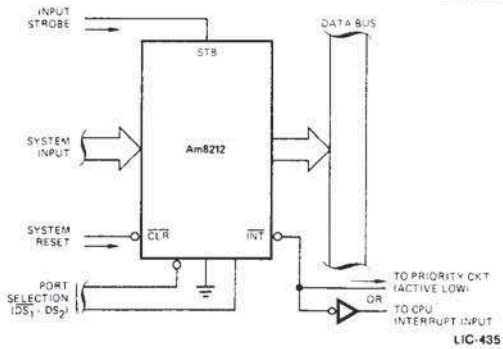
Interrupting Input Port

The Am8212 accepts a strobe from the system input source, which in turn clears the service request flip-flop and interrupts the processor. The processor then goes through a service routine, identifies the port, and causes the device selection logic to go true – enabling the system input data onto the data bus.



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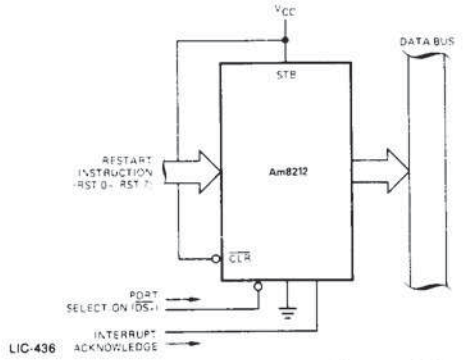
TYPICAL APPLICATIONS OF THE Am8212 (Cont'd)

Interrupt Instruction Port

The Am8212 can be used to gate the interrupt instruction, normally RESTART instructions, onto the data bus. The device is enabled from the interrupt acknowledge signal from the microprocessor and from a port selection signal. This signal is normally tied to ground. ($\overline{DS_1}$ could be used to multiplex a variety of interrupt instruction ports onto a common bus.)



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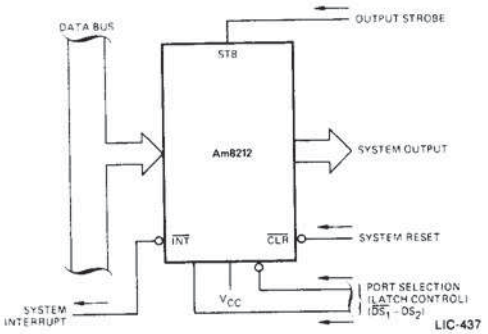
Output Port (With Hand-Shaking)

The Am8212 is used to transmit data from the data bus to a system output. The output strobe could be a hand-shaking signal such as "reception of data" from the device that the system is outputting to. It in turn, can interrupt the system signifying the reception of data. The selection of the port comes from the device selection logic. ($\overline{DS_1} - DS_2$.)



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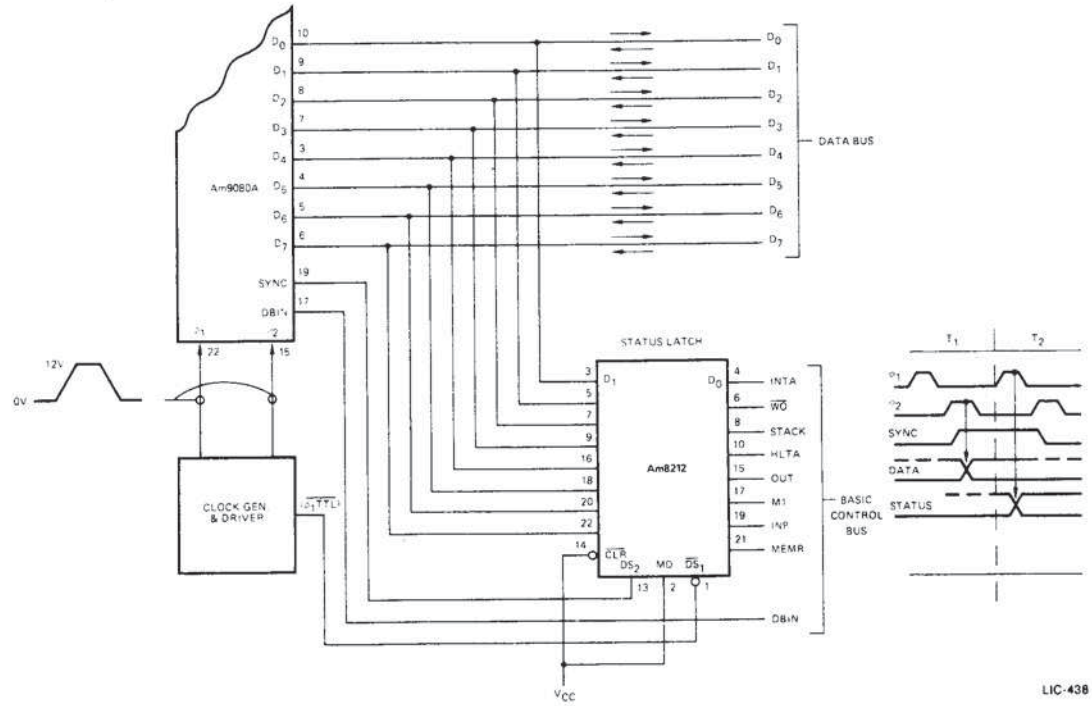
Am9080A Status Latch

The input to the Am8212 latch comes directly from the Am9080A data bus. Timing shows that when the SYNC signal is true ($\overline{DS_1}$ input), and $\phi 1$ is true, ($\overline{DS_1}$ input) then the status data will be latched into the Am8212. The mode signal is tied high so that the output on the latch is active and enabled all the time.



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